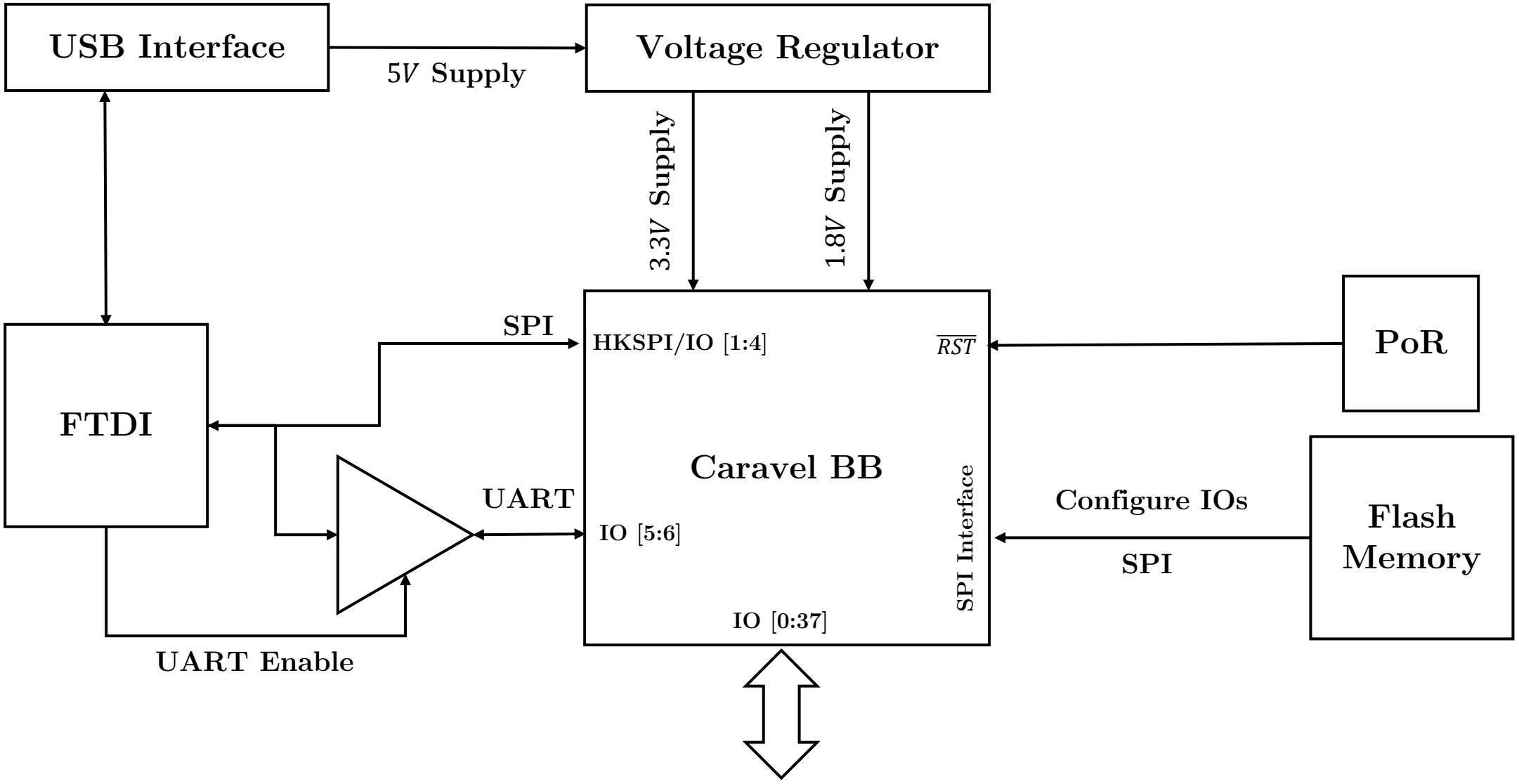
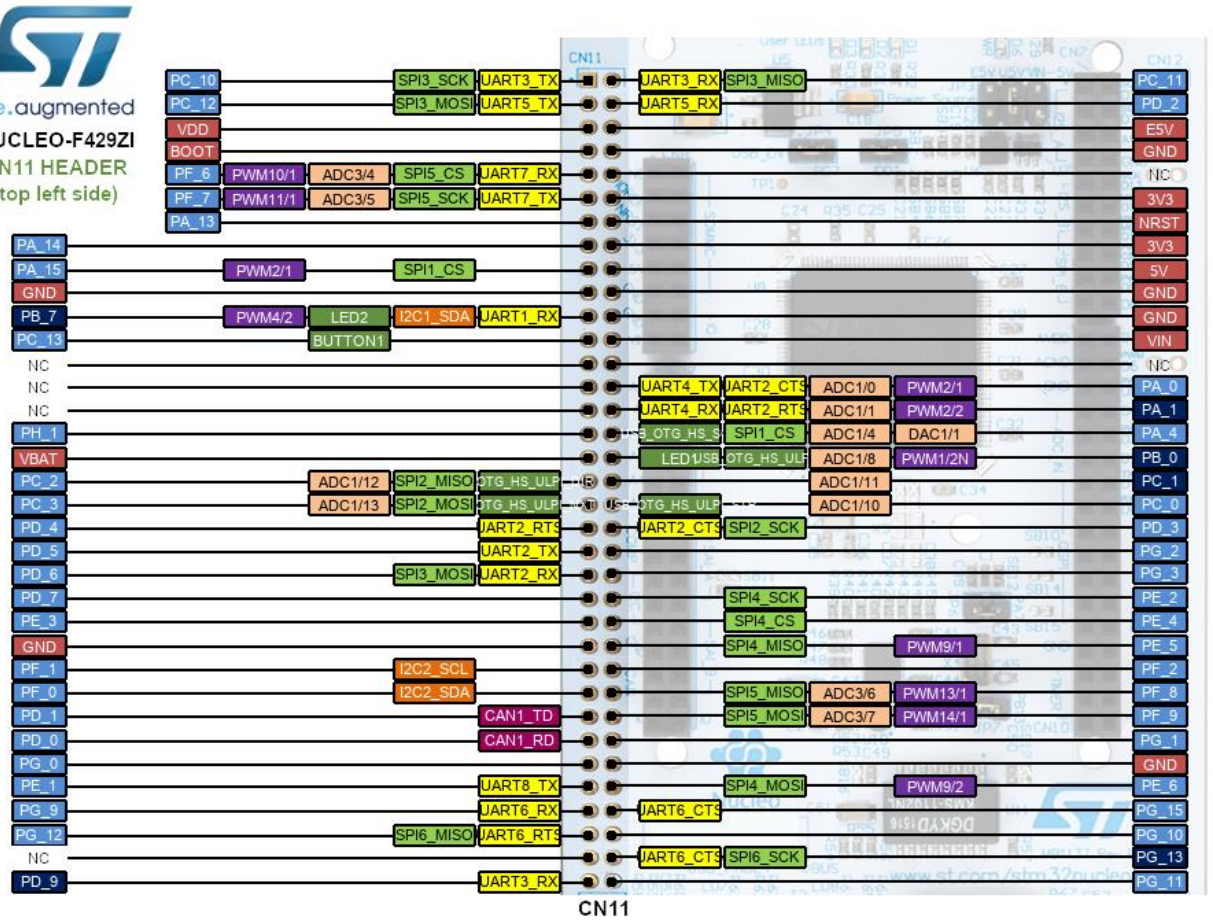
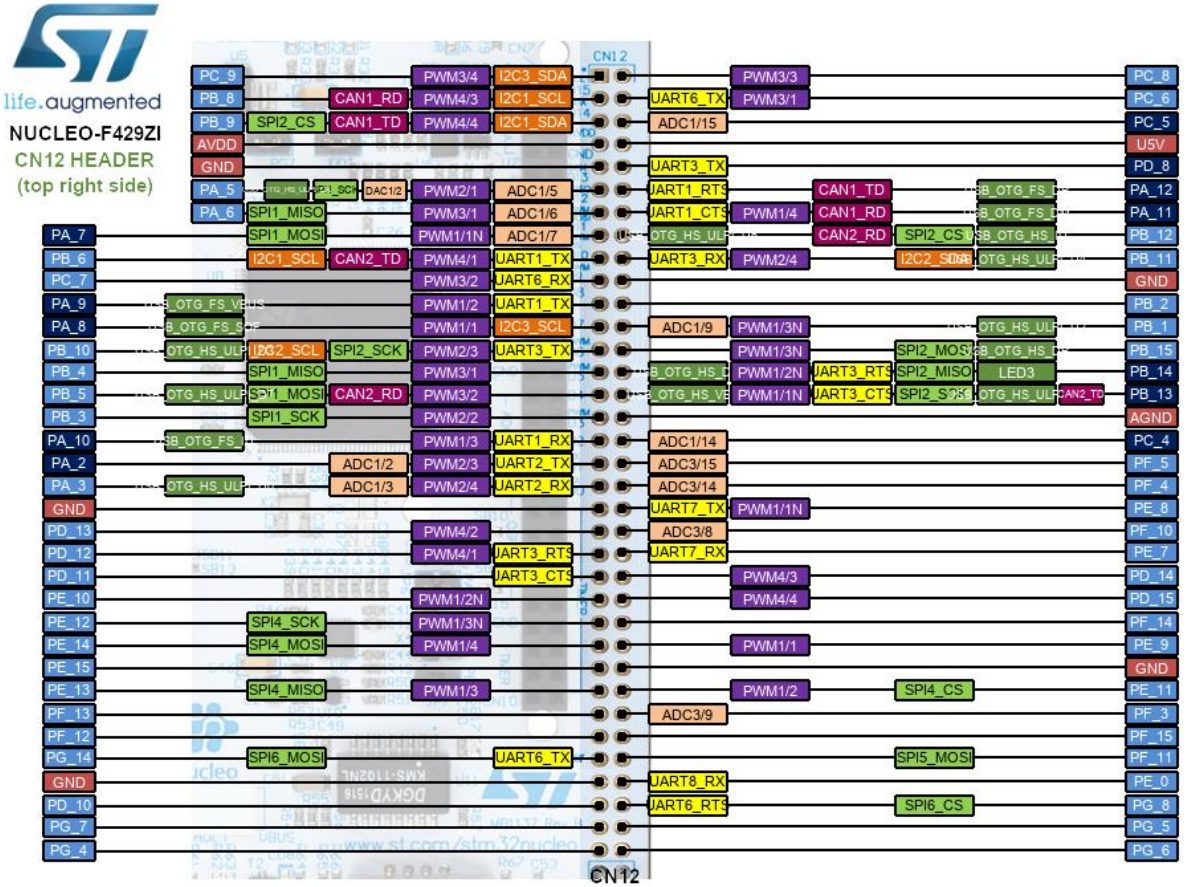
Caravel + Nucleo Board

Caravel Board V4 Block Diagram



Nucleo Board: ST Morpho Connectors



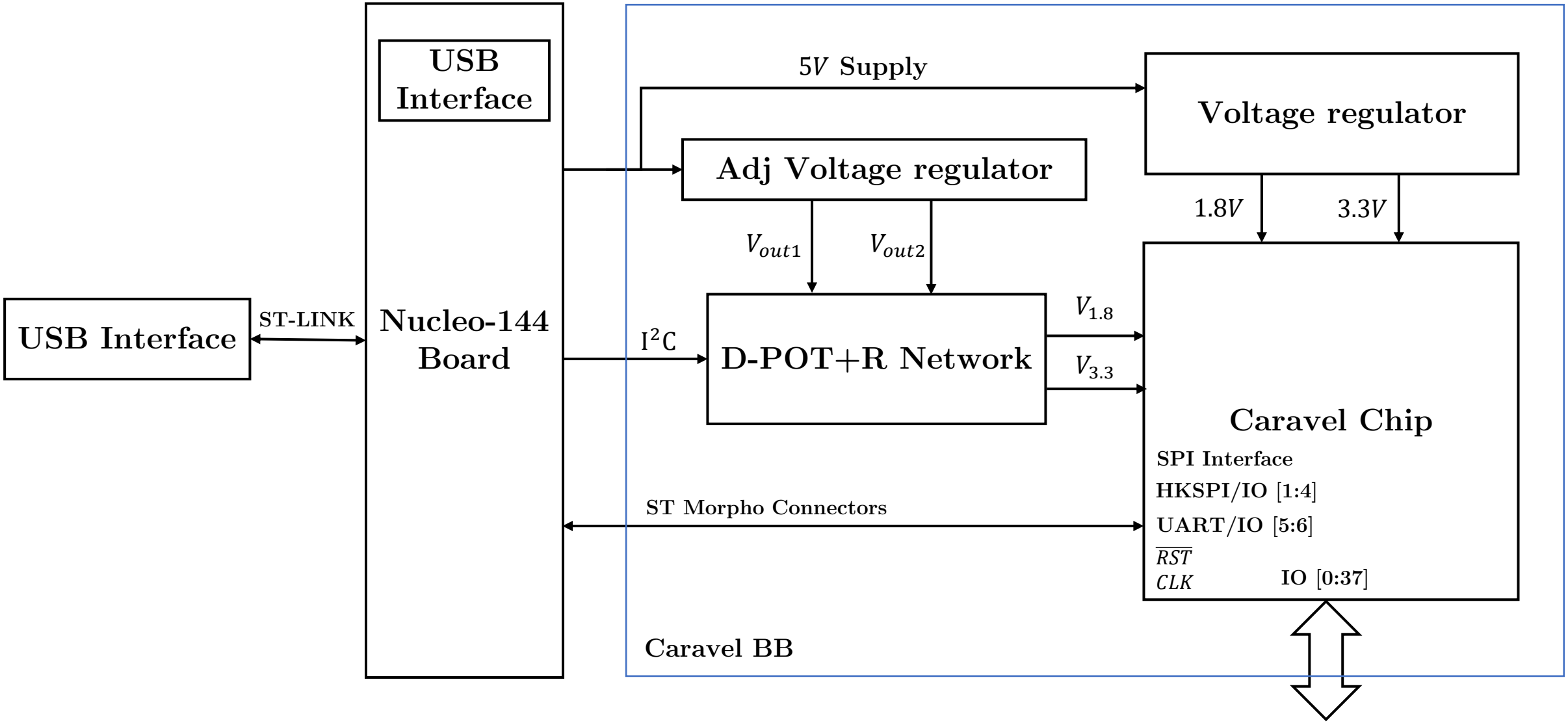


[1]: https://os.mbed.com/platforms/ST-Nucleo-F429ZI/#board-pinout

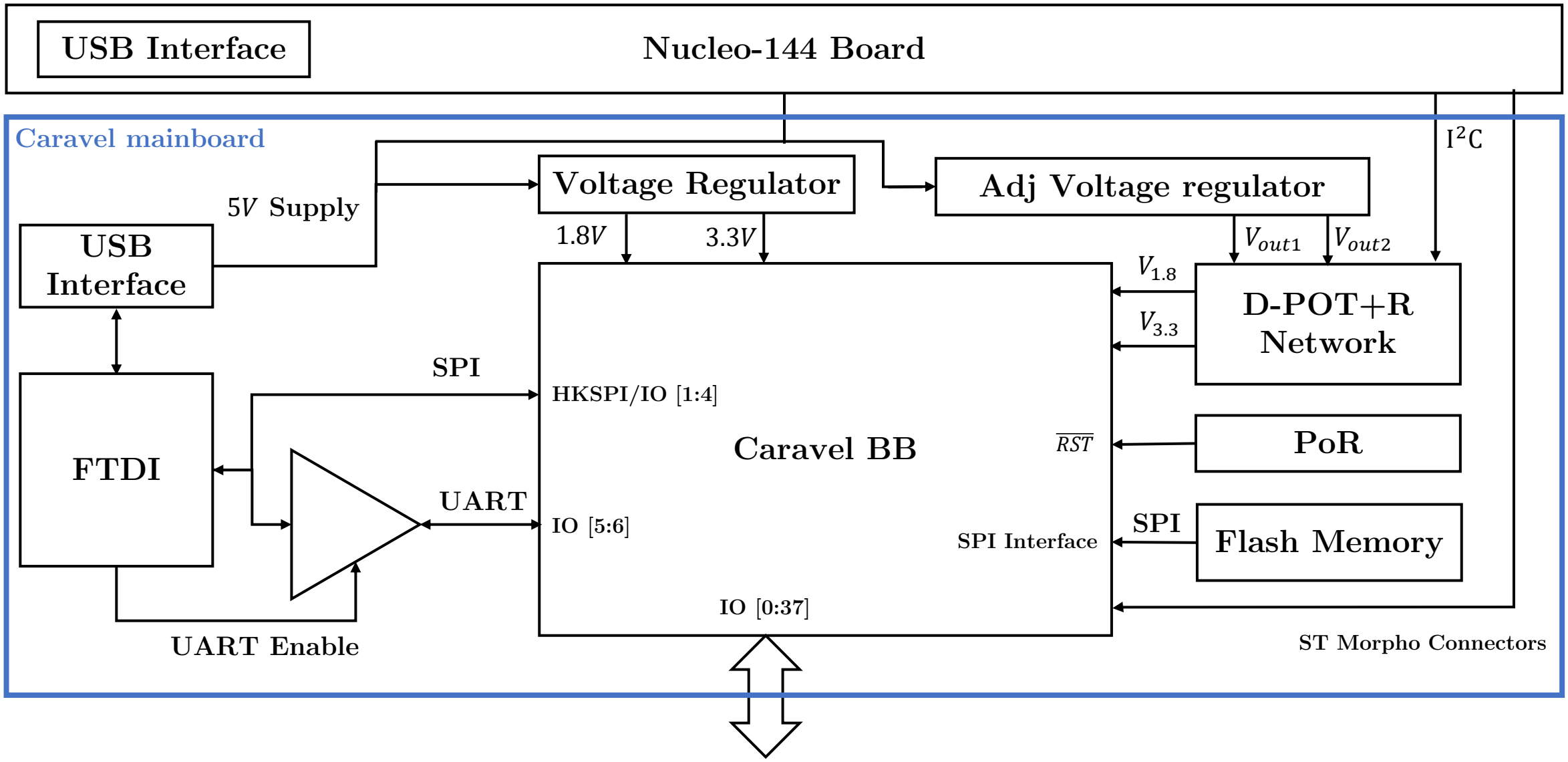
Nucleo Board: Interface with Caravel

- $CN4$ jumpers in ST-Link part is used to program ST32 microcontroller, hence, configuring Caravel I/Os
- The board has a 3.3V Regulator (Max $500mA$)
- Default clock supply is $8\,MHz$ from ST-Link on $PF0$
- Caravel SPI/HKSPI interface could be on $PE11:PE14$ or $PF6:PF9$
- Caravel UART interface could be on $PC10:PC11$
- $PA13$ and $PA14$ are shared with SWD signals connected to ST-LINK. If ST-LINK part is not cut, it is not recommended to use them as I/Os.
- Caravel BB dimensions would be $67.5mm \times 92.5mm$

Caravel + Nucleo Board Block Diagram



Caravel + Nucleo Board Block Diagram



Dynamic Voltage Scaling (DVS)

- Dynamic power supply is required to test the chip with non-nominal supplies
- The required ranges are from $1.4V$ to $2.2V$ for $V_{1.8}$ and $3V$ to $3.6V$ for $V_{3.3}$
- Adjustable dual LDO (MIC2211) is capable of suppling from $1.25V$ to $5V$ at $150mA$ for V_{out1} and at $300mA$ for V_{out2}
- A digital potentiometer (D-POT) could be used with R network to dynamically tune the voltage outputs of the LDO using I^2C on $PF0{:}PF1$
- D-POT ($10\,k\Omega$ device) range to be used in the calculations is from $0\,k\Omega$ to $7\,k\Omega$, since its maximum resistance range is from $8\,k\Omega$ to $12\,k\Omega$
- MCP4661 has 257 taps

$$N = \frac{R_{MAX}}{R_{TOT}} * 256 = 179.2 \approx 179$$

$$R_{step} = \frac{R_{TOT}}{256} = 39\ \Omega$$

[2]: https://www.ti.com/lit/ug/tidu950/tidu950.pdf?ts=1661679201370&ref_url=https%253A%252F%252Fwww.google.com%252F

Resistance Calculations

- For $V_{1.8}$,

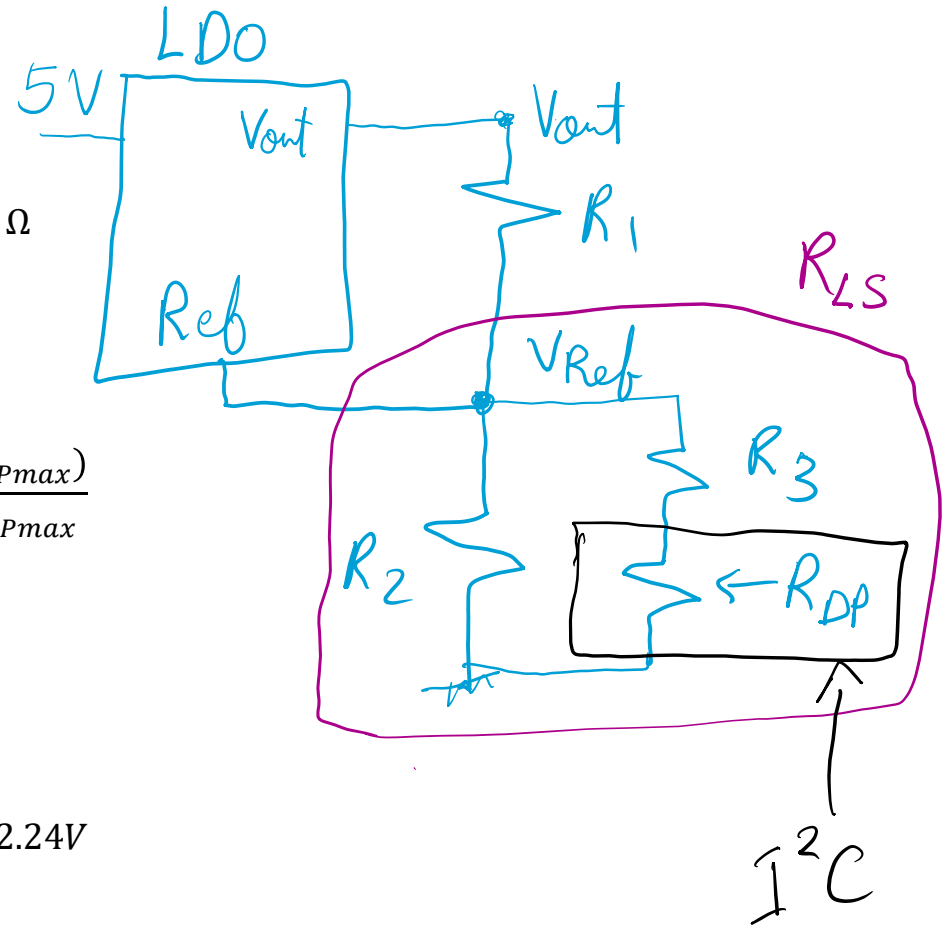
$$V_{out1min} = 1.4V \qquad V_{out1max} = 2.2V$$
$$R_{LSmax} = 3\ k\Omega \qquad V_{Ref} = 1.25V$$

$$V_{out1min} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmax}}\right) \quad \therefore R_1 = R_{LSmax}\left(\frac{V_{out1min}}{V_{Ref}} - 1\right) = 360\ \Omega$$

$$R_{LSmin} = R_1 * \left(\frac{V_{Ref}}{V_{out1max} - V_{Ref}}\right) = 473.7\Omega$$

$$R_{DPmin} = 0\ k\Omega \qquad R_{DPmax} = 7\ k\Omega$$

$$R_{LSmin} = \frac{R_2 * (R_3 + R_{DPmin})}{R_2 + R_3 + R_{DPmin}} = \frac{R_2 * R_3}{R_2 + R_3} \qquad R_{LSmax} = \frac{R_2 * (R_3 + R_{DPmax})}{R_2 + R_3 + R_{DPmax}}$$



Assume $R_3 = 500\ \Omega$,

$$R_2 = \frac{R_{LSmax} * (R_3 + R_{DPmax})}{(R_3 + R_{DPmax}) - R_{LSmax}} = 5\ k\Omega$$

Verify:

$$R_{LSmin} = \frac{R_2 * R_3}{R_2 + R_3} = 455\ \Omega \qquad \therefore V_{out2max} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmin}}\right) = 2.24V$$

Notes:

- **V_{Ref} is from the adjustable dual LDO (MIC2211) datasheet**
- **R_{LSmax} is set to ensure loop stability, not sure of the basis of this value**

Resistance Calculations

- **For $V_{3.3}$,**

$$V_{out2min} = 3V \qquad V_{out2max} = 3.6V$$
$$R_{LSmax} = 3\ k\Omega \qquad V_{Ref} = 1.25V$$
$$V_{out2min} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmax}}\right) \quad \therefore R_1 = R_{LSmax}\left(\frac{V_{out2min}}{V_{Ref}} - 1\right) = 4.2\ k\Omega$$
$$R_{LSmin} = R_1 * \left(\frac{V_{Ref}}{V_{out2max} - V_{Ref}}\right) = 2.2k\Omega$$
$$R_{DPmin} = 0\ k\Omega \qquad R_{DPmax} = 7\ k\Omega$$
$$R_{LSmin} = \frac{R_2 * (R_3 + R_{DPmin})}{R_2 + R_3 + R_{DPmin}} = \frac{R_2 * R_3}{R_2 + R_3} \qquad R_{LSmax} = \frac{R_2 * (R_3 + R_{DPmax})}{R_2 + R_3 + R_{DPmax}}$$

Assume $R_3 = 5\ k\Omega$,

$$R_2 = \frac{R_{LSmax} * (R_3 + R_{DPmax})}{(R_3 + R_{DPmax}) - R_{LSmax}} = 4\ k\Omega$$

Verify:

$$R_{LSmin} = \frac{R_2 * R_3}{R_2 + R_3} = 2.2\ k\Omega \qquad \therefore V_{out2max} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmin}}\right) = 3.64V$$

Notes:

- **V_{Ref} is from the dual LDO (MIC2211) datasheet**
- **R_{LSmax} is set to ensure loop stability in the TI note, not sure of the basis of this value**

Resistance Calculations

- **For nominal supplies:**

$$V_{out1} = 1.8V \qquad V_{out2} = 3.3V$$

$$R_{LS} = R_1 * \left(\frac{V_{Ref}}{V_{out} - V_{Ref}}\right)$$

$$\therefore R_{LS1} = 818.2\ \Omega \qquad \therefore R_{LS2} = 2.6\ k\Omega$$

$$R_{LS} = \frac{R_2 * (R_3 + R_{DP})}{R_2 + R_3 + R_{DP}} \qquad \therefore R_{DP} = \frac{R_{LS} * (R_2 + R_3) - R_2 R_3}{R_2 - R_{LS}}$$

$$\therefore R_{DP1} = 478\ \Omega \qquad \therefore R_{DP2} = 2.4k\Omega$$

$$R_{DP} = \frac{R_{TOT} N}{256} + R_W \qquad \therefore N = (R_{DP} - R_W) * \frac{256}{R_{TOT}}$$

$$R_W = 75\ \Omega \qquad R_{TOT} = 10\ k\Omega$$

$$\therefore N_1 = 10.3 \approx 11\ (Bh) \qquad \therefore N_2 = 59.5 \approx 60\ (3Ch)$$

Resistors Components

Output	Resistor	Computed Value	Size 0805 1%
V_{out1}	R_1	360 Ω	360 Ω
	R_2	5 $k\Omega$	4.99 $k\Omega$
	R_3	500 Ω	499 Ω
V_{out2}	R_1	4.2 $k\Omega$	4.22 $k\Omega$
	R_2	4 $k\Omega$	4.02 $k\Omega$
	R_3	5 $k\Omega$	4.99 $k\Omega$

Notes:

- **MIC2211 datasheet recommends that to prevent low quiescent current performance being compromised Resistor values are between 100kΩ and 500kΩ. This can't be achieved with the R_{LSmax} assumption**

Caravel + Nucleo Board Schematic

Notes:

- MCO clock is 8 MHz on $PF0$ and a timer should be used to supply the clock to caravel. I followed this and I connected the clock to $TIM3\_CH2$ on $PB5$ but I am not sure if this is the right way to do that
- Caravel SPI connected to SPI4 ($PE2$ $PE4$:$PE6$)and HKSPI to SPI5 ($PF6$:$PF9$)
- Caravel UART connected to UART3 ($PC10$:$PC11$)
- Caravel Reset with $\overline{RST}$
- Caravel remaining 32 I/Os connected to pins that have no conflict on them and in the WCSP package order
- I connected the supplies to external pin header with *gpio* and *xclk*
- Nucleo Board: NUCLEO144-F429ZI

Caravel + Nucleo Pinout

Caravel BB Pin	ST Morpho Pin
1: io[37]	98: PB15
2: io[36]	96: PB1
3: io[35]	94: PB2
4: io[34]	89: PB6
5: GND	88: PB12
6: vccd	-
7: vddio	-
8: GND	75: PB8
9: io[33]	88: PB12
10: io[32]	77: PB9
11: io[31]	76: PC6
12: io[30]	75: PB8
13: io[29]	74: PC8
14: io[28]	73: PC9

Caravel BB Pin	ST Morpho Pin
15: io[27]	4: PD2
16: io[26]	13: PA13
17: io[25]	15: PA14
18: io[24]	17: PA15
19: io[23]	28: PA0
20: io[22]	32: PA4
21: io[21]	35: PC2
22: io[20]	37: PC3
23: io[19]	38: PC0
24: io[18]	39: PD4
25: io[17]	40: PD3
26: io[16]	41: PD5
27: io[15]	42: PG2
28: io[14]	43: PD6

Caravel + Nucleo Pinout

Caravel BB Pin	ST Morpho Pin
29: io[13]	44: PG3
30: io[12]	45: PD7
31: io[11]	58: PG1
32: io[10]	59: PG0
33: io[9]	63: PG9
34: io[8]	64: PG15
35: io[7]	66: PG10
36: io[6]/tx	2: PC11
37: io[5]/rx	1: PC10
38: io[4]/SCK	11: PF7
39: io[3]/CSB	9: PF6
40: io[2]/SDI	54: PF8
41: io[1]/SDO	56: PF9
42: io[0]	65: PG12

Caravel BB Pin	ST Morpho Pin
43: vccd1	-
44: vdda1	-
45: vdda	-
46: Caravel/SCK	121: PE12
47: gpio	-
48: Caravel/D1	127: PE13
49: Caravel/D0	123: PE14
50: vccd	-
51: Caravel/CSB	128: PE11
52: xclk	101: PB5
53: NRST	14: NRST
54: vdda2	-
55: vddio	-
56: vccd2	-

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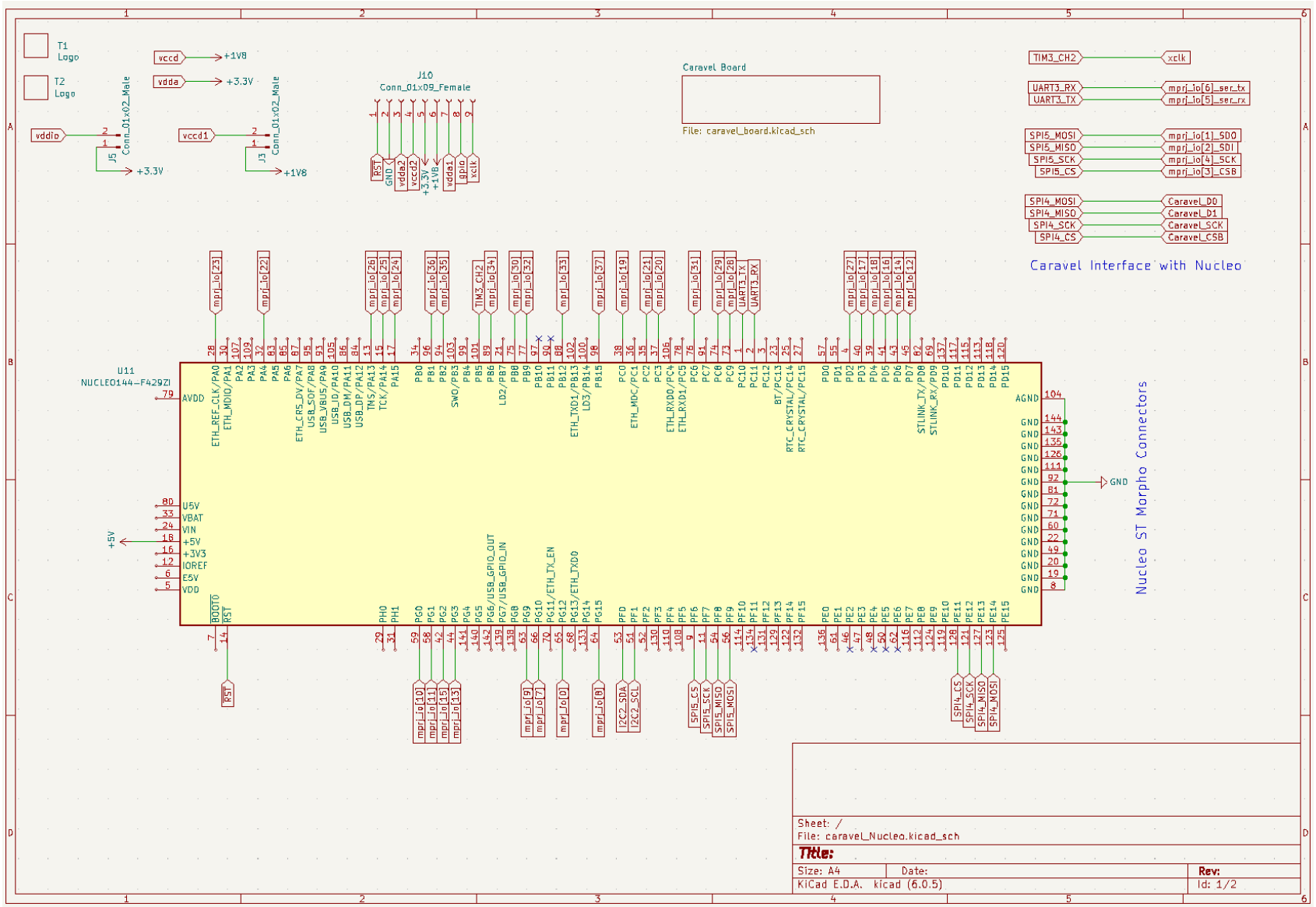

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