Caravel + Nucleo Board

Specifications

The board required features:

- **To be physically compatible to act as a hat to the ST Nucleo board using the ST morpho connectors (plug-in). This would provide test setups for characterizing IOs configuration using the Nucleo board**
- **Includes programmable power supply on board to test the Caravel chip at a range of power supplies**
- **The programmable power supply is programmed with SPI/I^2C**
- **It can function as a stand-alone Caravel evaluation board similar to the Caravel V4 evaluation board system**
- **The reset could be programmed and not only activated with the push-button**

Programmable Power Supply

- A programmable power supply is required to test the chip with non-nominal supplies
- The required ranges are from $1.4V$ to $2.2V$ for $V_{1.8}$ and $3V$ to $3.6V$ for $V_{3.3}$
- Adjustable dual LDO (MIC2211) is capable of suppling from $1.25V$ to $5V$ at $150mA$ for V_{out1} and at $300mA$ for V_{out2}
- A digital potentiometer (D-POT) MCP4661 could be used with R network to dynamically tune the voltage outputs of the LDO using I^2C interface
- D-POT ($10\,k\Omega$ device) range to be used in the calculations is from $0\,k\Omega$ to $7\,k\Omega$, since its maximum resistance range at temperature corners is $8\,k\Omega$ and $12\,k\Omega$
- MCP4661 has 257 taps

$$N = \frac{R_{MAX}}{R_{TOT}} * 256 = 179.2 \approx 179$$

$$R_{step} = \frac{R_{TOT}}{256} = 39\,\Omega$$

[1]: https://www.ti.com/lit/ug/tidu950/tidu950.pdf?ts=1661679201370&ref_url=https%253A%252F%252Fwww.google.com%252F

Resistance Calculations

- For $V_{1.8}$,

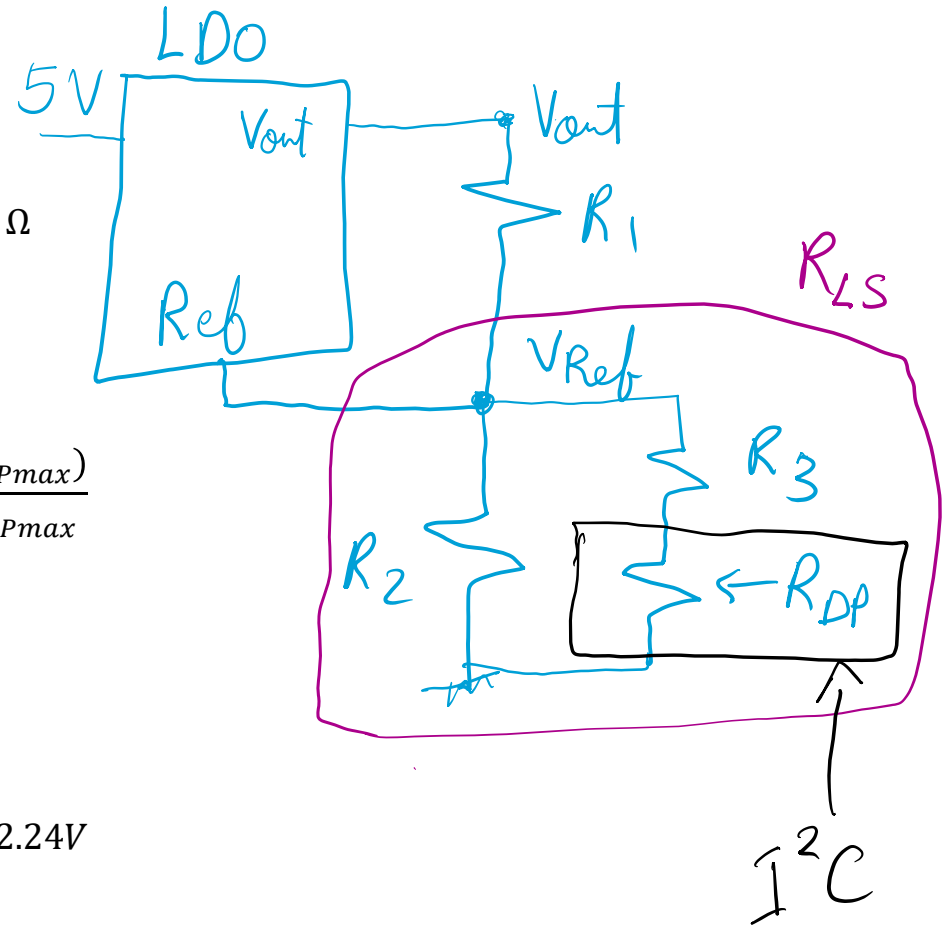
$$V_{out1min} = 1.4V \qquad V_{out1max} = 2.2V$$
$$R_{LSmax} = 3\ k\Omega \qquad V_{Ref} = 1.25V$$

$$V_{out1min} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmax}}\right) \quad \therefore R_1 = R_{LSmax}\left(\frac{V_{out1min}}{V_{Ref}} - 1\right) = 360\ \Omega$$

$$R_{LSmin} = R_1 * \left(\frac{V_{Ref}}{V_{out1max} - V_{Ref}}\right) = 473.7\Omega$$

$$R_{DPmin} = 0\ k\Omega \qquad R_{DPmax} = 7\ k\Omega$$

$$R_{LSmin} = \frac{R_2 * (R_3 + R_{DPmin})}{R_2 + R_3 + R_{DPmin}} = \frac{R_2 * R_3}{R_2 + R_3} \qquad R_{LSmax} = \frac{R_2 * (R_3 + R_{DPmax})}{R_2 + R_3 + R_{DPmax}}$$



Assume $R_3 = 500\ \Omega$,

$$R_2 = \frac{R_{LSmax} * (R_3 + R_{DPmax})}{(R_3 + R_{DPmax}) - R_{LSmax}} = 5\ k\Omega$$

Verify:

$$R_{LSmin} = \frac{R_2 * R_3}{R_2 + R_3} = 455\ \Omega \qquad \therefore V_{out2max} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmin}}\right) = 2.24V$$

Notes:

- **V_{Ref} is from the adjustable dual LDO (MIC2211) datasheet**
- **R_{LSmax} is set to ensure loop stability, not sure of the basis of this value**

Resistance Calculations

- **For $V_{3.3}$,**

$$V_{out2min} = 3V \qquad V_{out2max} = 3.6V$$
$$R_{LSmax} = 3\ k\Omega \qquad V_{Ref} = 1.25V$$
$$V_{out2min} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmax}}\right) \quad \therefore R_1 = R_{LSmax}\left(\frac{V_{out2min}}{V_{Ref}} - 1\right) = 4.2\ k\Omega$$
$$R_{LSmin} = R_1 * \left(\frac{V_{Ref}}{V_{out2max} - V_{Ref}}\right) = 2.2k\Omega$$
$$R_{DPmin} = 0\ k\Omega \qquad R_{DPmax} = 7\ k\Omega$$
$$R_{LSmin} = \frac{R_2 * (R_3 + R_{DPmin})}{R_2 + R_3 + R_{DPmin}} = \frac{R_2 * R_3}{R_2 + R_3} \qquad R_{LSmax} = \frac{R_2 * (R_3 + R_{DPmax})}{R_2 + R_3 + R_{DPmax}}$$

Assume $R_3 = 5\ k\Omega$,

$$R_2 = \frac{R_{LSmax} * (R_3 + R_{DPmax})}{(R_3 + R_{DPmax}) - R_{LSmax}} = 4\ k\Omega$$

Verify:

$$R_{LSmin} = \frac{R_2 * R_3}{R_2 + R_3} = 2.2\ k\Omega \qquad \therefore V_{out2max} = V_{Ref}\left(1 + \frac{R_1}{R_{LSmin}}\right) = 3.64V$$

Notes:

- **V_{Ref} is from the dual LDO (MIC2211) datasheet**
- **R_{LSmax} is set to ensure loop stability in the TI note, not sure of the basis of this value**

Resistance Calculations

- **For nominal supplies:**

$$V_{out1} = 1.8V \qquad V_{out2} = 3.3V$$

$$R_{LS} = R_1 * \left(\frac{V_{Ref}}{V_{out} - V_{Ref}}\right)$$

$$\therefore R_{LS1} = 818.2\ \Omega \qquad \therefore R_{LS2} = 2.6\ k\Omega$$

$$R_{LS} = \frac{R_2 * (R_3 + R_{DP})}{R_2 + R_3 + R_{DP}} \qquad \therefore R_{DP} = \frac{R_{LS} * (R_2 + R_3) - R_2 R_3}{R_2 - R_{LS}}$$

$$\therefore R_{DP1} = 478\ \Omega \qquad \therefore R_{DP2} = 2.4k\Omega$$

$$R_{DP} = \frac{R_{TOT} N}{256} + R_W \qquad \therefore N = (R_{DP} - R_W) * \frac{256}{R_{TOT}}$$

$$R_W = 75\ \Omega \qquad R_{TOT} = 10\ k\Omega$$

$$\therefore N_1 = 10.3 \approx 11\ (Bh) \qquad \therefore N_2 = 59.5 \approx 60\ (3Ch)$$

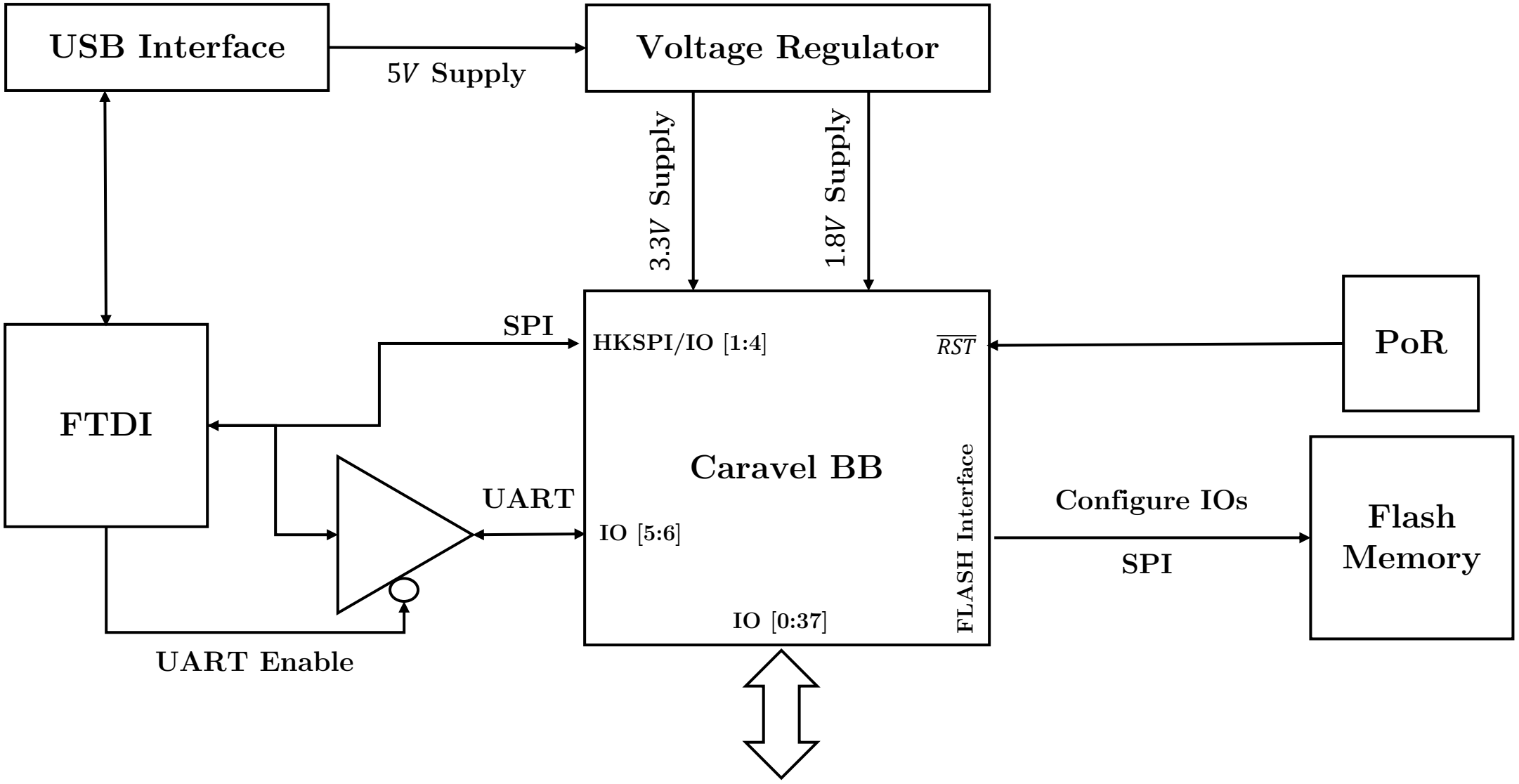
Resistors

Output	Resistor	Computed Value	Size 0805 1%
V_{out1}	R_1	360 Ω	360 Ω
	R_2	5 $k\Omega$	4.99 $k\Omega$
	R_3	500 Ω	499 Ω
V_{out2}	R_1	4.2 $k\Omega$	4.22 $k\Omega$
	R_2	4 $k\Omega$	4.02 $k\Omega$
	R_3	5 $k\Omega$	4.99 $k\Omega$

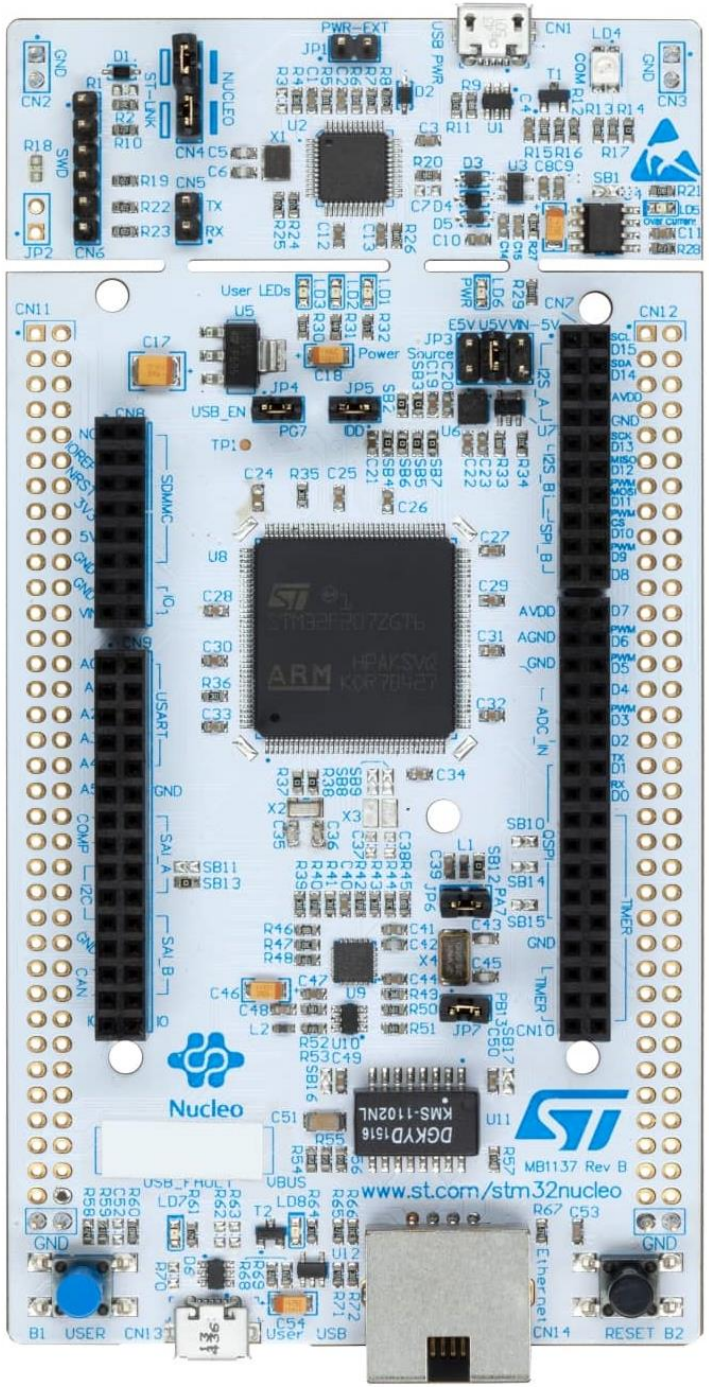
Notes:

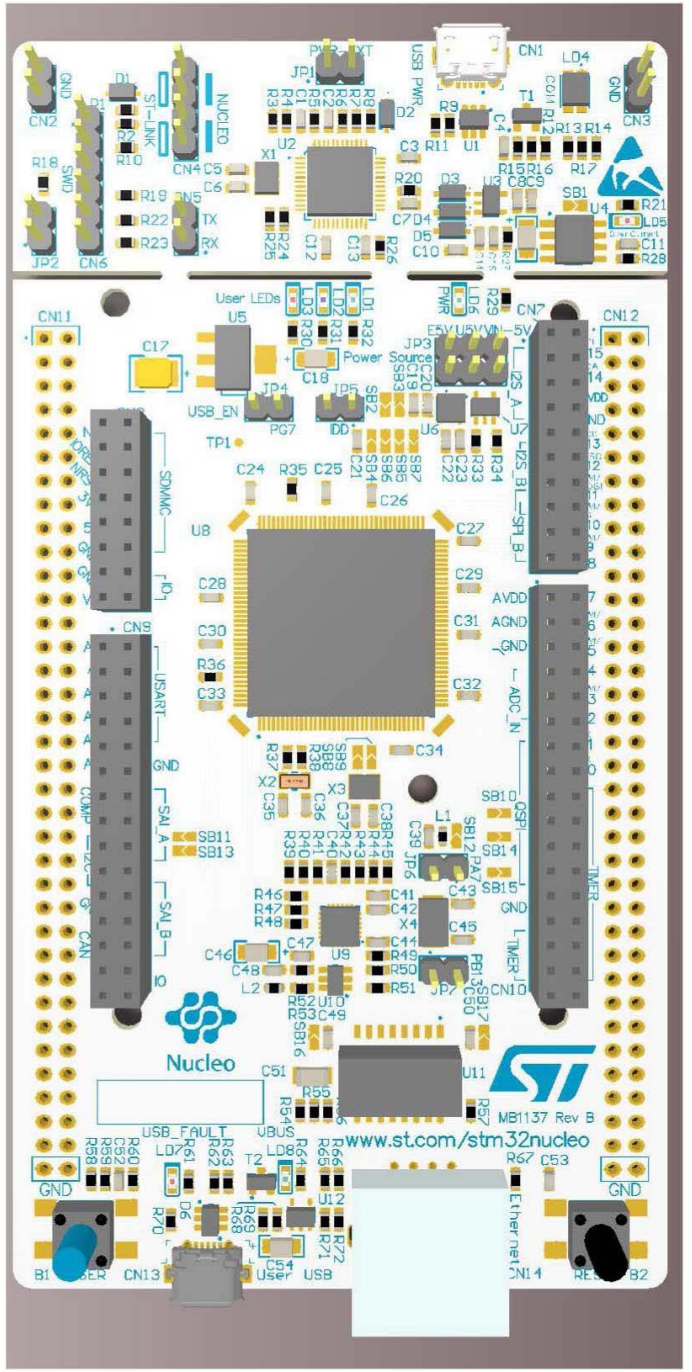
- **MIC2211 datasheet recommends the resistor values should be between 100kΩ and 500kΩ to prevent compromising the low quiescent current performance. This can't be achieved with the R_{LSmax} assumption**

Caravel Board V4 Block Diagram



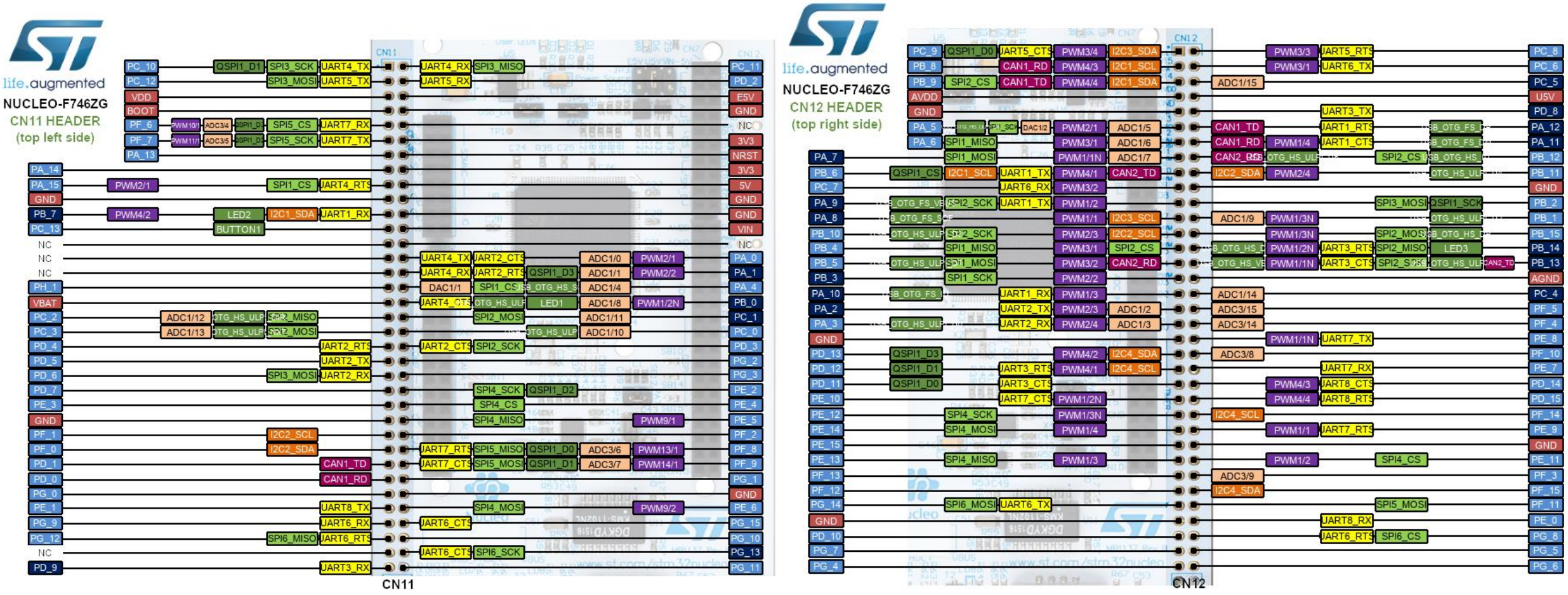
Nucleo Board: NUCLEO144-F746ZG





[2]: https://www.st.com/en/evaluation-tools/nucleo-F746ZG.html

Nucleo Board: ST Morpho Connectors



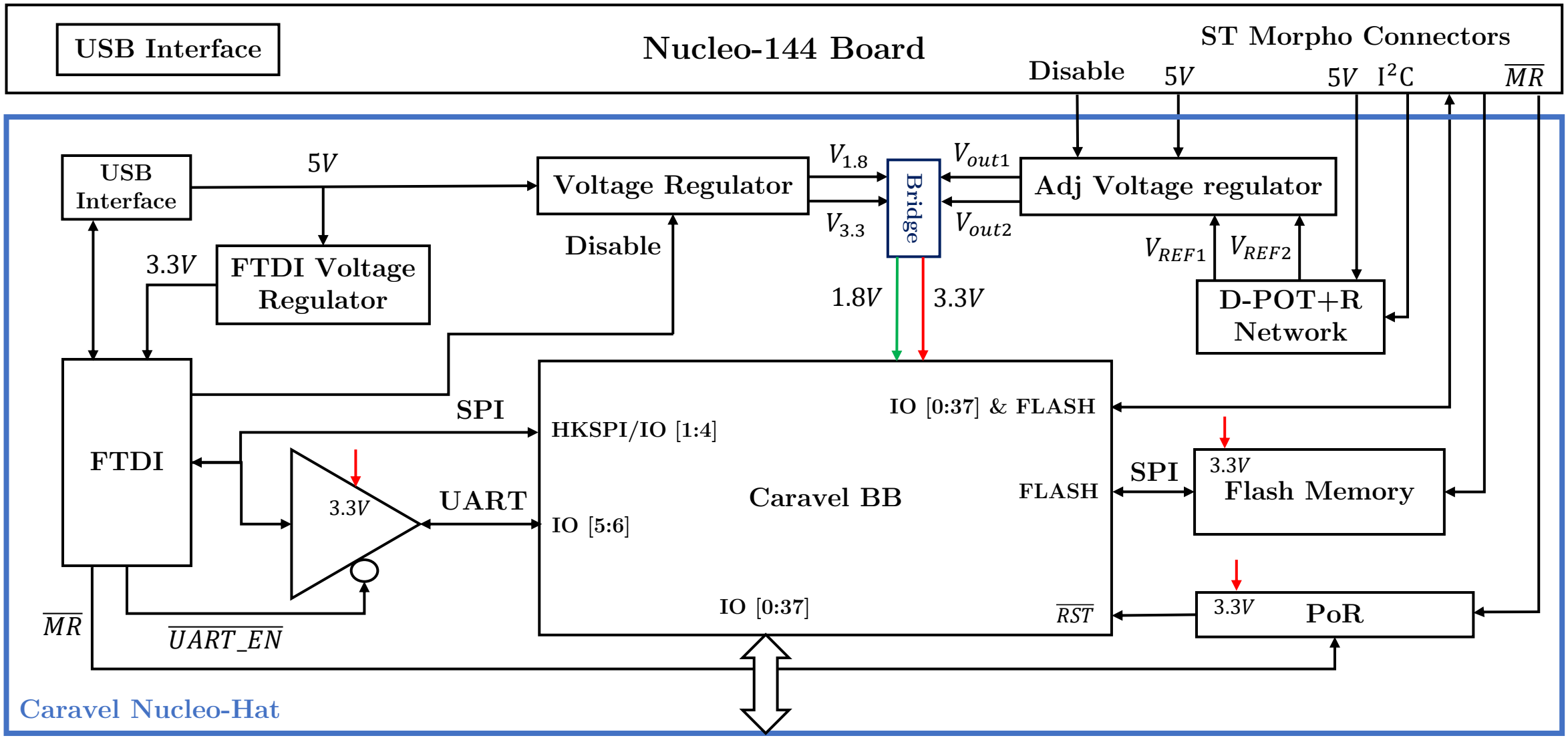
[3]: https://os.mbed.com/platforms/ST-Nucleo-F746ZG/#board-pinout

Nucleo Board: Interface with Caravel

Nucleo Board: NUCLEO144-F746ZG

- **$CN4$ jumpers in ST-Link part is used to program STM32 MCU**
- **The board is used as a test setup for characterizing the I/O configuration**
- **The board has a 3.3V Regulator (Max $500mA$)**
- **Default clock supply is $8\,MHz$ from ST-Link on $PH0$**
- **Caravel FLASH/HKSPI interface could be connected to STM32 MCU SPI interfaces**
- **Caravel UART interface could be connected to STM32 MCU interface**
- **$PA13$ and $PA14$ are shared with SWD signals connected to ST-LINK. If ST-LINK part is not cut, it is not recommended to use them as I/Os.**

Caravel + Nucleo Board Block Diagram

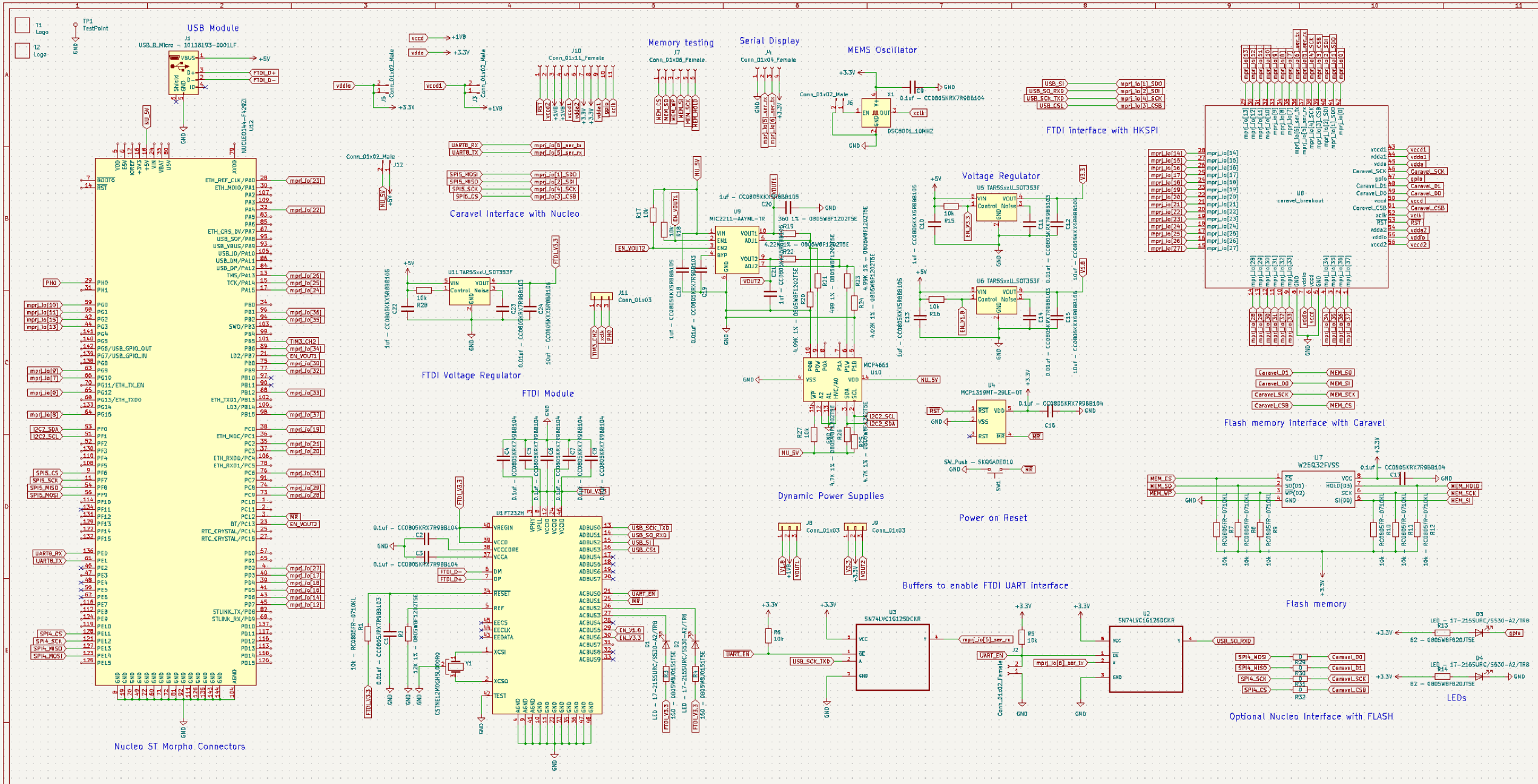


Caravel + Nucleo Board Schematic

Notes:

- Default clock is 8 MHz on $PH0$ and a timer could be used to supply the clock to caravel as a PWM signal for example, $TIM3\_CH2$ on $PB5$
- Caravel FLASH connected to SPI4 ($PE2$ $PE4{:}PE6$)
- Caravel HKSPI to SPI5 ($PF6{:}PF9$)
- Caravel UART connected to UART8 ($PE0{:}PE1$)
- The manual reset $\overline{MR}$ is connected to $PC12$
- Caravel remaining 32 I/Os connected to ST Morpho pins that have no conflict on them and support the order of the breakout board pinout
- The supplies are connected to external pin header J10 with $gpio$, $xclk$ and $\overline{RST}$
- Nucleo Board: NUCLEO144-F746ZG
- Cravel Breakout Board: V2 breakout board with Caravel WCSP chip
- J4 connector is available to support connecting a serial display easily
- J10 connector is available to support testing the flash memory pins

Caravel + Nucleo Board Schematic



Caravel + Nucleo Board Components

Component	Reference	Description
MCP1319MT-29LE-OT	U4	Power on Reset (PoR) circuit with internal pull-up resistors
TAR5SxxU_SOT353F	U5 & U6	Fixed voltage regulators that provide $1.8V$ and $3.3V$. The footprint is the same for a wide range of LDO devices from 1.5V to 5V which allows installing $1.6V$ LDO in place of the $1.8V$ for example
MIC2211-AAYML-TR	U9	Adjustable voltage regulator that is used to provide a programmable power supply by adjusting the resistors of each output. It is supplied with $5V$ from the Nucelo Board
MCP4661	U10	Digital Potentiometer that is programmed using I^2C interface to provide desired resistive loads for U9 to achieve the programmable power supply. It also has an EEPROM which allows stand-alone operation after saving the desired values. It is supplied with $5V$ from the Nucelo Board
NUCLEO144-F429ZI	U11	The Nucleo-144-F429ZI board ST Morpho connectors that has 144 pins interfacing with STM32 MCU

Caravel + Nucleo Pinout

Caravel BB Pin	ST Morpho Pin
1: io[37]	98: PB15
2: io[36]	96: PB1
3: io[35]	94: PB2
4: io[34]	89: PB6
5: GND	GND
6: vccd	-
7: vddio	-
8: GND	GND
9: io[33]	88: PB12
10: io[32]	77: PB9
11: io[31]	76: PC6
12: io[30]	75: PB8
13: io[29]	74: PC8
14: io[28]	73: PC9

Caravel BB Pin	ST Morpho Pin
15: io[27]	4: PD2
16: io[26]	13: PA13
17: io[25]	15: PA14
18: io[24]	17: PA15
19: io[23]	28: PA0
20: io[22]	32: PA4
21: io[21]	35: PC2
22: io[20]	37: PC3
23: io[19]	38: PC0
24: io[18]	39: PD4
25: io[17]	40: PD3
26: io[16]	41: PD5
27: io[15]	42: PG2
28: io[14]	43: PD6

Caravel + Nucleo Pinout

Caravel BB Pin	ST Morpho Pin
29: io[13]	44: PG3
30: io[12]	45: PD7
31: io[11]	58: PG1
32: io[10]	59: PG0
33: io[9]	63: PG9
34: io[8]	64: PG15
35: io[7]	66: PG10
36: io[6]/tx	136:PE0
37: io[5]/rx	61: PE1
38: io[4]/SCK	11: PF7
39: io[3]/CSB	9: PF6
40: io[2]/SDI	54: PF8
41: io[1]/SDO	56: PF9
42: io[0]	65: PG12

Caravel BB Pin	ST Morpho Pin
43: vccd1	-
44: vdda1	-
45: vdda	-
46: Caravel/SCK	121: PE12
47: gpio	-
48: Caravel/D1	127: PE13
49: Caravel/D0	123: PE14
50: vccd	-
51: Caravel/CSB	128: PE11
52: xclk	-
53: NRST	-
54: vdda2	-
55: vddio	-
56: vccd2	-

Caravel + Nucleo Board Power Supply

Mode	Main Power	Power Domains	Jumper State	Components	Notes
HAT	Nucleo Board $5V$	U9: $3.3V$	J9: 2 to 3 (HAT)	Caravel, FLASH, buffers, X1	Programmable
		U9: $1.8V$	J8: 2 to 3 (HAT)	Caravel	Programmable
MAIN	USB Module $5V$	U5: $3.3V$	J9: 2 to 1 ($MAIN$)	Caravel, FLASH, buffers, X1	Fixed
		U9: $3.3V$	J9: 2 to 3 (HAT) J12: 1 to 2 (NU_$5V$)	Caravel, FLASH, buffers, X1	Fixed: DVS saved setting
		U11: $3.3V$	–	FTDI	
		U6: $1.8V$	J8: 2 to 1 ($MAIN$)	Caravel	Fixed
		U9: $1.8V$	J9: 2 to 3 (HAT) J12: 1 to 2 (NU_$5V$)	Caravel	Fixed: DVS saved setting

- Both modes support supplying $3.3V$ and $1.8V$ externally through J10 pins and leaving J8 and J9 floating

Caravel + Nucleo Board Reset

Mode	Reset Mechanism	Pin Activated
HAT	SW1 Push-Button	PoR: $\overline{MR}$
	Nucleo Program configures PC12	PoR: $\overline{MR}$
	Externally through J10	$\overline{RESET}$
MAIN	SW1 Push-Button	PoR: $\overline{MR}$
	FTDI Program configures ACBUS1	PoR: $\overline{MR}$
	Externally through J10	$\overline{RESET}$

Caravel + Nucleo Board Modes

MAIN mode:

- **The board is programmed through the USB module communicating with the FTDI.**
- **The $5V$ supply is provided from the USB module to power the fixed voltage supplies (U5 and U6) which in turn power up the other system components except for the programmable power supply.**
- **J8 and J9 are set to connect pin 2 to pin 1 ($MAIN$).**
- **J8 and J9 are left floating if the $3.3V$ and $1.8V$ are to be supplied externally.**
- **J11 is left with no connections as the clock is driven from X1 with $10MHz$ frequency.**
- **Other frequencies could be supported by disabling X1 through J6 and driving the clock externally.**
- **To reset the board, use SW1 button or FTDI $ACBUS1$.**
- **By default, the FTDI interface with the Caravel HKSPI. To switch to the UART interface of Caravel, set $\overline{UART\_EN}$ to 0 either using J2 or the FTDI $ACBUS0$**
- **To use the programmable power supplies saved setting instead of the fixed voltage supplies:**
  1. **connect pin 2 to pin 3 on J8 and J9 (HAT).**
  2. **connect J12 pins to provide the $5V$ supply to U9 and U10 (short $5V$ with NU_5V).**

Caravel + Nucleo Board Modes

HAT mode:

- **The board acts as a hat for Nucleo-144 test setup.**
- **The $5V$ supply is provided from the Nucleo board to power the programmable power supply (U9 and U10) which in turn power up the other system components except for the fixed power supply and the FTDI module.**
- **U10 is programmed from the Nucleo using I^2C interface to provide the desired supplies**
- **J8 and J9 are set to connect pin 2 to pin 3 (HAT).**
- **The clock could be driven from the Nucleo through J11 with either of the following:**
  1. **connect pin 2 to pin 1 to drive it as a PWM signal generated from Timer 3.**
  2. **connect pin 2 to pin 3 to drive it from the default clock of the MCO output of ST-LINK with a fixed $8MHz$ frequency.**
- **J6 is set to disable X1 in the case of driving the clock with J11.**
- **To reset the board, use the Nucleo to program $PC12$ or SW1 button.**

Caravel + Nucleo Board PCB

Dimensions:
$68.072 * 92.0128\ mm^2$