TNETV1060 Communications Processor for VoIP Gateway Applications

Data Manual

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1 TNETV1060 Features

MIPS32™ 4KEc™ 32-Bit Reduced Instruction Set Computer (RISC) Processor

- 165 MHz Providing up to 223 Dhrystone Million Instructions Per Second (MIPS)
- 16K-Byte Four-Way Set Associative Instruction Cache
- 16K-Byte Four-Way Set Associative Data Cache
- Programmable Memory Management Unit (MMU)
- 4K-Byte Random-Access Memory (RAM) On Chip
- 4K-Byte Read-Only Memory (ROM) On Chip With Boot Code
- Interrupt Handler
  - 40 Primary Interrupts With Programmable Priority
  - 5 Primary Interrupts May Be Sourced Externally
  - 32 Secondary Interrupts With Fixed Priority
- Three 16-Bit Timers With Prescaled Clock
  - Two Universal Timers
  - One Dedicated Watchdog Timer
- Enhanced JTAG IEEE Std 1149.1 Debug Interface

Digital Signal Processor (DSP) C55x™

- 125 MHz Providing up to 250 MIPS
- 12K-Word Two-Way Set Associative Instruction Cache
- 64K-Word RAM On Chip
  - 32K-Word Dual Access
  - 32K-Word Single Access
- Interrupt Handler
- Two 16-Bit Timers With Prescaled Clock
  - One Universal Timer
  - One Dedicated Watchdog Timer
- Universal Four-Channel Direct Memory Access (DMA) Controller
- Dedicated Peripheral DMA Controller
- JTAG IEEE Std 1149.1 Debug Interface

On-Chip Peripherals

- External Memory Interface (EMIF) Supports:
  - Two SDRAM Chip Selects Providing 128M Byte
  - Three Chip Selects Providing 16M-Byte Each RAM or ROM
  - One Chip Select Providing 32M-Byte Flash
- Universal Four-Channel DMA Controller
- 52 General-Purpose Input/Output (GPIO) Signals
  - 8 GPIOs (Primary I/O Functions)
  - 44 GPIOs (Secondary I/O Functions)
- Keypad Interface Featuring:
  - 8 × 8 Matrix Accommodating 64 Keys
  - Expanded Key Range With GPIO
  - Hardware Debounce Feature
- Universal Asynchronous Receiver/Transmitter (UART) With Hardware Automatic Flow Control
- Sequencer-Based Serial Port Providing Programmable Configuration for Standard Serial Interfaces
  - Serial Port Interface (SPI)
  - Inter-Integrated Circuit (I^2C)
  - Microwire™
  - Numerous Standard and Nonstandard Variations
- VLYNQ™ Serial Communication Port Featuring One 5-Terminal Port
- Liquid Crystal Display (LCD) Controller Supports:
  - Alphanumeric Character Displays
  - Rasterized Graphic Displays up to 1024 × 1024 Pixels
  - Micro-Interface Graphic Displays

Ethernet Subsystem

- **Two Ethernet Ports Each Featuring:**
  - **Integrated IEEE Std 802.3/802.3u 10/100 Base-T PHY in Both Half and Full Duplex**
    - **Auto Negotiation**
    - **Parallel Detection**
    - **Support IEEE Std 802.3af Inline Power Through Glueless Connection to TI TPS2375**
  - **Integrated Ethernet Media Access Controller (MAC)**
    - **Full Duplex**
    - **Jumbo Packet**
    - **Copy Short/Error Frames**
    - **Hardware Flow Control**
    - **Address Filtering (Unicast, Multicast, Broadcast, or Promiscuous Mode)**
  - **External Media Independent Interface (MII) and LED Status Indicators Available**
  - **Remote Network Monitoring (RMO) Management Information Base (MIB) Statistics Gathering Registers**
- **Three-Port Wire-Speed Ethernet Switch Featuring:**
  - **Layer-2 Ethernet Switch Functionality**
  - **IEEE Std 802.1p With up to Eight Configurable Prioritization Queues Including Priority Regeneration**
  - **Nonblocking Architecture to Ensure Fast Packet Delivery With up to 64 MAC Address Table Lookup and Packet Forwarding Via Store-and-Forward Architecture**
  - **Software Management Capabilities**
    - **IEEE Std 802.1D Spanning Tree Protocol (STP)**
    - **IEEE Std 802.1Q With Shared and Independent Virtual Local Area Network (VLAN) Learning (SVL/IVL) for up to 16 File Identifications (FIDs)**
    - **VLAN Tag Insertion/Deletion Based on Port VLAN Parameters**
    - **GARP Multicast Registration Protocol (GMRP) Support**
  - **Broadcast Storm Protection**
  - **Dedicated 32K-Byte Packet Memory With Automated Remote Overflow Expandability**
  - **64-Bit $\times$ 64-Bit Content Addressable Memory (CAM)**
  - **Dedicated Host DMA Controller**

Additional System Information

- **324-Terminal Plastic Ball Grid Array (PBGA) Package**
- **3.3-V I/O Supply Input Voltage**
- **Integrated Voltage Regulator for 1.5-V Core Supply**
- **1.4-W Typical Power Consumption**

1.1 Description

The TNETV1060 is a communications processor based on a MIPS32™ reduced instruction set computer (RISC) processor along with a C55x™ digital signal processor (DSP). This device has a rich peripheral set architected specifically for voice over internet protocol (VoIP) customer premise equipment (CPE) gateway applications, reducing bill of materials (BOM), time, and complexity, to develop a residential small office, home office (SOHO) gateway product with up to four low-bit-rate channels.

The TNETV1060 combines the key processor, communication, and peripheral functions necessary to build a complete CPE gateway solution. The TNETV1060 architecture uses advanced design features to provide flexibility and performance throughput, while conserving power consumption. Combined with Telogy Software™ for gateway applications, the TNETV1060 provides a complete hardware/software solution capable of reducing system design cycle times.

- The RISC processor supplies the overall system services and performs user interface, network management, protocol stack management, call management, and task scheduling functions. The DSP provides real-time telephony processing that drives the voice, FAX, and signal units.
- Two 10/100 Base-T Ethernet media access controllers (MACs) and physical interfaces (PHYs) are attached to an integrated layer-2 three-port Ethernet switch, providing a complete Ethernet solution for telephony applications.
- Gateway designs are simplified through on-chip peripherals such as a VLYNQ™ interface, programmable serial port, and several general-purpose inputs/outputs (GPIOs).
- The external McBSP serial interface and telephony interface provide glueless attachment to a wide variety of telephony peripherals. These two interfaces are capable of supplying the necessary pulse-code modulation (PCM) signaling and control signaling needed to drive most central-office coder/decoder (codec), PCM codec, filter combo, or line-card codec devices, providing a gateway to the two-wire analog public telephone system.

1.2 TNETV1060 Functional Block Diagram

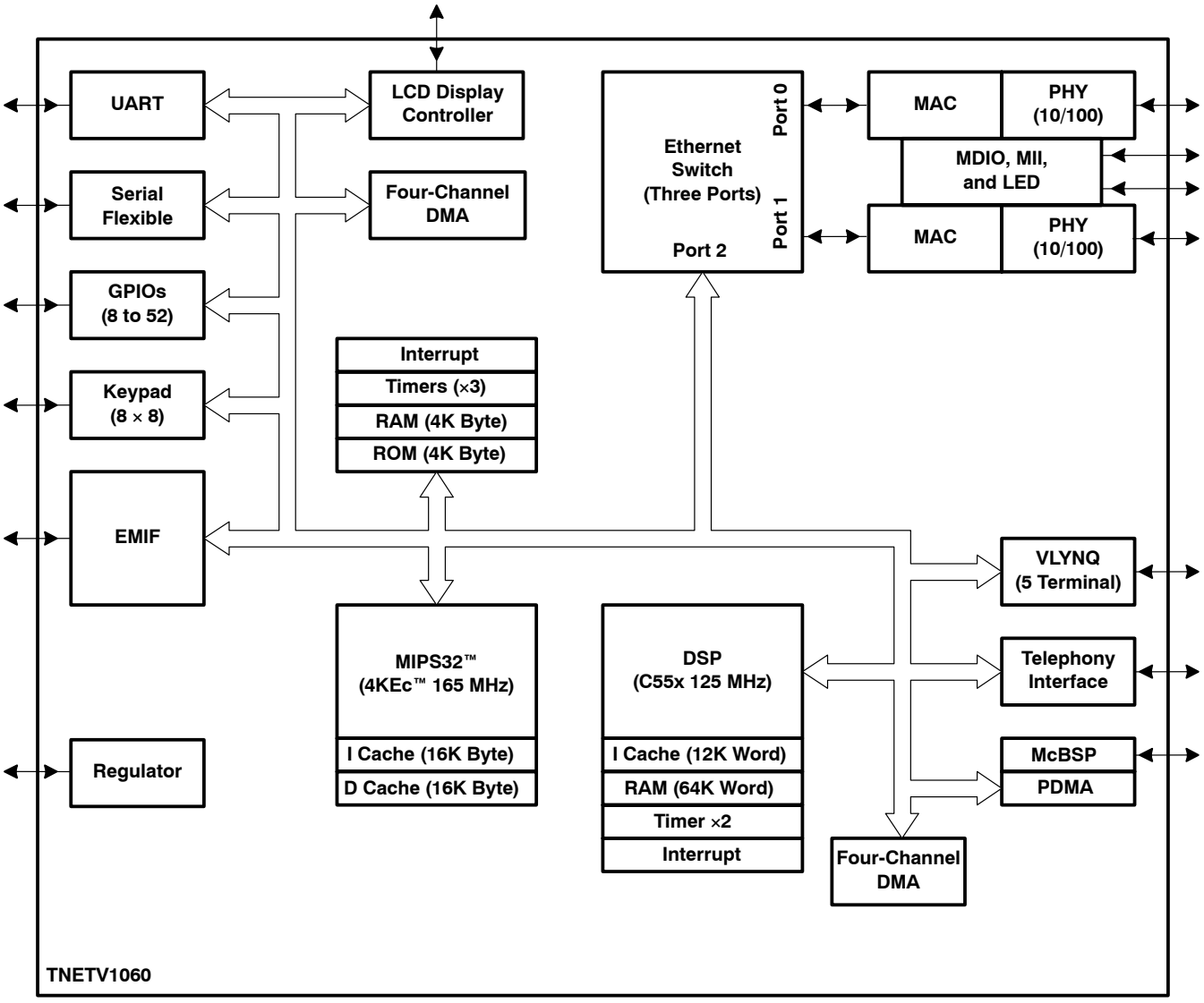


Figure 1–1. TNETV1060 Functional Block Diagram

2 Introduction

The TNETV1060 is a communications processor consisting of a MIPS32 RISC and a C55x DSP. Also included are integrated peripherals designed for VoIP CPE gateway applications.

The highly integrated features of the TNETV1060 support rapid implementation of VoIP CPE gateway residential SOHO solutions through software-differentiated control as described in the following items:

- MIPS32 RISC processor

  The MIPS32 processor functions as the master controller providing the overall system services, including the bootstrap loader and the real-time operating system (RTOS). This processor also performs network-manager, call-manager, and application-manager functions. The network manager handles standard network protocol stacks (H.323, SIP, and MGCP). The call manager handles telephony protocols including call setup and teardown. The application manager provides a control mechanism for interfaces and functions in the TNETV1060 that provide value beyond a basic telephony product (LCD, VLYNQ, UART, and serial port).

- DSP

  This DSP functions as the real-time voice controller. Activity for this processor includes PCM data reception, tone generation, acoustic echo cancellation/suppression, voice activity detection, voice playout, jitter buffer management, silence suppression, and a variety of voice-compression options. This processor has the capability to provide features for deluxe telephony products such as full-duplex speakerphones, three-way conferencing, wideband codec requirements, and fax requirements.

- Ethernet subsystem

  The integrated features of the Ethernet subsystem provide a complete Ethernet solution for telephony applications. The three-port switch provides one internal path to the TNETV1060 applications and two external paths. The external paths run through IEEE Std 802.3-compliant MACs and IEEE Std 802.3/802.3u-compliant 10/100 Base-T physical layer devices (PHYs). Logical features supported by this Ethernet solution include IEEE Std 802.1p prioritization queues, IEEE Std 802.1D spanning tree protocol, IEEE Std 802.1Q virtual local area network (VLAN) support (both shared and independent), GARP multicast registration protocol (GMRP) support, and broadcast storm protection.

- Telephony subsystem

  The integrated features of this subsystem provide a complete telephony solution for voice and fax applications.

- On-chip peripherals

  The TNETV1060 includes a wide range of integrated peripherals that provide value beyond a basic processor. Included in this list of peripherals is an LCD controller capable of providing glueless attachment to a wide range of displays. The VLYNQ interface provides a standard high-speed serial interface to a variety of TI devices that can supplement the processing power or external connectivity of the TNETV1060. Additional serial port attachment is provided through the UART and sequencer serial port (SSP) interfaces. The SSP may be programmed to interface to a variety of standard (I^2C, SPI, or IDM-2) and nonstandard external serial devices.

3 Terminal Definitions

The TNETV1060 is packaged in a 324-terminal plastic ball grid array (PBGA). Package details are provided in section 6, *Mechanical Specification*. A top view of the 324-terminal PBGA package showing all of the primary TNETV1060 I/O terminals is shown in Figure 3–1. In addition to the primary (1st) I/O functions shown in Figure 3–1, many TNETV1060 I/O terminals have a secondary (2nd) or even tertiary (3rd) functions. All of these multifunctional I/O terminals are listed in Table 3–2. TNETV1060 PBGA I/Os (sorted by terminal) are listed in Table 3–2.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22	VSS	VSS	EM_A19	EM_A16	EM_A12	EM_A08	EM_A05	EM_A02	TELE_CLK_O	TELE_RESET	TELE_RING IN4	TELE_RING IN2	REF_CLK_O	REF_CLK_I	P1_TX_P	P1_TX_M	VDDA_PHY1_1	P0_TX_M	P0_TX_P	VR_BASE 3	P1_FDUP LEX	P1_ACTI VITY	22
21	VSS	VSS	EM_A20	EM_A17	EM_A13	EM_A09	EM_A06	EM_A03	EM_A00	TELE_INT	TELE_RING IN3	TELE_RING IN1	VSS_REF_CLK	ALT_CLK_I	VSS_PHY1_1	VSS_PHY1_1	VDDA_PHY0_1	VSS_PHY0_1	VSS_PHY0_1	PHY_TEST	P1_LINK	P1_100MB	21
20	EM_A23	EM_A22	VSS	EM_A18	EM_A14	EM_A10	EM_A07	EM_A04	EM_A01	TELE_CS	TELE_FS	TELE_DO	TELE_DI	VDDA_PHY1_34	VSS_PHY1_34	VSS_PHY1_2	VDDA_PHY0_2	VSS_PHY0_2	VSS_PHY0_34	VDDA_PHY0_34	P0_FDUP LEX	P0_ACTI VITY	20
19	EM_D01	EM_D00	EM_A21	VSS	EM_A15	EM_A11	VDDS	VDDS	VDDS	VDDS	TELE_CLK_I	TELE_DCLK	VDD_PLL	P1_RX_P	P1_RX_M	VSS_PHY1_ESD	VDDA_PHY1_2	VSS_PHY0_ESD	P0_RX_M	P0_RX_P	P0_LINK	P0_100MB	19
18	EM_D04	EM_D05	EM_D03	EM_D02															PHY_REF	PHY_REF_RTN	LCD_D15	LCD_D14	18
17	EM_D08	EM_D09	EM_D07	EM_D06															LCD_D13	LCD_D12	LCD_D11	LCD_D10	17
16	EM_D11	EM_D12	EM_D10	VDDS															VDDS	LCD_D09	LCD_D08	LCD_D07	16
15	EM_D14	EM_D15	EM_D13	VDDS															VDDS	LCD_D06	LCD_D05	LCD_D04	15
14	EM_D17	EM_D18	EM_D16	VDDS					VSS	VDD	VDD	VDD	VDD	VSS_PLL					VDDS	LCD_D03	LCD_D02	LCD_D01	14
13	EM_D20	EM_D21	EM_D19	VDDS					VDD	VSS	VSS	VSS	VSS	VDD					VDDS	LCD_D00	LCD_VSYNC_A	LCD_E1	13
12	EM_D24	EM_D25	EM_D23	EM_D22					VDD	VSS	VSS	VSS	VSS	VDD					LCD_HSYNC_W	LCD_PIXEL_STRB	LCD_BIAS_E0	KEY PAD 15	12
11	EM_D28	EM_D29	EM_D27	EM_D26					VDD	VSS	VSS	VSS	VSS	VDD					KEY PAD 13	KEY PAD 14	KEY PAD 12	KEY PAD 11	11
10	EM_D30	EM_D31	EM_WE_DQM0	VDDS					VDD	VSS	VSS	VSS	VSS	VDD					VDDS	KEY PAD 10	KEY PAD 09	KEY PAD 08	10
9	EM_WE_DQM3	EM_WE_DQM2	EM_WE_DQM1	VDDS					VSS	VDD	VDD	VDD	VDD	VSS_AIC_CLK					VDDS	KEY PAD 07	KEY PAD 06	KEY PAD 05	9
8	EM_CS2	EM_CS1	EM_CS0	VDDS															N/C	KEY PAD 04	KEY PAD 03	KEY PAD 02	8
7	EM_CS5	EM_CS4	EM_CS3	VDDS															N/C	N/C	KEY PAD 01	KEY PAD 00	7
6	EM_RAS	EM_WAIT	EM_HIZ	EM_CLK															N/C	N/C	VR_ENBL	VR_BASE1	6
5	EM_CAS	EM_OE	EM_RW	EM_CKE															N/C	N/C	N/C	N/C	5
4	EM_WE	UART_RX	UART_TX	VSS	SSP 3	TEST	VDDS	VDDS	VDDS	VDDS	N/C	N/C	VDDS	VDDS	N/C	N/C	N/C	N/C	VSS_AIC	N/C	N/C	N/C	4
3	UART_RTS	UART_CTS	VSS	SSP 0	EJTAG_DINT	EJTAG_TRST_0	EJTAG_TDI	JTAG_EMU0	JTAG_TCK	VLYNQ 5_CLK	N/C	McBSP_CLK_RX	McBSP_D_RX	McBSP_FS_TX	GPIO 0	GPIO 1	GPIO 2	N/C	N/C	VSS_AIC	N/C	N/C	3
2	VSS	VSS	RE_SET_O	SSP 2	EJTAG_SYSRST	EJTAG_TCK	EJTAG_TMS	JTAG_TRST	JTAG_TD0	VLYNQ 5_RX_D0	VLYNQ 5_TX_D0	N/C	McBSP_CLK_TX	McBSP_FS_RX	VR_BASE 2	GPIO 3	GPIO 4	GPIO 5	N/C	N/C	VSS_AIC	VSS_AIC	2
1	VSS	VSS	RE_SET_I	SSP 1	EJTAG_TRST 1	EJTAG_TD0	JTAG_EMU1	JTAG_TDI	JTAG_TMS	VLYNQ 5_RX_D1	VLYNQ 5_TX_D1	N/C	N/C	McBSP_D_TX	AIC_CLK_I	AIC_CLK_O	GPIO 6	GPIO 7	N/C	N/C	VSS_AIC	VSS_AIC	1

Figure 3–1. TNETV1060 324-Terminal PBGA I/O Assignments, Top View

3.1 Functional Symbol Definitions

Use the following functional symbol definitions when reading section 3.2, *Terminal Assignments*, and section 3.3, *Signal Descriptions*.

Table 3–1. I/O Functional Symbol Definitions

FUNCTIONAL SYMBOL	DEFINITION	TABLE 3–2 COLUMN HEADINGS
I	Input	Type
O	Output	Type
P	Power input voltage terminal highlighting I/O (3.3 V), core (1.5 V), and analog voltages	Type
G	Ground input voltage terminal highlighting both digital and analog grounds	Type
N/C	No connection. Do not bias or use as a routing point.	Type
U	Internal 100-μA pullup provided for this terminal, with power supplied from VDDS (3.3-V I/O power)	Pullup/down
u	Internal 20-μA pullup provided for this terminal, with power supplied from VDDS (3.3-V I/O power)	Pullup/down
D	Internal 100-μA pulldown provided for this terminal	Pullup/down
4	4-mA source and 4-mA sink for the defined output driver	Drive
8	8-mA source and 8-mA sink for the defined output driver	Drive
FS	Provides a fail-safe feature to the input receiver or output driver. The fail-safe feature provides power-down protection for TNETV1060 I/Os connected to an actively powered-up external device. This allows the fail-safe terminal to be driven above its own supply-voltage level. A fail-safe terminal has no diodes to the power-supply rail, which ensures that no current flows into the terminal if a signal is applied when VDD or VDDS are 0 V (powered down).	Fail safe
LN	Provides a low-noise feature to the defined output driver	Low noise
3.3-V I/O	I/O input power, typically 3.3 V	Other
1.5-V core	Core input power, typically supplied at 1.5 V by the internal voltage regulator	Other
V analog	Analog input power that may have special needs	Other
GND	Ground input voltage, typically 0 V	Other
GND analog	Analog ground input voltage, typically 0 V, that may have special needs	Other
oscillator	Special oscillator I/O terminals	Other
analog	Analog input terminal that may have special needs	Other
V regulator	Special voltage regulator I/O terminals	Other
_M	Indicates the minus input or output terminal for a differential pair	Names
_P	Indicates the plus input or output terminal for a differential pair	Names
_I	Indicates an input terminal	Names
_O	Indicates an output terminal	Names
_DI	Indicates an input terminal	Names
_DO	Indicates an output terminal	Names

3.2 Terminal Assignments

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)†

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
A1	G					GND	VSS		
A2	G					GND	VSS		
A3	O		4				UART_RTS		
A4	O		8				$\overline{\text{EM\_WE}}$		
A5	O		8				$\overline{\text{EM\_CAS}}$		
A6	O		8				$\overline{\text{EM\_RAS}}$		
A7	O		8				$\overline{\text{EM\_CS5}}$		
A8	O		8				$\overline{\text{EM\_CS2}}$		
A9	O		8				$\overline{\text{EM\_WE\_DQM3}}$		
A10	I/O	u	8				EM_D30		
A11	I/O	u	8				EM_D28		
A12	I/O	u	8				EM_D24		
A13	I/O	u	8				EM_D20		
A14	I/O	u	8				EM_D17		
A15	I/O	u	8				EM_D14		
A16	I/O	u	8				EM_D11		
A17	I/O	u	8				EM_D08		
A18	I/O	u	8				EM_D04		
A19	I/O	u	8				EM_D01		
A20	I/O	u	8				EM_A23		
A21	G					GND	VSS		
A22	G					GND	VSS		
AA1	G					GND analog	VSS_AIC		
AA2	G					GND analog	VSS_AIC		
AA3	N/C						N/C		
AA4	N/C						N/C		
AA5	N/C						N/C		
AA6	I					analog	$\overline{\text{VR\_ENBL}}$		
AA7	I/O	D	4	FS	LN		KEYPAD01		GPIO09
AA8	I/O	D	4	FS	LN		KEYPAD03		GPIO11
AA9	I/O	D	4	FS	LN		KEYPAD06		GPIO14
AA10	I/O	U	4		LN		KEYPAD09		GPIO17
AA11	I/O	U	4		LN		KEYPAD12		GPIO20
AA12	I/O	U	4				LCD_BIAS_E0	$\overline{\text{AIC\_RESET}}$	
AA13	I/O	U	4				LCD_VSYNC_A	MII_MD_CLK	
AA14	I/O	U	4				LCD_D02	MII_P0_TX_D1	GPIO26
AA15	I/O	U	4				LCD_D05	MII_P0_TX_ENBL	GPIO29
AA16	I/O	U	4				LCD_D08	MII_P0_COL	GPIO32
AA17	I/O	U	4				LCD_D11	MII_P0_RX_DV	GPIO35

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
AA18	I/O	U	4				LCD_D15	MII_P0_RX_D3	GPIO39
AA19	I/O	U	8				$\overline{\text{P0\_LINK}}$	AIC_DI	P0_FX_RX
AA20	I/O	U	8				$\overline{\text{P0\_FDUPLEX}}$	AIC_S_CLK	P0_FX_ENBL
AA21	I/O	U	8				$\overline{\text{P1\_LINK}}$	MII_P1_RX_D1	P1_FX_RX
AA22	I/O	U	8				$\overline{\text{P1\_FDUPLEX}}$	MII_P1_RX_D3	P1_FX_ENBL
AB1	G					GND analog	VSS_AIC		
AB2	G					GND analog	VSS_AIC		
AB3	N/C						N/C		
AB4	N/C						N/C		
AB5	N/C						N/C		
AB6	O					V regulator	VR_BASE1		
AB7	I/O	D	4	FS	LN		KEYPAD00		GPIO08
AB8	I/O	D	4	FS	LN		KEYPAD02		GPIO10
AB9	I/O	D	4	FS	LN		KEYPAD05		GPIO13
AB10	I/O	U	4		LN		KEYPAD08		GPIO16
AB11	I/O	U	4		LN		KEYPAD11		GPIO19
AB12	I/O	U	4		LN		KEYPAD15		GPIO23
AB13	I/O	U	8				LCD_E1	DSP_FUNCTEST1	
AB14	I/O	U	4				LCD_D01	MII_P0_TX_D0	GPIO25
AB15	I/O	U	4				LCD_D04	MII_P0_TX_D3	GPIO28
AB16	I/O	U	4				LCD_D07	MII_P0_LINK	GPIO31
AB17	I/O	U	4				LCD_D10	MII_P0_RX_CLK	GPIO34
AB18	I/O	U	4				LCD_D14	MII_P0_RX_D2	GPIO38
AB19	I/O	U	8	FS	LN		$\overline{\text{P0\_100MB}}$	AIC_DO	P0_FX_SD
AB20	I/O	U	8				$\overline{\text{P0\_ACTIVITY}}$	AIC_FS	P0_FX_TX
AB21	I/O	U	8				$\overline{\text{P1\_100MB}}$	$\overline{\text{AIC\_PWRDWN}}$	P1_FX_SD
AB22	I/O	U	8				$\overline{\text{P1\_ACTIVITY}}$	MII_P1_RX_D2	P1_FX_TX
B1	G					GND	VSS		
B2	G					GND	VSS		
B3	I	U					UART_CTS		
B4	I	U					UART_RX		
B5	O		8				$\overline{\text{EM\_OE}}$		
B6	I	D					EM_WAIT		
B7	O		8				$\overline{\text{EM\_CS4}}$		
B8	O		8				$\overline{\text{EM\_CS1}}$		
B9	O		8				$\overline{\text{EM\_WE\_DQM2}}$		
B10	I/O	u	8				EM_D31		
B11	I/O	u	8				EM_D29		
B12	I/O	u	8				EM_D25		

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
B13	I/O	u	8				EM_D21		
B14	I/O	u	8				EM_D18		
B15	I/O	u	8				EM_D15		
B16	I/O	u	8				EM_D12		
B17	I/O	u	8				EM_D09		
B18	I/O	u	8				EM_D05		
B19	I/O	u	8				EM_D00		
B20	I/O	u	8				EM_A22		
B21	G					GND	VSS		
B22	G					GND	VSS		
C1	I			FS			$\overline{\text{RESET\_I}}$		
C2	O		4	FS	LN		$\overline{\text{RESET\_O}}$		
C3	G					GND	VSS		
C4	O		4				UART_TX		
C5	O		8				EM_$\overline{\text{RW}}$		
C6	I	D					EM_HIZ		
C7	O		8				$\overline{\text{EM\_CS3}}$		
C8	O		8				$\overline{\text{EM\_CS0}}$		
C9	O		8				$\overline{\text{EM\_WE\_DQM1}}$		
C10	O		8				$\overline{\text{EM\_WE\_DQM0}}$		
C11	I/O	u	8				EM_D27		
C12	I/O	u	8				EM_D23		
C13	I/O	u	8				EM_D19		
C14	I/O	u	8				EM_D16		
C15	I/O	u	8				EM_D13		
C16	I/O	u	8				EM_D10		
C17	I/O	u	8				EM_D07		
C18	I/O	u	8				EM_D03		
C19	I/O	u	8				EM_A21		
C20	G					GND	VSS		
C21	I/O	u	8				EM_A20		
C22	I/O	u	8				EM_A19		
D1	I/O	D	4		LN		SSP1		
D2	I/O	D	4		LN		SSP2		
D3	I/O	D	4		LN		SSP0		
D4	G					GND	VSS		
D5	O		8				EM_CKE		
D6	I/O		8				EM_CLK		
D7	P					3.3-V I/O	VDDS		
D8	P					3.3-V I/O	VDDS		
D9	P					3.3-V I/O	VDDS		
D10	P					3.3-V I/O	VDDS		

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
D11	I/O	u	8				EM_D26		
D12	I/O	u	8				EM_D22		
D13	P					3.3-V I/O	VDDS		
D14	P					3.3-V I/O	VDDS		
D15	P					3.3-V I/O	VDDS		
D16	P					3.3-V I/O	VDDS		
D17	I/O	u	8				EM_D06		
D18	I/O	u	8				EM_D02		
D19	G					GND	VSS		
D20	I/O	u	8				EM_A18		
D21	I/O	u	8				EM_A17		
D22	I/O	u	8				EM_A16		
E1	I	D		FS			$\overline{\text{EJTAG\_TRST1}}$		
E2	I	U					$\overline{\text{EJTAG\_SYSRST}}$		
E3	I	U					EJTAG_DINT		
E4	I/O	D	4		LN		SSP3		
E19	I/O	u	8				EM_A15		
E20	I/O	u	8				EM_A14		
E21	I/O	u	8				EM_A13		
E22	I/O	u	8				EM_A12		
F1	O		4	FS	LN		EJTAG_TDO		
F2	I	U					EJTAG_TCK		
F3	I	D		FS			$\overline{\text{EJTAG\_TRST0}}$		
F4	I	D		FS			TEST		
F19	I/O	u	8				EM_A11		
F20	I/O	u	8				EM_A10		
F21	I/O	u	8				EM_A09		
F22	I/O	u	8				EM_A08		
G1	I/O	U	4		LN		JTAG_EMU1		
G2	I	U					EJTAG_TMS		
G3	I	U					EJTAG_TDI		
G4	P					3.3-V I/O	VDDS		
G19	P					3.3-V I/O	VDDS		
G20	I/O	u	8				EM_A07		
G21	I/O	u	8				EM_A06		
G22	I/O	u	8				EM_A05		
H1	I	U					JTAG_TDI		
H2	I	D		FS			$\overline{\text{JTAG\_TRST}}$		
H3	I/O	U	4		LN		JTAG_EMU0		
H4	P					3.3-V I/O	VDDS		
H19	P					3.3-V I/O	VDDS		
H20	I/O	u	8				EM_A04		

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
H21	I/O	u	8				EM_A03		
H22	I/O	u	8				EM_A02		
J1	I	U					JTAG_TMS		
J2	O		4	FS	LN		JTAG_TDO		
J3	I	U					JTAG_TCK		
J4	P					3.3-V I/O	VDDS		
J9	G					GND	VSS		
J10	P					1.5-V core	VDD		
J11	P					1.5-V core	VDD		
J12	P					1.5-V core	VDD		
J13	P					1.5-V core	VDD		
J14	G					GND	VSS		
J19	P					3.3-V I/O	VDDS		
J20	I/O	u	8				EM_A01		
J21	I/O	u	8				EM_A00		
J22	I/O	U	4				TELE_CLK_O	MII_P1_RX_D0	
K1	I						VLYNQ5_RX_D1		
K2	I						VLYNQ5_RX_D0		
K3	I/O	U	8				VLYNQ5_CLK		
K4	P					3.3-V I/O	VDDS		
K9	P					1.5-V core	VDD		
K10	G					GND	VSS		
K11	G					GND	VSS		
K12	G					GND	VSS		
K13	G					GND	VSS		
K14	P					1.5-V core	VDD		
K19	P					3.3-V I/O	VDDS		
K20	I/O	U	4				$\overline{\text{TELE\_CS}}$	MII_P1_RX_ERR	GPIO49
K21	I/O	U	4				TELE_INT	MII_P1_RX_CLK	GPIO50
K22	I/O	U	4				$\overline{\text{TELE\_RESET}}$	MII_P1_RX_DV	GPIO51
L1	I/O		8				VLYNQ5_TX_D1		
L2	I/O		8				VLYNQ5_TX_D0		
L3	N/C						N/C		
L4	N/C						N/C		
L9	P					1.5-V core	VDD		
L10	G					GND	VSS		
L11	G					GND	VSS		
L12	G					GND	VSS		
L13	G					GND	VSS		
L14	P					1.5-V core	VDD		
L19	I/O	U	4				TELE_CLK_I	MII_P1_TX_D2	GPIO43
L20	I/O	U	4				TELE_FS	MII_P1_COL	GPIO48

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
L21	I/O	U	4				TELE_RINGIN3	MII_P1_TX_CLK	GPIO46
L22	I/O	U	4				TELE_RINGIN4	MII_P1_LINK	GPIO47
M1	N/C						N/C		
M2	N/C						N/C		
M3	I/O	U	4		LN		McBSP_CLK_RX		
M4	N/C						N/C		
M9	P					1.5-V core	VDD		
M10	G					GND	VSS		
M11	G					GND	VSS		
M12	G					GND	VSS		
M13	G					GND	VSS		
M14	P					1.5-V core	VDD		
M19	I/O	U	4				TELE_DCLK	MII_P1_CRS	GPIO40
M20	I/O	U	4				TELE_DO	MII_P1_TX_D1	GPIO42
M21	I/O	U	4				TELE_RINGIN1	MII_P1_TX_D3	GPIO44
M22	I/O	U	4				TELE_RINGIN2	MII_P1_TX_ENBL	GPIO45
N1	N/C						N/C		
N2	I/O	U	4		LN		McBSP_CLK_TX		
N3	I	D		FS			McBSP_D_RX		
N4	P					3.3-V I/O	VDDS		
N9	P					1.5-V core	VDD		
N10	G					GND	VSS		
N11	G					GND	VSS		
N12	G					GND	VSS		
N13	G					GND	VSS		
N14	P					1.5-V core	VDD		
N19	P					V analog	VDD_PLL		
N20	I/O	U	4				TELE_DI	MII_P1_TX_D0	GPIO41
N21	G					GND analog	VSS_REF_CLK		
N22	O					oscillator	REF_CLK_O		
P1	O		4	FS	LN		McBSP_D_TX		
P2	I/O	D	4	FS	LN		McBSP_FS_RX		
P3	I/O	D	4	FS	LN		McBSP_FS_TX		
P4	P					3.3-V I/O	VDDS		
P9	G					GND analog	VSS_AIC_CLK		
P10	P					1.5-V core	VDD		
P11	P					1.5-V core	VDD		
P12	P					1.5-V core	VDD		
P13	P					1.5-V core	VDD		

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
P14	G					GND analog	VSS_PLL		
P19	I					analog	P1_RX_P		
P20	P					V analog	VDDA_PHY1_34		
P21	I	D					ALT_CLK_I		
P22	I/O					oscillator	REF_CLK_I		
R1	I/O					oscillator	AIC_CLK_I		
R2	O					V regulator	VR_BASE2		
R3	I/O	U	4		LN		GPIO0		EXT_INT1
R4	P					V analog	VDDA_AIC		
R19	I					analog	P1_RX_M		
R20	G					GND analog	VSS_PHY1_34		
R21	G					GND analog	VSS_PHY1_1		
R22	O					analog	P1_TX_P		
T1	O					oscillator	AIC_CLK_O		
T2	I/O	U	4		LN		GPIO3		EXT_INT4
T3	I/O	U	4		LN		GPIO1		EXT_INT2
T4	P					V analog	VDDA_AIC		
T19	G					GND analog	VSS_PHY1_ESD		
T20	G					GND analog	VSS_PHY1_2		
T21	G					GND analog	VSS_PHY1_1		
T22	O					analog	P1_TX_M		
U1	I/O	U	4		LN		GPIO6		
U2	I/O	U	4		LN		GPIO4		
U3	I/O	U	4		LN		GPIO2		EXT_INT3
U4	N/C						N/C		
U19	P					V analog	VDDA_PHY1_2		
U20	P					V analog	VDDA_PHY0_2		
U21	P					V analog	VDDA_PHY0_1		
U22	P					V analog	VDDA_PHY1_1		
V1	I/O	U	4		LN		GPIO7		
V2	I/O	U	4		LN		GPIO5		SSP4
V3	N/C						N/C		
V4	N/C						N/C		
V19	G					GND analog	VSS_PHY0_ESD		

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
V20	G					GND analog	VSS_PHY0_2		
V21	G					GND analog	VSS_PHY0_1		
V22	O					analog	P0_TX_M		
W1	N/C						N/C		
W2	N/C						N/C		
W3	N/C						N/C		
W4	G					GND analog	VSS_AIC		
W5	N/C						N/C		
W6	N/C						N/C		
W7	P					V analog	VDDA_AIC		
W8	P					V analog	VDDA_AIC		
W9	P					3.3-V I/O	VDDS		
W10	P					3.3-V I/O	VDDS		
W11	I/O	U	4		LN		KEYPAD13		GPIO21
W12	I/O	U	4				$\overline{\text{LCD\_HSYNC\_W}}$	MII_MD_IO	
W13	P					3.3-V I/O	VDDS		
W14	P					3.3-V I/O	VDDS		
W15	P					3.3-V I/O	VDDS		
W16	P					3.3-V I/O	VDDS		
W17	I/O	U	4				LCD_D13	MII_P0_RX_D1	GPIO37
W18	O					analog	PHY_REF		
W19	I					analog	P0_RX_M		
W20	G					GND analog	VSS_PHY0_34		
W21	G					GND analog	VSS_PHY0_1		
W22	O					analog	P0_TX_P		
Y1	N/C						N/C		
Y2	N/C						N/C		
Y3	G					GND analog	VSS_AIC		
Y4	N/C						N/C		
Y5	N/C						N/C		
Y6	N/C						N/C		
Y7	N/C						N/C		
Y8	I/O	D	4	FS	LN		KEYPAD04		GPIO12
Y9	I/O	D	4	FS	LN		KEYPAD07		GPIO15
Y10	I/O	U	4		LN		KEYPAD10		GPIO18
Y11	I/O	U	4		LN		KEYPAD14		GPIO22
Y12	I/O	U	8				LCD_PIXEL_STRB	DSP_FUNCTEST0	

† See Table 3–1 for functional symbol definitions.

Table 3–2. TNETV1060 PBGA I/Os (Sorted by Terminal)† (Continued)

TERMINAL NO.	TYPE	PULL UP/DOWN	DRIVE I (mA)	FAIL SAFE	LOW NOISE	OTHER	TERMINAL FUNCTION NAMES		
							PRIMARY	SECONDARY	TERTIARY
Y13	I/O	U	4				LCD_D00	MII_P0_CRS	GPIO24
Y14	I/O	U	4				LCD_D03	MII_P0_TX_D2	GPIO27
Y15	I/O	U	4				LCD_D06	MII_P0_TX_CLK	GPIO30
Y16	I/O	U	4				LCD_D09	MII_P0_RX_ERR	GPIO33
Y17	I/O	U	4				LCD_D12	MII_P0_RX_D0	GPIO36
Y18	I					analog	PHY_REF_RTN		
Y19	I					analog	P0_RX_P		
Y20	P					V analog	VDDA_PHY0_34		
Y21	I					analog	PHY_TEST		
Y22	O					V regulator	VR_BASE3		

† See Table 3–1 for functional symbol definitions.

3.3 Signal Descriptions

Because useful I/O signals are multiplexed over the primary I/O signals, three columns are provided in the following tables. The columns are defined as 1st for the primary I/O signals, 2nd for the secondary I/O signals, and 3rd for the tertiary I/O signals. Signals of interest that are described in each table are highlighted in **bold** text.

Due to the multiplexing capabilities of several of the TNETV1060 I/O terminals, certain Type terminal definitions may not accurately define the input or output designation of a particular signal. In these special cases, the correct input designation is defined as (IN), while the correct output designation is defined as (OUT) in the Description field.

3.3.1 External Memory Interface (EMIF)

The EMIF provides glueless connectivity to the following memory device types (see Tables 3–3 through 3–5):

- Synchronous DRAM (SDRAM)
- Asynchronous memory (includes flash, ROM, or RAM)
- Host-port interface (HPI), a memory-mapped registered interface to standard TI DSP subsystems utilizing asynchronous memory (flash, ROM, or RAM)

3.3.1.1 Address Bus

Table 3–3. EMIF Address I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
J21	I/O	**EM_A00**			EMIF address bus (OUT). This bus (EM_A[23:00]) provides an address when accessing the EMIF. The function of EM_A[23:21] changes dependent on the data bus width of the external device (detailed in the User's Guide) . Boot configuration (IN). This bus (EM_A[23:00]) is sampled at $\overline{\text{RESET\_I}}$ deactivation. The information sampled determines certain boot configuration modes (for more information, see section 3.4, *Boot Configuration*).
J20		**EM_A01**			
H22		**EM_A02**			
H21		**EM_A03**			
H20		**EM_A04**			
G22		**EM_A05**			
G21		**EM_A06**			
G20		**EM_A07**			
F22		**EM_A08**			
F21		**EM_A09**			
F20		**EM_A10**			
F19		**EM_A11**			
E22		**EM_A12**			
E21		**EM_A13**			
E20		**EM_A14**			
E19		**EM_A15**			
D22		**EM_A16**			
D21		**EM_A17**			
D20		**EM_A18**			
C22		**EM_A19**			
C21		**EM_A20**			
C19		**EM_A21**			
B20		**EM_A22**			
A20		**EM_A23**			

3.3.1.2 Data Bus

Table 3–4. EMIF Data I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
B19	I/O	**EM_D00**			EMIF data bus. This bus (EM_D[31:00]) provides the data path when accessing the EMIF. Valid external data bus widths include 32 bit, 16 bit, and 8 bit (for asynchronous only).
A19		**EM_D01**			
D18		**EM_D02**			
C18		**EM_D03**			
A18		**EM_D04**			
B18		**EM_D05**			
D17		**EM_D06**			
C17		**EM_D07**			
A17		**EM_D08**			
B17		**EM_D09**			
C16		**EM_D10**			
A16		**EM_D11**			
B16		**EM_D12**			
C15		**EM_D13**			
A15		**EM_D14**			
B15		**EM_D15**			
C14		**EM_D16**			
A14		**EM_D17**			
B14		**EM_D18**			
C13		**EM_D19**			
A13		**EM_D20**			
B13		**EM_D21**			
D12		**EM_D22**			
C12		**EM_D23**			
A12		**EM_D24**			
B12		**EM_D25**			
D11		**EM_D26**			
C11		**EM_D27**			
A11		**EM_D28**			
B11		**EM_D29**			
A10		**EM_D30**			
B10		**EM_D31**			

3.3.1.3 Control Signals

Table 3–5. EMIF Control I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
C8	O	EM_CS0			EMIF chip select 0. Designated for asynchronous memory (flash) accesses (32M-byte addressability).
B8	O	EM_CS1			EMIF chip select 1. Designated for SDRAM accesses (64M-byte addressability).
A8	O	EM_CS2			EMIF chip select 2. Designated for SDRAM accesses (64M-byte addressability).
C7	O	EM_CS3			EMIF chip select 3. Designated for asynchronous memory accesses (16M-byte addressability).
B7	O	EM_CS4			EMIF chip select 4. Designated for asynchronous memory accesses (16M-byte addressability).
A7	O	EM_CS5			EMIF chip select 5. Designated for asynchronous memory accesses (16M-byte addressability).
D6	I/O	EM_CLK			SDRAM clock (OUT)
A6	O	EM_RAS			SDRAM row address strobe
A5	O	EM_CAS			SDRAM column address strobe
A4	O	EM_WE			SDRAM write enable control. Asynchronous memory write strobe control.
D5	O	EM_CKE			SDRAM clock enable
C10	O	EM_WE_DQM0			SDRAM ($\overline{DQM}$): Data byte masked when this control signal is sampled high for either reads or writes. The data byte is read or written when sampled low. Asynchronous memory ($\overline{WE}$): Write strobe control. In addition, may be used as read-mode byte enable through register program control.
C9		EM_WE_DQM1			
B9		EM_WE_DQM2			
A9		EM_WE_DQM3			
B5	O	EM_OE			Asynchronous memory read strobe control
C5	O	EM_R/$\overline{W}$			Asynchronous memory read or write enable control
B6	I	EM_WAIT			External device wait state control during asynchronous memory accesses. Must be register bit enabled to become effective and can be positive or negative active.
C6	I	EM_HIZ			EMIF 3-state control. For test purposes only. Must be held low (with internal pulldown) for normal operation.

3.3.2 Ethernet

The TNETV1060 provides two Ethernet ports referred to as Port 0 (P0) and Port 1 (P1). Each of these ports provides the following I/O options:

- Fully integrated IEEE Std 802.3/802.3u-compatible 10-Mbps/100-Mbps Ethernet PHY
- Optional IEEE Std 802.3 media independent interface (MII) port capable of operating up to 30 external PHY devices. Reverse MII, reduced MII (RMII), and serial MII (SMII) modes of operation are not supported. Each MII can accommodate the following operational options:
  - Internal PHY mode. The external MII port is inactive.
  - Internal PHY mode with MII observation. This test mode allows external visibility of the information passed between the internal switch and the internal PHY on the MII.
  - Internal PHY disabled. The internal PHY is disabled and the MII is being driven by the switch in order to control an external PHY.
  - Internal switch disabled. This test mode allows the PHY connection to the internal switch to be replaced with an external MII driver.
- Internal PHY LED status control outputs

3.3.2.1 Management MII

This two-terminal serial interface provides register programmability to any PHY attached to the TNETV1060 as defined in the following:

- The TNETV1060 can provide register control to external PHY devices (up to 30).
- External controllers can provide register control of the internal TNETV1060 PHY devices.

Table 3–6. Management Data MII I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
W12	I/O	$\overline{\text{LCD\_HSYNC\_W}}$	**MII_MD_IO**		Serial management data stream for PHY register control
AA13	I/O	LCD_VSYNC_A	**MII_MD_CLK**		Serial management clock that synchronizes the MII_MD_IO

3.3.2.2 Analog PHY

Table 3–7. Analog PHY I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
W18	O	**PHY_REF**			A 12.4-kΩ 1% resistor is connected between these two I/O terminals.
Y18	I	**PHY_REF_RTN**			

3.3.2.3 Port 0 PHY

Table 3–8. Port 0 PHY I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
W19	I	**P0_RX_M**			Port 0 differential receiver +/– pair, to magnetics
Y197		**P0_RX_P**			
V22	O	**P0_TX_M**			Port 0 differential transmit +/– pair, to magnetics
W22		**P0_TX_P**			
AB19	I/O	**$\overline{\text{P0\_100MB}}$**	AIC_DO	**P0_FX_SD**	$\overline{\text{P0\_100MB}}$ (OUT) LED 1, low = 100 Mbps, high = 10 Mbps P0_FX_SD (IN) 100 Base-FX signal detect indicating a valid received signal from the external FX transceiver
AA19	I/O	**$\overline{\text{P0\_LINK}}$**	AIC_DI	**P0_FX_RX**	$\overline{\text{P0\_LINK}}$ (OUT) LED 2, low = port 0 link established with the internal PHY P0_FX_RX (IN) 100 Base-FX receiver data
AB20	I/O	**$\overline{\text{P0\_ACTIVITY}}$**	AIC_FS	**P0_FX_TX**	$\overline{\text{P0\_ACTIVITY}}$ (OUT) LED 3, low = carrier sense activity P0_FX_TX (OUT) 100 Base-FX transmit data
AA20	I/O	**$\overline{\text{P0\_FDUPLEX}}$**	AIC_S_CLK	**P0_FX_ENBL**	$\overline{\text{P0\_FDUPLEX}}$ (OUT) LED 4, low = full duplex, high = half duplex P0_FX_ENBL (OUT) Enable the external FX-compatible driver for P0_FX_TX

3.3.2.4 Port 1 PHY

Table 3–9. Port 1 PHY I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
R19	I	**P1_RX_M**			Port 1 differential receiver +/– pair, to magnetics
P19		**P1_RX_P**			
T22	O	**P1_TX_M**			Port 1 differential transmit +/– pair, to magnetics
R22		**P1_TX_P**			
AB21	I/O	**$\overline{\text{P1\_100MB}}$**	$\overline{\text{AIC\_PWRDWN}}$	**P1_FX_SD**	$\overline{\text{P1\_100MB}}$ (OUT) LED 1, low = 100 Mbps, high = 10 Mbps P1_FX_SD (IN) 100 Base-FX signal detect indicating a valid received signal from the external FX transceiver
AA21	I/O	**$\overline{\text{P1\_LINK}}$**	MII_P1_RX_D1	**P1_FX_RX**	$\overline{\text{P1\_LINK}}$ (OUT) LED 2, low = port 1 link established with the internal PHY P1_FX_RX (IN) 100 Base-FX receiver data
AB22	I/O	**$\overline{\text{P1\_ACTIVITY}}$**	MII_P1_RX_D2	**P1_FX_TX**	$\overline{\text{P1\_ACTIVITY}}$ (OUT) LED 3, low = carrier sense activity P1_FX_TX (OUT) 100 Base-FX transmit data
AA22	I/O	**$\overline{\text{P1\_FDUPLEX}}$**	MII_P1_RX_D3	**P1_FX_ENBL**	$\overline{\text{P1\_FDUPLEX}}$ (OUT) LED 4, low = full duplex, high = half duplex P1_FX_ENBL (OUT) Enable the external FX-compatible driver for P1_FX_TX

If only one PHY is to be used in the system implementation, the following are recommended:

- Use Port 0 PHY. Port 1 PHY is not used.
- Supply power and grounds to both PHYs (related to VSS_PHY0, VSS_PHY1, VDDA_PHY0, and VDDA_PHY1).
- On Port 1 PHY, pull up the TX lines (P1_TX_M and P1_TX_P) using the standard 50-Ω resistors to VDDA_PHY1_1. The magnetics are not connected to Port 1.
- On Port 1 PHY, ground the RX lines (P1_RX_M and P1_RX_P).
- Place the Port 1 PHY in reset.

3.3.2.5 Port 0 MII

Table 3–10. Port 0 MII I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
AA15	I/O	LCD_D05	**MII_P0_TX_ENBL**	GPIO29	Port 0 MII transmit enable (OUT)
Y15	I/O	LCD_D06	**MII_P0_TX_CLK**	GPIO30	Port 0 MII transmit clock (IN)
AB14	I/O	LCD_D01	**MII_P0_TX_D0**	GPIO25	Port 0 MII transmit data nibble (OUT). Data is synchronous with MII_P0_TX_CLK. Data is valid when MII_P0_TX_ENBL is active.
AA14		LCD_D02	**MII_P0_TX_D1**	GPIO26	
Y14		LCD_D03	**MII_P0_TX_D2**	GPIO27	
AB15		LCD_D04	**MII_P0_TX_D3**	GPIO28	
AB17	I/O	LCD_D10	**MII_P0_RX_CLK**	GPIO34	Port 0 MII receiver clock (IN)
Y17	I/O	LCD_D12	**MII_P0_RX_D0**	GPIO36	Port 0 MII receiver data nibble. (IN). Data is synchronous with MII_P0_RX_CLK. Data is valid when MII_P0_RX_DV is active.
W17		LCD_D13	**MII_P0_RX_D1**	GPIO37	
AB18		LCD_D14	**MII_P0_RX_D2**	GPIO38	
AA18		LCD_D15	**MII_P0_RX_D3**	GPIO39	
AA17	I/O	LCD_D11	**MII_P0_RX_DV**	GPIO35	Port 0 MII receiver data valid (IN)
Y16	I/O	LCD_D09	**MII_P0_RX_ERR**	GPIO33	Port 0 MII receiver data coding error (IN)
Y13	I/O	LCD_D00	**MII_P0_CRS**	GPIO24	Port 0 MII carrier sense (IN). A frame carrier signal is being received.
AA16	I/O	LCD_D08	**MII_P0_COL**	GPIO32	Port 0 MII collision sense (IN). In half-duplex mode, indicates network collision. In full-duplex mode, transmission of new frames does not commence.
AB16	I/O	LCD_D07	**MII_P0_LINK**	GPIO31	Port 0 MII link active (IN). The external PHY activates this signal when a link is established.

3.3.2.6 Port 1 MII

Table 3–11. Port 1 MII I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
M22	I/O	TELE_RINGIN2	**MII_P1_TX_ENBL**	GPIO45	Port 1 MII transmit enable (OUT)
L21	I/O	TELE_RINGIN3	**MII_P1_TX_CLK**	GPIO46	Port 1 MII transmit clock (IN)
N20	I/O	TELE_DI	**MII_P1_TX_D0**	GPIO41	Port 1 MII transmit data nibble (OUT). Data is synchronous with MII_P1_TX_CLK. Data is valid when MII_P1_TX_ENBL is active.
M20		TELE_DO	**MII_P1_TX_D1**	GPIO42	
L19		TELE_CLK_I	**MII_P1_TX_D2**	GPIO43	
M21		TELE_RINGIN1	**MII_P1_TX_D3**	GPIO44	
K21	I/O	TELE_INT	**MII_P1_RX_CLK**	GPIO50	Port 1 MII receiver clock (IN)
J22	I/O	TELE_CLK_O	**MII_P1_RX_D0**		Port 1 MII receiver data nibble (IN). Data is synchronous with MII_P1_RX_CLK. Data is valid when MII_P1_RX_DV is active.
AA21		$\overline{\text{P1\_LINK}}$	**MII_P1_RX_D1**	P1_FX_RX	
AB22		$\overline{\text{P1\_ACTIVITY}}$	**MII_P1_RX_D2**	P1_FX_TX	
AA22		$\overline{\text{P1\_FDUPLEX}}$	**MII_P1_RX_D3**	P1_FX_ENBL	
K22	I/O	$\overline{\text{TELE\_RESET}}$	**MII_P1_RX_DV**	GPIO51	Port 1 MII receiver data valid (IN)
K20	I/O	$\overline{\text{TELE\_CS}}$	**MII_P1_RX_ERR**	GPIO49	Port 1 MII receiver data coding error (IN)
M19	I/O	TELE_DCLK	**MII_P1_CRS**	GPIO40	Port 1 MII carrier sense (IN). A frame carrier signal is being received.
L20	I/O	TELE_FS	**MII_P1_COL**	GPIO48	Port 1 MII collision sense (IN). In half-duplex mode, indicates network collision. In full-duplex mode, transmission of new frames does not commence.
L22	I/O	TELE_RINGIN4	**MII_P1_LINK**	GPIO47	Port 1 MII link active (IN). The external PHY activates this signal when a link is established.

3.3.3 Multichannel Buffered Serial Port (McBSP) Interface

The McBSP is a standard TI serial interface controller supporting a wide variety of serial configurations through register control. This interface may be used to drive external codec devices in place of, or in addition to, the internal integrated voice codec. In addition, each signal may be programmed as a DSP-directed GPIO.

Table 3–12. McBSP I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
M3	B	**McBSP_CLK_RX**			Receiver clock or DSP GPIO. Synchronizes McBSP_D_RX and McBSP_FS_RX. If not used, hold high (with internal pullup).
N3	I	**McBSP_D_RX**			Receiver data or DSP GPIO. If not used, hold low (with internal pulldown).
P2	B	**McBSP_FS_RX**			Receiver frame synchronization or DSP GPIO. If not used, hold low (with internal pulldown).
N2	B	**McBSP_CLK_TX**			Transmitter clock or DSP GPIO. Synchronizes McBSP_D_TX and McBSP_FS_TX. If not used, hold high (with internal pullup).
P1	O	**McBSP_D_TX**			Transmitter data or DSP general-purpose output only
P3	B	**McBSP_FS_TX**			Transmitter frame synchronization or DSP GPIO. If not used, hold low (with internal pulldown).

3.3.4 Line Codec Interface

The line codec interface provides a glueless digital connection to external telephony circuitry implementing voice over packet (VOP) applications suc as telephony codecs.

The line codec interface consists of a digital voice data interface and a digital control interface:

- Voice data interface: A data PCM data stream generally supplied to/from the on-chip McBSP. In addition, the PCM-related signals of the telephony interface supplement this PCM data stream (TELE_FS, TELE_CLK, TELE_CLK0).
- Control data interface: A serial data path supplied by either the telephony interface signals (defined below) or the McBSP.

Voice circuits may require the following additional digital control signals:

- Interrupt: This incoming interrupt is supplied by the telephony interface signals (see Table 3–13).
- Ring in: These low-frequency clock signals are supplied by the telephony interface signals (see Table 3–13).

Table 3–13. Line Codec Interface I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
N20	I	**TELE_DI**	MII_P1_TX_D0	GPIO41	Control data interface serial port data input
M20	I/O	**TELE_DO**	MII_P1_TX_D1	GPIO42	Control data interface serial port data output when the serial interface specifies separate input and output data bits. This is a bidirectional signal when the serial interface specifies a single bidirectional data terminal.
K20	O	**$\overline{\text{TELE\_CS}}$**	MII_P1_RX_ERR	GPIO49	Control data interface chip select or enable output
M19	O	**TELE_DCLK**	MII_P1_CRS	GPIO40	Control data interface clock output. Synchronizes the control data interface signals TELE_DI, TELE_DO, and $\overline{\text{TELE\_CS}}$.
M21	O	**TELE_RINGIN1**	MII_P1_TX_D3	GPIO44	Ring in control driver output. When inactive, they produce a low frequency (~20-Hz programmable) clock output used to drive the ringer control input on certain SLICs. When inactive, these signals are held low. For true 5-V drive capability, an external transistor is required.
M22		**TELE_RINGIN2**	MII_P1_TX_ENBL	GPIO45	
L21		**TELE_RINGIN3**	MII_P1_TX_CLK	GPIO46	
L22		**TELE_RINGIN4**	MII_P1_LINK	GPIO47	
K21	I	**TELE_INT**	MII_P1_RX_CLK	GPIO50	Voice interface subsystem interrupt input
K22	O	**$\overline{\text{TELE\_RESET}}$**	MII_P1_RX_DV	GPIO51	Voice Interface subsystem reset output. Activated by $\overline{\text{RESET\_I}}$ and register control in the DSP subsystem.
L20	O	**TELE_FS**	MII_P1_COL	GPIO48	PCM interface frame synchronization output
L19	I	**TELE_CLK_I**	MII_P1_TX_D2	GPIO43	PCM interface clock in input. External clock source for the PCM subsystem. The PCM subsystem may be programmed for internal (one-half DSP_CLK) or external clock source.
J22	O	**TELE_CLK_O**	MII_P1_RX_D0		PCM interface clock output

3.3.5 LCD Interface

The TNETV1060 LCD controller supports glueless attachment to three different external display types: character displays, rasterized graphics displays (16-bit monochrome or color), and micro-interface graphic displays.

- The character display driver may be used to interface to standard HD44780-type displays.
- The rasterized graphics display driver may be used to interface to passive (STN) or active (TFT) displays.
- The micro-interface graphic display driver may be used to interface to 6800 or 8080 interface-type displays.

Table 3–14. LCD I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
AA13	I/O	**LCD_VSYNC_A**	0MII_MD_CLK		Character display mode (OUT), register select (RS) Raster display mode (OUT) STN type = frame clock (FP) TFT type = vertical sync (VSYNC) Micro display mode (OUT) 6800 and 8080 type = Data/not address select (A0)
W12	I/O	**$\overline{\text{LCD\_HSYNC\_W}}$**	MII_MD_IO		Character display mode (OUT), read/not write select (R/$\overline{W}$) Raster display mode (OUT) STN type = line clock (LP) TFT type = horizontal synchronization (HSYNC) Micro display mode (OUT) 6800 type = read/not write select (R/$\overline{W}$) 8080 type = not write strobe (WR)
Y12	I/O	**LCD_PIXEL_STRB**	DSP_FUNCTEST0		Character display mode (OUT), enable strobe (E0), first display Raster display mode (OUT) STN type = pixel clock (CP) TFT type = pixel clock (CLK) Micro-display mode (OUT) 6800 type = enable strobe (E) 8080 type = not read strobe (RD)
AA12	I/O	**LCD_BIAS_E0**	$\overline{\text{AIC\_RESET}}$		Character display mode not used Raster display mode (OUT) STN type = AC bias (M) TFT type = AC bias (ENABLE) Micro display mode (OUT) 6800 and 8080 type = chip select (CS0), first display
AB13	I/O	**LCD_E1**	DSP_FUNCTEST1		Character display mode (OUT), enable strobe (E1), second display Raster display mode not used Micro display mode (OUT) 6800 and 8080 type = chip select (CS1), second display or clock when programmed for synchronous mode

Table 3–14. LCD I/Os (Continued)

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
Y13	I/O	**LCD_D00**	MII_P0_CRS	GPIO24	LCD data bus providing a 4-, 8-, 12-, or 16-bit data path Character display mode (IN/OUT) Read and write the command and data registers Raster display mode (OUT) Constant-flow (~70 Hz) pixel data Micro-display mode (IN/OUT) Read and write the command and data registers As shown in section 5.2, *Recommended Operating Conditions*, the TNETV1060 input cells should not be driven above 3.6 V. Transceivers are required when reading from displays driving 5-V TTL signals.
AB14		**LCD_D01**	MII_P0_TX_D0	GPIO25	
AA14		**LCD_D02**	MII_P0_TX_D1	GPIO26	
Y14		**LCD_D03**	MII_P0_TX_D2	GPIO27	
AB15		**LCD_D04**	MII_P0_TX_D3	GPIO28	
AA15		**LCD_D05**	MII_P0_TX_ENBL	GPIO29	
Y15		**LCD_D06**	MII_P0_TX_CLK	GPIO30	
AB16		**LCD_D07**	MII_P0_LINK	GPIO31	
AA16		**LCD_D08**	MII_P0_COL	GPIO32	
Y16		**LCD_D09**	MII_P0_RX_ERR	GPIO33	
AB17		**LCD_D10**	MII_P0_RX_CLK	GPIO34	
AA17		**LCD_D11**	MII_P0_RX_DV	GPIO35	
Y17		**LCD_D12**	MII_P0_RX_D0	GPIO36	
W17		**LCD_D13**	MII_P0_RX_D1	GPIO37	
AB18		**LCD_D14**	MII_P0_RX_D2	GPIO38	
AA18		**LCD_D15**	MII_P0_RX_D3	GPIO39	

3.3.6 Sequencer Serial Port (SSP)

Within the SSP there are two state machines (serial port 0 and serial port 1). Each of these state machines provides input and output control of the standard set of serial signals (enable, clock, and data). The five TNETV1060 I/O signals (SSP[4:0]) can be multiplexed to any one of these six serial port signals. In addition, these I/O signals can be controlled as GPIOs.

Table 3–15. SSP I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
D3	I/O	**SSP0**			Each of these I/O signals can be multiplexed to any one of the following serial port functions: – Serial port 0 enable – Serial port 0 clock – Serial port 0 data – Serial port 1 enable – Serial port 1 clock – Serial port 1 data – GPIO input – GPIO output The input or output control, as well as the polarity of the port functions, is determined by the program in the port state machine.
D1		**SSP1**			
D2		**SSP2**			
E4		**SSP3**			
V2		GPIO5		SSP4	

3.3.7 Keypad Interface

The keypad I/O may be configured as an 8 × 8 row and column matrix, accommodating 64 keys. Activation of any key produces a debounced MIPS interrupt. The MIPS can determine which key (or keys) activated the interrupt through write sequences of the column lines.

Table 3–16. Keypad I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
AB7	I/O	**KEYPAD00**		GPIO08	Keypad column lines that should be configured as outputs. The internal pulldowns provide proper bias (OUT).
AA7		**KEYPAD01**		GPIO09	
AB8		**KEYPAD02**		GPIO10	
AA8		**KEYPAD03**		GPIO11	
Y8		**KEYPAD04**		GPIO12	
AB9		**KEYPAD05**		GPIO13	
AA9		**KEYPAD06**		GPIO14	
Y9		**KEYPAD07**		GPIO15	
AB10	I/O	**KEYPAD08**		GPIO16	Keypad row lines that should be configured as inputs. The internal pullups provide proper bias (IN).
AA10		**KEYPAD09**		GPIO17	
Y10		**KEYPAD10**		GPIO18	
AB11		**KEYPAD11**		GPIO19	
AA11		**KEYPAD12**		GPIO20	
W11		**KEYPAD13**		GPIO21	
Y11		**KEYPAD14**		GPIO22	
AB12		**KEYPAD15**		GPIO23	

3.3.8 VLYNQ™ Serial Communication Port

The VLYNQ serial communication interface provided on the TNETV1060 supports host-to-peripheral or peer-to-peer communication modes. This five-terminal version (VLYNQ5) provides a two-bit transmit and receive serial path, with clock rates up to 125 MHz, which can be configured to attach to either a three-terminal or five-terminal external VLYNQ-compatible device.

Table 3–17. VLYNQ5 I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
K3	I/O	**VLYNQ5_CLK**			VLYNQ5 serial clock (IN and OUT). This clock signal provides synchronization to VLYNQ5_RX_D0, VLYNQ5_RX_D1, VLYNQ5_TX_D0, and VLYNQ5_TX_D1. This signal can be programmed as either an internal or external source. If not used, hold high with the internal pullup.
K2	I	**VLYNQ5_RX_D0**			VLYNQ5 serial receive data. This data is coded 8-bit/10-bit data that is received on this two-bit bus as TNETV1060 read data (and requests) or as write data issued from the external VLYNQ device. If not used, hold low with an external 47-kΩ pulldown resistor.
K1		**VLYNQ5_RX_D1**			
L2	I/O	**VLYNQ5_TX_D0**			VLYNQ5 serial transmit data (OUT). This data is coded 8-bit/10-bit data that is presented on this 2-bit bus as TNETV1060 requests and TNETV1060 write data and read data in response to a request from the external VLYNQ device. VLYNQ reset configuration (IN). Two thousand clock cycles after the VLYNQ5 subsystem is released from reset, the state of this signal determines the VLYNQ bus width. For attachment to an external VLYNQ three-terminal device, both bits must be held low with an external pulldown. For attachment to an external VLYNQ five-terminal device, D1 is held low with an external pulldown, while D0 must be held high with an external pullup. If not used, hold low with an external 47-kΩ pulldown resistor.
L1		**VLYNQ5_TX_D1**			

3.3.9 Universal Asynchronous Receiver/Transmitter (UART)

The UART is compliant and compatible with many standard UART implementations. Due to the 3.3-V limits of the TNETV1060 I/O, an external 5-V compliant transceiver is required for those applications requiring a 5-V driver.

Table 3–18. UART I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
B3	I	**UART_CTS**			Clear to send control
A3	O	**UART_RTS**			Request to send control
B4	I	**UART_RX**			Receiver data
C4	O	**UART_TX**			Transmitter data

3.3.10 General-Purpose I/Os (GPIOs)

The TNETV1060 provides 52 GPIOs. Of the 52 GPIOs, only 8 are dedicated for primary use. All 52 GPIOs have the following register-programmable capabilities:

- Individual enable control
- Individual input or output designation

3.3.10.1 Dedicated GPIOs

Table 3–19. Dedicated GPIOs

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
R3	I/O	**GPIO0**		EXT_INT1	GPIOs designated as outputs send information out of the TNETV1060 from a control register. GPIOs designated as inputs receive external information through a different control register.
T3		**GPIO1**		EXT_INT2	
U3		**GPIO2**		EXT_INT3	
T2		**GPIO3**		EXT_INT4	
U2		**GPIO4**			
V2		**GPIO5**		SSP4	
U1		**GPIO6**			
V1		**GPIO7**			

3.3.10.2 Multiplexed GPIOs

Table 3–20. Multiplexed GPIOs

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
AB7	I/O	KEYPAD00		**GPIO08**	GPIOs designated as outputs send information out of the TNETV1060 from a control register. GPIOs designated as inputs receive external information through a different control register.
AA7		KEYPAD01		**GPIO09**	
AB8		KEYPAD02		**GPIO10**	
AA8		KEYPAD03		**GPIO11**	
Y8		KEYPAD04		**GPIO12**	
AB9		KEYPAD05		**GPIO13**	
AA9		KEYPAD06		**GPIO14**	
Y9		KEYPAD07		**GPIO15**	
AB10		KEYPAD08		**GPIO16**	
AA10		KEYPAD09		**GPIO17**	
Y10		KEYPAD10		**GPIO18**	
AB11		KEYPAD11		**GPIO19**	
AA11		KEYPAD12		**GPIO20**	
W11		KEYPAD13		**GPIO21**	
Y11		KEYPAD14		**GPIO22**	
AB12		KEYPAD15		**GPIO23**	
Y13		LCD_D00	MII_P0_CRS	**GPIO24**	
AB14		LCD_D01	MII_P0_TX_D0	**GPIO25**	
AA14		LCD_D02	MII_P0_TX_D1	**GPIO26**	
Y14		LCD_D03	MII_P0_TX_D2	**GPIO27**	
AB15		LCD_D04	MII_P0_TX_D3	**GPIO28**	
AA15		LCD_D05	MII_P0_TX_ENBL	**GPIO29**	
Y15		LCD_D06	MII_P0_TX_CLK	**GPIO30**	
AB16		LCD_D07	MII_P0_LINK	**GPIO31**	
AA16		LCD_D08	MII_P0_COL	**GPIO32**	
Y16		LCD_D09	MII_P0_RX_ERR	**GPIO33**	
AB17		LCD_D10	MII_P0_RX_CLK	**GPIO34**	
AA17		LCD_D11	MII_P0_RX_DV	**GPIO35**	
Y17		LCD_D12	MII_P0_RX_D0	**GPIO36**	
W17		LCD_D13	MII_P0_RX_D1	**GPIO37**	
AB18		LCD_D14	MII_P0_RX_D2	**GPIO38**	
AA18		LCD_D15	MII_P0_RX_D3	**GPIO39**	
M19		TELE_DCLK	MII_P1_CRS	**GPIO40**	
N20		TELE_DI	MII_P1_TX_D0	**GPIO41**	
M20		TELE_DO	MII_P1_TX_D1	**GPIO42**	
L19		TELE_CLK_I	MII_P1_TX_D2	**GPIO43**	
M21		TELE_RINGIN1	MII_P1_TX_D3	**GPIO44**	
M22		TELE_RINGIN2	MII_P1_TX_ENBL	**GPIO45**	
L21		TELE_RINGIN3	MII_P1_TX_CLK	**GPIO46**	
L22		TELE_RINGIN4	MII_P1_LINK	**GPIO47**	
L20		TELE_FS	MII_P1_COL	**GPIO48**	
K20		$\overline{\text{TELE\_CS}}$	MII_P1_RX_ERR	**GPIO49**	
K21		TELE_INT	MII_P1_RX_CLK	**GPIO50**	
K22		$\overline{\text{TELE\_RESET}}$	MII_P1_RX_DV	**GPIO51**	

3.3.10.3 Additional GPIOs

Certain TNETV1060 subsystems provide additional GPIO terminal capabilities as shown in Table 3–21. The control for these GPIO terminals is retained in the defined subsystem rather than the GPIO subsystem.

Table 3–21. Additional GPIOs

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
D3	I/O	**SSP0**			These SSP subsystem I/O signals can be configured as GPIOs [see section 3.3.6, *Sequencer Serial Port (SSP*)].
D1		**SSP1**			
D2		**SSP2**			
E4		**SSP3**			
V2		GPIO5		SSP4	
M3	I/O	**McBSP_CLK_RX**			These McBSP subsystem I/O signals can be configured as GPIOs [see section 3.3.6, *Sequencer Serial Port (SSP*)].
N3	I	**McBSP_D_RX**			
P2	I/O	**McBSP_FS_RX**			
N2	I/O	**McBSP_CLK_TX**			
P1	O	**McBSP_D_TX**			
P3	I/O	**McBSP_FS_TX**			
AB7	I/O	**KEYPAD00**		GPIO08	Any keypad terminal may be used as a GPIO when not in use as a keypad. There is no need to select the GPIO function placed on the 3rd I/O multiplexer.
AA7		**KEYPAD01**		GPIO09	
AB8		**KEYPAD02**		GPIO10	
AA8		**KEYPAD03**		GPIO11	
Y8		**KEYPAD04**		GPIO12	
AB9		**KEYPAD05**		GPIO13	
AA9		**KEYPAD06**		GPIO14	
Y9		**KEYPAD07**		GPIO15	
AB10		**KEYPAD08**		GPIO16	
AA10		**KEYPAD09**		GPIO17	
Y10		**KEYPAD10**		GPIO18	
AB11		**KEYPAD11**		GPIO19	
AA11		**KEYPAD12**		GPIO20	
W11		**KEYPAD13**		GPIO21	
Y11		**KEYPAD14**		GPIO22	
AB12		**KEYPAD15**		GPIO23	

3.3.11 MIPS Interrupt

Table 3–22. MIPS Interrupt I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
R3	I/O	GPIO0		**EXT_INT1**	Interrupt 1 (IN). This external interrupt enters the MIPS as INT_1.
T3	I/O	GPIO1		**EXT_INT2**	Interrupt 2 (IN). This external interrupt enters the MIPS as INT_2.
U3	I/O	GPIO2		**EXT_INT3**	Interrupt 3 (IN). This external interrupt enters the MIPS as INT_3.
T2	I/O	GPIO3		**EXT_INT4**	Interrupt 4 (IN). This external interrupt enters the MIPS as INT_4.
K21	I/O	**TELE_INT**	MII_P1_RX_CLK	GPIO50	Telephony subsystem interrupt (IN). This external interrupt enters the MIPS as INT_23 and the DSP as DSP_INT_12. This is the only externally-sourced DSP interrupt signal.

3.3.12 JTAG

3.3.12.1 MIPS and ASIC

This enhanced JTAG (EJTAG)-compliant port provides MIPS emulation control, MIPS boundary-scan control, and ASIC boundary-scan control. The ASIC boundary scan encompasses all TNETV1060 logic including the MIPS and DSP, but excludes the analog I/O signals found in the internal PHY devices and internal voice codec device. Besides the internal pulldown configuration on several of the I/Os, this JTAG implementation is IEEE Std 1149.1 compliant.

Table 3–23. MIPS JTAG I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
E3	I	**EJTAG_DINT**			MIPS and ASIC JTAG exception request. If not used, hold high (with internal pullup).
E2	I	**$\overline{\text{EJTAG\_SYSRST}}$**			Similar function as $\overline{\text{RESET\_I}}$. If not used, hold high (with internal pullup). Do not use this signal.
F3	I	**$\overline{\text{EJTAG\_TRST0}}$**			MIPS JTAG test reset. If not used, hold low (with internal pulldown). An external pullup should not be used.
E1	I	**$\overline{\text{EJTAG\_TRST1}}$**			ASIC JTAG test reset. If not used, hold low (with internal pulldown). An external pullup should not be used.
F2	I	**EJTAG_TCK**			MIPS and ASIC JTAG test clock. If not used, hold high (with internal pullup).
G3	I	**EJTAG_TDI**			MIPS and ASIC JTAG test data input. If not used, hold high (with internal pullup).
F1	O	**EJTAG_TDO**			MIPS and ASIC JTAG test data output
G2	I	**EJTAG_TMS**			MIPS and ASIC JTAG test mode select. If not used, hold high (with internal pullup).

3.3.12.2 DSP

This JTAG-compliant port provides DSP emulation control and DSP boundary-scan control. Besides the internal pulldown configuration on several of the I/Os, this JTAG implementation is IEEE Std 1149.1 compliant.

Table 3–24. DSP JTAG I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
H3	I/O	**JTAG_EMU0**			DSP special-emulation control modes. More information link TBD. If not used, hold high (with internal pullup).
G1		**JTAG_EMU1**			
H2	I	**$\overline{\text{JTAG\_TRST}}$**			DSP JTAG test reset. If not used, hold low (with internal pulldown). An external pullup should not be used.
J3	I	**JTAG_TCK**			DSP JTAG test clock. If not used, hold high (with internal pullup).
H1	I	**JTAG_TDI**			DSP JTAG test data input. If not used, hold high (with internal pullup).
J2	O	**JTAG_TDO**			DSP JTAG test data output
J1	I	**JTAG_TMS**			DSP JTAG test mode select. If not used, hold high (with internal pullup).

3.3.13 System Clock and Reset

Table 3–25. Clock and Reset I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
P22	I/O	**REF_CLK_I**			Differential crystal pair for the entire TNETV1060 (see Figure 3–2 for the TNETV1060 clock structure) The target input frequency is 25 MHz.
N22	O	**REF_CLK_O**			
P21	I	**ALT_CLK_I**			Alternate non-crystal clock input. This clock can be programmed to replace the REF_CLK in any TNETV1060 subsystem (see Figure 3–2 for the TNETV1060 clock structure). The target input frequency is 25 MHz.
R1	I/O	**AIC_CLK_I**			Differential crystal pair for the internal telephony clock (see Figure 3–2 for the TNETV1060 clock structure) The recommended frequency is 8.1920 MHz.
T1	O	**AIC_CLK_O**			
C1	I	**$\overline{\text{RESET\_I}}$**			Reset input for the TNETV1060 is provided by the external power-on-reset supervisor.
C2	O	**$\overline{\text{RESET\_O}}$**			Reset output from the TNETV1060 is register controlled (on/off), as well as activated, by $\overline{\text{RESET\_I}}$.
E2	I	**$\overline{\text{EJTAG\_SYSRST}}$**			Similar function as $\overline{\text{RESET\_I}}$. If not used, hold high (with internal pullup). Do not use this signal.
K22	I/O	**$\overline{\text{TELE\_RESET}}$**	MII_P1_RX_DV	GPIO51	Telephony subsystem reset (OUT). This reset is activated by $\overline{\text{RESET\_I}}$ and register control in the DSP subsystem.

3.3.14 Power

3.3.14.1 I/O

Table 3–26. I/O Power

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
D7	P	VDDS			3.3-V power supply for the I/O ring
D8		VDDS			
D9		VDDS			
D10		VDDS			
D13		VDDS			
D14		VDDS			
D15		VDDS			
D16		VDDS			
G4		VDDS			
G19		VDDS			
H4		VDDS			
H19		VDDS			
J4		VDDS			
J19		VDDS			
K4		VDDS			
K19		VDDS			
N4		VDDS			
P4		VDDS			
W9		VDDS			
W10		VDDS			
W13		VDDS			
W14		VDDS			
W15		VDDS			
W16		VDDS			

3.3.14.2 Core

Table 3–27. Core Power

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
J10	P	**VDD**			1.5-V power supply for the logic core If the internal voltage regulator is used, this power is provided by the external npn pass transistors.
J11		**VDD**			
J12		**VDD**			
J13		**VDD**			
K9		**VDD**			
K14		**VDD**			
L9		**VDD**			
L14		**VDD**			
M9		**VDD**			
M14		**VDD**			
N9		**VDD**			
N14		**VDD**			
P10		**VDD**			
P11		**VDD**			
P12		**VDD**			
P13		**VDD**			

3.3.14.3 Analog

Table 3–28. Analog Power

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
N19	P	**VDD_PLL**			1.5-V isolated supply power for the internal analog PLL devices
U21	P	**VDDA_PHY0_1**			3.3-V isolated analog supply power for internal Ethernet PHY port 0 (TX)
U20	P	**VDDA_PHY0_2**			3.3-V isolated analog supply power for internal Ethernet PHY port 0 (RX and ADC)
Y20	P	**VDDA_PHY0_34**			3.3-V isolated analog supply power for internal Ethernet PHY port 0 (all other internal circuits)
U22	P	**VDDA_PHY1_1**			3.3-V isolated analog supply power for internal ethernet PHY port 1 (TX)
U19	P	**VDDA_PHY1_2**			3.3-V isolated analog supply power for internal Ethernet PHY port 1 (RX and ADC)
P20	P	**VDDA_PHY1_34**			3.3-V isolated analog supply power for internal Ethernet PHY port 1 (all other internal circuits)

3.3.15 Ground

3.3.15.1 Digital

Table 3–29. Digital Ground

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
A1	G	VSS			Ground
A2		VSS			
A21		VSS			
A22		VSS			
B1		VSS			
B2		VSS			
B21		VSS			
B22		VSS			
C3		VSS			
C20		VSS			
D4		VSS			
D19		VSS			
J9		VSS			
J14		VSS			
K10		VSS			
K11		VSS			
K12		VSS			
K13		VSS			
L10		VSS			
L11		VSS			
L12		VSS			
L13		VSS			
M10		VSS			
M11		VSS			
M12		VSS			
M13		VSS			
N10		VSS			
N11		VSS			
N12		VSS			
N13		VSS			

3.3.15.2 Analog

Table 3–30. Analog Ground

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
W4	G	**VSS_AIC**			Isolated analog ground
Y3		**VSS_AIC**			
AA1		**VSS_AIC**			
AA2		**VSS_AIC**			
AB1		**VSS_AIC**			
AB2		**VSS_AIC**			
V21	G	**VSS_PHY0_1**			Isolated analog ground for internal Ethernet PHY port 0 (TX)
W21		**VSS_PHY0_1**			
V20	G	**VSS_PHY0_2**			Isolated analog ground for internal Ethernet PHY port 0 (RX and ADC)
W20	G	**VSS_PHY0_34**			Isolated analog ground for internal Ethernet PHY port 0 (all other internal circuits)
V19	G	**VSS_PHY0_ESD**			ESD-specific ground for internal Ethernet PHY port 0
R21	G	**VSS_PHY1_1**			Isolated analog ground for internal Ethernet PHY port 1 (TX)
T21		**VSS_PHY1_1**			
T20	G	**VSS_PHY1_2**			Isolated analog ground for internal Ethernet PHY port 1 (RX and ADC)
R20	G	**VSS_PHY1_34**			Isolated analog ground for internal Ethernet PHY port 1 (all other internal circuits)
T19	G	**VSS_PHY1_ESD**			ESD-specific ground for internal Ethernet PHY port 1
P14	G	**VSS_PLL**			Isolated ground for the internal analog PLL devices
N21	G	**VSS_REF_CLK**			Isolated ground for the REF_CLK oscillator (see REF_CLK_I and REF_CLK_O). This V_{SS} terminal remains independent of all other V_{SS} terminals and must not be connected to the common board ground.
P9	G	**VSS_AIC_CLK**			Isolated ground for the telephony AIC_CLK oscillator (see AIC_CLK_I and AIC_CLK_O). This V_{SS} terminal remains independent of all other V_{SS} terminals and must not be connected to the common board ground.

3.3.16 Voltage Regulators

Three internal voltage regulators are required to supply the power consumption needs of the TNETV1060 VDD (1.5 V) core voltage. The maximum supply current capacity of these three voltage regulators is 1.33 A. The necessary 1.2-V bandgap reference is created internally (with an additional small voltage regulator) through the VDDS (3.3 V) power rail. As shown in Table 3–31 and Figure 4–7, three external npn pass transistors are required to regulate current into the TNETV1060. In addition, one 10-μF tantalum capacitor is necessary in the external-regulator design.

TI recommends a 2.0-W supply be used for the 3.3-V (V_{DDS}) power rail and that the internal voltage regulator be used to generate the 1.5-V (V_{DD}) core voltage. This provides margin for the TNETV1060 to power up.

Table 3–31. Voltage Regulator I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
AB6	O	**VR_BASE1**			Voltage regulator 1 drive to the base of external npn pass transistor one
R2	O	**VR_BASE2**			Voltage regulator 2 drive to the base of external npn pass transistor two
Y22	O	**VR_BASE3**			Voltage regulator 3 drive to the base of external npn pass transistor three
AA6	I	**$\overline{\text{VR\_ENBL}}$**			Voltage regulator enable. When high (3.3 V), the internal regulators are in power-down mode. When low (0 V), the regulators are functional, and power for VDD (1.5 V) can be supplied from the external npn pass transistors.

3.3.17 Test

Table 3–32. Test I/Os

TERMINAL NO.	TYPE	1st	2nd	3rd	DESCRIPTION
F4	I	**TEST**			For normal operation, must be held low (with internal pulldown).
Y21	I	**PHY_TEST**			For normal operation, must be held low with external pulldown.
Y12	I/O	LCD_PIXEL_STRB	**DSP_FUNCTEST0**		For test purposes only. Do not select multiplexer for use.
AB13	I/O	LCD_E1	**DSP_FUNCTEST1**		For test purposes only. Do not select multiplexer for use.

3.3.18 No Connection

Table 3–33. No Connection Terminals

TERMINAL NO.	TYPE	DESCRIPTION
L3, L4, M1, M2, M4, N1, R4, T4, U4, V3, V4, W1, W2, W3, W5, W6, W7, W8, Y1, Y2, Y4, Y5, Y6, Y7, AA3, AA4, AA5, AB3, AB4, AB5	N/C	No connection. Do not bias. These terminals may be connected internally. Do not use as a routing point.

3.4 Boot Configuration

Certain TNETV1060 I/O terminals provide a boot-configuration option. These special I/O terminals read the state of the incoming signal at $\overline{\text{RESET\_I}}$ deactivation and store the received value for the uses shown in Table 3–34. Many of the stored values can be viewed in the SYS_CONFIG (BOOT) register. External pullup or pulldown resistors should be placed on these boot configuration I/O terminals to obtain the desired results.

Table 3–34. Boot Configuration I/Os

EXTERNAL TERMINAL	REGISTER		DEFAULT BIT CODE	DESCRIPTION
	NAME	BIT		
EM_A[23:22]	FLASH_WIDTH	8:7	01	Flash width. Defines the flash ($\overline{\text{EM\_CS0}}$) data bus width. 11 = 32-bit flash 10 = 32-bit flash 01 = 16-bit flash 00 = 8-bit flash The width of the flash data bus may be adjusted through program control using the EMIF (ASYNCHRONOUS_CONFIG_BANK_1) register.
EM_A[21]	ENDIAN_MODE	6	N/A	Endian mode. Defines the endian operating mode for the TNETV1060. 1 = Big endian 0 = Little endian A default is not available. This bit must be programmed externally, even when DEFAULT = 1.
EM_A[20:18]	BOOT_SELECT	2:0	001	Boot memory location select. The MIPS processor always starts the TNETV1060 boot from the internal 4K-byte ROM. Within this ROM, the MIPS code interrogates these bits and determines where the rest of the boot code resides. 111 = Boot from VLYNQ5 port 110 = Boot from serial EEPROM through the SSP 101 = Boot from $\overline{\text{EM\_CS5}}$ (asynchronous memory) 100 = Boot from $\overline{\text{EM\_CS4}}$ (asynchronous memory) 011 = Boot from $\overline{\text{EM\_CS3}}$ (asynchronous memory) 010 = Boot from $\overline{\text{EM\_CS1}}$ and $\overline{\text{EM\_CS2}}$ (SDRAM) 001 = Boot from $\overline{\text{EM\_CS0}}$ (flash) 000 = Boot from internal 4K-Byte ROM only The boot location value may be adjusted through program control using the BOOT_OVERRIDE bits in the SYS_CONFIG (BOOT) register.
EM_A[17]	PLL_MODE	5	0	PLL mode. As shown in Figure 3–2, several TNETV1060 PLL generators can be bypassed. 1 = Bypass the PLL, for test-mode use only 0 = Use the standard PLL configuration
EM_A[16]	WD_MODE (inverted)	4	0	System watchdog timer disable mode. This terminal may be used to permanently disable the system watchdog timer. The WD_MODE register bit contents are inverted from the following definition. 1 = System watchdog timer is always disabled. 0 = System watchdog timer may be enabled (see EM_A15).
EM_A[15]	WD_WR_MODE	3	0	System watchdog timer write protect mode. This terminal may be used to generate a write protect feature, permanently preventing any changes to the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register. 1 = The system watchdog timer is write protected. The operational state of the timer is determined from the reset contents of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register. 0 = The system watchdog timer may be enabled and disabled through the use of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register.

Table 3–34. Boot Configuration I/Os (Continued)

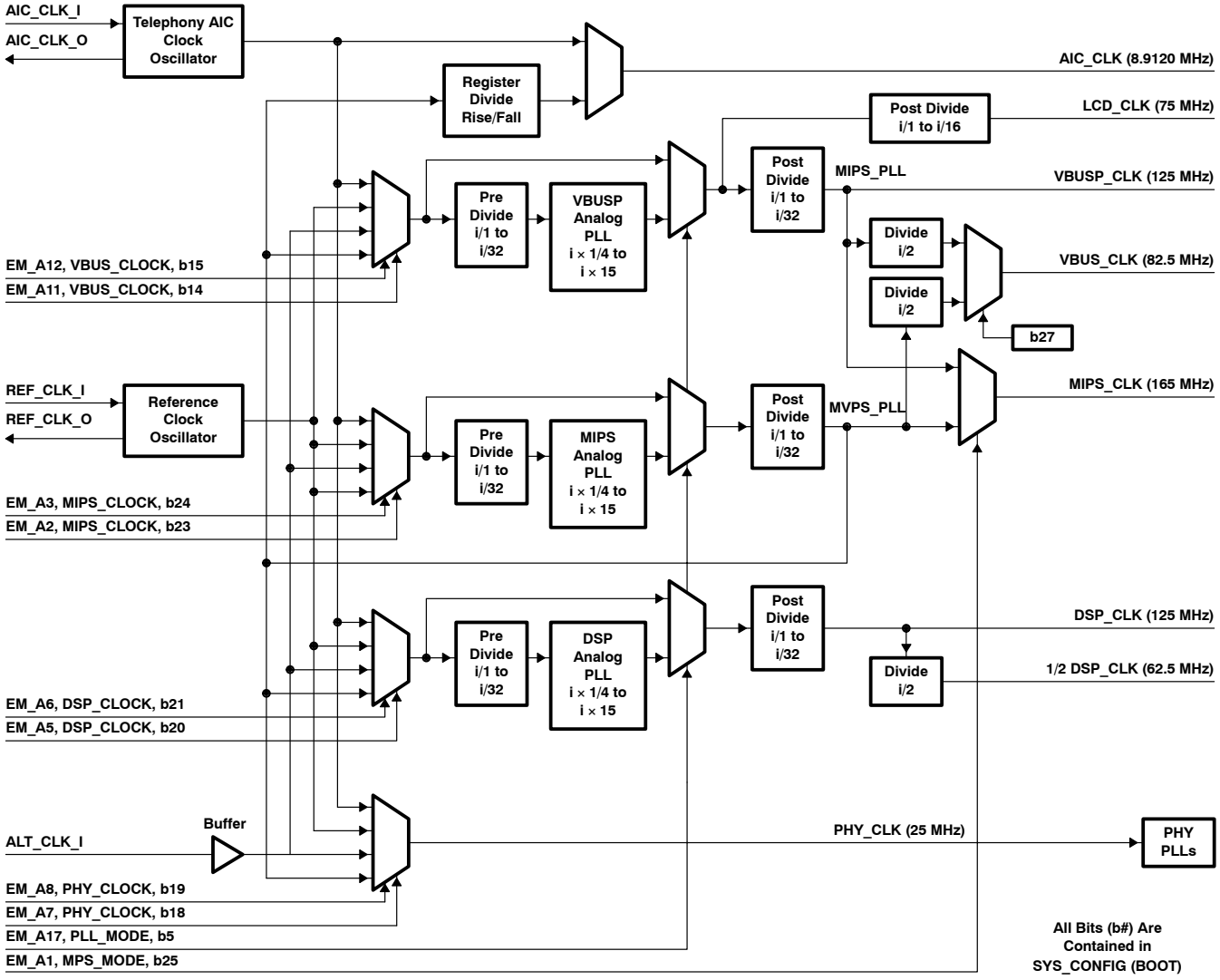
EXTERNAL TERMINAL	REGISTER		DEFAULT BIT CODE	DESCRIPTION
	NAME	BIT		
EM_A[14]	SDRAM_MODE	9	1	EMIF SDRAM clock mode. The EMIF external clock EM_CLK (SDRAM clock) may be programmed for half speed (VBUSP_CLK/2). In either mode, the SDRAM and asynchronous memory external timing follows the clock speed. Thus, the EMIF external timing runs at one-half rate when selected for half-speed mode. 1 = EMIF runs at full speed (VBUSP_CLK) 0 = EMIF runs at half speed (1/2 VBUSP_CLK)
EM_A[13]	SDRAM_INIT	10	0	EMIF SDRAM initialization mode. The SDRAM initialization sequence is reduced by forcing the SDRAM refresh counter to a minimum value as defined in the EMIF (SDRAM_REFRESH_CTRL) register. This minimum time value drastically reduces the long delay at the start of the SDRAM initialization. 1 = Reduced SDRAM initialization timing for test purposes 0 = Normal SDRAM initialization operation
EM_A[12:11]	VBUSP_CLOCK	15:14	01	VBUSP clock input multiplexer select. As shown in Figure 3–2, the input clock source for the VBUSP_CLK is determined by the state of these I/O terminals: 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[10:9]	NC_CLOCK	17:16	01	No connect input multiplexer select. These I/O balls should be programmed to the same state as the MIPS_CLOCK bits EM_A[3:2]. This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[8:7]	PHY_CLOCK	19:18	01	Ethernet PHY clock input multiplexer select (see Figure 3–2). The input clock source for the Ethernet PHY_CLK is determined by the state of these I/O terminals: 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[6:5]	DSP_CLOCK	21:20	01	DSP clock input multiplexer select (see Figure 3–2). The input clock source for the DSP_CLK is determined by the state of these I/O terminals: 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.

Table 3–34. Boot Configuration I/Os (Continued)

EXTERNAL TERMINAL	REGISTER		DEFAULT BIT CODE	DESCRIPTION
	NAME	BIT		
EM_A[4]	NC_MODE	22	1	No connect mode. This I/O ball should be programmed to the default value. This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register.
EM_A[3:2]	MIPS_CLOCK	24:23	01	MIPS clock input multiplexer select (see Figure 3–2). The input clock source for the MIPS_CLK is determined by the state of these I/O terminals: 11 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[1]	MIPS_MODE	25	1	MIPS clock mode (see Figure 3–2). The clock source for the MIPS_CLK may be synchronous utilizing the VBUSP_CLK or asynchronous derived from the MIPS PLL. 1 = MIPS_CLK is asynchronous. 0 = MIPS_CLK is synchronous.
EM_A[0]	DEFAULT	26	N/A	Default control. Defines the $\overline{\text{RESET\_I}}$ contents of the SYS_CONFIG (BOOT) register. 1 = Boot configuration is defined by the Default field in this table, initialization state of EM_A[23:1] is ignored. 0 = Initialization state of EM_A[23:1] determines the boot configuration.
VLYNQ5_TX_D0 **VLYNQ5_TX_D1**	N/A	N/A	N/A	VLYNQ 5-terminal configuration. After a VLYNQ 5-terminal subsystem reset event, the state of this signal determines the VLYNQ bus width. For attachment to an external VLYNQ 3-terminal device, both bits must be held low with an external pulldown. For attachment to an external VLYNQ 5-terminal device, VLYNQ5_TX_D1 is held low with an external pulldown while VLYNQ5_TX_D0 must be held high with an external pullup.

3.4.1 Clock Distribution

Figure 3–2 shows the TNETV1060 clock distribution network. As shown in Table 3–34, the multiplexed selection network is defined at $\overline{\text{RESET\_I}}$ deactivation through the use of the special boot configuration I/O terminals.



NOTE: All bits (b#) are contained in SYS_CONFIG (BOOT).

Figure 3–2. TNETV1060 Clock Distribution

3.4.2 SYS_CONFIG (BOOT)

Bits [31:8] of the 32-bit VBUSP address bus define the block location of the system configuration controller (SYS_CONFIG) starting at 0x0861:1A00 and ending at 0x0861:1AFF. Address bits [7:0] are used to define each 32-bit-wide address location within the SYS_CONFIG block. The SYS_CONFIG block only uses address bits [3:0], thus, register addressing greater than 0x0861:1A0F allows aliased writes and reads of SYS_CONFIG registers in the range 0x0861:1A00 to 0x0861:1A0F. The bit map is shown in Table 3–35, with bit descriptions shown in Table 3–36.

Table 3–35. SYS_CONFIG (BOOT) Register

0x0861:1A00	SYS_CONFIG				BOOT				Boot Configuration							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VBUS MODE	DEFAULT (rd-only)	MIPS MODE (rd-only)	MIPS CLOCK		NC MODE	DSP CLOCK		PHY CLOCK		NC CLOCK	
Reset 0 Reset 1	0 0	0 0	0 0	0 0	0 0	EM_A0 EM_A0	EM_A1 1	EM_A3 0	EM_A2 1	EM_A4 1	EM_A6 0	EM_A5 1	EM_A8 0	EM_A7 1	EM_A10 0	EM_A9 1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBUSP CLOCK			BOOT OVERRIDE		SDRAM INIT (rd-only)	SDRAM MODE (rd-only)	FLASH WIDTH (rd-only)		ENDIAN MODE (rd-only)	PLL MODE (rd-only)	WD MODE (rd-only)	WD WR MODE (rd-only)		BOOT SELECT (rd-only)	
Reset 0 Reset 1	EM_A12 0	EM_A11 1	0 0	0 0	0 0	EM_A13 0	EM_A14 1	EM_A23 0	EM_A22 1	EM_A21 EM_A21	EM_A17 0	EM_A16 1	EM_A15 0	EM_A20 0	EM_A19 0	EM_A18 1

Table 3–36. SYS_CONFIG (BOOT) Register Bits

BIT	NAME	DESCRIPTION
31:28	Reserved	Always returns zero when read
27	VBUS_MODE	VBUS clock mode. The state of this bit determines the VBUS_CLK source (see Figure 3–2). 1 = VBUS_CLK = 1/2(MIPS PLL output after the post divider) 0 = VBUS_CLK = 1/2(VBUSP_CLK) Because this bit is adjusted through program control, all VBUS_CLK receiver logic must have clocks powered off through the SYS_CLK (PWR_DWN) register. In addition, the same VBUS_CLK receiver logic should be held in reset through the SYS_RESET (PERIPH_CTRL) register. Failure to follow these precautions can introduce metastability, causing undesirable system problems.
26	DEFAULT	Default control (read only). The state of this bit is always determined by EM_A0 after a $\overline{\text{RESET\_I}}$ event (see Table 3–34). The contents of the rest of the bits in this register depend on the state of this bit after an $\overline{\text{RESET\_I}}$ event: 1 = Reset 1 event = Content of the bits in this register are fixed by the hardware. 0 = Reset 0 event = Content of the bits in this register are dependent on the state of EM_A[23:1].
25	MIPS_MODE	MIPS clock mode (read only). The state of this bit is determined by EM_A1 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 1 = MIPS_CLK is asynchronous. 0 = MIPS_CLK is synchronous.
24:23	MIPS_CLOCK	MIPS clock input multiplexer select. The state of these bits is determined by EM_A[3:2] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 11 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.

Table 3–36. SYS_CONFIG (BOOT) Register Bits (Continued)

BIT	NAME	DESCRIPTION
22	NC_MODE	No connect mode. The state of this bit is determined by EM_A4 after a RESET_I event when DEFAULT = 0b (see Table 3–34). In addition, this bit may be changed through program control.
21:20	DSP_CLOCK	DSP clock input multiplexer select. The state of these bits is determined by EM_A[6:5] after a RESET_I event when DEFAULT = 0b (see Table 3–34). 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
19:18	PHY_CLOCK	Ethernet clock input multiplexer select. The state of these bits is determined by EM_A[8:7] after a RESET_I event when DEFAULT = 0b (see Table 3–34). 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
17:16	NC_CLOCK	No connect clock input multiplexer select. The state of these bits is determined by EM_A[10:9] after a RESET_I event when DEFAULT = 0b (see Table 3–34). In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
15:14	VBUSP_CLOCK	VBUSP clock input multiplexer select. The state of these bits is determined by EM_A[12:11] after a RESET_I event when DEFAULT = 0b (see Table 3–34). 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Telephony clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
13:11	BOOT_OVERRIDE	Boot select overide. These bits may be adjusted through program control in order to override the BOOT_SELECT configuration bits contained in this same register. Reset events not employing the RESET_I input terminal are able to boot from a location other than the one defined by BOOT_SELECT. 111 = Boot from VLYNQ5 port 110 = Boot from serial EEPROM through the sequencer serial port 101 = Boot from EM_CS5 (asynchronous memory) 100 = Boot from EM_CS4 (asynchronous memory) 011 = Boot from EM_CS3 (asynchronous memory) 010 = Boot from EM_CS1 and EM_CS2 (SDRAM) 001 = Boot from EM_CS0 (flash) 000 = Ignore this BOOT_OVERIDE, the BOOT_SELECT bits in this same register define the boot location.

Table 3–36. SYS_CONFIG (BOOT) Register Bits (Continued)

BIT	NAME	DESCRIPTION
10	SDRAM_INIT	EMIF SDRAM initialization mode (read only). The state of this bit is determined by EM_A13 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 1 = Reduced SDRAM initialization timing for test purposes 0 = Normal SDRAM initialization operation
9	SDRAM_MODE	EMIF SDRAM clock mode (read only). The state of this bit is determined by EM_A14 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 1 = EMIF runs at full speed (VBUSP_CLK). 0 = EMIF runs at one-half speed (1/2 VBUSP_CLK).
8:7	FLASH_WIDTH	FLASH width (read only). The state of these bits is determined by EM_A[23:22] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 11 = 32-bit flash 10 = 32-bit flash 01 = 16-bit flash 00 = 8-bit flash
6	ENDIAN_MODE	Endian mode (read only). The state of this bit is determined by EM_A21 after a $\overline{\text{RESET\_I}}$ event, regardless of the state of DEFAULT (see Table 3–34). 1 = Big endian 0 = Little endian
5	PLL_MODE	PLL mode (read only). The state of this bit is determined by EM_A17 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 1 = Bypass the PLL, for test-mode use only 0 = Use the standard PLL configuration
4	WD_MODE	Watchdog timer disable mode (read only). The state of this bit is determined by inverted contents of EM_A16 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 1 = System watchdog timer may be enabled, see AD_WR_MODE. 0 = System watchdog timer is always disabled.
3	WD_WR_MODE	System watchdog timer write protect mode (read only). The state of this bit is determined by EM_A15 after a $\overline{\text{RESET\_I}}$ event (see Table 3–34). 1 = The system watchdog timer is write protected. The operational state of the timer is determined from the reset contents of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register. 0 = The system watchdog timer may be enabled and disabled through the use of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register.
2:0	BOOT_SELECT	Boot memory location select (read only). The state of these bits is determined by EM_A[20:18] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3–34). 111 = Boot from VLYNQ5 port 110 = Boot from serial EEPROM through the sequencer serial port 101 = Boot from $\overline{\text{EM\_CS5}}$ (asynchronous memory) 100 = Boot from $\overline{\text{EM\_CS4}}$ (asynchronous memory) 011 = Boot from $\overline{\text{EM\_CS3}}$ (asynchronous memory) 010 = Boot from $\overline{\text{EM\_CS1}}$ and $\overline{\text{EM\_CS2}}$ (SDRAM) 001 = Boot from $\overline{\text{EM\_CS0}}$ (flash) 000 = Boot from internal 4K-byte ROM only

3.5 Multiplex Configuration

The TNETV1060 contains 324 I/O terminals. Of the 324 terminals, 71 provide multiple I/O functional modes. The I/Os featuring multiple functional modes are shown in Table 3–2. The SYS_RESET (PIN_SEL_NO) register set may be used to individually select the desired functionality of each TNETV1060 I/O terminal. The entire register set is shown in Table 3–37.

All of the terminals with multiple I/O functional modes are set to the nonfunctional 3-state mode by power-on reset (POR). To be used, these I/O terminals must be programmed as shown in Table 3–37.

Table 3–37. SYS_RESET (PIN_SEL) Register Set

ADDRESS	BLOCK FUNCTION	NAME	DESCRIPTION
0x0861:160C	SYS_RESET	PIN_SEL_1	I/O multiplex pin select 1
0x0861:1610	SYS_RESET	PIN_SEL_2	I/O multiplex pin select 2 (N/A, no multiplexed I/O in this set)
0x0861:1614	SYS_RESET	PIN_SEL_3	I/O multiplex pin select 3 (N/A, no multiplexed I/O in this set)
0x0861:1618	SYS_RESET	PIN_SEL_4	I/O multiplex pin select 4
0x0861:161C	SYS_RESET	PIN_SEL_5	I/O multiplex pin select 5
0x0861:1620	SYS_RESET	PIN_SEL_6	I/O multiplex pin select 6 (N/A, no multiplexed I/O in this set)
0x0861:1624	SYS_RESET	PIN_SEL_7	I/O multiplex pin select 7
0x0861:1628	SYS_RESET	PIN_SEL_8	I/O multiplex pin select 8
0x0861:162C	SYS_RESET	PIN_SEL_9	I/O multiplex pin select 9
0x0861:1630	SYS_RESET	PIN_SEL_10	I/O multiplex pin select 10
0x0861:1634	SYS_RESET	PIN_SEL_11	I/O multiplex pin select 11
0x0861:1638	SYS_RESET	PIN_SEL_12	I/O multiplex pin select 12 (N/A, no multiplexed I/O in this set)
0x0861:163C	SYS_RESET	PIN_SEL_13	I/O multiplex pin select 13
0x0861:1640	SYS_RESET	PIN_SEL_14	I/O multiplex pin select 14
0x0861:1644	SYS_RESET	PIN_SEL_15	I/O multiplex pin select 15 (N/A, no multiplexed I/O in this set)
0x0861:1648	SYS_RESET	PIN_SEL_16	I/O multiplex pin select 16 (N/A, no multiplexed I/O in this set)
0x0861:164C	SYS_RESET	PIN_SEL_17	I/O multiplex pin select 17 (N/A, no multiplexed I/O in this set)
0x0861:1650	SYS_RESET	PIN_SEL_18	I/O multiplex pin select 18 (N/A, no multiplexed I/O in this set)
0x0861:1654	SYS_RESET	PIN_SEL_19	I/O multiplex pin select 19 (N/A, no multiplexed I/O in this set)
0x0861:1658	SYS_RESET	PIN_SEL_20	I/O multiplex pin select 20 (N/A, no multiplexed I/O in this set)
0x0861:165C	SYS_RESET	PIN_SEL_21	I/O multiplex pin select 21

Bits 31–8 of the 32-bit VBUSP address bus define the block location of the system reset controller (SYS_RESET) starting at 0x0861:1600 and ending at 0x0861:16FF. Address bits 7–0 are used to define each 32-bit-wide address location within the SYS_RESET block. The SYS_RESET block only uses address bits 6–0, thus, register addressing greater than 0x0861:167F allows aliased writes and reads of SYS_RESET registers in the range 0x0861:1600 to 0x0861:167F.

3.5.1 SYS_RESET (PIN_SEL)

Tables 3–38 through 3–58 are detailed maps covering the memory range 0x0861:160C to 0x0861:165C, with bit descriptions in Table 3–59.

Table 3–38. SYS_RESET (PIN_SEL_1) Register

0x0861:160C	SYS_RESET				PIN_SEL_1				I/O Multiplex Pin Select 1							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL H4		N/A TERMINAL E1		N/A TERMINAL F3		N/A TERMINAL E2		N/A TERMINAL E3		N/A TERMINAL A2		SSP3 TERMINAL E4		SSP2 TERMINAL D2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SSP1 TERMINAL D1		SSP0 TERMINAL D3		N/A TERMINAL G4		N/A TERMINAL K9		N/A TERMINAL C2		N/A TERMINAL C1		N/A TERMINAL A1		N/A TERMINAL F4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–39. SYS_RESET (PIN_SEL_2) Register

0x0861:1610	SYS_RESET				PIN_SEL_2				I/O Multiplex Pin Select 2							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL K2		N/A TERMINAL K3		N/A TERMINAL J1		N/A TERMINAL L11		N/A TERMINAL J2		N/A TERMINAL H1		N/A TERMINAL J4		N/A TERMINAL J3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL H2		N/A TERMINAL G1		N/A TERMINAL H3		N/A TERMINAL G2		N/A TERMINAL B1		N/A TERMINAL F1		N/A TERMINAL G3		N/A TERMINAL F2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–40. SYS_RESET (PIN_SEL_3) Register

0x0861:1614	SYS_RESET				PIN_SEL_3				I/O Multiplex Pin Select 3							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL N4		N/A TERMINAL M11		N/A TERMINAL M3		N/A TERMINAL N1		N/A TERMINAL M1		N/A TERMINAL M9		N/A TERMINAL M2		N/A TERMINAL M4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL L4		N/A TERMINAL L10		N/A TERMINAL L3		N/A TERMINAL L9		N/A TERMINAL K4		N/A TERMINAL L1		N/A TERMINAL L2		N/A TERMINAL K1	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–41. SYS_RESET (PIN_SEL_4) Register

0x0861:1618	SYS_RESET				PIN_SEL_4				I/O Multiplex Pin Select 4							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO3 TERMINAL T2		GPIO2 TERMINAL U3		GPIO1 TERMINAL T3		GPIO0 TERMINAL R3		N/A TERMINAL N11		N/A TERMINAL N9		N/A TERMINAL T1		N/A TERMINAL P9	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL R1		N/A TERMINAL M10		N/A TERMINAL R2		N/A TERMINAL P3		N/A TERMINAL P2		N/A TERMINAL P1		N/A TERMINAL N3		N/A TERMINAL N2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–42. SYS_RESET (PIN_SEL_5) Register

0x0861:161C	SYS_RESET				PIN_SEL_5				I/O Multiplex Pin Select 5							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL W7		N/A TERMINAL W3		N/A TERMINAL V3		N/A TERMINAL AB2		N/A TERMINAL T4		N/A TERMINAL V4		N/A TERMINAL U4		N/A TERMINAL R4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL AB1		GPIO7 TERMINAL V1		GPIO6 TERMINAL U1		GPIO5 TERMINAL V2		GPIO4 TERMINAL U2		N/A TERMINAL N10		N/A TERMINAL P4		N/A TERMINAL P10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–43. SYS_RESET (PIN_SEL_6) Register

0x0861:1620	SYS_RESET				PIN_SEL_6				I/O Multiplex Pin Select 6							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL Y6		N/A TERMINAL Y7		N/A TERMINAL AB5		N/A TERMINAL AA5		N/A TERMINAL Y5		N/A TERMINAL Y4		N/A TERMINAL AA4		N/A TERMINAL AA3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL AB4		N/A TERMINAL AB3		N/A TERMINAL Y2		N/A TERMINAL W2		N/A TERMINAL Y1		N/A TERMINAL W1		N/A TERMINAL W4		N/A TERMINAL AA1	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–44. SYS_RESET (PIN_SEL_7) Register

0x0861:1624	SYS_RESET				PIN_SEL_7				I/O Multiplex Pin Select 7							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KEYPAD07 TERMINAL Y9		KEYPAD06 TERMINAL AA9		KEYPAD05 TERMINAL AB9		N/A TERMINAL W9		KEYPAD04 TERMINAL Y8		KEYPAD03 TERMINAL AA8		KEYPAD02 TERMINAL AB8		KEYPAD01 TERMINAL AA7	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYPAD00 TERMINAL AB7		N/A TERMINAL AB6		N/A TERMINAL AA6		N/A TERMINAL Y3		N/A TERMINAL W6		N/A TERMINAL W8		N/A TERMINAL W5		N/A TERMINAL AA2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–45. SYS_RESET (PIN_SEL_8) Register

0x0861:1628	SYS_RESET				PIN_SEL_8				I/O Multiplex Pin Select 8							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LCD_PIXEL_STRB TERMINAL Y12		N/A TERMINAL W13		LCD_BIAS_E0 TERMINAL AA12		N/A TERMINAL P12		N/A TERMINAL M12		KEYPAD15 TERMINAL AB12		KEYPAD14 TERMINAL Y11		KEYPAD13 TERMINAL W11	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYPAD12 TERMINAL AA11		N/A TERMINAL P11		KEYPAD11 TERMINAL AB11		N/A TERMINAL W10		N/A TERMINAL L12		KEYPAD10 TERMINAL Y10		KEYPAD09 TERMINAL AA10		KEYPAD08 TERMINAL AB10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–46. SYS_RESET (PIN_SEL_9) Register

0x0861:162C	SYS_RESET				PIN_SEL_9				I/O Multiplex Pin Select 9							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LCD_D09 TERMINAL Y16		LCD_D08 TERMINAL AA16		LCD_D07 TERMINAL AB16		LCD_D06 TERMINAL Y15		N/A TERMINAL N12		LCD_D05 TERMINAL AA15		LCD_D04 TERMINAL AB15		N/A TERMINAL W14	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCD_D03 TERMINAL Y14		LCD_D02 TERMINAL AA14		LCD_D01 TERMINAL AB14		LCD_D00 TERMINAL Y13		N/A TERMINAL M13		LCD_VSYNC_A TERMINAL AA13		$\overline{\text{LCD\_HSYNC\_W}}$ TERMINAL W12		LCD_E1 TERMINAL AB13	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–47. SYS_RESET (PIN_SEL_10) Register

0x0861:1630	SYS_RESET				PIN_SEL_10				I/O Multiplex Pin Select 10							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	$\overline{\text{P1\_100MB}}$ TERMINAL AB21		$\overline{\text{P0\_FDUPLEX}}$ TERMINAL AA20		N/A TERMINAL P13		N/A TERMINAL W16		N/A TERMINAL K13		$\overline{\text{P0\_ACTIVITY}}$ TERMINAL AB20		$\overline{\text{P0\_LINK}}$ TERMINAL AA19		$\overline{\text{P0\_100MB}}$ TERMINAL AB19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCD_D15 TERMINAL AA18		LCD_D14 TERMINAL AB18		LCD_D13 TERMINAL W17		LCD_D12 TERMINAL Y17		N/A TERMINAL N13		N/A TERMINAL W15		LCD_D11 TERMINAL AA17		LCD_D10 TERMINAL AB17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–48. SYS_RESET (PIN_SEL_11) Register

0x0861:1634	SYS_RESET				PIN_SEL_11				I/O Multiplex Pin Select 11							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL W21		N/A TERMINAL U21		N/A TERMINAL V19		N/A TERMINAL W19		N/A TERMINAL Y19		N/A TERMINAL U20		N/A TERMINAL V20		N/A TERMINAL Y21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL W18		N/A TERMINAL Y18		N/A TERMINAL W20		N/A TERMINAL Y20		N/A TERMINAL Y22		$\overline{\text{P1\_FDUPLEX}}$ TERMINAL AA22		$\overline{\text{P1\_ACTIVITY}}$ TERMINAL AB22		$\overline{\text{P1\_LINK}}$ TERMINAL AA21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–49. SYS_RESET (PIN_SEL_12) Register

0x0861:1638	SYS_RESET				PIN_SEL_12				I/O Multiplex Pin Select 12							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL N14		N/A TERMINAL P20		N/A TERMINAL R20		N/A TERMINAL T20		N/A TERMINAL U19		N/A TERMINAL P19		N/A TERMINAL R19		N/A TERMINAL T19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL U22		N/A TERMINAL R21		N/A TERMINAL R22		N/A TERMINAL T22		N/A TERMINAL T21		N/A TERMINAL V21		N/A TERMINAL V22		N/A TERMINAL W22	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–50. SYS_RESET (PIN_SEL_13) Register

0x0861:163C	SYS_RESET				PIN_SEL_13				I/O Multiplex Pin Select 13							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TELE_RINGIN4 TERMINAL L22		TELE_RINGIN3 TERMINAL L21		TELE_RINGIN2 TERMINAL M22		TELE_RINGIN1 TERMINAL M21		N/A TERMINAL P14		N/A TERMINAL N19		TELE_CLK_I TERMINAL L19		TELE_DO TERMINAL M20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TELE_DI TERMINAL N20		TELE_DCLK TERMINAL M19		N/A TERMINAL M14		N/A TERMINAL N22		N/A TERMINAL N21		N/A TERMINAL P22		N/A TERMINAL L13		N/A TERMINAL P21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–51. SYS_RESET (PIN_SEL_14) Register

0x0861:1640	SYS_RESET				PIN_SEL_14				I/O Multiplex Pin Select 14							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL G21		N/A TERMINAL G22		N/A TERMINAL H20		N/A TERMINAL J19		N/A TERMINAL H21		N/A TERMINAL H22		N/A TERMINAL J20		N/A TERMINAL J21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TELE_CLK_O TERMINAL J22		$\overline{\text{TELE\_RESET}}$ TERMINAL K22		N/A TERMINAL J14		TELE_INT TERMINAL K21		$\overline{\text{TELE\_CS}}$ TERMINAL K20		N/A TERMINAL L14		TELE_FS TERMINAL L20		N/A TERMINAL K19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–52. SYS_RESET (PIN_SEL_15) Register

0x0861:1644	SYS_RESET				PIN_SEL_15				I/O Multiplex Pin Select 15							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL D20		N/A TERMINAL D21		N/A TERMINAL D22		N/A TERMINAL K14		N/A TERMINAL E19		N/A TERMINAL E20		N/A TERMINAL C20		N/A TERMINAL E21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL E22		N/A TERMINAL H19		N/A TERMINAL F19		N/A TERMINAL F20		N/A TERMINAL F21		N/A TERMINAL F22		N/A TERMINAL G20		N/A TERMINAL D19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–53. SYS_RESET (PIN_SEL_16) Register

0x0861:1648	SYS_RESET				PIN_SEL_16				I/O Multiplex Pin Select 16							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B22		N/A TERMINAL B18		N/A TERMINAL A18		N/A TERMINAL C18		N/A TERMINAL D18		N/A TERMINAL D16		N/A TERMINAL J13		N/A TERMINAL A19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL B19		N/A TERMINAL B21		N/A TERMINAL A20		N/A TERMINAL B20		N/A TERMINAL C19		N/A TERMINAL C21		N/A TERMINAL C22		N/A TERMINAL G19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–54. SYS_RESET (PIN_SEL_17) Register

0x0861:164C	SYS_RESET				PIN_SEL_17				I/O Multiplex Pin Select 17							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL A14		N/A TERMINAL D14		N/A TERMINAL A22		N/A TERMINAL C14		N/A TERMINAL B15		N/A TERMINAL A15		N/A TERMINAL C15		N/A TERMINAL B16	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL A16		N/A TERMINAL A21		N/A TERMINAL C16		N/A TERMINAL D15		N/A TERMINAL B17		N/A TERMINAL A17		N/A TERMINAL C17		N/A TERMINAL D17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–55. SYS_RESET (PIN_SEL_18) Register

0x0861:1650	SYS_RESET				PIN_SEL_18				I/O Multiplex Pin Select 18							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B11		N/A TERMINAL A11		N/A TERMINAL C11		N/A TERMINAL K11		N/A TERMINAL D11		N/A TERMINAL J12		N/A TERMINAL B12		N/A TERMINAL D13	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL A12		N/A TERMINAL C12		N/A TERMINAL K12		N/A TERMINAL D12		N/A TERMINAL B13		N/A TERMINAL A13		N/A TERMINAL C13		N/A TERMINAL B14	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–56. SYS_RESET (PIN_SEL_19) Register

0x0861:1654	SYS_RESET				PIN_SEL_19				I/O Multiplex Pin Select 19							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B7		N/A TERMINAL C7		N/A TERMINAL A8		N/A TERMINAL D9		N/A TERMINAL B8		N/A TERMINAL J9		N/A TERMINAL C8		N/A TERMINAL A9	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL B9		N/A TERMINAL C9		N/A TERMINAL C10		N/A TERMINAL B10		N/A TERMINAL K10		N/A TERMINAL D10		N/A TERMINAL A10		N/A TERMINAL J11	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–57. SYS_RESET (PIN_SEL_20) Register

0x0861:1658	SYS_RESET				PIN_SEL_20				I/O Multiplex Pin Select 20							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B2		N/A TERMINAL C4		N/A TERMINAL B4		N/A TERMINAL B5		N/A TERMINAL C5		N/A TERMINAL A4		N/A TERMINAL A5		N/A TERMINAL C3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL A6		N/A TERMINAL D8		N/A TERMINAL C6		N/A TERMINAL B6		N/A TERMINAL D5		N/A TERMINAL D6		N/A TERMINAL D4		N/A TERMINAL A7	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–58. SYS_RESET (PIN_SEL_21) Register

0x0861:165C	SYS_RESET				PIN_SEL_21				I/O Multiplex Pin Select 21							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Test TERMINAL B3		N/A TERMINAL A3		N/A TERMINAL J10		N/A TERMINAL D7	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–59. SYS_RESET (PIN_SEL_1 to PIN_SEL_21) Register Bits

BIT	NAME	DESCRIPTION
31:8	PIN_SEL_21 only Reserved	Always returns zero when read
	PIN_SEL_21 to PIN_SEL_1, terminal number	I/O multiplex pin select. Of the 324 TNETV1060 terminals, 71 provide multiple I/O terminal functional modes. All of the I/Os featuring multiple functional modes are shown in Table 3–2. This SYS_RESET (PIN_SEL_X) register set provides a 2-bit field for every I/O terminal, even though only 71 are useful. 11 = 3rd (tertiary) = Selects the tertiary multiplex feature 10 = 2nd (secondary) = Selects the secondary multiplex feature 01 = 1st (primary) = Selects the primary multiplex feature 00 = 3-state = POR mode: I/Os with multiple functional modes must be programmed to be useful. I/Os with multiple functional modes are identified in the registers listed in Tables 3–38 to 3–58 with their primary (1st) mode name. N/A = Indicates terminal locations that do not have a multiplexed I/O feature. The 2-bit selection contents can be written to any binary state, but the I/O always remains at the primary 1st selection function. Test-mode multiplex I/O features are selected through activation of the TEST terminal and override any other multiplex selection.

3.6 Pullup/Pulldown Configuration

The TNETV1060 provides the ability to power off any internal I/O terminal pullup or pulldown (see Table 3–2). This power-down feature is provided through the registers shown in Table 3–60.

Table 3–60. SYS_CLK (PULL_POWER) Register Set

ADDRESS	BLOCK	NAME	DESCRIPTION
0x0861:0A08	SYS_CLK	PULL_POWER_1	Pullup/pulldown power down 1
0x0861:0A10	SYS_CLK	PULL_POWER_2	Pullup/pulldown power down 2
0x0861:0A14	SYS_CLK	PULL_POWER_3	Pullup/pulldown power down 3

3.6.1 SYS_CLK (PULL_POWER)

Tables 3–61 through 3–63 are detailed maps coving the memory range 0x0861:0A08 to 0x0861:0A14, with bit descriptions in Table 3–64.

Table 3–61. SYS_CLK (PULL_POWER_1) Register

0x0861:0A08	SYS_CLK				PULL_POWER_1				Pullup/pulldown power down 1							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO6 U1	GPIO5 V2	GPIO4 U2	GPIO3 T2	GPIO2 U3	GPIO1 T3	GPIO0 R3	McBSP FS_TX P3	McBSP FS_RX P2	McBSP D_RX N3	McBSP CLK_TX N2	McBSP CLK_RX M3	VLYNQ 3 CLK L3	VLYNQ 5 CLK K3	JTAG TMS J1	JTAG TDI H1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JTAG TCK J3	JTAG TRST H2	JTAG EMU1 G1	JTAG EMU0 H3	EJTAG TMS G2	EJTAG TDI G3	EJTAG TCK F2	EJTAG TRST1 E1	EJTAG TRST0 F3	EJTAG SYSRST E2	EJTAG DINT E3	SSP3 E4	SSP2 D2	SSP1 D1	SSP0 D3	TEST F4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–62. SYS_CLK (PULL_POWER_2) Register

0x0861:0A10	SYS_CLK				PULL_POWER_2				Pullup/pulldown power down 2							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1 ACTIVITY AB22	P1 LINK AA21	P1 100MB AB21	P0 FDUPLEX AA20	P0 ACTIVITY AB20	P0 LINK AA19	P0 100MB AB19	MULTI 3	MULTI 2	MULTI 1	LCD VSYNCA AA13	LCD HSYNCW W12	LCD E1 AB13	LCD PIXEL STRB Y12	LCD BIAS E0 AA12	KEYPAD 15 AB12
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYPAD 14 Y11	KEYPAD 13 W11	KEYPAD 12 AA11	KEYPAD 11 AB11	KEYPAD 10 Y10	KEYPAD 09 AA10	KEYPAD 08 AB10	KEYPAD 07 Y9	KEYPAD 06 AA9	KEYPAD 05 AB9	KEYPAD 04 Y8	KEYPAD 03 AA8	KEYPAD 02 AB8	KEYPAD 01 AA7	KEYPAD 00 AB7	GPIO7 V1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–63. SYS_CLK (PULL_POWER_3) Register

0x0861:0A14	SYS_CLK				PULL_POWER_3				Pullup/pulldown power down 3							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NOTHING						MULTI 10	MULTI 9	MULTI 8	UART CTS B3	UART RX B4	EM HIZ C6	EM WAIT B6	MULTI 7	MULTI 6	MULTI 5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MULTI 4	TELE CLK_O J22	TELE RESET K22	TELE INT K21	TELE CS K20	TELE FS L20	TELE RINGIN4 L22	TELE RINGIN3 L21	TELE RINGIN2 M22	TELE RINGIN1 M21	TELE CLK_I L19	TELE DO M20	TELE DI N20	TELE DCLK M19	ALT CLK_I P21	P1 FDUPLEX AA22
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–64. SYS_CLK (PULL_POWER_3) Register Bits

BIT	NAME	DESCRIPTION
31:26	PULL_POWER_3, Nothing	May be written to any value, but values do nothing.
	PULL_POWER_3 to PULL_POWER_1, terminal number	Disable pullup/pulldown for the defined terminal 1 = Power off the pullup/pulldown 0 = Power on the pullup/pulldown The primary (1st) mode name is provided for all individual I/O locations. Multiple number locations are defined below.
	PULL_POWER_3 and PULL_POWER_2, multiple number	Disable pullup/pulldown for multiple terminals MULTI_10 = EM_A[23:16]: with terminals = D22, D21, D20, C22, C21, C19, B20, and A20 MULTI_9 = EM_A[15:8]: with terminals = F22, F21, F20, F19, E22, E21, E20, and E19 MULTI_8 = EM_A[7:0]: with terminals = J21, J20, H22, H21, H20, G22, G21, and G20 MULTI_7 = EM_D[31:24]: with terminals = A12, B12, D11, C11, A11, B11, A10, and B10 MULTI_6 = EM_D[23:16]: with terminals = C14, A14, B14, C13, A13, B13, D12, and C12 MULTI_5 = EM_D[15:8]: with terminals = A17, B17, C16, A16, B16, C15, A15, and B15 MULTI_4 = EM_D[7:0]: with terminals = B19, A19, D18, C18, A18, B18, D17, and C17 MULTI_3 = LCD_D[15:08]: with terminals = AA16, Y16, AB17, AA17, Y17, W17, AB18, and AA18 MULTI_2 = LCD_D[07:04]: with terminals = AB15, AA15, Y15, and AB16 MULTI_1 = LCD_D[03:01]: with terminals = Y13, AB14, AA14, and Y14

4 Functional Description

4.1 Block Diagram

The TNETV1060 functional block diagram shows the internal components discussed in this section (see Figure 4–1).

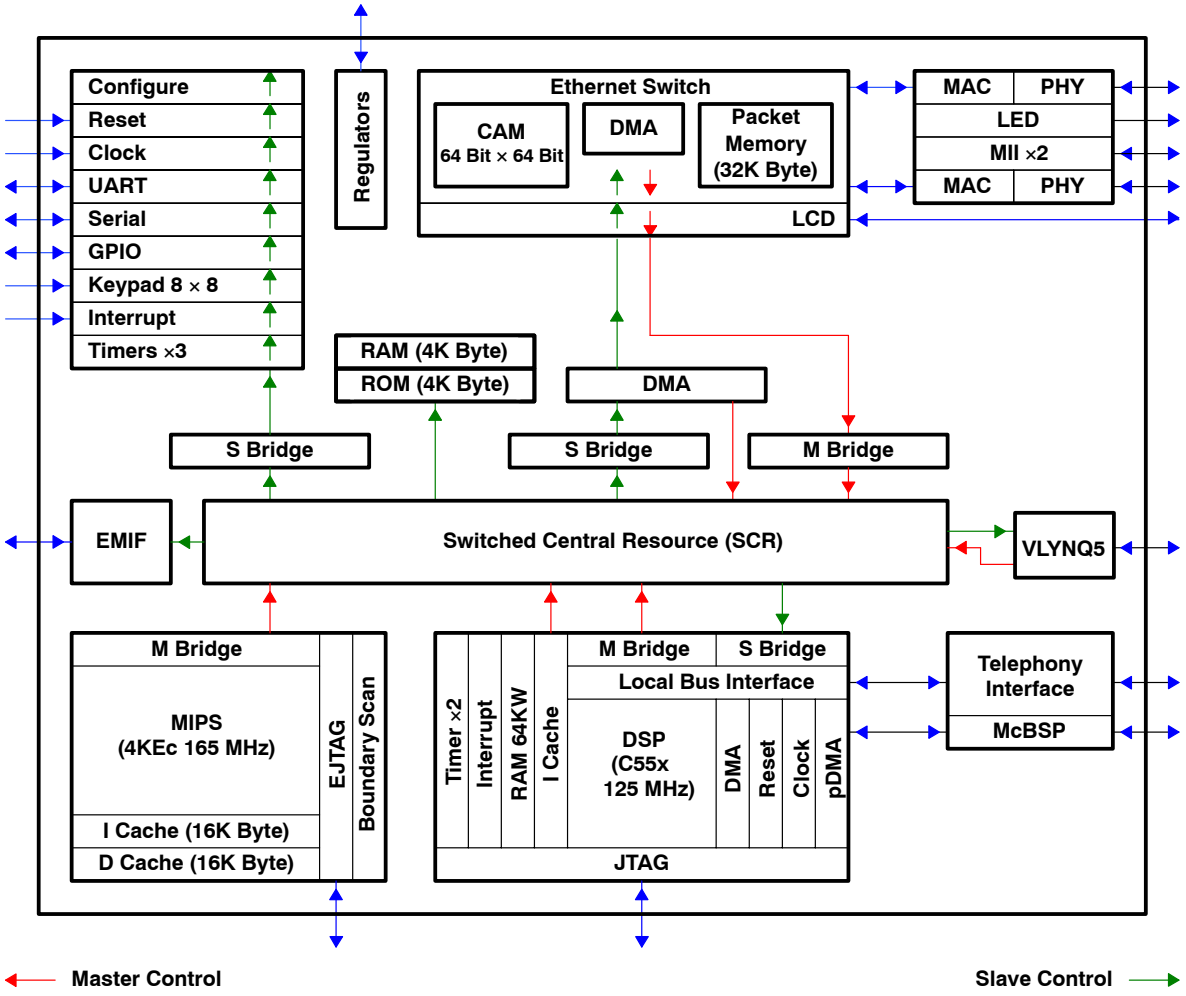


Figure 4–1. TNETV1060 Functional Block Diagram

Standard data flow connections are defined with blue arrows, showing data flow direction. Master control connections are defined with red arrows and slave control connections are defined with green arrows, showing the direction of control through the switched central resource rather than the direction of data flow. The MIPS is always a master and the internal RAM is always a slave. Thus, read and write requests from the MIPS to the RAM generate a master control event at the switch central resource, while the RAM always responds to the switch central resource as a slave despite the direction of data flow.

4.2 Bus Structure

Data flow between TNETV1060 subsystems is conducted through the switch central resource (SCR). Those subsystems defined as master can request data reads or data writes from those subsystems defined as slave. As shown in Table 4–1, not all masters have access to all slaves. Table 4–1 shows a data path map for the SCR, identifying which masters can direct requests from which slaves (identified with a Y). In addition, the definition of bus types and bridges may be useful when utilizing these subsystems.

Table 4–1. Internal Bus Structure

		Speed	VBUSP				VBUS		VBUSP
		Bridge	Y	Y	Y		South		
Speed	Bridge	Masters / Slaves	MIPS	DSP I Cache	DSP	VLYNQ5	Ethernet	LCD	System DMA
VBUSP	Y	DSP	Y			Y			Y
		VLYNQ5	Y				Y		Y
		ROM	Y						
		RAM	Y			Y			Y
		EMIF	Y	Y	Y	Y	Y		Y
VBUS	South	Ethernet	Y			Y			Y
		LCD							
		System Timers							
		UART							
		Serial							
		GPIO							
		Keypad							
VBUSP	West	System DMA	Y		Y	Y	Y		
		System Reset							
		System Clock							
		System Configure							
		System Interrupt							

The system SCR connects masters to slaves through bus segments. Each bus segment contains a 32-bit-wide data path capable of performing an entire data transfer in a single clock cycle. Two bus clock speeds are supported (VBUSP_CLK and VBUS_CLK). With a maximum VBUSP_CLK frequency of 125 MHz, the data bandwidth can reach 500 Mbytes per second (MBps) on a single bus segment. Since the SCR is a nonblocking architecture, simultaneous transactions are possible on different bus segments. A different bus segment is a command from a different master to a different slave. Arbitration is only required when two or more masters desire to access the same slave. Arbitration is a background round-robin task, eliminating any control overhead from reducing data bandwidth. The slaves have the ability to insert wait states before completing a data transfer.

An important component of the SCR is the bridge. Not all masters or slaves require a bridge, but those that do use the bridge to synchronize clocks, control signals, and bus protocol. In addition, certain bridges isolate a whole group of lower-performing peripherals into a single segment. The west slave bridge, south slave bridge, and south master bridge are all examples of grouped peripheral bridges. A slave bridge group constitutes a bus segment end point, thus, only one slave in that group may be accessed in a single clock cycle SCR event. Likewise, a master bridge group constitutes a bus segment starting point and only one master in that group controls the SCR in a single clock cycle event. Arbitration for control of the SCR in the south master bridge is handled through an automated priority controller built into the bridge. This controller grants priority to the LCD first, followed by the Ethernet.

All elements of the system bus structure (masters, slaves, bridges, and SCR) are hardwired without any software setup or control. As long as accesses are restricted to areas of the system memory map (as defined in the *TNETV1050 User's Guide*) used by the TNETV1060, this system bus performs as expected. If accesses are directed to unused areas of the system memory map, a system hang may occur. The hang is created by the SCR as it waits for the nonexistent slave to end wait state insertion. If this hang occurs, the TNETV1060 needs to be reset through the I/O signal $\overline{\text{RESET\_I}}$.

In addition to the system SCR, the DSP and Ethernet subsystems contain a local SCR. These local SCR bus units operate like the system SCR previously described. Most of the bus traffic on these local SCR units remains local, minimizing the DSP and Ethernet bandwidth on the system SCR. Through a master bridge, both of these local SCR bus units may gain master access to the system SCR. Through a slave bridge, system SCR master devices may control both of these local SCR bus units.

4.3 MIPS Subsystem

The MIPS subsystem (see Figure 4–2) consists of:

- MIPS32 4KEc 32-bit RISC processor with clock speeds up to 165 MHz
- 16K-byte four-way set-associative instruction cache (I cache)
- 16K-byte four-way set-associative data cache (D cache)
- Programmable MMU
- Enhanced JTAG (EJTAG) port
- 4K-byte RAM (zero wait state) accessed through the system SCR
- 4K-byte ROM (zero wait state) accessed through the system SCR
- Interrupt handler accessed through the system SCR
- Two universal 16-bit timers each with a 16-bit prescaled clock accessed through the system SCR
- One 16-bit watchdog timer with a 16-bit prescaled clock accessed through the system SCR

Details of the MIPS core, instruction cache, data cache, MMU, and EJTAG port may be found in the MIPS documentation identified in section 7, *Documentation Support*. The MIPS memory map and details of MIPS subsystem components not covered by the MIPS documentation may be found in the *TNETV1050 User's Guide.*

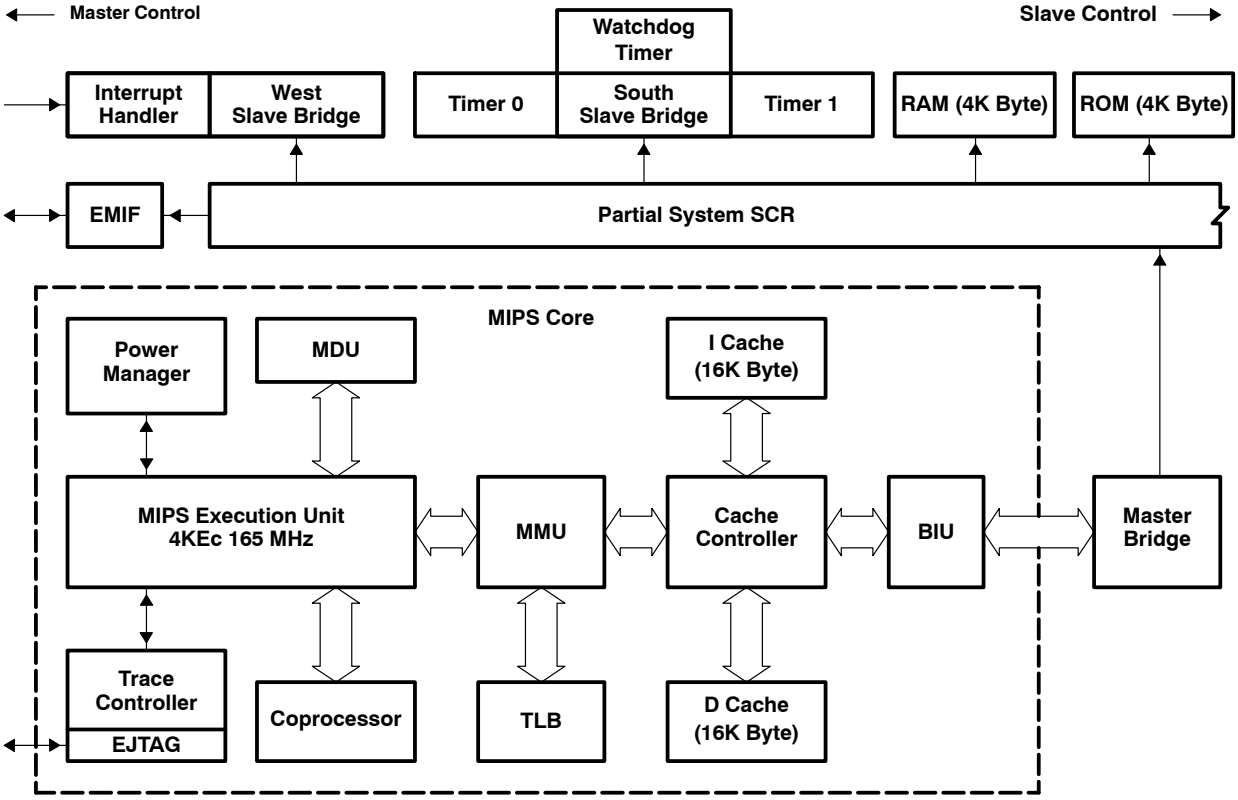


Figure 4–2. MIPS Block Diagram

4.3.1 Memory

The 4K-byte RAM may be used for either data variables or instructions.

The 4K-byte ROM is defined and loaded at the factory, containing just enough code to initialize and boot the TNETV1060 MIPS processor. Once initialized, the ROM directs the MIPS through the rest of the boot process as defined in section 3.4, *Boot Configuration*.

4.3.2 Interrupt Handler

One interrupt is presented to the MIPS from the TNETV1060 system. This interrupt is synthesized from 40 primary programmable-priority sources and 32 secondary fixed-priority sources. The interrupt source map is defined in the *TNETV1050 User's Guide*. Interrupt sources are individually programmable.

4.3.3 Universal Timers

Two universal 16-bit timers with programmable prescaled clocks are available for the MIPS. Each timer may be programmed for single-shot or auto-reload applications. An interrupt may be programmed to alert the MIPS when the timer count has expired.

4.3.4 Watchdog Timer

One 16-bit watchdog timer with a programmable prescaled clock is available for the MIPS. When the timer is programmed to run, the MIPS periodically must kick the watchdog timer. Kicking the watchdog timer prevents the timer count from expiring, thus preventing a system-initiated hardware reset.

4.4 DSP Subsystem

The DSP subsystem (see Figure 4−3) consists of:

- C55x DSP with clock speeds up to 125 MHz
- JTAG port
- 12K-word two-way set associative instruction cache (I cache)
- 32K-word dual access RAM (DARAM) (zero wait state)
- 32K-word single access RAM (SARAM) (zero wait state)
- Interrupt handler
- 16-bit universal timer with prescaled clock
- 16-bit watchdog timer with prescaled clock
- Universal four-channel DMA controller
- Dedicated peripheral DMA controller

Details of the DSP and JTAG may be found in the DSP documentation identified in section 7, *Documentation Support*. The DSP memory map and details of DSP subsystem components not covered by the DSP documentation may be found in the *TNETV1050 User's Guide.*

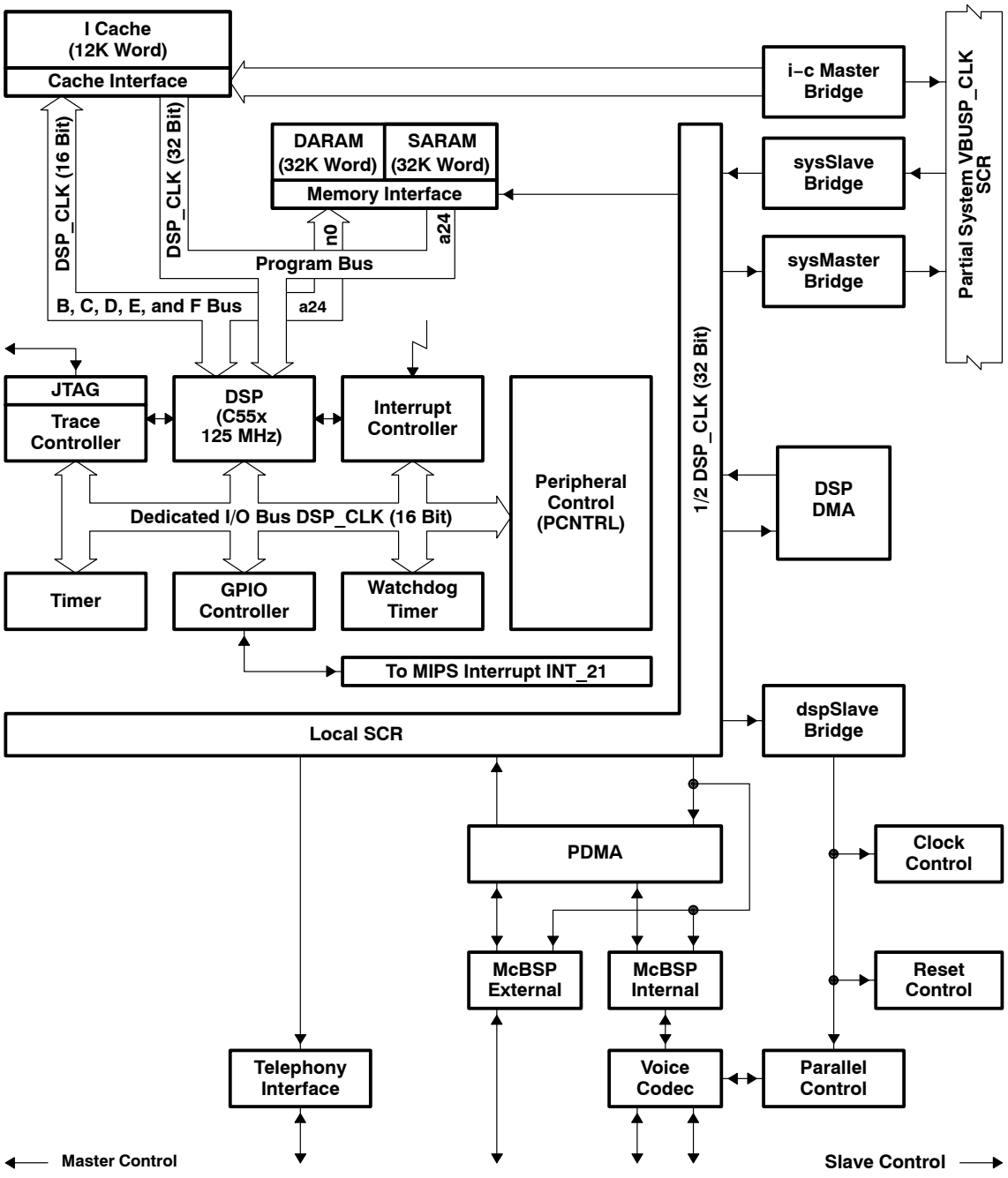


Figure 4–3. DSP Block Diagram

4.5 Ethernet Subsystem

The Ethernet subsystem (see Figure 4–4) consists of:

- Two external Ethernet ports that run through IEEE Std 802.3-compliant MACs and IEEE Std 802.3/802.3u-compliant 10/100 Base-T PHYs
- One internal (virtual) port that attaches to the TNETV1060 system bus through the host DMA and master bridge and is driven by the switch control block
- Embedded switch control block that processes packet traffic between all three ports. The switch control block handles Ethernet activity, providing efficient execution of common switch packet-handling tasks.
- Content addressable memory (CAM) that is directed by the switch control block
- Local and system packet memory
- Switch subsystem that has a dedicated SCR. An asynchronous bridge isolates the Ethernet SCR from the main system bus. This allows heavy switch packet traffic, with no impact on the rest of TNETV1060 system performance.
- MIPS processor that initializes the subsystem and optionally provides switch protocol support through the slave bridge
- EMIF that provides access to external memory (SDRAM) so the switch control block can automatically send port 2 frame data or optionally offload the packet memory.

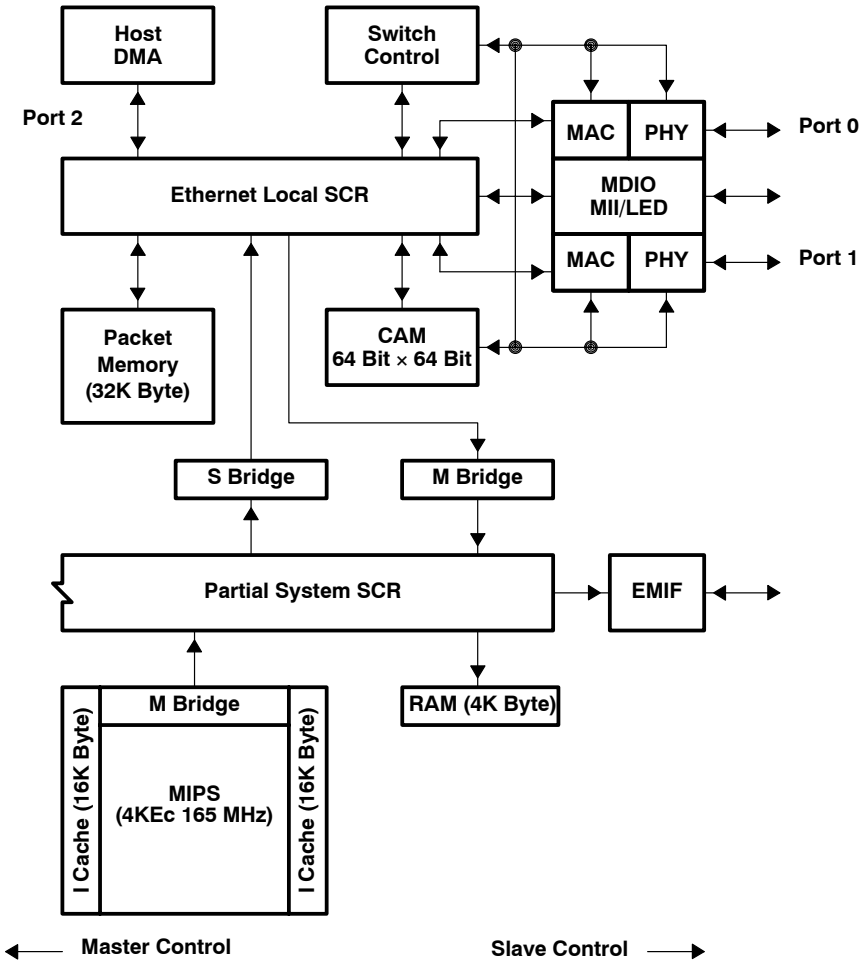


Figure 4–4. Ethernet Subsystem Block Diagram

4.6 Internal Voltage Regulator

TI recommends a 2.0-W supply for the 3.3-V (V_{DDS}) power rail and that the internal voltage regulator be used to produce the 1.5-V (V_{DD}) core voltage. This provides margin for the TNETV1060 to power up.

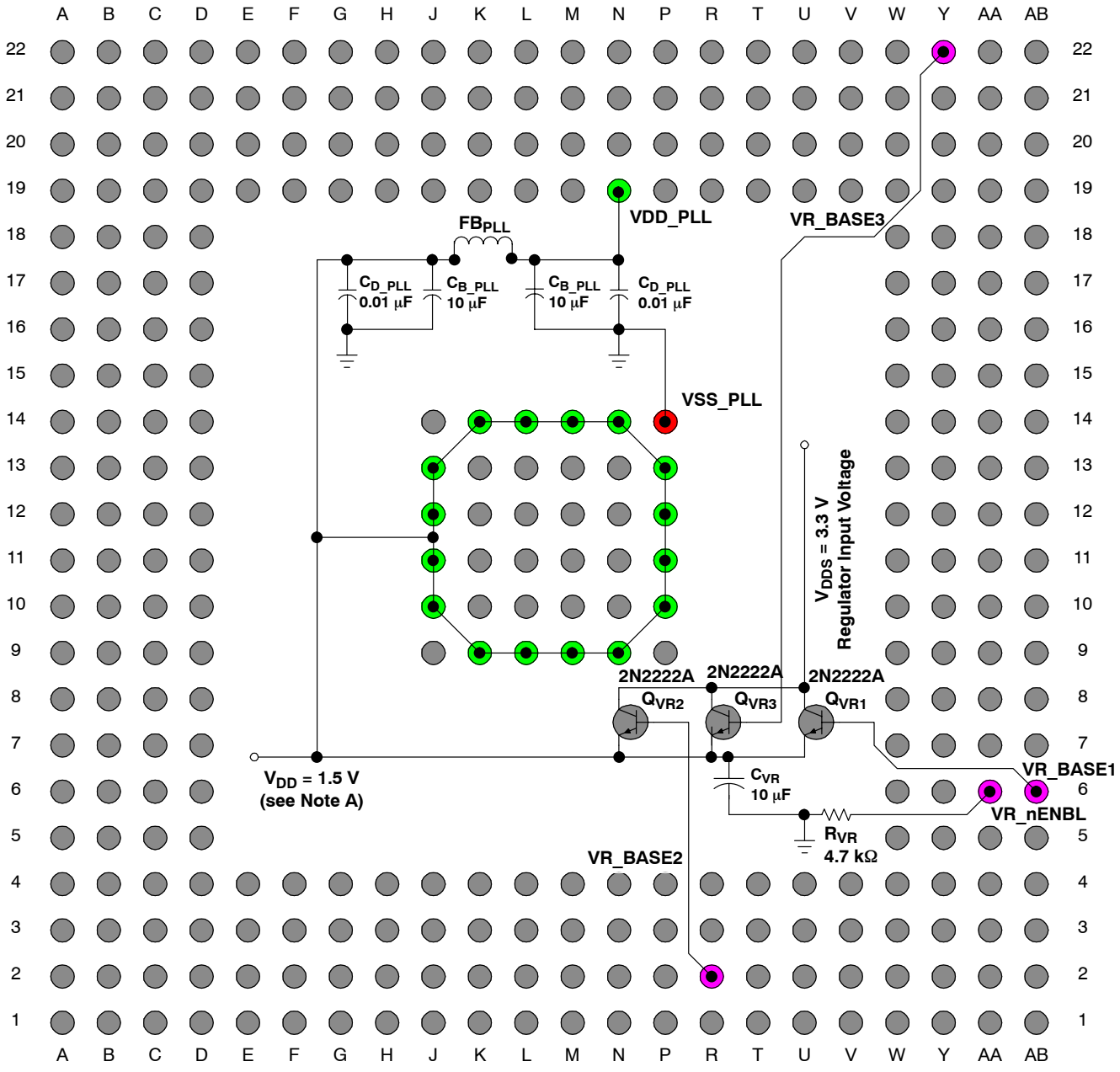
Three internal voltage regulators are required for the power consumption needs of the TNETV1060 V_{DD} (1.5-V) core voltage. The maximum supply current capacity of these three voltage regulators is 1.33 A.

A top-view schematic (see Figure 4-5) shows the necessary external circuitry required to implement the TNETV1060 internal voltage regulator (see Table 4-2). In addition, the following guidelines should be followed when using the regulator:

- The TNETV1060 V_{DD} (1.5-V) power rail may be created with this internal voltage regulator. Power provided from the V_{DDS} (3.3-V) power rail is regulated down to 1.5 V with the help of three external pass transistors. The 1.5-V power produced by this internal voltage regulator provides power to all V_{DD} terminals (16 total), as well as the VDD_PLL terminal.
- To use the internal voltage regulator, it must be enabled by connecting the VR_nENBL terminal to system ground (V_{SS}) through a pulldown resistor (R_{VR}).
- Each VR_BASE terminal is connected to the base of an external npn pass transistor (Q_{VR}). All three transistors are required to produce the maximum V_{DD} supply current of 1.33 A (2 W/1.5 V). In addition, a 10-μF tantalum capacitor (C_{VR}) must be used as shown in Figure 4-5.
- For best results, a separate split V_{DD} power plane should be created to route power to the TNETV1060. The 16 V_{DD} terminals have been placed conveniently in the center of the TNETV1060 to facilitate isolation for this split power plane.
- Decoupling capacitors (C_D) should be placed close to each V_{DD} terminal.

Table 4–2. Voltage Regulator Components

ITEM	DESCRIPTION	VALUE	UNIT
Q_{VR1}	VR_BASE1 npn transistor	2N2222A	
Q_{VR2}	VR_BASE2 npn transistor	2N2222A	
Q_{VR3}	VR_BASE3 npn transistor	2N2222A	
C_{VR}	VR_BASE tantalum capacitor (±10%)	10	μF
R_{VR}	VR_nENBL pulldown resistor enabling the voltage regulator	4.7	kΩ
C_D	VDD 1.5-V decoupling capacitor	0.01	μF
V_{DDS}	Regulator input voltage	3.3	V
V_{DD}	Regulator output voltage	1.5	V



NOTE A: Regulator output voltage:

- Supplied to all 16 V_{DD} power terminals and one PLL terminal.
- Must include a C_D decoupling capacitor close to each terminal.

Figure 4–5. Voltage Regulator Schematic

4.7 TNETV1060 Device Nomenclature

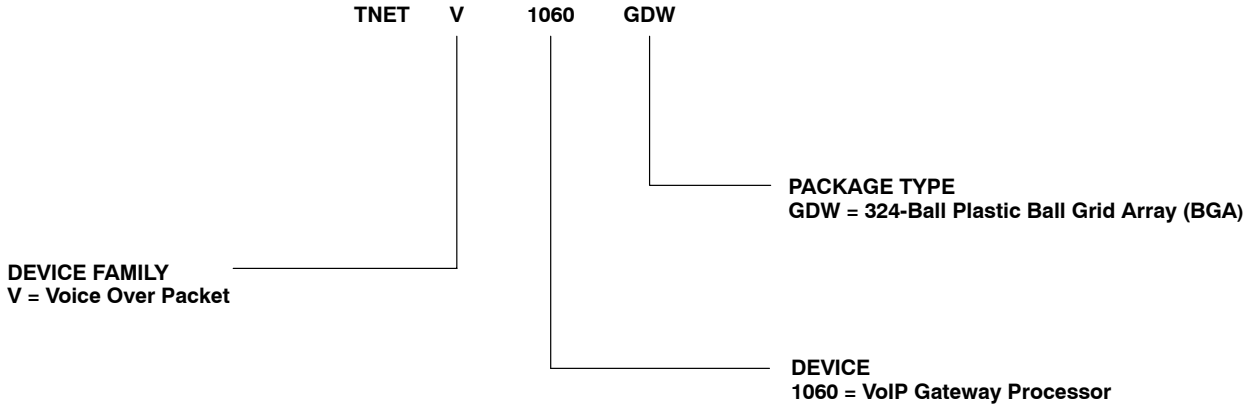


Figure 4–6. TNETV1060 Device Nomenclature

5 Electrical Specification

This section provides the absolute maximum ratings, recommended operating conditions, electrical characteristics, timing requirements, and operating/switching characteristics for the TNETV1060 broadband communications processor.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions, unless otherwise specified.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings (Table 5−1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions (Table 5−2) is not implied. Exposure to absolute maximum ratings (Table 5−1) for extended periods may affect device reliability.

Table 5−1. Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{DD}: Core logic	−0.5 V to 1.836 V
V_{DDS}: I/O	−0.5 V to 4 V
V_{DDA}: Analog, Ethernet PHY	−0.5 V to 3.6 V
Input voltage range, V_I: Except oscillator, analog PHY, and voltage regulator	−0.5 V to 4.5 V
Oscillator (AIC_CLK_I and REF_CLK_I)	−0.5 V to 2.336 V
Analog PHY (PHY_REF)	−0.3 V to 3.6 V
Voltage regulator ($\overline{\text{VR\_ENBL}}$)	−0.5 V to 4 V
Output voltage range, V_O: Except oscillator, analog PHY, and voltage regulator	−0.3 V to V_{DDS}
Analog PHY differential (|P0_TX_P − P0_TX_M| − |P1_TX_P − P1_TX_M|)	2.8 V
Voltage regulator (VR_BASE1, VR_BASE2, and VR_BASE3)	−0.3 V to 1.52 V
Maximum junction temperature, T_J	105°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

Table 5–2. Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	Core logic	1.425	1.5	1.575	V
V_{DDS}		I/O	3.135	3.3	3.465	
V_{DDA}		Analog, including Ethernet PHY	3.29	3.3	3.31	
V_{SS}	Supply ground		0			V
V_{IH}	High-level input voltage	Except oscillator, analog PHY, and voltage regulator	$0.7 \times V_{DDS}$		V_{DDS}	V
		Oscillator: AIC_CLK_I and REF_CLK_I	$0.7 \times V_{DD}$		1.575	
		Analog PHY, 10M bit: P0_RX_M, P0_RX_P, P1_RX_M, and P1_RX_P			2.5	
		Analog PHY, 100M bit: P0_RX_M, P0_RX_P, P1_RX_M, and P1_RX_P			1.3	
		Voltage regulator: VR_ENBL	2.5		3.6	
V_{IL}	Low-level input voltage	Except oscillator, analog PHY, and voltage regulator	0		$0.3 \times V_{DDS}$	V
		Oscillator: AIC_CLK_I and REF_CLK_I	0		$0.3 \times V_{DD}$	
		Analog PHY, 10M bit: P0_RX_M, P0_RX_P, P1_RX_M, and P1_RX_P	–2.5			
		Analog PHY, 100M bit: P0_RX_M, P0_RX_P, P1_RX_M, and P1_RX_P	–1.3			
		Voltage regulator: VR_ENBL	0		0.9	
I_{OH}	High-level output current	All output terminals defined as 4 in the Drive I (mA) column of Table 3–2			–4	mA
		All output terminals defined as 8 in the Drive I (mA) column of Table 3–2			–8	
I_{OL}	Low-level output current	All output terminals defined as 4 in the Drive I (mA) column of Table 3–2			4	mA
		All output terminals defined as 8 in the Drive I (mA) column of Table 3–2			8	
t_r	Rise time	10% to 90%, for all digital signal inputs	0		25	ns
t_f	Fall time	10% to 90%, for all digital signal inputs	0		25	ns
T_C	Temperature	Operating case temperature	–40		85	°C

5.3 Electrical Characteristics

Electrical characteristics are over recommended ranges of supply voltage and operating case temperatures as defined in Table 5–3, unless otherwise noted.

Table 5–3. Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Except oscillator, analog PHY, and voltage regulator	I_{OH} = MAX, V_{DDS} = 3.3 V	$0.8 \times V_{DDS}$		V_{DDS}	V
		Oscillator: AIC_CLK_O and REF_CLK_O	I_{OH} = MAX, V_{DD} = 1.3 V	$0.8 \times V_{DD}$		1.65	
V_{OL}	Low-level output voltage	Except oscillator and analog PHY	I_{OL} = MAX, V_{DD} = 3.3 V	0		$0.22 \times V_{DDS}$	V
		Oscillator: AIC_CLK_O and REF_CLK_O	I_{OL} = MAX, V_{DDS} = 1.3 V	0		$0.22 \times V_{DD}$	
V_{DO}	Differential output voltage	Analog PHY, 10M bit: |P0_TX_P – P0_TX_M|, |P1_TX_P – P1_TX_M|		0		2.8	V
		Analog PHY, 100M bit: |P0_TX_P – P0_TX_M|, |P1_TX_P – P1_TX_M|		0		1.05	
I_I	Input current		V_{DD} = MAX, V_I = V_{SS} to V_{DDS}			±10	μA
I_{OZ}	Off-state output current		V_O = V_{SS} to V_{DDS}			±10	μA
I_{OZ}	Off-state output current		No pullup/pulldown, driver disabled			±20	μA
			Pullup/pulldown active, driver disabled			±100	
C_i	Input capacitance					10	pF
C_o	Output capacitance					10	pF
P_{TOTAL}	Total power consumption	Total power consumption: with VOP call up running echo cancellation, driving an 8-Ω speaker, MIPS = 162.5 MHz, DSP = 125 MHz, using internal voltage regulator	V_{DD} = MAX, V_{DDS} = MAX, V_{DDA} = MAX		1.4		W
I_{DDC}	Current core	Core supply only: MIPS = 162.5 MHz running Dhyrstone code benchmark application from SDRAM, DSP = 125 MHz running 75% dual MAC and 25% ADD code with moderate data bus activity (table of sine values) from the SDRAM. Excludes I/O and analog supplies.	V_{DD} = MAX, V_{DDS} = MAX, V_{DDA} = MAX		360		mA
I_{DDS}	Current I/O	I/O supply only: supply for I/O ring	V_{DD} = MAX, V_{DDS} = MAX, V_{DDA} = MAX		50		mA
I_{DDA}	Current analog Ethernet PHY	Ethernet subsystem only: running 100M-bit bidirectional full-duplex switch traffic with 64-byte frames at 75% utilization	V_{DD} = MAX, V_{DDS} = MAX, V_{DDA} = MAX		85		mA

† Specified by design

5.4 Package Thermal-Resistance Characteristics

Table 5–4 provides the thermal-resistance characteristics for the recommended package types used on the TNETV1060.

Table 5–4. Thermal Characteristics

PARAMETER		AIR FLOW (meters/s)	GDW PACKAGE	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-free air	0.0	22.5	°C/W
		0.5	21.1	
		1.0	20.3	
		2.0	19.5	
$R_{\theta JC}$	Thermal resistance, junction-to-case	NA	9.4	°C/W
$R_{\theta JB}$	Thermal resistance, junction-to-board	NA	14.0	°C/W
Ψ_{JT}	Thermal parameter, junction-to-package top	0.0	0.49	°C/W
		0.5	0.60	
		1.0	0.70	
		2.0	0.83	

5.5 Timing Parameter Symbol Definition

Timing parameter symbols used in the timing requirements and switching-characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, several of the terminal names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)

Letters and symbols and their meanings:

H	High
L	Low
I	Invalid
V	Valid
Z	High impedance
X	Unknown, changing, or don't care level

5.6 Clock Timing

This section provides the timing requirements and switching characteristics for the TNETV1060 clock network. For a complete view of the TNETV1060 clock structure, see Figure 3–2.

The TNETV1060 clock inputs include:

- REF_CLK (reference clock)—created with an internal oscillator that is driven by the two I/O signals REF_CLK_I and REF_CLK_O
- ALT_CLK (alternate clock)—created with the external clock that is supplied by the I/O signal ALT_CLK_I
- AIC_CLK (AIC clock)—created with an internal oscillator that is driven by the two I/O signals AIC_CLK_I and AIC_CLK_O
- MIPS_PLL—output of the MIPS PLL subsystem, which may be fed back as an input to the other PLL units

The TNETV1060 produces the following internal clock sources from the previously defined clock inputs:

- MIPS_CLK (MIPS clock)—clock source for the MIPS subsystem
- MIPS_PLL (MIPS PLL subsystem output)—may be used to create the clock for any of the following internal clock sources
- DSP_CLK (DSP clock)—clock source for the DSP subsystem, also generates 1/2 DSP_CLK
- VBUSP_CLK (virtual bus pipeline clock)—clock source for all VBUSP subsystem peripherals and the switch central resource (SCR)
- VBUS_CLK (virtual bus clock)—clock source for all VBUS subsystem peripherals and the SCR
- PHY_CLK (Ethernet PHY clock)—clock source for both internal integrated Ethernet PHY subsystems. Upon entering the PHY subsystem, this clock encounters another PLL included in each PHY unit.
- AIC_CLK (voice codec clock)—clock source for the internal integrated voice codec subsystem
- LCD_CLK (liquid crystal display clock)—clock source for the LCD subsystem used for the driver circuitry

5.6.1 Internal Clock Speed Limits

As shown in Figure 3–2, there are many ways to produce the internal clocks. Regardless of the method of creation, the limits shown in Table 5–5 may not be exceeded.

Table 5–5. Internal Clock Speed Limits

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
	MIPS_CLK	MIPS clock†‡	1		165	MHz
	DSP_CLK	DSP clock†	1		125	MHz
	1/2 DSP_CLK	One-half DSP clock†	1		62.5	MHz
	VBUSP_CLK	Virtual bus pipeline clock†	1		125	MHz
	VBUS_CLK	Virtual bus clock†§	1		82.5	MHz
	PHY_CLK	Ethernet PHY clock (may be 25 MHz or 50 MHz)	24.75	25	50	MHz
	AIC_CLK	Voice codec clock	4.096	8.1920	16.384	MHz
	LCD_CLK	Liquid-crystal display clock	1		75	MHz

† Specified by design
‡ Standard PLL configuration supports 162.5-MHz MIPs clock maximum.
§ Standard PLL configuration supports 81.25-MHz VBUS clock maximum.

5.6.2 Reference Clock Input (REF_CLK)

The reference clock is derived from an internal oscillator circuit driven from REF_CLK_I and REF_CLK_O (see Table 5–6). Use the following timing values when selecting an external crystal and see the *TNETV1050 User's Guide* for more information.

Table 5–6. Reference Clock Timing (See Figure 5–1)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
	$f_{clock(REF\_CLK)}$	Clock frequency, REF_CLK†	20	25	35	MHz
1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	28.57	40	50	ns
	$f_{s(REF\_CLK)}$	Frequency stability, REF_CLK†	–50		50	ppm

† Specified by design

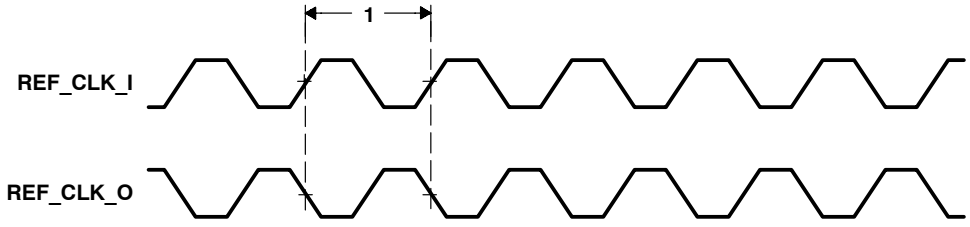


Figure 5–1. Reference Clock Input

5.6.3 Telephony AIC_CLK

The telephony AIC_CLK is derived from an internal oscillator circuit driven from AIC_CLK_I and AIC_CLK_O (see Table 5–7).

Table 5–7. Telephony AIC_CLK Timing (See Figure 5–2)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
		Clock frequency, AIC_CLK†	1	8.1920	20	MHz
1	$t_{c(AIC\_CLK)}$	Cycle time, AIC_CLK†	50	122.07	1000	ns
	$f_{s(AIC\_CLK)}$	Frequency stability, AIC_CLK†	–50		50	ppm

† Specified by design

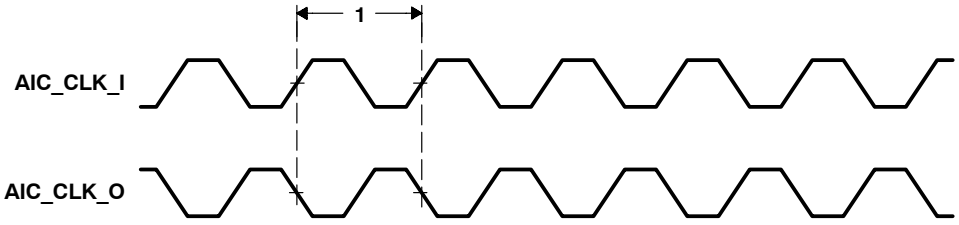


Figure 5–2. Telephony AIC_CLK

5.6.4 Alternate Clock Input

The alternate clock is derived from the ALT_CLK_I external clock source and has input timing shown in Table 5–8.

Table 5–8. Alternate Clock Timing (See Figure 5–3)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
	$f_{clock(ALT\_CLK)}$	Clock frequency, ALT_CLK†	10	25	100	MHz
1	$t_{c(ALT\_CLK)}$	Cycle time, ALT_CLK†	10	A	100	ns
2	$t_{w(ALT\_CLK-H)}$	Pulse duration, ALT_CLK high†	A – 1	A/2	A + 1	ns
3	$t_{w(ALT\_CLK-L)}$	Pulse duration, ALT_CLK low†	A – 1	A/2	A + 1	ns
		Duty cycle, ALT_CLK†	40%	50%	60%	
4	$t_{r(ALT\_CLK)}$	Rise time, ALT_CLK†			1	ns
5	$t_{f(ALT\_CLK)}$	Fall time, ALT_CLK†			1	ns

† Specified by design

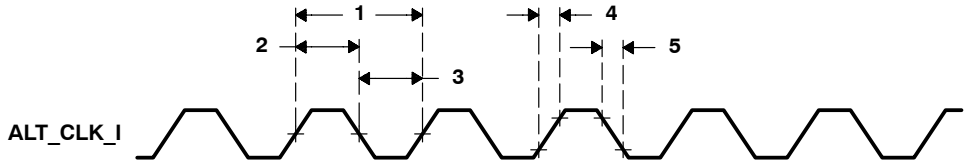


Figure 5–3. Alternate Clock

5.6.5 Analog PLL

Within the TNETV1060 there are four identical analog PLL units, each with the timing values shown in Table 5–9.

Table 5–9. Analog PLL Unit Timing (See Figures 5–4 and 5–5)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
	$f_{clock(PLL\_IN)}$	Clock frequency, analog PLL_IN	10		100	MHz
1	$t_{c(PLL\_IN)}$	Cycle time, analog PLL_IN	10		100	ns
	$f_{clock(PLL\_OUT)}$	Clock frequency, analog PLL_OUT	10		250	MHz
2	$t_{c(PLL\_OUT)}$	Cycle time, analog PLL_OUT	4		100	ns
3	$t_{d(PLL\_REG)}$	Delay time, #_CLK_CTRL valid to PLL_OUT valid†			50	µs

† Specified by design

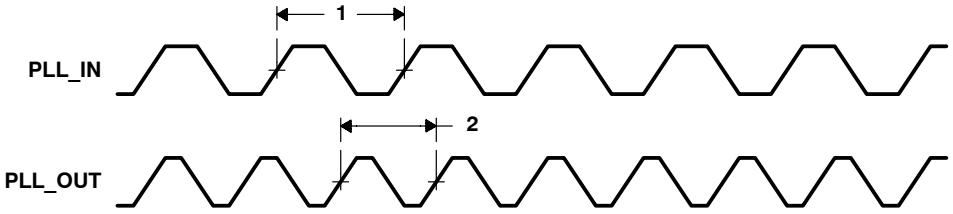


Figure 5–4. Analog PLL

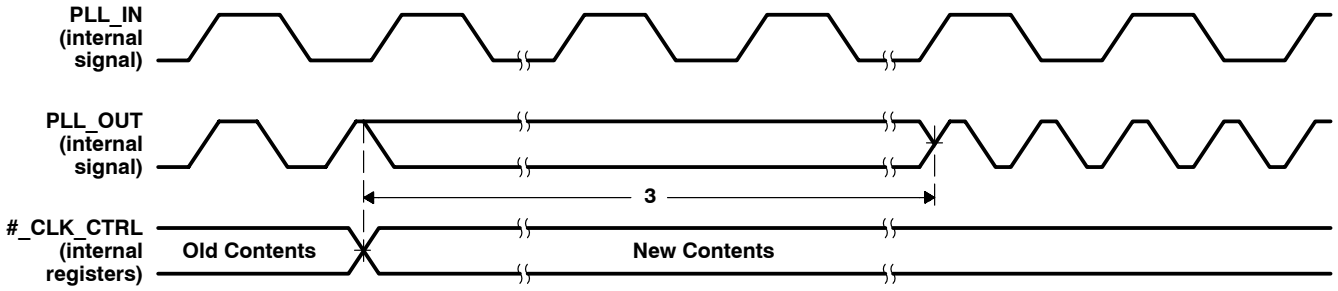


Figure 5–5. Analog PLL-OUT Transitory

5.6.6 PHY PLL

The PHY PLL takes an internal 25-MHz clock and generates the Ethernet PHY reference 20-MHz or 125-MHz clocks, respectively, for the 10 Base-T or 100 Base-T operating modes.

From a hardware or software reset, the internal logic gives the PHY PLL approximately 256 µs to allow for PHY PLL stabilization. IEEE Std 802.3u, Clause 22 (22.2.4.1.1), states that the reset process should be completed within 0.5 s from initiation of the reset signal.

5.7 System Reset Timing

There are two kinds of reset events within the TNETV1060 (see Table 5−10):

- Power-on reset
- Hardware reset: Produced when either one of the following external input signals is forced to a low state:
  - $\overline{\text{RESET\_I}}$
  - $\overline{\text{EJTAG\_SYSRST}}$

Table 5−10. System Reset Timing (See Figures 5−6 and 5−7)

NO.		DESCRIPTION	MIN	TYP	MAX	UNIT
1	$t_{d(XTAL\_LOCK)}$	Delay time, $\overline{\text{RESET\_I}}\downarrow$ to PLL_IN valid† (The external crystal oscillator dictates this parameter.)		10		ms
2	$t_{d(BOOT\_POR)}$¶	Delay time, PLL_IN valid to $\overline{\text{RESET\_I}}$ invalid‡	50			µs
3	$t_{d(BOOT\_HDW)}$¶	Delay time, PLL_IN valid to $\overline{\text{RESET\_I}}$ invalid‡	4 t_C			ns
4	$t_{d(BOOT)}$¶	Delay time, $\overline{\text{RESET\_I}}$ to EM_A[23:0] invalid‡			10	ns
5	$t_{h(BOOT)}$¶	Hold time, $\overline{\text{RESET\_I}}$ to EM_A[23:0] valid‡¶	0			ns
6	$t_{d(MUX\_POR)}$	Delay time, multiplexed I/O# 3-state to $\overline{\text{RESET\_I/EJAG\_SYSRST}}\uparrow$‡‖#	4 t_C			ns
7	$t_{d(MUX\_SET\_HDW)}$¶	Delay time, $\overline{\text{RESET\_I/EJAG\_SYSRST}}\uparrow$ to multiplexed I/O valid‡‖	50			µs
8	$t_{d(RSTOUT\_OFF\_HDW)}$	Delay time, $\overline{\text{RESET\_I/EJAG\_SYSRST}}\uparrow$ to $\overline{\text{RESET\_O/TELE\_RESET}}\uparrow$‡☆	50			µs
9	$t_{w(HDW\_RESET)}$	Pulse width, $\overline{\text{RESET\_I/EJAG\_SYSRST}}$ low‡#	64 t_C			ns
10	$t_{d(PLL\_CHANGE)}$	Delay time, PLL_OUT invalid to PLL_OUT valid§		50		µs

† PLL_IN: Represents the input source clock for all four internal analog PLL units shown in Figure 3−2. These clocks are not visible externally.

‡ Specified by design

§ PLL_OUT: Represents the output of all four internal analog PLL units shown in Figure 3−2. On hardware reset events, each analog PLL unit transitions to an active PLL mode, with the VCO running and the output defined as (f_{PLL_OUT}) = [(1)*(f_{PLL_IN})]. These clocks are not visible externally.

¶ Boot configuration: The EMIF address bus (EM_A[23:0]) changes from an output to an input when a hardware reset is active. The TNETV1060 holds the latched input when the hardware reset goes inactive. As shown in section 3.4, *Boot Configuration*, the values of the boot configuration define the internal analog PLL inputs and outputs.

t_C = clock cycle time of PLL_IN

‖ Multiplexed I/O: On hardware reset events, the multiplexed I/O transition to 3-state mode. After the reset event, these multiplexed I/O require software reprogramming to become useful. For more information related to the multiplexed I/O, see section 3.5, *Multiplex Configuration*.

☆Two reset output signals ($\overline{\text{RESET\_O}}$ and $\overline{\text{TELE\_RESET}}$) exit the TNETV1060. On both hardware and software reset events, both of these output signals are forced to an active low state. After the reset event, these external resets can be individually deactivated through software manipulation of registers in the SYS_RESET and DSP_RESET subsystems.

5.7.1 Power-On Reset

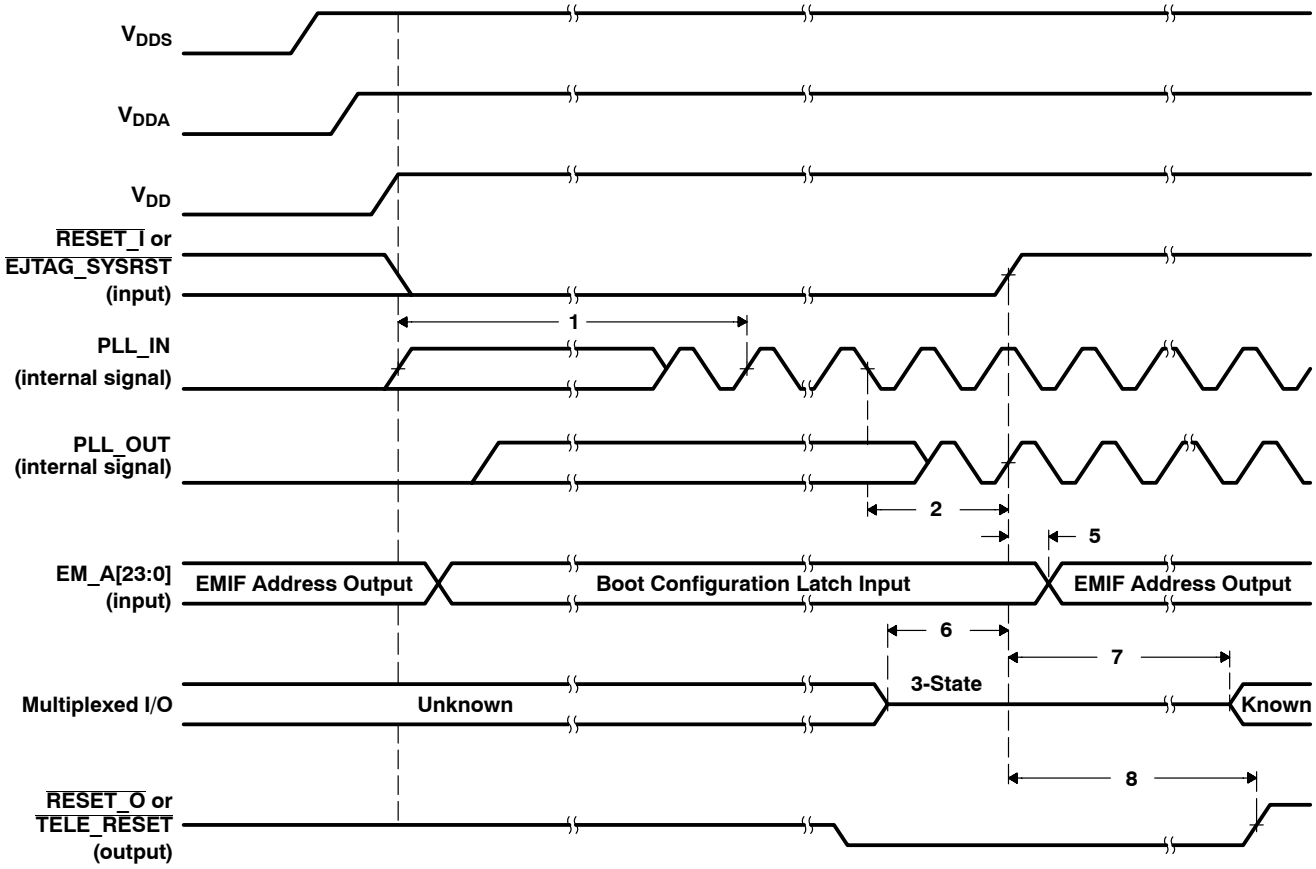


Figure 5–6. Power-On Reset

5.7.2 Hardware Reset

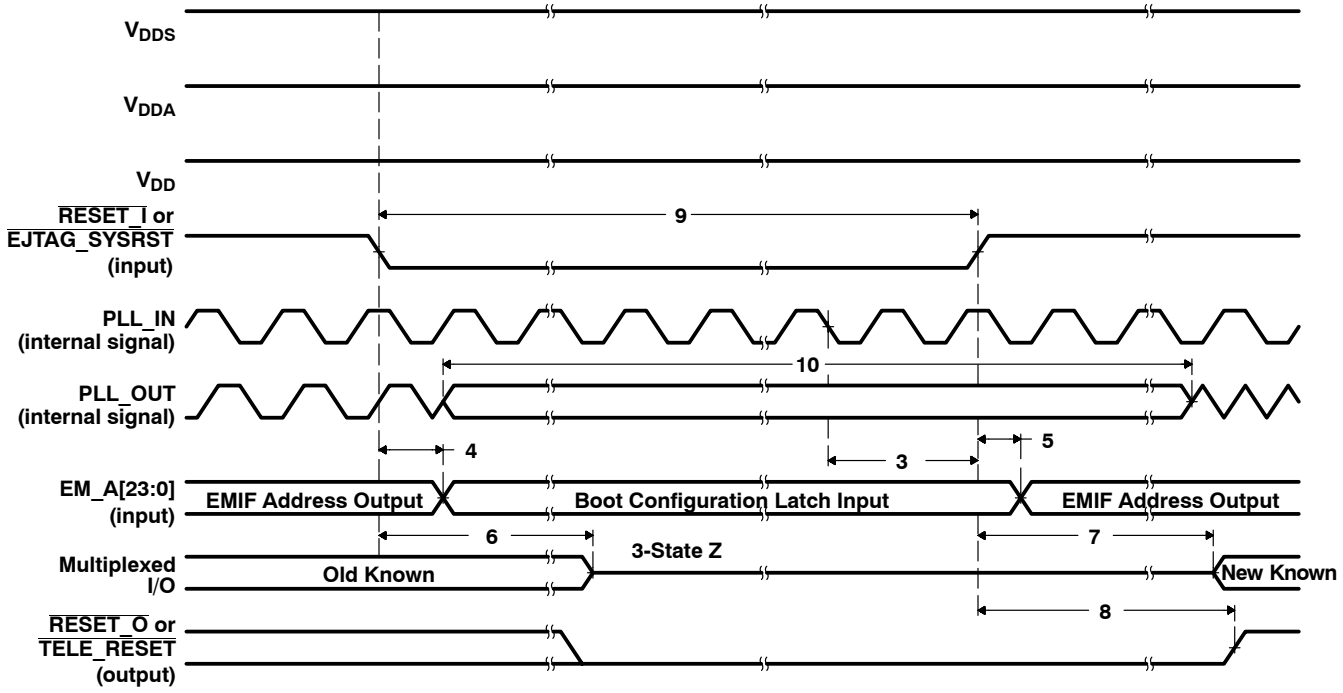


Figure 5–7. Hardware Reset

5.8 EMIF Timing

The EMIF shares several I/O signals, providing access to external SDRAM devices, as well as external asynchronous memory devices (see Table 5–11).

5.8.1 EMIF SDRAM

Table 5–11. EMIF SDRAM Timing (See Figures 5–8 and 5–9)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{c(SDRAM\_CLK)}$	Frequency, EM_CLK		125	MHz
1	$t_{c(SDRAM\_CLK)}$	Cycle time, EM_CLK	8		ns
2	$t_{w(SDRAM\_CLK\_H)}$	Pulse duration, EM_CLK high	4		ns
3	$t_{w(SDRAM\_CLK\_L)}$	Pulse duration, EM_CLK low	3.4		ns
4	$t_{d(CMD\_V)}$	Delay time, EM_CLK high to command valid	1.2	5.5	ns
5	$t_{d(CMD\_I)}$	Delay time, EM_CLK high to command invalid	1.2	5.5	ns
6	$t_{d(ROW\_V)}$	Delay time, EM_CLK high to EM_A[12:0] row valid	1.2	5.5	ns
7	$t_{d(ROW\_I)}$	Delay time, EM_CLK high to EM_A[12:0] row invalid	1.2	5.5	ns
8	$t_{d(BANK\_V)}$	Delay time, EM_CLK high to EM_A[23:22] bank valid	1.2	5.5	ns
9	$t_{d(BANK\_I)}$	Delay time, EM_CLK high to EM_A[23:22] bank invalid	1.2	5.5	ns
10	$t_{d(DQM\_V)}$	Delay time, EM_CLK high to EM_WE_DQM[3:0] valid	1.2	5.5	ns
11	$t_{d(DQM\_I)}$	Delay time, EM_CLK high to EM_WE_DQM[3:0] invalid	1.2	5.5	ns
12	$t_{d(COLUMN\_V)}$	Delay time, EM_CLK high to EM_A[12:0] column valid	1.2	5.5	ns
13	$t_{d(COLUMN\_I)}$	Delay time, EM_CLK high to EM_A[12:0] column invalid	1.2	5.5	ns
14	$t_{d(WR\_DATA\_V)}$	Delay time, EM_CLK high to EM_D[31:0] valid	1	5.5	ns
15	$t_{d(WR\_DATA\_I)}$	Delay time, EM_CLK high to EM_D[31:0] invalid	1.2	5.5	ns
16	$t_{d(RD\_DATA)}$	Delay time, EM_D[31:0] valid to EM_CLK high	2		ns
17	$t_{d(RD\_DATA)}$	Delay time, EM_CLK high to EM_D[31:0] invalid	1.2		ns
18	$t_{d(BUS\_Z)}$	Delay time, EM_CLK high to EM_D[31:0] Z (3-state valid)		6.5	ns
19	$t_{d(Z\_BUS)}$	Delay time, EM_CLK high to EM_D[31:0] Z (3-state invalid)		6.5	ns

The SDRAM command is made up from several EMIF I/O signals as defined in Table 5–12.

Table 5–12. EMIF SDRAM Commands

COMMAND	EM_CS2	EM_CS1	EM_RAS	EM_CAS	EM_WE	EM_WE_DQM3	EM_WE_DQM2	EM_WE_DQM1	EM_WE_DQM0	EM_A[12:0]	EM_A[23:22]	EM_CKE
COMMAND INHIBIT The SDRAM is deselected.	H	H	X	X	X	X	X	X	X	X	X	H
NOP No operation, although read and write bursts may be in progress.	H	L	H	H	H	X	X	X	X	X	X	H
	L	H										
ACTIVE Activate a row in a particular bank.	H	L	L	H	H	X	X	X	X	row	bank	H
	L	H										
READ Initiate a burst read access from an active row. The first data is returned after the CAS latency is exhausted. Data continues on subsequent clock cycles until the burst is exhausted or a BURST TERMINATE extinguishes the process.	H	L	H	L	H	L = EM_D[31:24]	L = EM_D[23:16]	L = EM_D[15:8]	L = EM_D[7:0]	column	bank	H
	L	H										
WRITE Initiate a burst write access to an active row. The first data is presented on the WRITE command. Data continues on subsequent clock cycles until the burst is exhausted or a BURST TERMINATE extinguishes the process.	H	L	L	H	H	L = EM_D[31:24]	L = EM_D[23:16]	L = EM_D[15:8]	L = EM_D[7:0]	column	bank	H
	L	H										

Table 5–12. MIF SDRAM Commands (Continued)

COMMAND	EM_CS2	EM_CS1	EM_RAS	EM_CAS	EM_WE	EM_WE_DQM3	EM_WE_DQM2	EM_WE_DQM1	EM_WE_DQM0	EM_A[12:0]	EM_A[23:22]	EM_CKE
BURST TERMINATE Used to terminate the most recently registered fixed-length or full-page (read or write) burst.	H	L	H	H	L	X	X	X	X	X	X	H
	L	H										
PRECHARGE Deactivate the open row in a particular bank or the open row in all banks. Use the code to select the bank or all banks.	H	L	L	H	L	X	X	X	X	code	code	H
	L	H										
AUTO REFRESH Force a refresh to a row. Defined by register EMIF (SDRAM_REFRESH_CTRL)	L	L	L	L	H	X	X	X	X	X	X	H
SELF REFRESH Force the SDRAM into the internally generated refresh mode.	L	L	L	L	H	X	X	X	X	X	X	L
LOAD MODE REGISTER SDRAM operating mode written after initialization. Defined by register EMIF (SDRAM_CONFIG_CS_1_2).	L	L	L	L	L	X	X	X	X	op-code	X	H

The LOAD MODE REGISTER portion of the SDRAM initialization procedure determines the CAS latency timing and the burst length. These parameters are programmable and provided in the EMIF (SDRAM_CONFIG_CS_1_2) register.

The following SDRAM command timing parameters are programmable through the EMIF (SDRAM_TIME_CTRL) register:

- TIME_RP
- TIME_RCD
- TIME_WR
- TIME_RAS
- TIME_RC
- TIME_RRD
- TIME_RFC

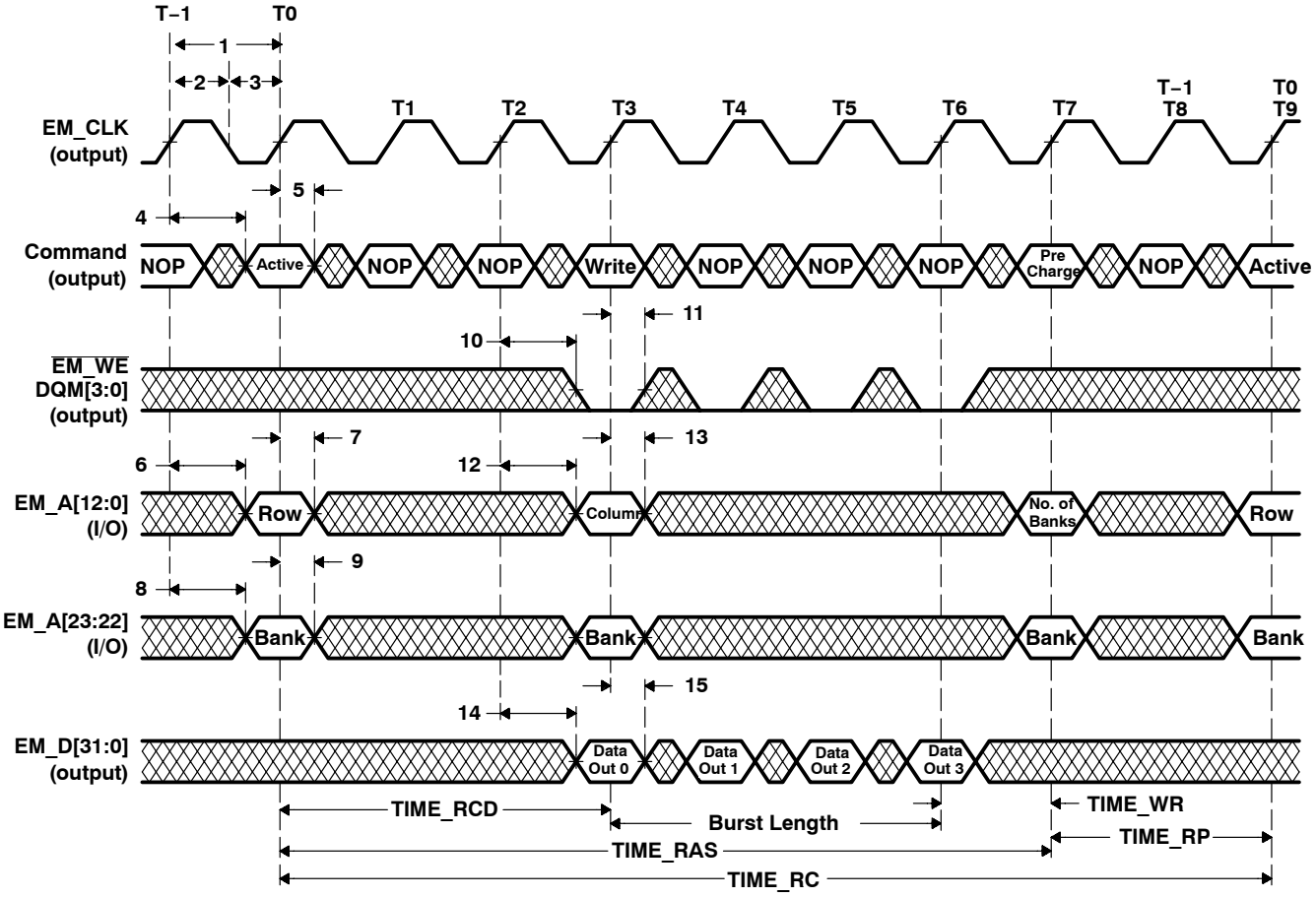


Figure 5–8. EMIF SDRAM Write

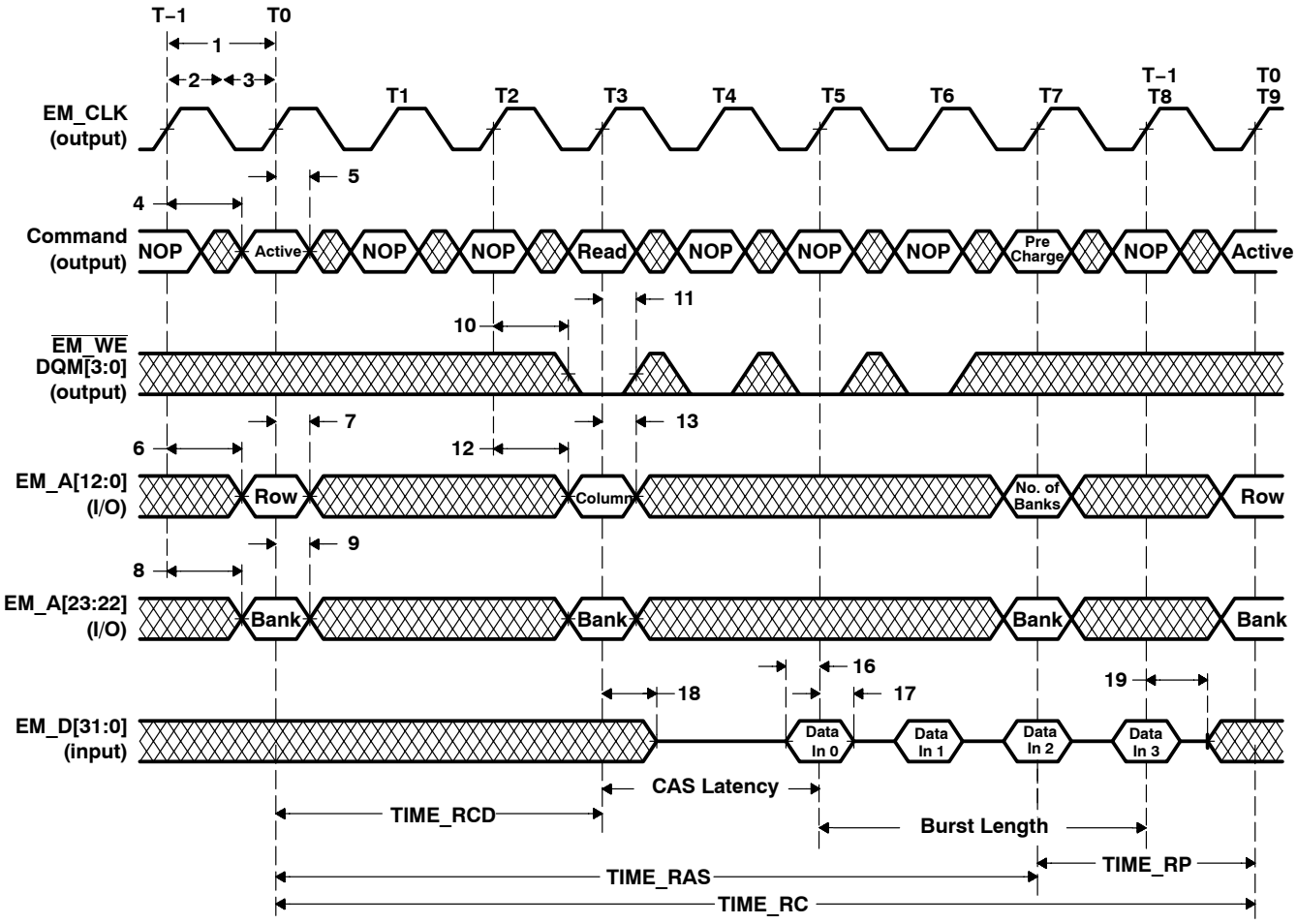


Figure 5–9. EMIF SDRAM Read

5.8.2 EMIF Asynchronous

Table 5–13. EMIF Asynchronous Timing (See Figures 5–10 Through 5–15)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{c(ASYNC\_CLK)}$	Frequency, EM_CLK		125	MHz
1	$t_{c(ASYNC\_CLK)}$	Cycle time, EM_CLK	8		ns
2	$t_{w(ASYNC\_CLK\_H)}$	Pulse duration, EM_CLK high	3.6		ns
3	$t_{w(ASYNC\_CLK\_L)}$	Pulse duration, EM_CLK low	3.6		ns
4	$t_{d(ADDR\_V)}$	Delay time, EM_CLK↑ to EM_A[23:0] valid	1.2	5.5	ns
5	$t_{d(ADDR\_I)}$	Delay time, EM_CLK↑ to EM_A[23:0] invalid	1.2	5.5	ns
6	$t_{d(DATA\_V)}$	Delay time, EM_CLK↑ to EM_D[31:0] valid	1.2	5.5	ns
7	$t_{d(DATA\_I)}$	Delay time, EM_CLK↑ to EM_D[31:0] invalid	1.2	5.5	ns
8	$t_{d(CS\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_CS(0,3,4,5)}$↓	1.2	5.5	ns
9	$t_{d(CS\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_CS(0,3,4,5)}$↑	1.2	5.5	ns
10	$t_{d(RW\_A)}$	Delay time, EM_CLK↑ to EM_R/$\overline{W}$↓	1.2	5.5	ns
11	$t_{d(RW\_I)}$	Delay time, EM_CLK↑ to EM_R/$\overline{W}$↑	1.2	5.5	ns
12	$t_{d(WE\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE}$↓	1.2	5.5	ns
13	$t_{d(WE\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE}$↑	1.2	5.5	ns
14	$t_{d(BYTE\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE\_DQM[3:0]}$↓	1.2	5.5	ns
15	$t_{d(BYTE\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE\_DQM[3:0]}$↑	1.2	5.5	ns
16	$t_{d(OE\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_OE}$↓	1	5.5	ns
17	$t_{d(OE\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_OE}$↑	1	5.5	ns
18	$t_{d(WAIT\_A)1}$	Setup, time, EM_WAIT to EM_CLK↑	4.5		ns
19	$t_{d(WAIT\_A)2}$	Hold time, EM_WAIT after EM_CLK↑	2.3		ns
20	$t_{d(DATA)1}$	Setup, time, EM_D[31:0] to EM_CLK↑	4.5		ns
21	$t_{d(DATA)2}$	Hold time, EM_D[31:0] after EM_CLK↑	2.3		ns

Each asynchronous chip select is provided with a control register, which allows individual adjustment of the write timing parameters (W_SU, W_STROBE, and W_HOLD), read timing parameters (R_SU, R_STROBE, and R_HOLD), and chip select delay timing (CS_DELAY). In addition, external wait states may be individually enabled for each asynchronous chip select with the polarity of the EM_WAIT input signal controlled through the register EMIF (ASYNC_WAIT_CONFIG). Byte enable control may also be enabled on asynchronous read events through this register set, allowing attachment to external static RAM devices requiring this feature. Note the timing differences introduced when evoking this byte-enable feature.

- $\overline{EM\_CS0}$, register EMIF (ASYNC_CONFIG_BANK_1)
- $\overline{EM\_CS3}$, register EMIF (ASYNC_CONFIG_BANK_2)
- $\overline{EM\_CS4}$, register EMIF (ASYNC_CONFIG_BANK_3)
- $\overline{EM\_CS5}$, register EMIF (ASYNC_CONFIG_BANK_4)

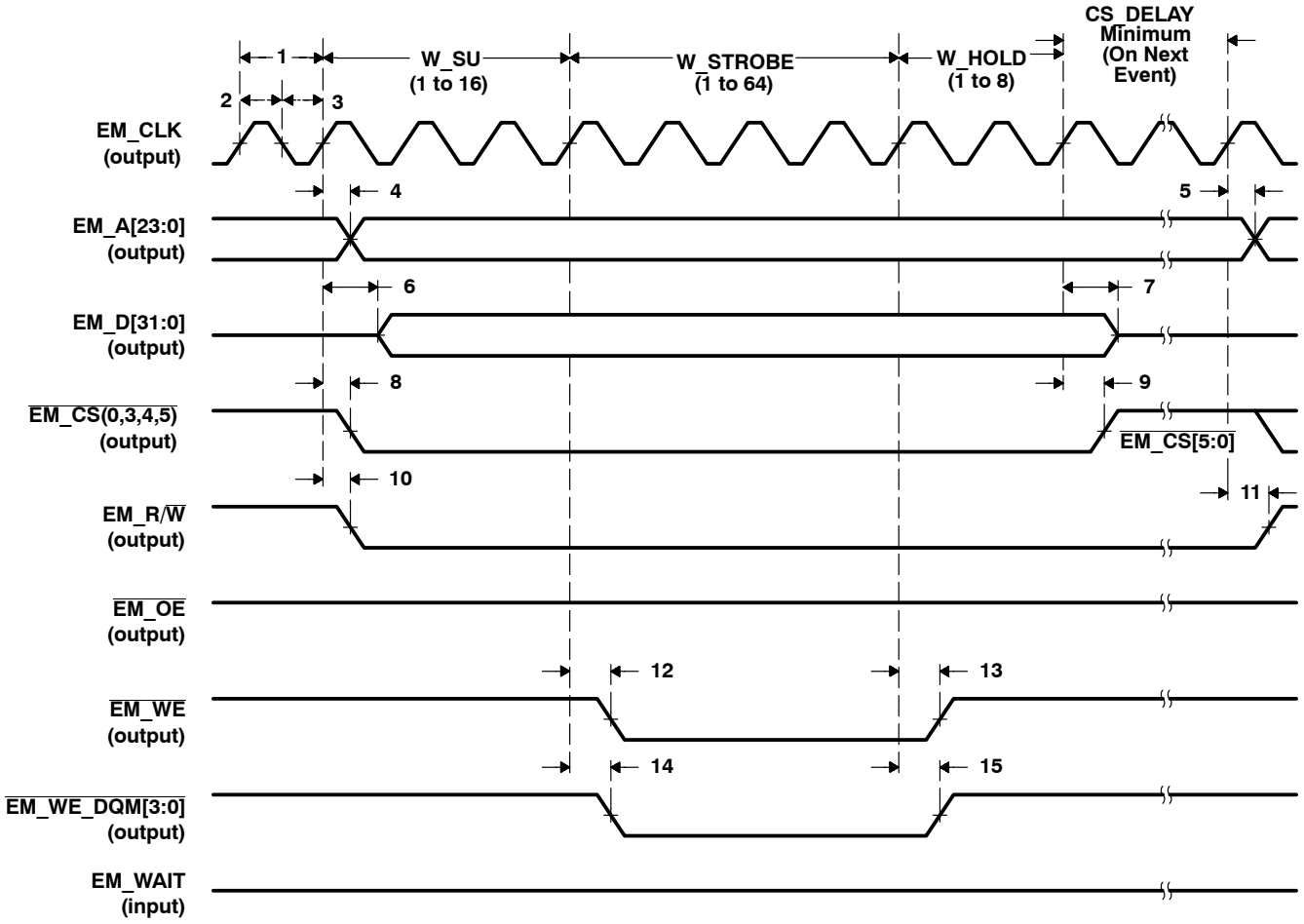


Figure 5–10. EMIF Asynchronous Write

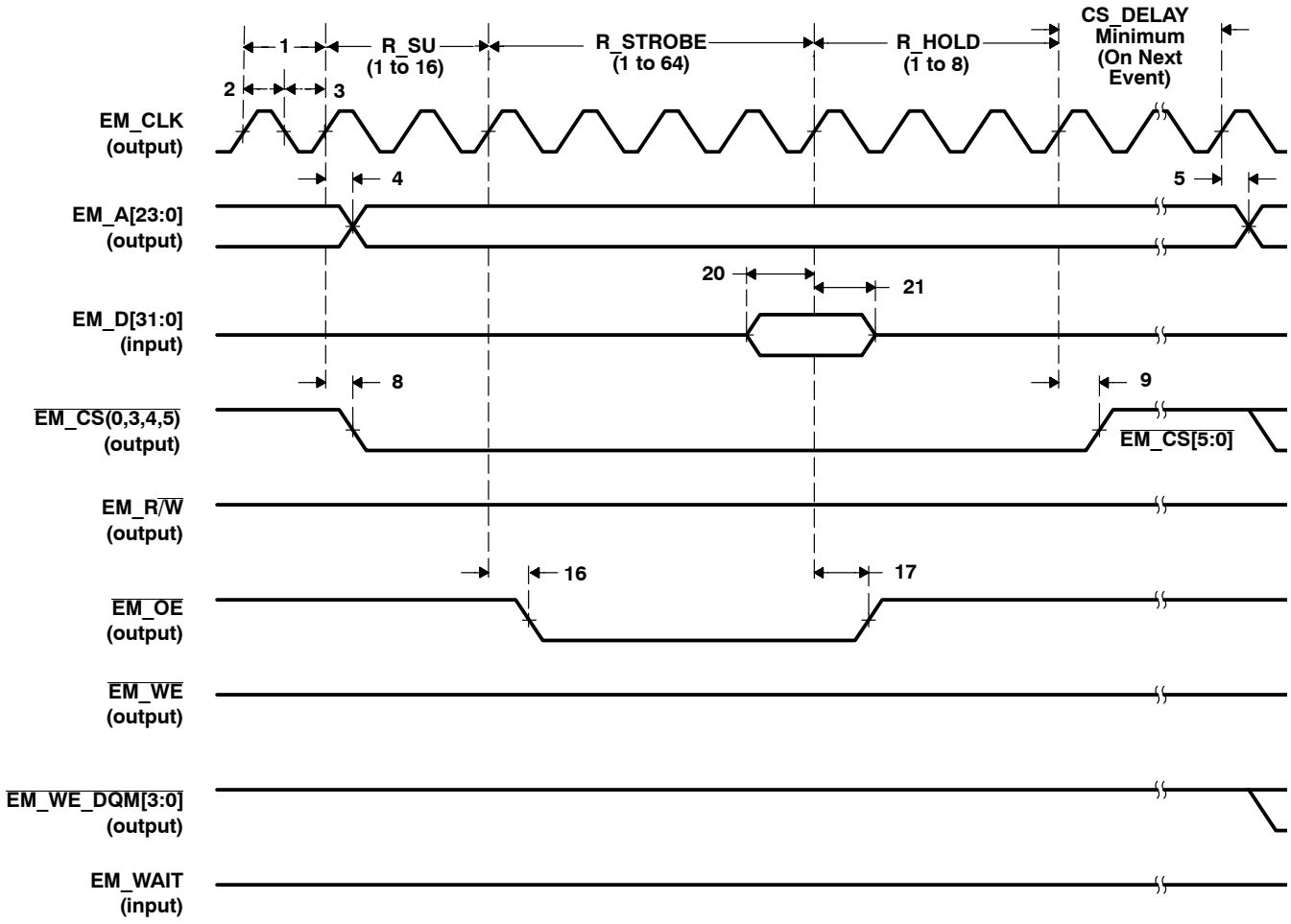


Figure 5–11. EMIF Asynchronous Read

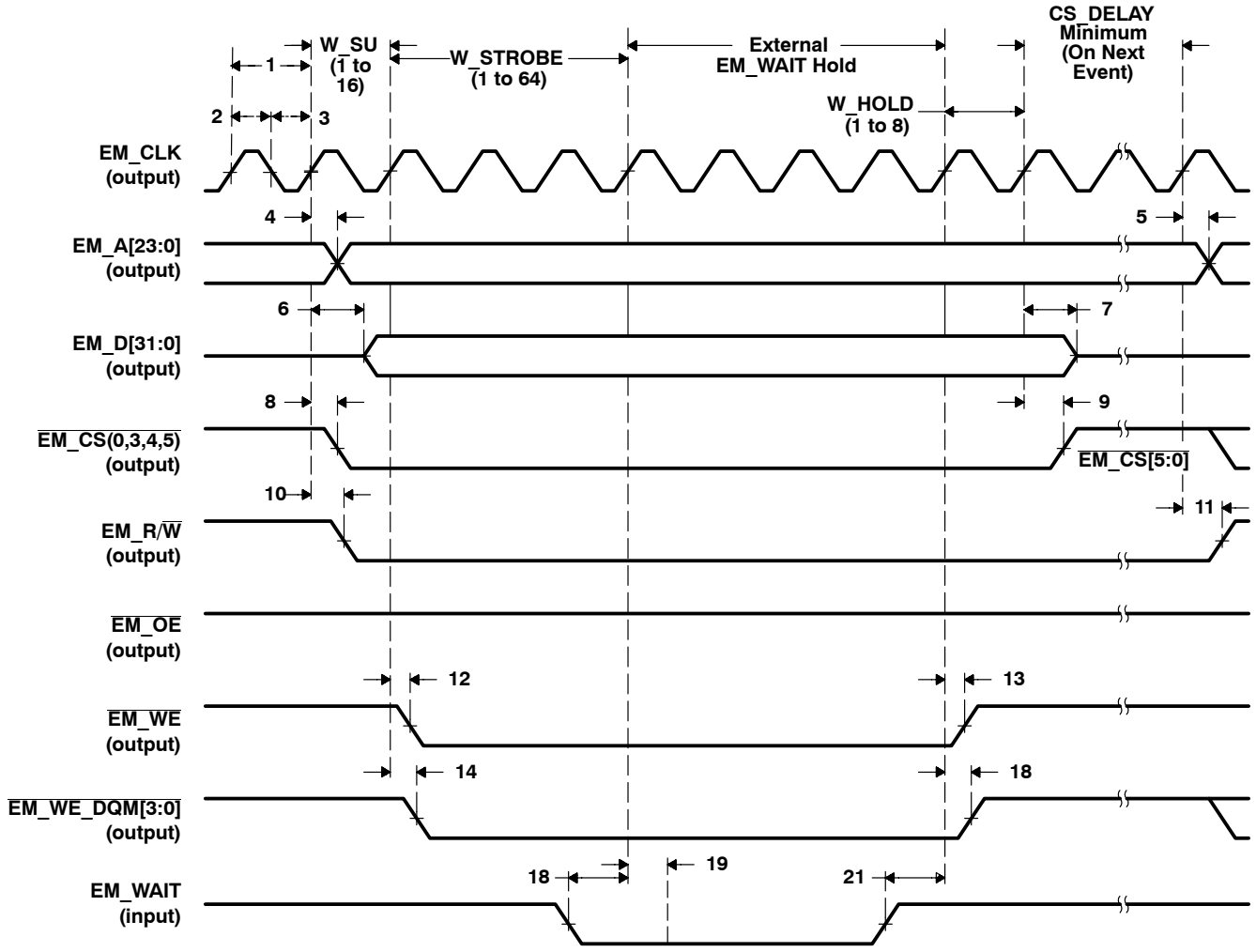


Figure 5–12. EMIF Asynchronous Write With Wait

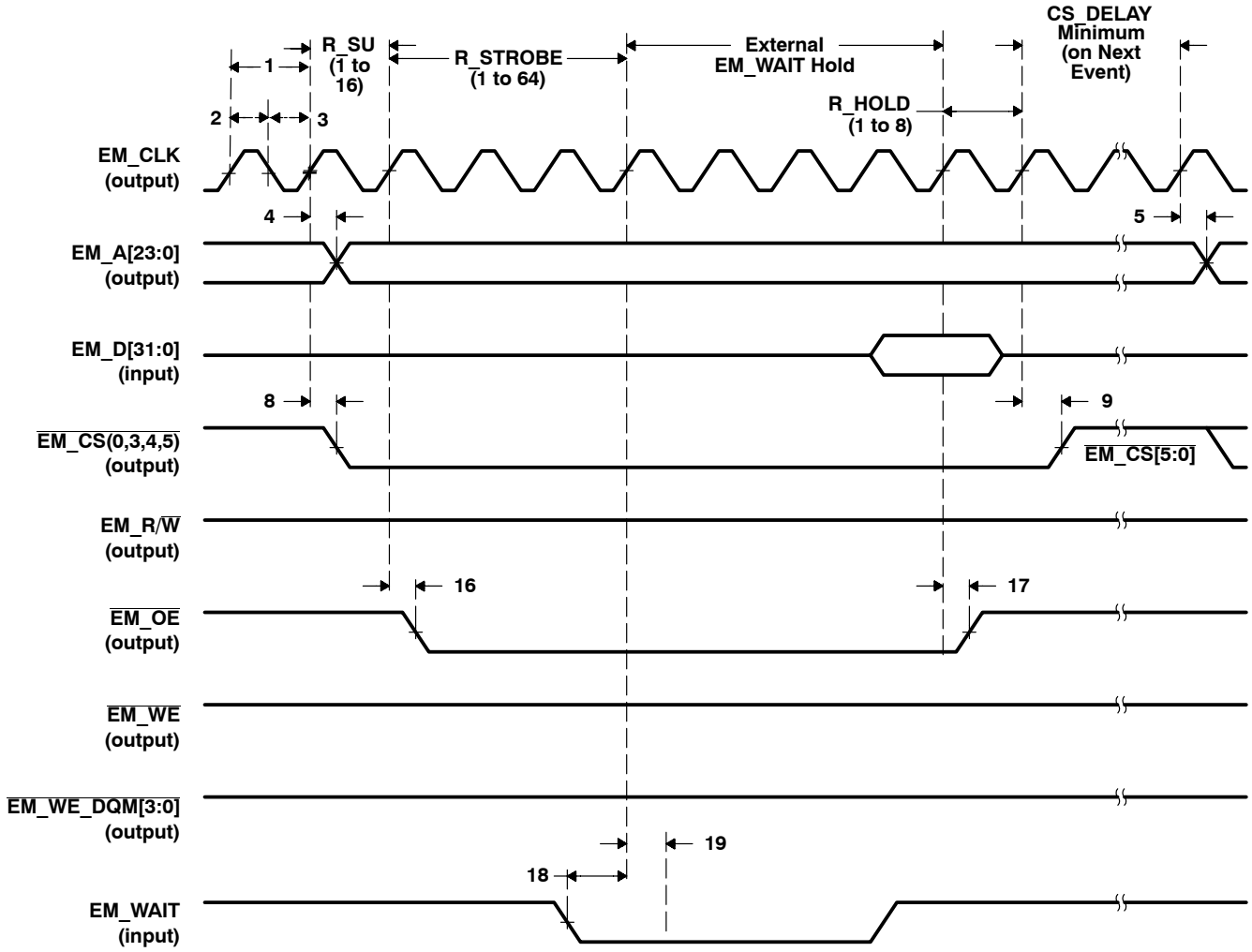


Figure 5–13. EMIF Asynchronous Read With Wait

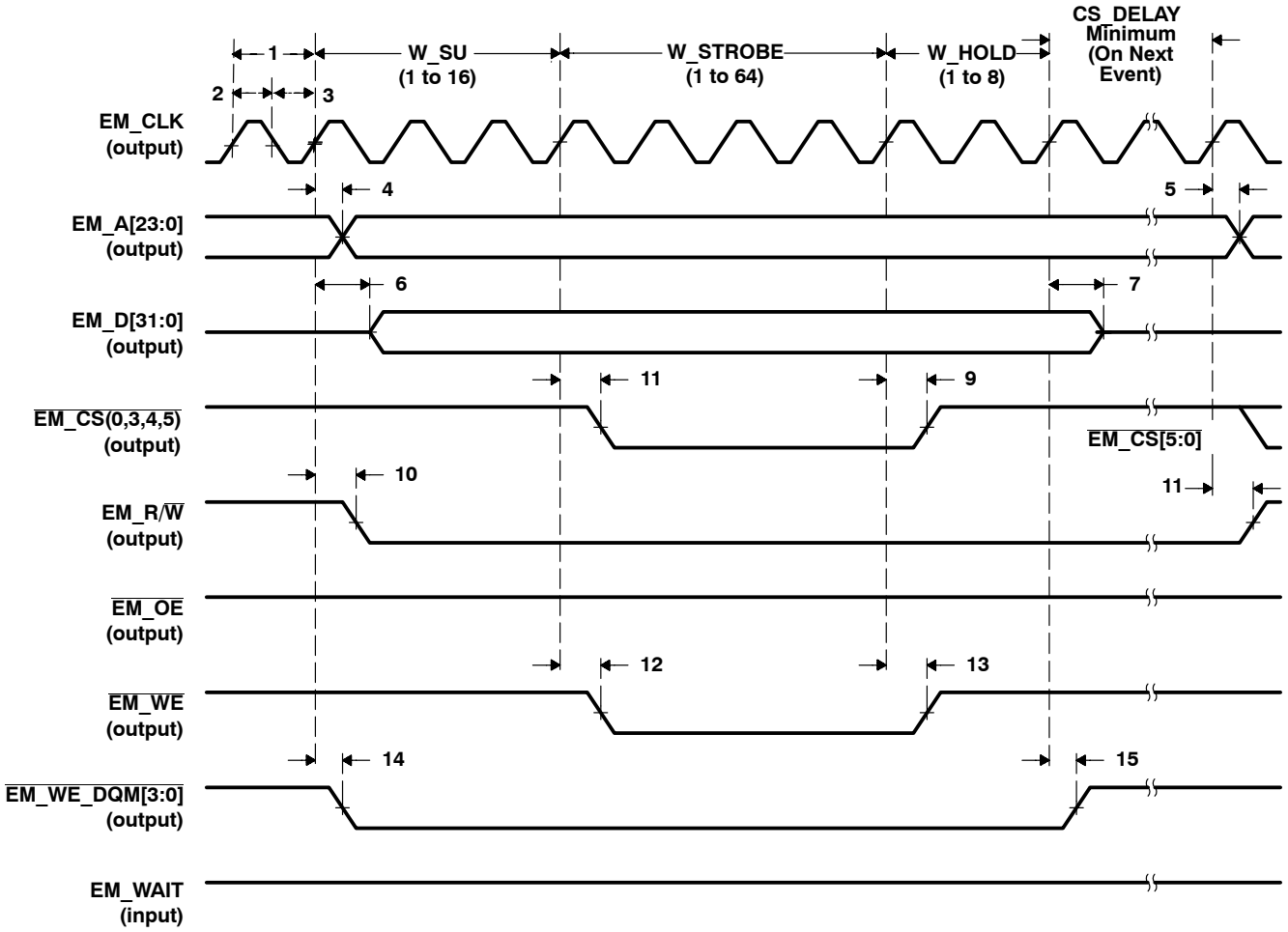


Figure 5–14. EMIF Asynchronous Write With Byte Enable

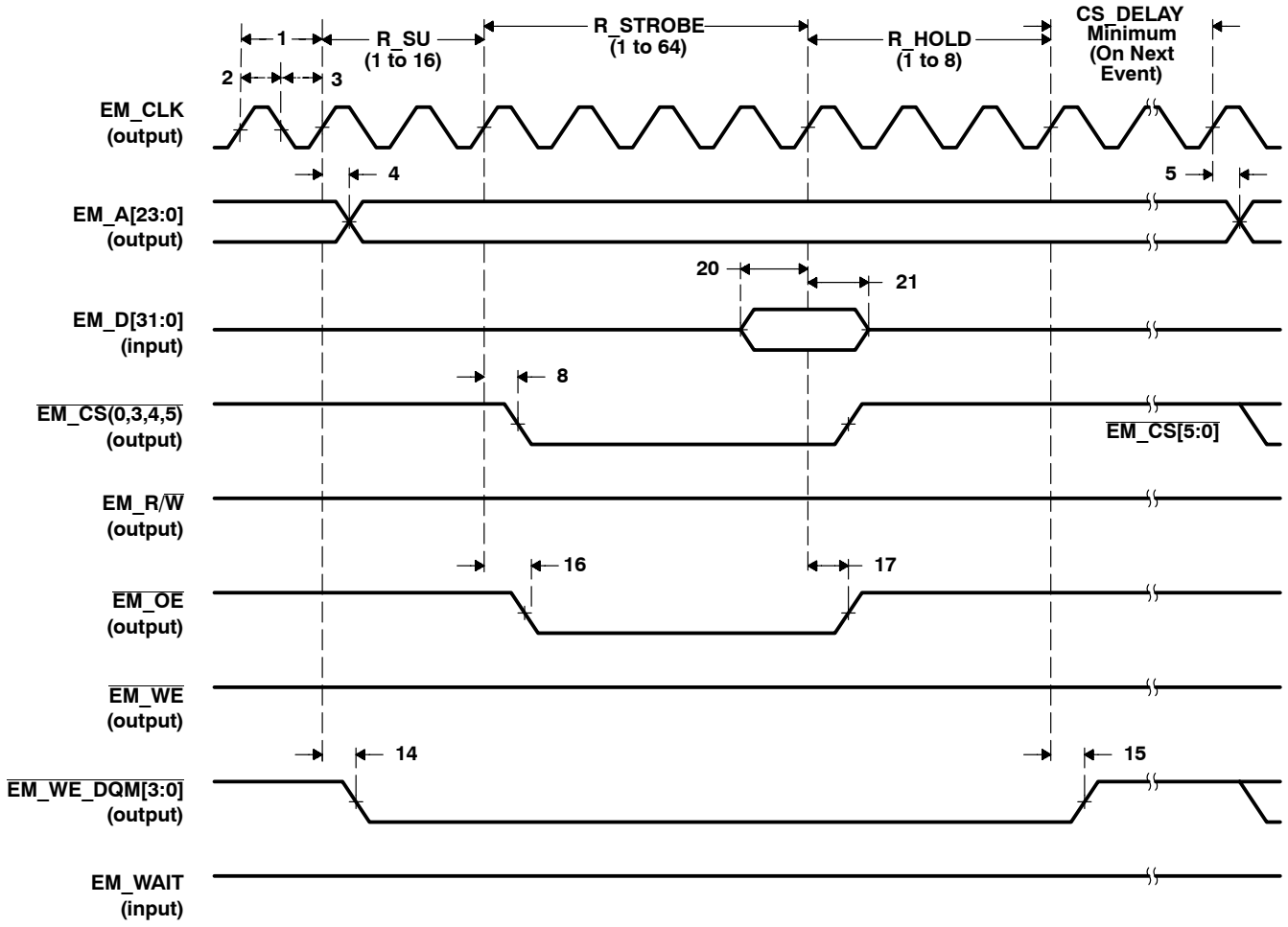


Figure 5–15. EMIF Asynchronous Read With Byte Enable

5.9 Ethernet Interface Timing

5.9.1 PHY

Table 5–14. Ethernet 10M-Bit TX Timing (See Figure 5–16)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
1	P0_TX_P/P1_TX_P, P0_TX_M/P1_TX_M	10M-bit transmit voltage output high level (V_{T10H})	2.2	2.5	2.8	V
2		10M-bit transmit voltage output mid level (V_{T10M})		0		V
3		10M-bit transmit voltage output low level (V_{T10L})	–2.8	–2.5	–2.2	V

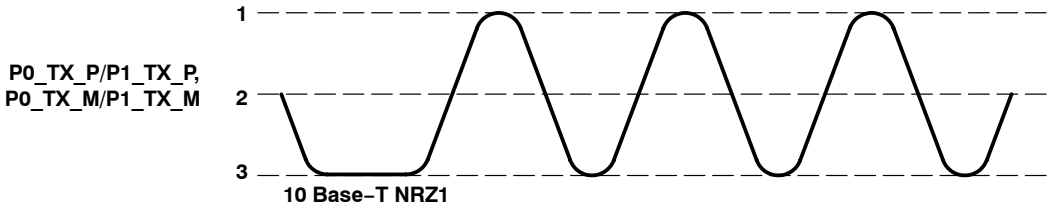


Figure 5–16. Ethernet 10M-Bit TX

Table 5–15. Ethernet 100M-Bit TX Timing (See Figure 5–17)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
1	P0_TX_P/P1_TX_P, P0_TX_M/P1_TX_M	100M-bit transmit voltage output high level (V_{T100H})	0.95	1	1.05	V
2		100M-bit transmit voltage output mid level (V_{T100M})	–0.5	0	0.5	V
3		100M-bit transmit voltage output low level (V_{T100L})	–1.05	–1	–0.95	V
4	$t_{r(T100\_m1)}$	Rise time, 100M-bit transmit –1	3	4	5	ns
5	$t_{r(T100\_p1)}$	Rise time, 100M-bit transmit 1	3	4	5	ns
6	$t_{f(T100\_p1)}$	Fall time, 100M-bit transmit 1	3	4	5	ns
7	$t_{f(T100\_m1)}$	Fall time, 100M-bit transmit –1	3	4	5	ns
8	$t_{d(T100\_JITTER)}$	Delay time, 100M-bit transmit jitter			1.4	ns

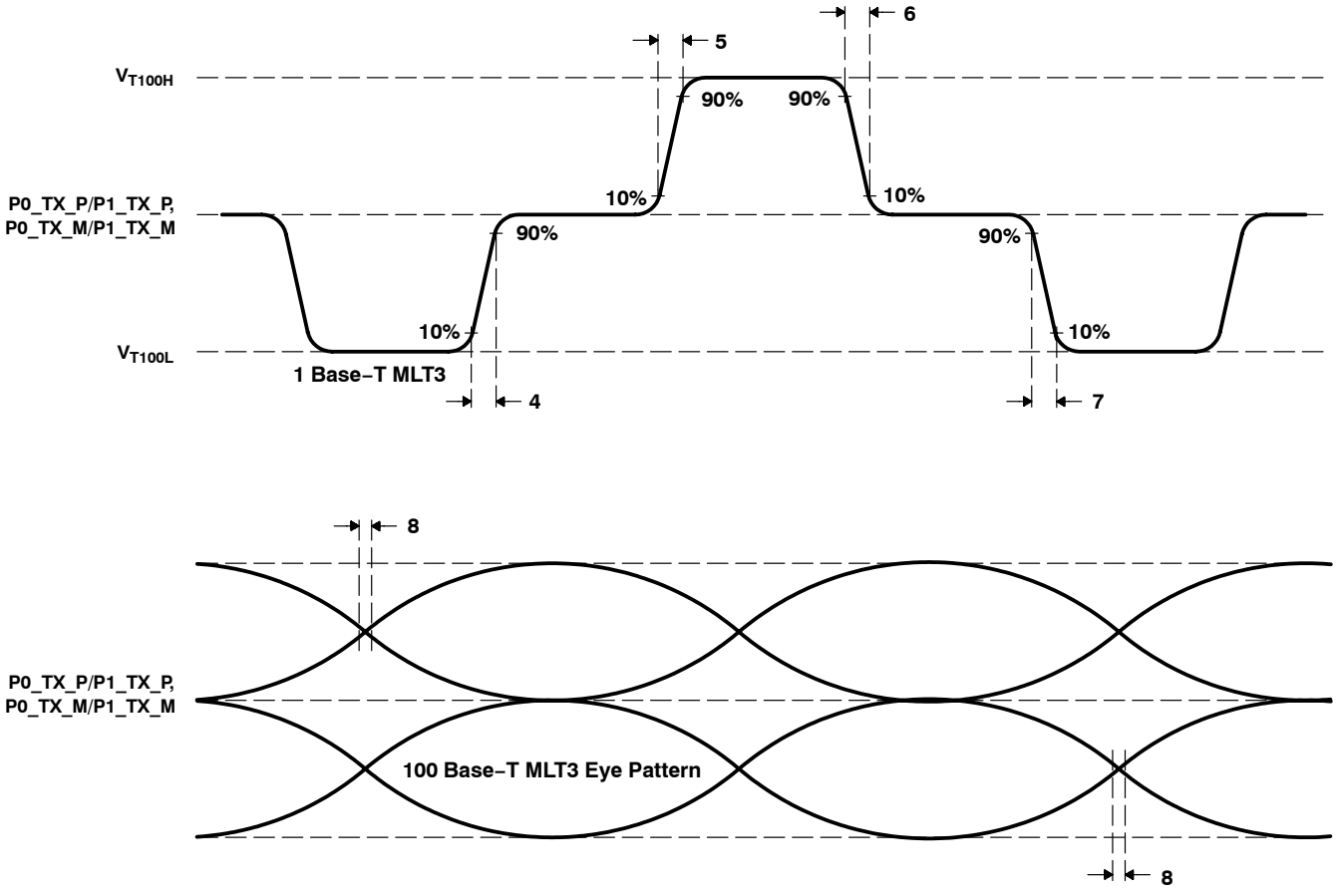


Figure 5–17. Ethernet 100M-Bit TX

Table 5–16. Ethernet 10M-Bit RX Timing (See Figure 5–18)

NO.	DESCRIPTION†		MIN	TYP	MAX	UNIT
1	P0_RX_P/P1_RX_P, P0_RX_M/P1_RX_M	10M-bit receive peak-to-peak voltage input squelch (V_{R10ppS})		300		mV
2		10M-bit receive peak-to-peak voltage input detect (V_{R10ppD})		585		mV

† The equalizer function in the PHY compensates for phase and amplitude distortion in the physical channel (magnetics, connectors, and CAT 5 cable). The signal can be restored for any good quality CAT 5 cable length between 1 m and 150 m. If the DC content of the signal is such that the low-frequency component falls below the low-frequency pole of the isolation transformer, then the droop characteristics of the transformer becomes significant, and baseline wander (BLW) on the received signal results. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD-defined killer packet with no bit errors.

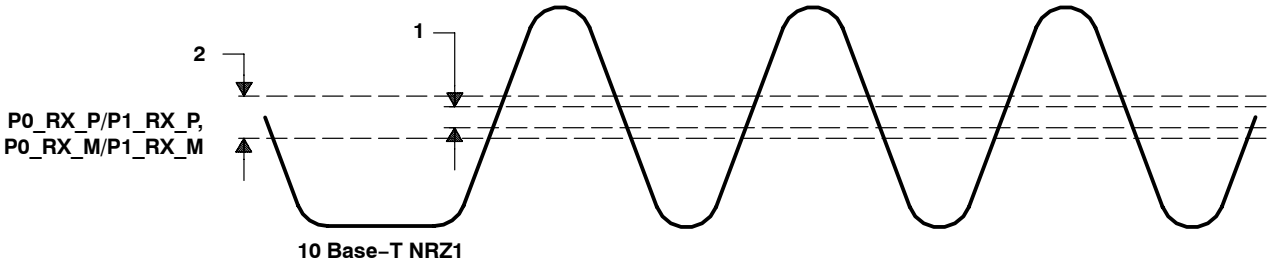


Figure 5–18. Ethernet 10M-Bit RX

Table 5–17. Ethernet 100M-Bit RX Timing (See Figure 5–19)

NO.	DESCRIPTION†		MIN	TYP	MAX	UNIT
1	P0_RX_P/P1_RX_P, P0_RX_M/P1_RX_M	100M-bit receive peak-to-peak voltage input undetectable ($V_{R100ppOFF}$)	200			mV
2		100M-bit receive peak-to-peak voltage input detectable ($V_{R100ppON}$)		300		mV

† The equalizer function in the PHY compensates for phase and amplitude distortion in the physical channel (magnetics, connectors, and CAT 5 cable). The signal can be restored for any good quality CAT 5 cable length between 1 m and 150 m. If the DC content of the signal is such that the low-frequency component falls below the low-frequency pole of the isolation transformer, then the droop characteristics of the transformer becomes significant, and baseline wander (BLW) on the received signal results. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD-defined killer packet with no bit errors.

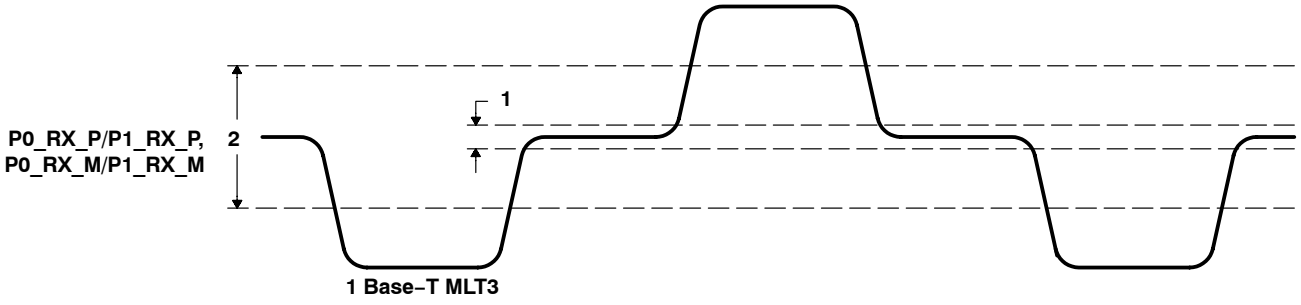


Figure 5–19. Ethernet 100M-Bit RX

5.9.2 MII

5.9.2.1 MII TX Port

Table 5–18. Ethernet MII TX Port Timing Requirements† (See Figure 5–20)

NO.	DESCRIPTION†		MIN	MAX	UNIT
1	$t_{c(MII\_TX\_CLK)1}$	Cycle time, MII_P0_TX_CLK/MII_P1_TX_CLK (100 Base-T), f_c = 25 MHz	40		ns
2	$t_{w(MII\_TX\_CLK\_H)1}$	Pulse duration, MII_P0_TX_CLK/MII_P1_TX_CLK high (100 Base-T)	16	24	ns
3	$t_{w(MII\_TX\_CLK\_L)1}$	Pulse duration, MII_P0_TX_CLK/MII_P1_TX_CLK low (100 Base-T)	16	24	ns
4	$t_{c(MII\_TX\_CLK)2}$	Cycle time, MII_P0_TX_CLK/MII_P1_TX_CLK (10 Base-T), f_c = 25 MHz	400		ns
5	$t_{w(MII\_TX\_CLK\_H)2}$	Pulse duration, MII_P0_TX_CLK/MII_P1_TX_CLK high (10 Base-T)‡	160	240	ns
6	$t_{w(MII\_TX\_CLK\_L)2}$	Pulse duration, MII_P0_TX_CLK/MII_P1_TX_CLK low (10 Base-T)‡	160	240	ns

† MII_P0_CRS, MII_P1_CRS, MII_P0_COL, and MII_P1_COL are driven asynchronously by the PHY. MII_P0_TX_D[3:0] and MII_P1_TX_D[3:0] are driven by the reconciliation sublayer synchronous to MII_P0_TX_CLK and MII_P1_TX_CLK, respectively. MII_P0_TX_ENBL and MII_P1_TX_ENBL are asserted and deasserted by the reconciliation sublayer synchronous to the rising edges of MII_P0_TX_CLK and MII_P1_TX_CLK, respectively.
The timing shown in Table 5–18 represents the internal PHY disabled mode; all other modes are not covered.
‡ Specified by design

Table 5–19. Ethernet MII TX Port Operating Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (See Figure 5–20)

NO.	DESCRIPTION†		MIN	MAX	UNIT
7	$t_{d(MII\_TX\_D\_V)}$	Delay time, MII_P0_TX_CLK/MII_P1_TX_CLK↑ to MII_P0_TX_D[3:0]/MII_P1_TX_D[3:0] valid	0	25	ns
8	$t_{d(MII\_TX\_ENBL\_V)}$	Delay time, MII_P0_TX_CLK/MII_P1_TX_CLK↑ to MII_P0_TX_ENBL/MII_P1_TX_ENBL valid‡	0	25	ns
9	$t_{d(MII\_TX\_ENBL\_I)}$	Delay time, MII_P0_TX_CLK/MII_P1_TX_CLK↑ to MII_P0_TX_ENBL/MII_P1_TX_ENBL invalid‡	0	25	ns

† MII_P0_CRS, MII_P1_CRS, MII_P0_COL, and MII_P1_COL are driven asynchronously by the PHY. MII_P0_TX_D[3:0] and MII_P1_TX_D[3:0] are driven by the reconciliation sublayer synchronous to MII_P0_TX_CLK and MII_P1_TX_CLK, respectively. MII_P0_TX_ENBL and MII_P1_TX_ENBL are asserted and deasserted by the reconciliation sublayer synchronous to the rising edges of MII_P0_TX_CLK and MII_P1_TX_CLK, respectively.
The timing shown in Table 5–19 represents the internal PHY disabled mode; all other modes are not covered.
‡ Specified by design

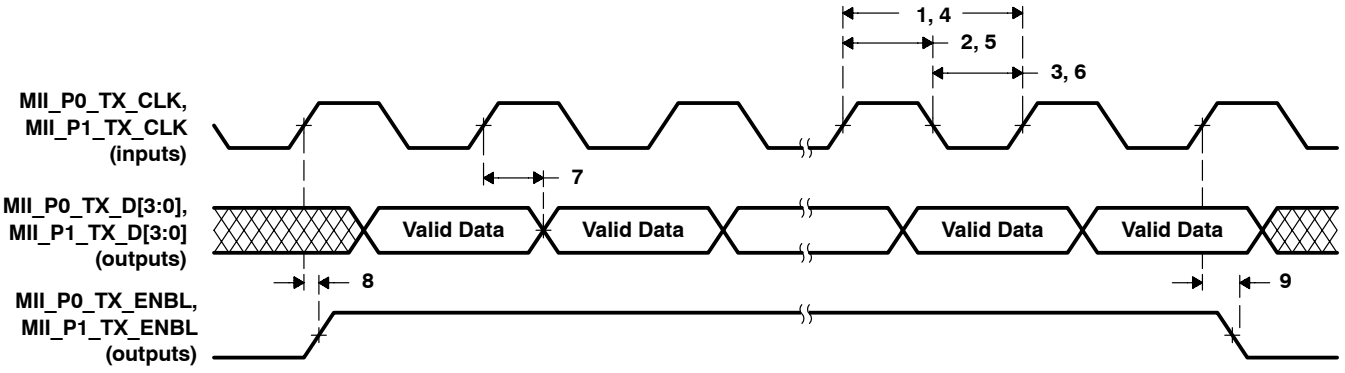


Figure 5–20. Ethernet MII TX Port

5.9.2.2 MII RX Port

Table 5–20. Ethernet MII RX Port Timing Requirements (See Figure 5–21)

NO.	DESCRIPTION†		MIN	MAX	UNIT
1	$t_{c(MII\_RX\_CLK)1}$	Cycle time, MII_P0_RX_CLK/MII_P1_RX_CLK (100 Base-T), f_c = 25 MHz	40		ns
2	$t_{w(MII\_RX\_CLK\_H)1}$	Pulse duration, MII_P0_RX_CLK/MII_P1_RX_CLK high (100 Base-T)	16	24	ns
3	$t_{w(MII\_RX\_CLK\_L)1}$	Pulse duration, MII_P0_RX_CLK/MII_P1_RX_CLK low (100 Base-T)	16	24	ns
4	$t_{c(MII\_RX\_CLK)2}$	Cycle time, MII_P0_RX_CLK/MII_P1_RX_CLK (10 Base-T), f_c = 25 MHz	400		ns
5	$t_{w(MII\_RX\_CLK\_H)2}$	Pulse duration, MII_P0_RX_CLK/MII_P1_RX_CLK high (10 Base-T)‡	160	240	ns
6	$t_{w(MII\_RX\_CLK\_L)2}$	Pulse duration, MII_P0_RX_CLK/MII_P1_RX_CLK low (10 Base-T)‡	160	240	ns
7	$t_{su(MII\_RX\_D)}$	Setup time, MII_P0_RX_D[3:0]/MII_P1_RX_D[3:0] valid before MII_P0_RX_CLK/MII_P1_RX_CLK↑	5		ns
8	$t_{h(MII\_RX\_D)}$	Hold time, MII_P0_RX_D[3:0]/MII_P1_RX_D[3:0] valid after MII_P0_RX_CLK/MII_P1_RX_CLK↑	5		ns
9	$t_{su(MII\_RX\_DV)}$	Setup time, MII_P0_RX_D[3:0]/MII_P1_RX_D[3:0] valid high before MII_P0_RX_CLK/MII_P1_RX_CLK↑	5		ns
10	$t_{h(MII\_RX\_DV)}$	Hold time, MII_P0_RX_D[3:0]/MII_P1_RX_D[3:0] valid high after MII_P0_RX_CLK/MII_P1_RX_CLK↑	5		ns
11	$t_{su(MII\_RX\_ERR)}$	Setup time, MII_P0_RX_ERR/MII_P1_RX_ERR valid before MII_P0_RX_CLK/MII_P1_RX_CLK↑	5		ns
12	$t_{h(MII\_RX\_ERR)}$	Hold time, MII_P0_RX_ERR/MII_P1_RX_ERR valid after MII_P0_RX_CLK/MII_P1_RX_CLK↑	5		ns

† MII_P0_CRS, MII_P1_CRS, MII_P0_COL, and MII_P1_COL are driven asynchronously by the PHY. MII_P0_RX_D[3–0] and MII_P1_RX_D[3–0] are driven by the PHY on the falling edge of MII_P0_RX_CLK and MII_P1_RX_CLK, respectively. MII_P0_RX_D[3–0] and MII_P1_RX_D[3–0] timing must be met during clock periods when MII_P0_RX_DV and MII_P1_RX_DV is asserted, respectively. MII_P0_RX_DV and MII_P1_RX_DV is asserted and deasserted by the PHY on the falling edge of MII_P0_RX_CLK and MII_P1_RX_CLK, respectively. MII_P0_RX_ERR and MII_P1_RX_ERR is driven by the PHY on the falling edge of MII_P0_RX_CLK and MII_P1_RX_CLK, respectively.

The timing shown in Table 5–20 represents the Internal PHY disabled mode; all other modes are not covered.

‡ Specified by design

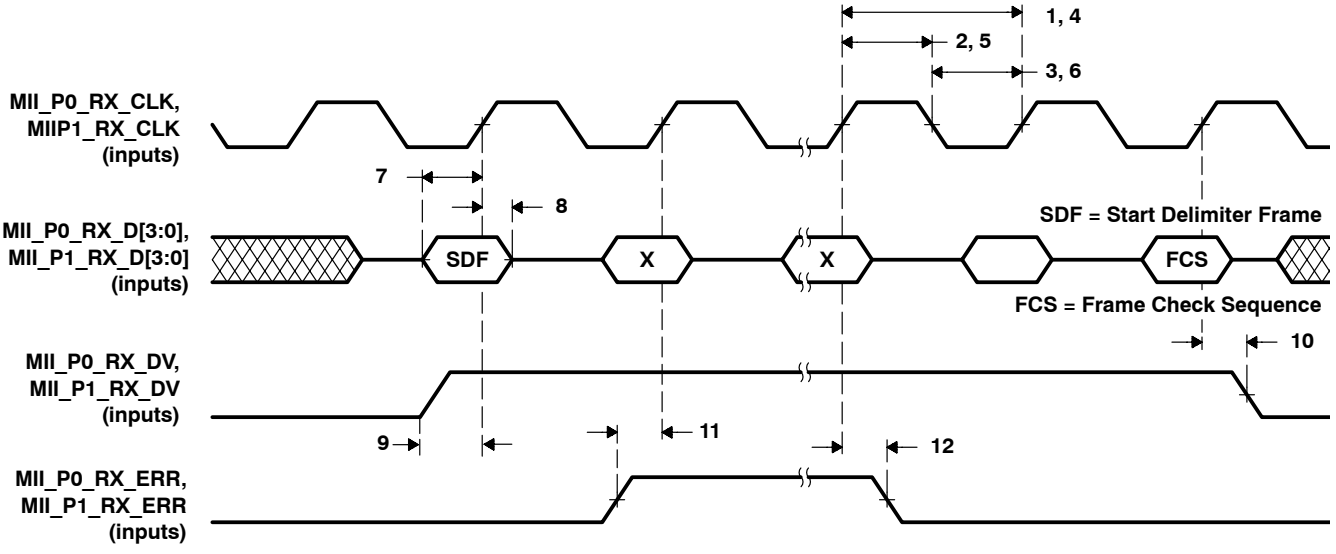


Figure 5–21. Ethernet MII RX Port

5.9.3 MDIO

Table 5–21. Ethernet MDIO TX Operating Characteristics (See Figure 5–22)

NO.	DESCRIPTION†		MIN	TYP	MAX	UNIT
	$f_{clock(MDIO\_CLK)}$	Clock frequency, MII_MD_CLK			8	MHz
1	$t_{c(MDIO\_CLK)}$	Cycle time, MII_MD_CLK	125			ns
2	$t_{w(MDIO\_CLK\_H)}$	Pulse duration, MII_MD_CLK high‡		62.5		ns
3	$t_{w(MDIO\_CLK\_L)}$	Pulse duration, MII_MD_CLK low‡		62.5		ns
4	$t_{d(MDIO\_TX\_D)}$	Delay time, MII_MD_CLK↑ to MII_MD_IO valid‡	0		150	ns

† The MDIO may be configured in any one of the following modes:
– Internal TNETV1060 driver. The TNETV1060 may control up to 30 external MII devices in this mode.
– External driver. An external device may control the two internal TNETV1060 PHY devices.
The timing shown in Table 5–21 represents the internal TNETV1060 driver mode; all other modes are not covered.
‡ Specified by design

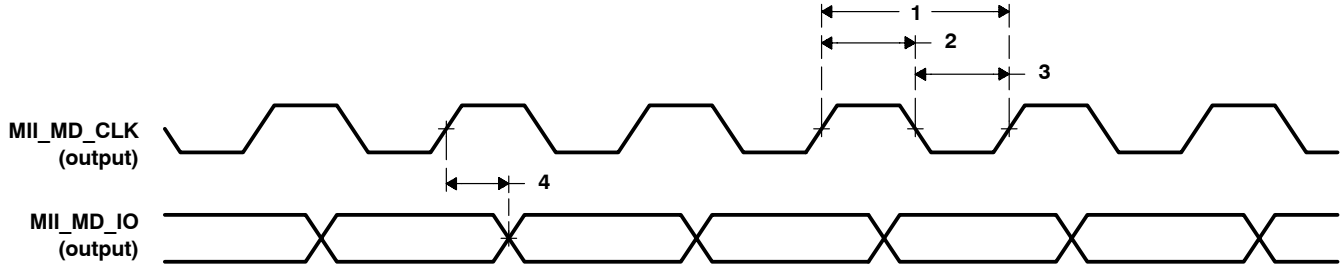


Figure 5–22. Ethernet MDIO TX

Table 5–22. Ethernet MDIO RX Operating Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (See Figure 5–23)

NO.	DESCRIPTION†		MIN	TYP	MAX	UNIT
	$f_{clockMDIO\_CLK)}$	Clock frequency, MII_MD_CLK			8	MHz
1	$t_{c(MDIO\_CLK)}$	Cycle time, MII_MD_CLK	125			ns
2	$t_{w(MDIO\_CLK\_H)}$	Pulse duration, MII_MD_CLK high‡		62.5		ns
3	$t_{w(MDIO\_CLK\_L)}$	Pulse duration, MII_MD_CLK low‡		62.5		ns
4	$t_{d(MDIO\_RX\_D)}$	Delay time, MII_MD_IO valid to MII_MD_CLK↑‡	10			ns
5	$t_{d(MDIO\_RX\_D)}$	Delay time, MII_MD_CLK↑ to MII_MD_IO valid‡	5			ns

† The MDIO may be configured in any one of the following modes:
– Internal TNETV1060 driver. The TNETV1060 may control up to 30 external MII devices in this mode.
– External driver. An external device may control the two internal TNETV1060 PHY devices.
The timing shown in Table 5–22 represents the Internal TNETV1060 driver mode; all other modes are not covered.
‡ Specified by design

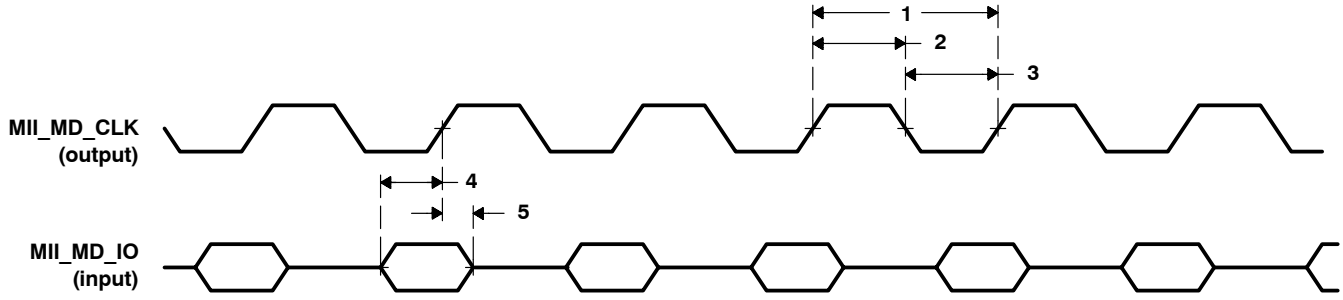


Figure 5–23. Ethernet MDIO RX

5.9.4 LED

Table 5–23. Ethernet LED Operating Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (See Figure 5–24)

NO.	DESCRIPTION†		MIN	MAX	UNIT
1	$t_{w(LED\_100\_1)}$	Pulse duration, $\overline{P0\_100MB}$/$\overline{P1\_100MB}$ high‡	64		ms
2	$t_{w(LED\_100\_0)}$	Pulse duration, $\overline{P0\_100MB}$/$\overline{P1\_100MB}$ low‡	64		ms
3	$t_{w(LED\_LINK\_1)}$	Pulse duration, $\overline{P0\_LINK}$/$\overline{P1\_LINK}$ high‡	64		ms
4	$t_{w(LED\_LINK\_0)}$	Pulse duration, $\overline{P0\_LINK}$/$\overline{P1\_LINK}$ low‡	64		ms
5	$t_{w(LED\_ACTIVITY\_1)}$	Pulse duration, $\overline{P0\_ACTIVITY}$/$\overline{P1\_ACTIVITY}$ high‡	64		ms
6	$t_{w(LED\_ACTIVITY\_0)}$	Pulse duration, $\overline{P0\_ACTIVITY}$/$\overline{P1\_ACTIVITY}$ low‡	128		ms
7	$t_{w(LED\_DUPLEX\_1)}$	Pulse duration, $\overline{P0\_FDUPLEX}$/$\overline{P1\_FDUPLEX}$ high‡	64		ms
8	$t_{w(LED\_DUPLEX\_0)}$	Pulse duration, $\overline{P0\_FDUPLEX}$/$\overline{P1\_FDUPLEX}$ low‡	64		ms

† All LED output drivers are 8 mA, with an internal pullup.
‡ Specified by design

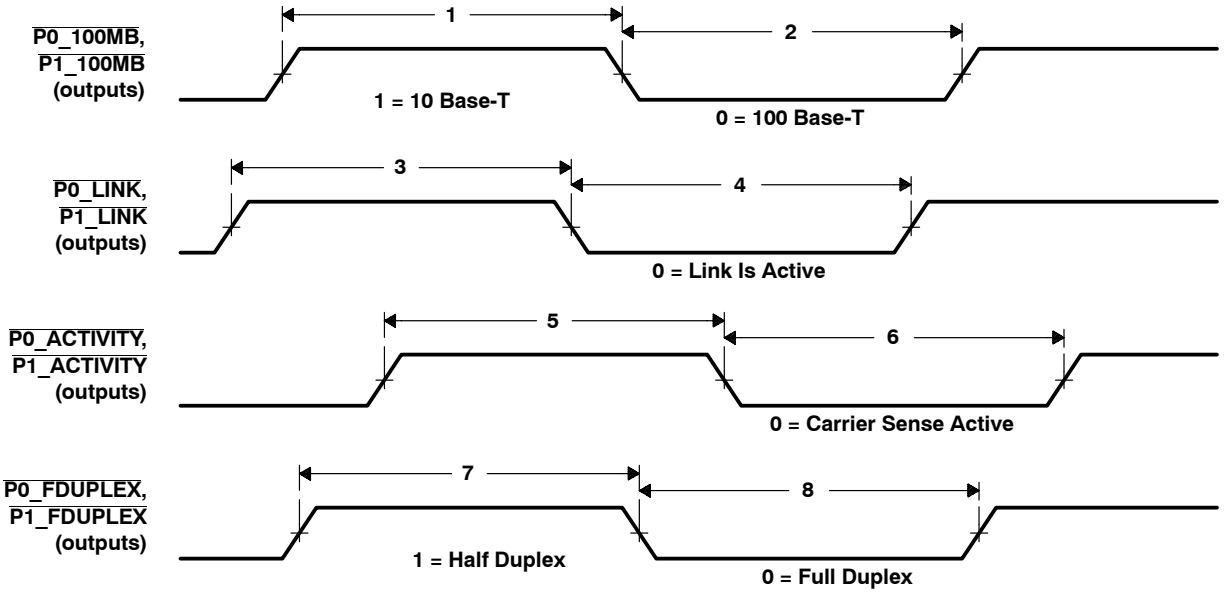


Figure 5–24. Ethernet LED

5.10 McBSP Interface Timing

Table 5–24. McBSP Clock Operating Characteristics (See Figure 5–25)

NO.	DESCRIPTION†		MIN	TYP	MAX	UNIT
	$f_{clock(CLKSRG\_DSP)}$	Clock frequency, CLKSRG, source 1/2 DSP_CLK†#			62.5	MHz
1	$t_{c(CLKSRG\_DSP)}$	Cycle time, CLKSRG, source 1/2 DSP_CLK#	16			ns
2	$t_{w(CLKSRG\_DSP\_H)}$	Pulse duration, CLKSRG, source 1/2 DSP_CLK high#		8		ns
3	$t_{w(CLKSRG\_DSP\_L)}$	Pulse duration, CLKSRG, source 1/2 DSP_CLK low#		8		ns
4	$t_{r(CLKSRG\_DSP)}$	Rise time, CLKSRG, source 1/2 DSP_CLK#		1		ns
5	$t_{f(CLKSRG\_DSP)}$	Fall time, CLKSRG, source 1/2 DSP_CLK#		1		ns
	$f_{clock(CLKSRG\_CLKX)}$	Clock frequency, CLKSRG, source McBSP_CLK_TX#			8.192	MHz
6	$t_{c(CLKSRG\_CLKX)}$	Cycle time, CLKSRG, source McBSP_CLK_TX#	122			ns
7	$t_{w(CLKSRG\_CLKX\_H)}$	Pulse duration, CLKSRG, source McBSP_CLK_TX high#		61		ns
8	$t_{w(CLKSRG\_CLKX\_L)}$	Pulse duration, CLKSRG, source McBSP_CLK_TX low#		61		ns
9	$t_{r(CLKSRG\_CLKX)}$	Rise time, CLKSRG, source McBSP_CLK_TX#			5	ns
10	$t_{f(CLKSRG\_CLKX)}$	Fall time, CLKSRG, source McBSP_CLK_TX#			5	ns
	$f_{clock(CLKSRG\_CLKR)}$	Clock frequency, CLKSRG, source McBSP_CLK_RX#			8.192	MHz
11	$t_{c(CLKSRG\_CLKR)}$	Cycle time, CLKSRG, source McBSP_CLK_RX#	122			ns
12	$t_{w(CLKSRG\_CLKR\_H)}$	Pulse duration, CLKSRG, source McBSP_CLK_RX high#		61		ns
13	$t_{w(CLKSRG\_CLKR\_L)}$	Pulse duration, CLKSRG, source McBSP_CLK_RX low#		61		ns
14	$t_{r(CLKSRG\_CLKR)}$	Rise time, CLKSRG, source McBSP_CLK_RX#			5	ns
15	$t_{f(CLKSRG\_CLKR)}$	Fall time, CLKSRG, source McBSP_CLK_RX#			5	ns
	$f_{clock(CLKG\_O)}$	Clock frequency, CLKG, when used to drive McBSP_CLK_TX and/or McBSP_CLK_RX#			8.192	MHz
	$f_{clock(CLKG\_I)}$	Clock frequency, CLKG, when used for internal synchronization#			62.5	
16	$t_{c(CLKG)}$	Cycle time, CLKG#	1	X‡	256	CLK_1§
		External, driving McBSP_CLK_TX and/or McBSP_CLK_RX#	122			ns
		Internal use only, used for synchronization and may run faster#	16			
17	$t_{w(CLKG\_H)}$	Pulse duration, CLKG high — When X is even#	0.5	$(X/2)_t$	128	CLK_1
		Pulse duration, CLKG high — When X is odd and greater than 1#		$(X/2)_t+1$		
18	$t_{w(CLKG\_L)}$	Pulse duration, CLKG low#	0.5	$(X/2)_t$	128	CLK_1
19	$t_{w(FSG\_P)}$	Pulse duration, FSG pulse width#	1		256	CLK_2¶
20	$t_{w(FSG\_W)}$	Pulse duration, FSG period#	1		4096	CLK_2

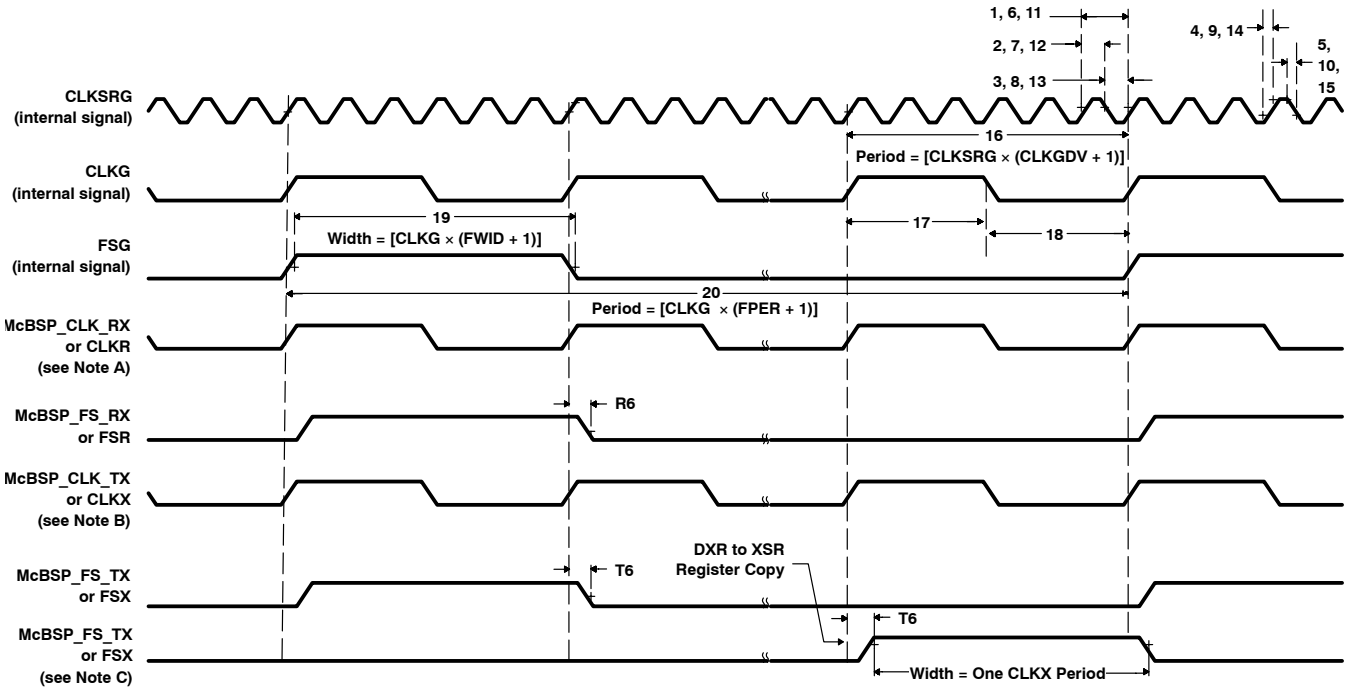
† Programmable clock source: Either McBSP_CLK_TX, McBSP_CLK_RX, or 1/2 DSP_CLK may become the clock source, dependent on the state of the DSP_McBSP_EXT (SRGR) and DSP_McBSP_EXT (PCR) registers.

‡ X: The total number of programmable clock-source periods defined in the DSP_McBSP_EXT (SRGR) register bits CLKGDV. The value X is (CLKDV + 1). In addition, the value $(X/2)_t$ is (1/2(CLKDV + 1)) truncated, except when CLKDV is 1.

§ CLK_1: Clock periods based on the programmable clock source

¶ CLK_2: Clock periods based on CLKG

Specified by design



NOTES: A. When CLKR and FSR are not used as inputs, then they may be outputs generated by CLKG and FSG, with polarity defined by CLKRP and FSRP.

B. When CLKX and FSX are not used as inputs, then they may be outputs generated by CLKG and FSG, with polarity defined by CLKXP and FSXP.

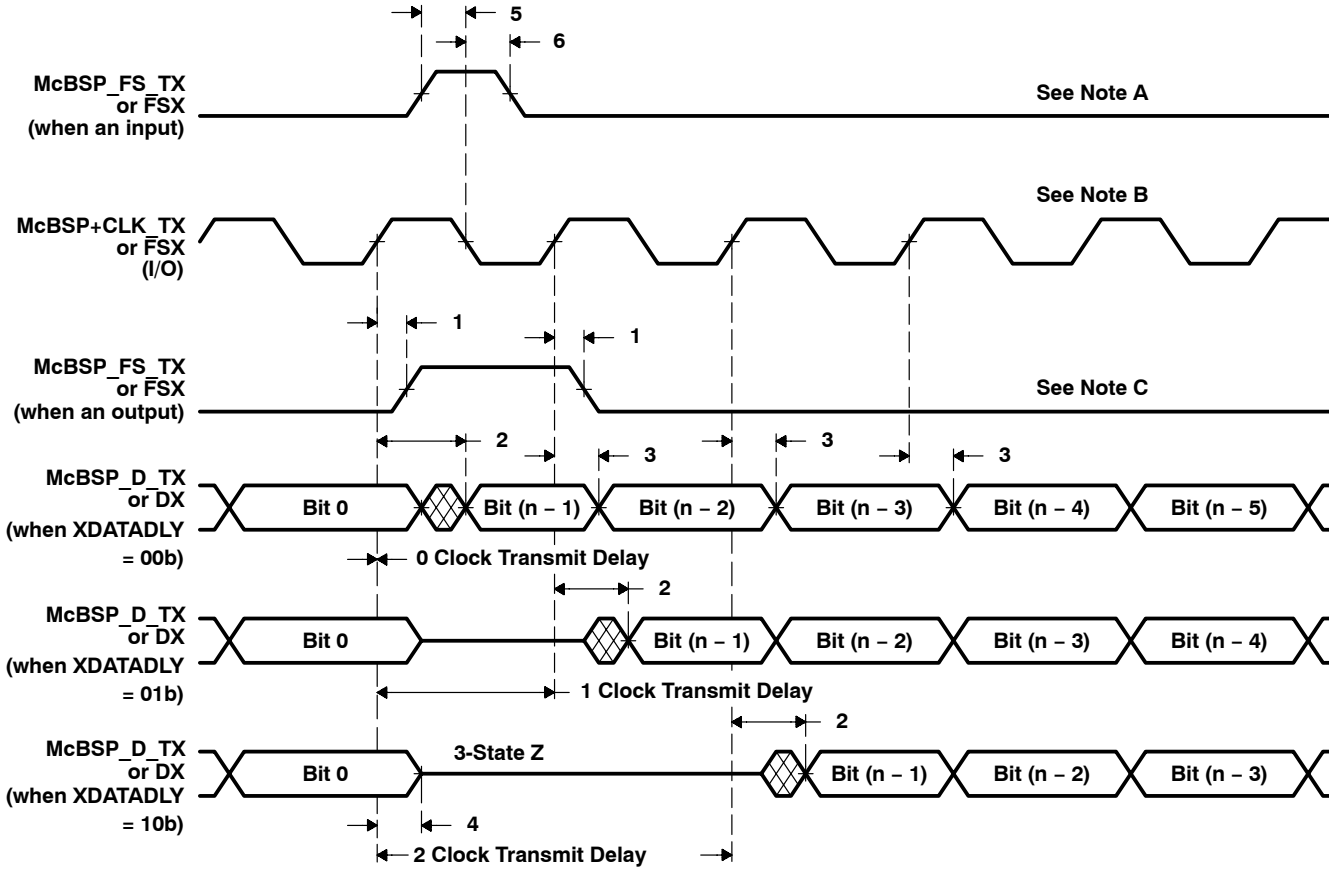
C. Configured as an output, with FSGM = 0b, allowing an FSX on load of the serial transmit register

Figure 5–25. McBSP Clock

Table 5–25. McBSP Transmit Timing (See Figure 5–26)

NO.	DESCRIPTION		CLKX	MIN	MAX	UNIT
1	$t_{d(FSX\_OUT)}$	Delay time, McBSP_CLK_TX↑ to outbound McBSP_FS_TX↑ or ↓‡	Input	5	22	ns
			Output	1	6	
2	$t_{d(DX\_DXENA)}$	Delay time, McBSP_CLK_TX↑ to first McBSP_D_TX bit valid when DXENA is enabled†‡	Input	2P+5	2P+22	ns
			Output	2P+1	2P+6	
3	$t_{d(DX\_V)}$	Delay time, McBSP_CLK_TX↑ to next McBSP_D_TX bit valid‡	Input	5	22	ns
			Output	1	6	
4	$t_{d(DX\_I)}$	Delay time, McBSP_CLK_TX active to McBSP_D_TX high impedance (Z) after last bit‡	Input	5	22	ns
			Output	1	6	
5	$t_{su(FSX\_IN)}$	Setup time, inbound McBSP_FS_TX high before McBSP_CLK_TX↓‡	Input	5		ns
			Output	22		
6	$t_{h(FSX\_IN)}$	Hold time, inbound McBSP_FS_TX high after McBSP_CLK_TX↓‡	Input	5		ns
			Output	10		

† When enabled, the DXENA bit in the DSP_McBSP_EXT (SPCR) register provides a two-clock-period (P) delay before the first data bit exits on McBSP_D_TX. Subsequent bits exit without the delay. The value P is one 1/2 DSP_CLK period.
‡ Specified by design



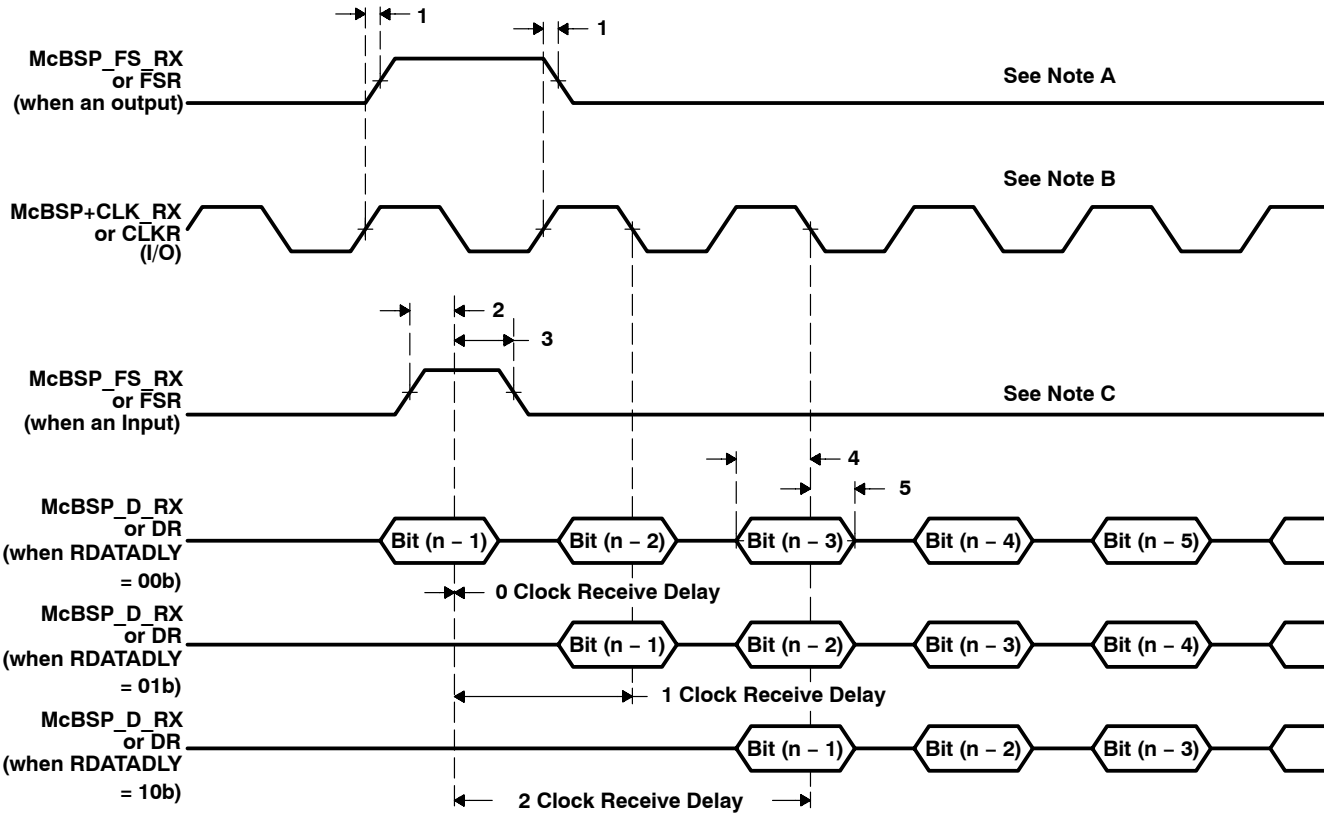
NOTES: A. McBSP_FS_TX polarity may be inverted with the FSXP register bit.
B. McBSP_CLK_TX polarity may be inverted with the CLKXP register bit. All timing references are also inverted.
C. McBSP_FS_TX polarity may be inverted with the FSXP register bit.

Figure 5–26. McBSP Transmit

Table 5–26. McBSP Receive Timing (See Figure 5–27)

NO.	DESCRIPTION		CLKX	MIN	MAX	UNIT
1	$t_{d(FSR\_OUT)}$	Delay time, McBSP_CLK_RX↑ to McBSP_FS_RX↑/↓†	Input	5	22	ns
			Output	1	6	
2	$t_{su(FSR\_IN)}$	Setup time, inbound McBSP_FS_RX high before McBSP_CLK_RX↓†	Input	5		ns
			Output	22		
3	$t_{h(FSR\_IN)}$	Hold time, inbound McBSP_FS_RX high after McBSP_CLK_RX↓†	Input	5		ns
			Output	10		
4	$t_{su(DR)}$	Setup time, inbound McBSP_D_RX valid before McBSP_CLK_RX↓†	Input	5		ns
			Output	22		
5	$t_{h(DR)}$	Hold time, inbound McBSP_D_RX valid after McBSP_CLK_RX↓†	Input	5		ns
			Output	10		

† Specified by design



NOTES: A. McBSP_FS_RX polarity may be inverted with the FSRP register bit.
B. McBSP_CLK_RX polarity may be inverted with the CLKRP register bit. All timing references are also inverted.
C. McBSP_FS_RX polarity may be inverted with the FSRP register bit.

Figure 5–27. McBSP Receive

5.10.1 SPI Mode

Table 5–27. McBSP SPI Mode Master Timing (See Figure 5–28)

NO.	DESCRIPTION†		MIN	MAX	UNIT
	$f_{clock(SIP\_M\_CLKG)}$	Clock frequency, CLKG‡#		8.192	MHz
1	$t_{c(SPI\_M\_CLKG)}$	Cycle time, CLKG#	122		ns
			2		CLK_1§
2†	$t_{d(SPI\_M\_FSX\_A)}$	Delay time, CLKG↑ to McBSP_FS_TX↓#	1	6	ns
3	$t_{d(SPI\_M\_FSX\_I)}$	Delay time, CLKG↑ to McBSP_FS_TX↑#	1	6	ns
4	$t_{d(SPI\_M\_DX\_D)}$	Delay time, CLKG↓ to McBSP_D_TX valid driven#	1	6	ns
5	$t_{d(SPI\_M\_DX\_V)}$	Delay time, McBSP_CLK_TX↓ to McBSP_D_TX valid#	1	6	ns
6	$t_{d(SPI\_M\_DX\_I)}$	Delay time, McBSP_CLK_TX↓ to McBSP_D_TX invalid#	1	6	ns
7	$t_{su(SPI\_M\_DR)}$	Setup time, McBSP_D_RX valid before McBSP_CLK_TX↑#	22		ns
8	$t_{h(SPI\_M\_DR)}$	Hold time, McBSP_D_RX valid after McBSP_CLK_TX↑#	10		ns
9	$t_{w(SPI\_M\_FSX\_2)}$	Pulse duration, McBSP_FS_TX high#	2		CLK_2¶

† SPI mode master: The McBSP is run in clock stop mode, with the McBSP providing clock timing through the internal generator (CLKG). The signals McBSP_CLK_TX, McBSP_FS_TX, and McBSP_D_TX are all outputs. The signal McBSP_D_RX is an input. The signals McBSP_CLK_RX and McBSP_FS_RX are not used, with McBSP_CLK_RX driven internally by McBSP_CLK_FX through an automatic connection.

‡ The master clock polarity and delay are programmable, with the outcome shown in Figure 5–28.

§ CLK_1: Clock periods based on 1/2 DSP_CLK

¶ CLK_2: Clock periods based on CLKG

Specified by design

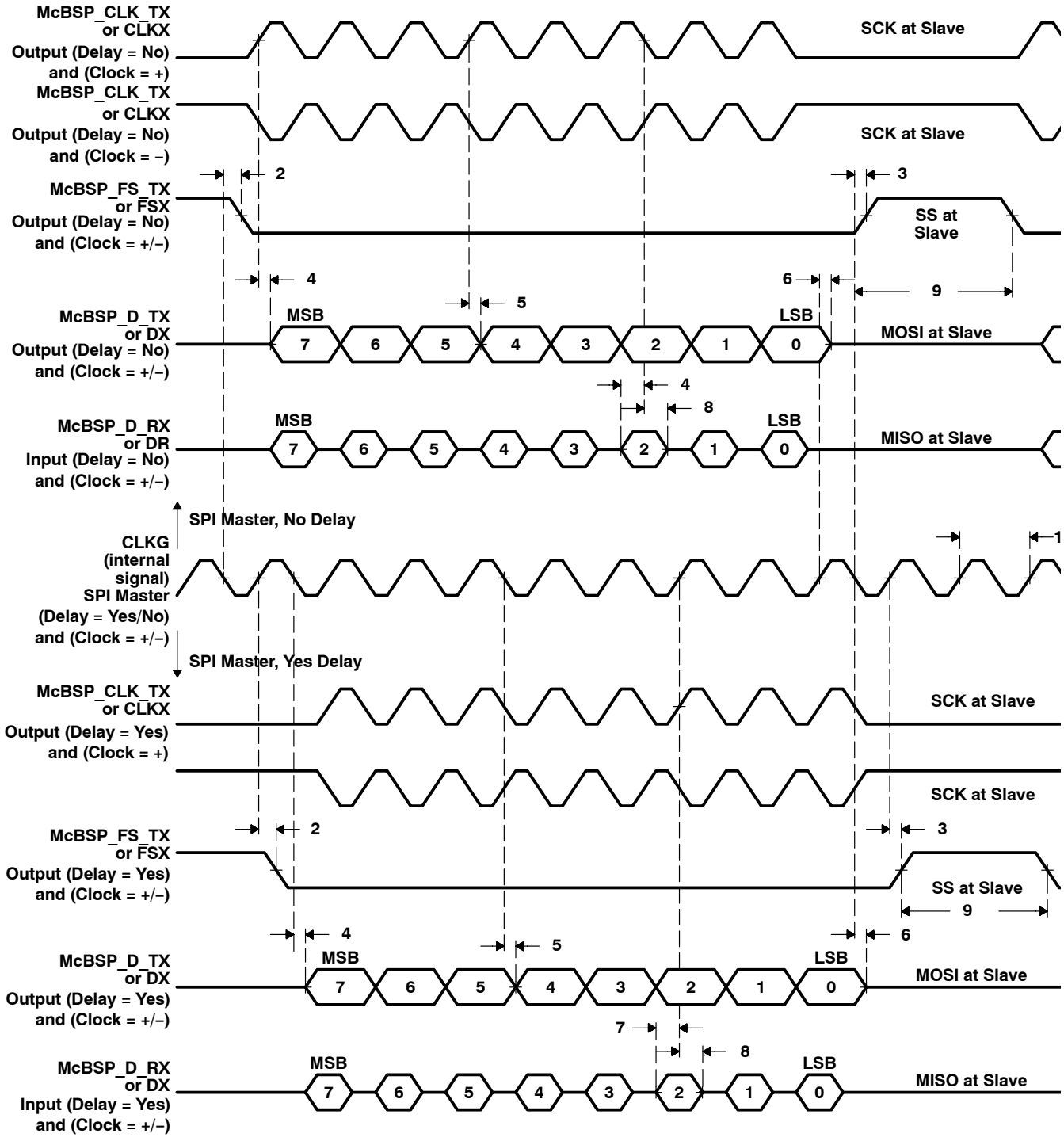


Figure 5–28. McBSP SPI Mode Master

Table 5–28. McBSP SPI Mode Slave Timing (See Figure 5–29)

NO.	DESCRIPTION†		MIN	MAX	UNIT
	$f_{clock(SPI\_S\_CLKX)}$	Clock frequency, McBSP_CLK_TX, from master‡‖		3.90625	MHz
1	$t_{c(SPI\_S\_CLKX)}$	Cycle time, McBSP_CLK_TX, from master‖	256		ns
1	$t_{c(SPI\_S\_CLKG)}$	Cycle time, CLKG, inside slave‖	16		CLK_1¶
2	$t_{h(SPI\_S\_CLKX\_A)}$	Hold time, McBSP_FS_TX low before first McBSP_CLK_TX transition↑§‖	20		ns
3	$t_{d(SPI\_S\_DX\_A)}$	Delay time, McBSP_FS_TX↓ to McBSP_D_TX valid driven‖	3P+5	5P+22	ns
4	$t_{d(SPI\_S\_DX\_V)}$	Delay time, McBSP_CLK_TX↑ to McBSP_D_TX valid‖	3P+5	3P+22	ns
5	$t_{d(SPI\_S\_DX\_I)}$	Delay time, McBSP_CLK_TX↓ to McBSP_D_TX invalid released‖	3P+5	3P+22	ns
6	$t_{su(SPI\_S\_DR)}$	Setup time, McBSP_D_RX valid before McBSP_CLK_TX↓‖	5		ns
7	$t_{h(SPI\_S\_DR)}$	Hold time, McBSP_D_RX valid after McBSP_CLK_TX↓‖	5		ns
8	$t_{w(SPI\_S\_FSX\_2)}$	Pulse duration, McBSP_FS_TX high, minimum idle duration‖	2		CLK_2#

† SPI mode slave: The McBSP is run in clock stop mode with the external device performing all master functions. The signal McBSP_D_TX is an output. The signals McBSP_CLK_TX, McBSP_FS_TX, and McBSP_D_RX are all inputs. The signals McBSP_CLK_RX and McBSP_FS_RX are not used, with McBSP_CLK_RX driven internally by McBSP_CLK_FX through an automatic connection. Even though the external master device provides the clock through McBSP_CLK_TX, the internal clock generator must be activated and programmed to divide-by-two of the 1/2 DSP_CLK to provide proper synchronization.

‡ Delay: In slave mode, the delay feature has no meaning and should not be programmed.

§ Clock polarity: The clock polarity is programmable, with the outcome shown in Figure 5–29.

¶ CLK_1: Clock periods based on 1/2 DSP_CLK

CLK_2: Clock periods based on CLKG

‖ Specified by design

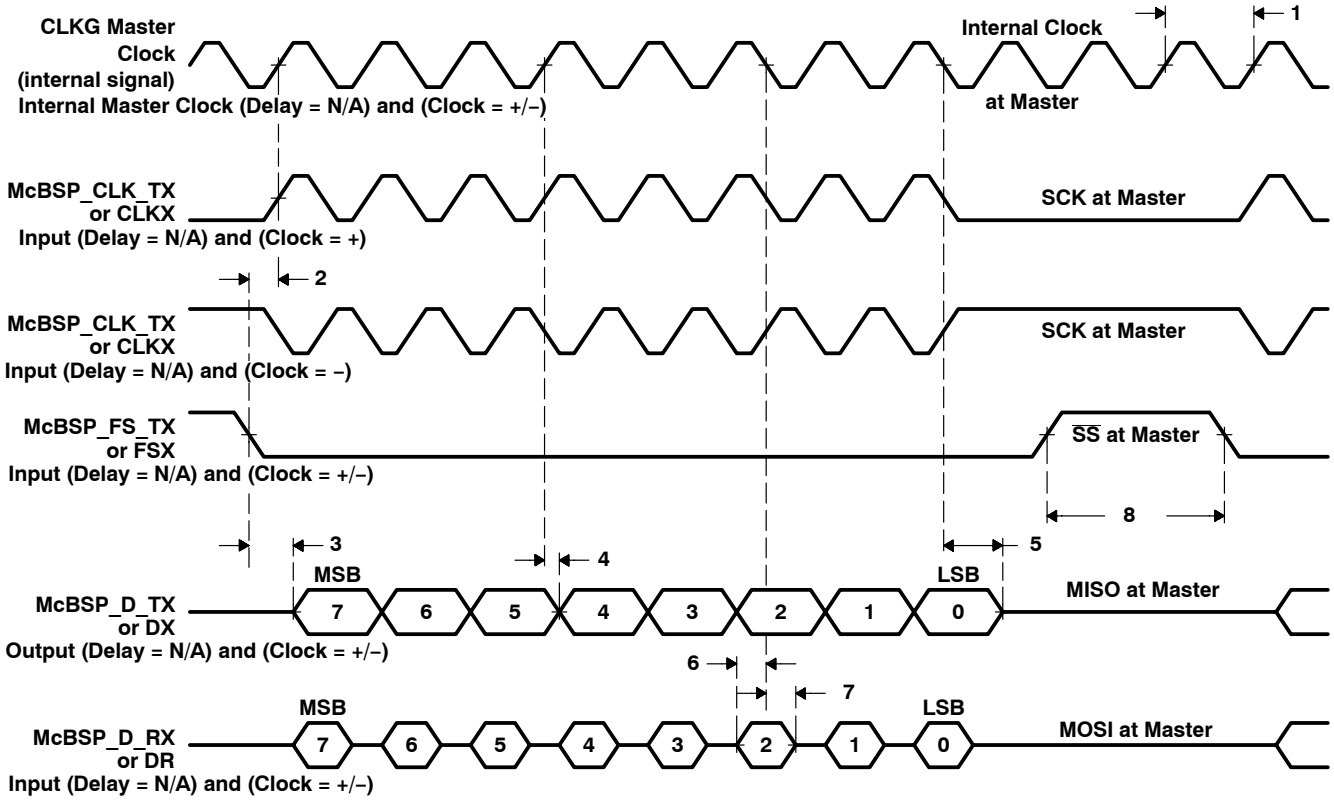


Figure 5–29. McBSP SPI Mode Slave

5.11 Line Codec Interface Timing

5.11.1 PCM

Table 5–29. Line Codec Interface PCM Timing (See Figure 5–30)

NO.	DESCRIPTION		DESCRIPTION	MIN	TYP	MAX	UNIT
	$f_{clock(TELE\_CLK\_I)}$	Clock frequency, TELE_CLK_I (programmable clock source)†#				75	MHz
1	$t_{c(TELE\_CLK\_I)}$	Cycle time, TELE_CLK_I#		13.33			ns
2	$t_{w(TELE\_CLK\_I\_H)}$	Pulse duration, TELE_CLK_I high#		6			ns
3	$t_{w(TELE\_CLK\_I\_L)}$	Pulse duration, TELE_CLK_I low#		6			ns
	$f_{clock(HALF\_DSP\_CLK)}$	Clock frequency, 1/2 DSP_CLK (programmable clock source)#				62.5	MHz
4	$t_{c(HALF\_DSP\_CLK)}$	Cycle time, 1/2 DSP_CLK#		16			ns
5	$t_{w(HALF\_DSP\_CLK\_H)}$	Pulse duration, 1/2 DSP_CLK high#		7			ns
6	$t_{w(HALF\_DSP\_CLK\_L)}$	Pulse duration, 1/2 DSP_CLK low#		7			ns
	$f_{clock(TELE\_CLK\_O)}$	Clock frequency, TELE_CLK_O#				37.5	MHz
7	$t_{c(TELE\_CLK\_O)}$	Cycle time, TELE_CLK_O#		26.67			ns
				2	X‡	4096	CLK_1§
8	$t_{w(TELE\_CLK\_O\_H)}$	Pulse duration, TELE_CLK_O, high	When X is even#	1	$(X/2)_t$	2048	CLK_1
			When X is odd#		$((X/2)_t+1)$		
9	$t_{w(TELE\_CLK\_O\_L)}$	Pulse duration, TELE_CLK_O, low#		1	$(X/2)_t$	2048	CLK_1
10	$t_{w(TELE\_FS\_L)}$	Pulse duration, TELE_FS, low#		1		16,383	CLK_2¶
11	$t_{d(TELE\_FS)}$	Delay time, TELE_CLK_O↑ to TELE_FS↑/↓#		1		15	ns

† Programmable clock source: Either TELE_CLK_I or 1/2 DSP_CLK may become the clock source, dependent on the state of the DSP_TELE (PCM_CTRL_2) register.
‡ X: The total number of programmable clock source periods defined in the DSP_TELE (PCM_CTRL_1) register bits PCM_CLK_DIV. The value X is (PCM_CLK_DIV + 1), with zero invalid. In addition, the value $(X/2)_t$ is [1/2(PCM_CLK_DIV + 1)] truncated.
§ CLK_1: Clock periods based on the programmable clock source
¶ CLK_2: Clock periods based on TELE_CLK_O
# Specified by design

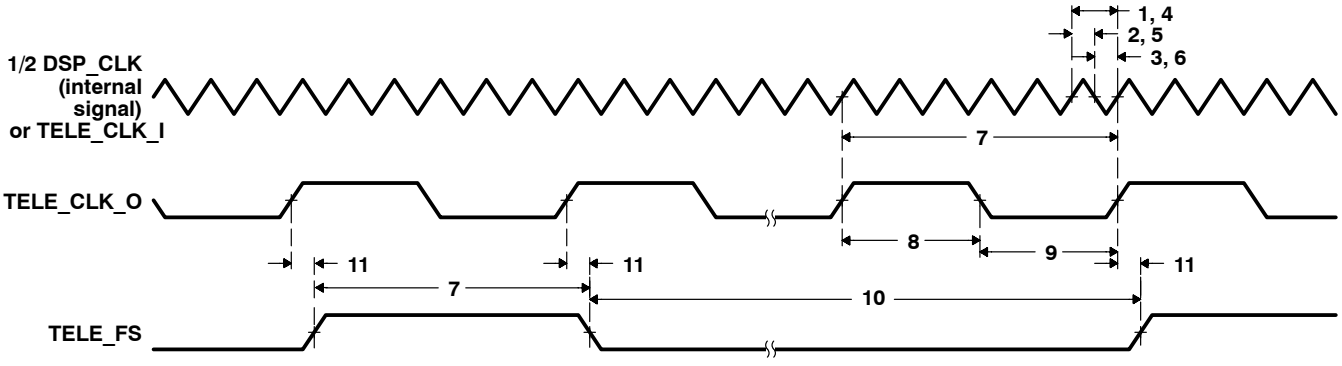


Figure 5–30. Line Codec Interface PCM

5.11.2 Serial Port

Figures 5−31 and 5−32 show a 4-bit serial data transfer, while valid data transfer sizes may be from 1 to 16 bits, dependent on the state of the DATA_LEN bits in the DSP_TELE (SERIAL_CTRL_1) register.

Table 5−30. Line Codec Interface Serial Port Timing (See Figures 5−31 and 5−32)

NO.	DESCRIPTION		MIN	TYP	MAX	UNIT
	$f_{clock(TELE\_DCLK)}$ Clock frequency, TELE_DCLK				31.25	MHz
1	$t_{c(TELE\_DCLK)}$ Cycle time, TELE_DCLK		32			ns
			2	X†	65,536	Clock‡
2	$t_{w(TELE\_DCLK\_H)}$ Pulse duration, TELE_DCLK high	When X is even	1	$(X/2)_t$	32,782	Clock
		When X is odd	1	$((X/2)_t+1)$	32,782	
3	$t_{w(TELE\_DCLK\_L)}$ Pulse duration, TELE_DCLK low		1	$(X/2)_t$	32,782	Clock
4	$t_{d(TELE\_DO\_D)}$ Delay time, TELE_DCLK↑ to TELE_DO valid (driven)		1		15	ns
5	$t_{d(TELE\_DO\_R)}$ Delay time, TELE_DCLK↑ to TELE_DO invaild (released)		1		15	ns
6	$t_{d(TELE\_DO\_V)}$ Delay time, TELE_DCLK↑ to TELE_DO data bit invalid		1		15	ns
7	$t_{d(TELE\_DI)1}$§ Delay time, TELE_DI valid to TELE_DCLK↑		8			ns
8	$t_{d(TELE\_DO)1}$§ Delay time, TELE_DO valid to TELE_DCLK↑		8			ns
9	$t_{d(TELE\_DI)2}$ Delay time, TELE_DI valid after TELE_DCLK↑ to TELE_DI invalid		4			ns
10	$t_{d(TELE\_DO)2}$ Delay time, TELE_DCLK↑ to TELE_DO invalid		4			ns
11	$t_{d(\overline{TELE\_CS\_A})}$ Delay time, TELE_DCLK↑ to $\overline{TELE\_CS}$↓		1		15	ns
12	$t_{d(\overline{TELE\_CS\_I})}$ Delay time, TELE_DCLK↑ to $\overline{TELE\_CS}$↑		1		15	ns
13	$t_{d(TELE\_DI\_ST)}$ Delay time, TELE_DCLK↑ to TELE_DI valid (read start)		1		15	ns
14	$t_{d(TELE\_DO\_ST)}$ Delay time, TELE_DCLK↑ to TELE_DO valid (read start)		1		15	ns
15	$t_{d(TELE\_DI\_SP)}$ Delay time, TELE_DCLK↑ to TELE_DI invalid (read stop)		1		15	ns
16	$t_{d(TELE\_DO\_SP)}$ Delay time, TELE_DCLK↑ to TELE_DO invalid (read stop)		1		15	ns

† X: The total number of 1/2 DSP_CLK clock divider values defined in the DSP_TELE (SERIAL_CTRL_1) register bits CLK_DIV. The value X is (CLK_DIV + 1), with zero invalid. In addition, the value $(X/2)_t$ is [1/2(CLK_DIV + 1)] truncated.

‡ Clock: One unit of clock period where the clock source is defined as 1/2 DSP_CLK

§ Bidirectional mode: The serial data input source on reads may be TELE_DI or TELE_DO, depending on the state of the D_MODE bit in the DSP_TELE (SERIAL_CTRL_1) register.

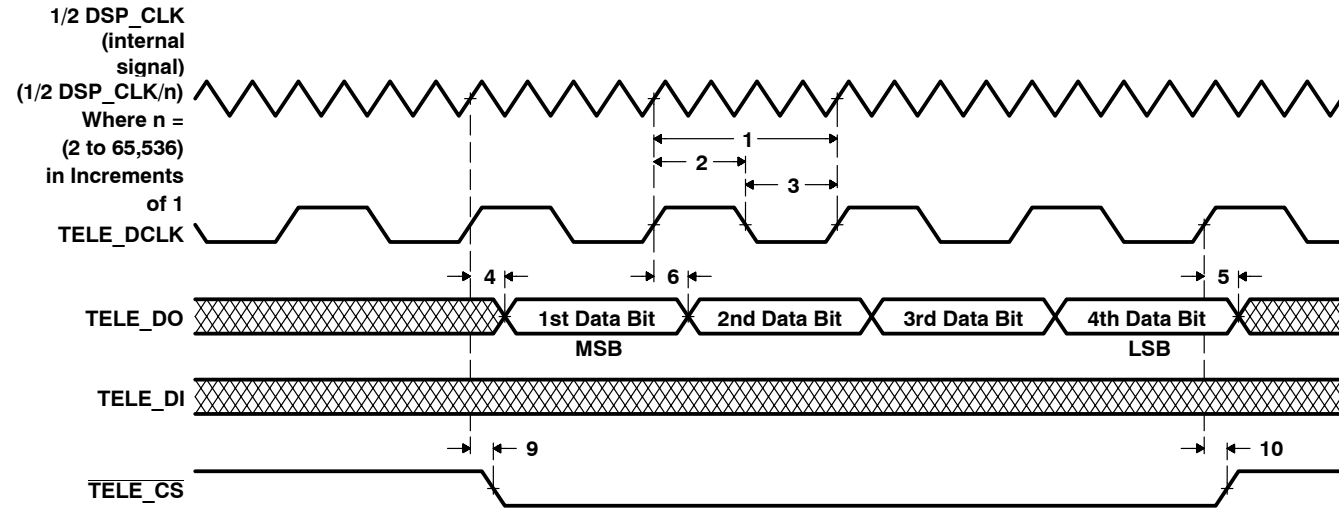


Figure 5–31. Line Codec Interface Serial Port Write

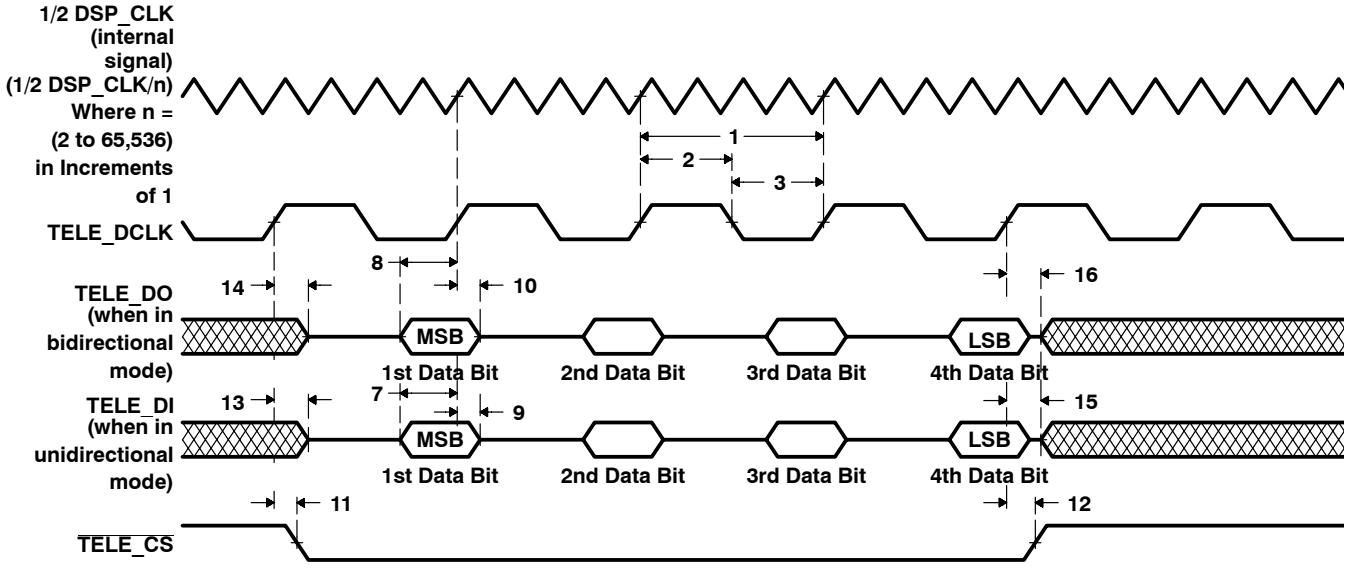


Figure 5–32. Line Codec Interface Serial Port Read

5.11.3 In

Table 5–31. Line Codec Interface Ring Timing (See Figure 5–33)†

NO.	DESCRIPTION		MIN	MAX	UNIT
1	$t_{w(RING\_PRESCALE\_CLK)}$	Pulse duration, ring prescale clock period	2	8192	CLK_1‡
2	$t_{w(RING\_CLK)}$	Pulse duration, ring clock one-half period	1	65,535	CLK_2§

† TELE_RINGIN1/TELE_RINGIN2/TELE_RINGIN3/TELE_RINGIN4 signals are enabled through DSP_TELE(RINGIN).
‡ CLK_1: One 1/2 DSP_CLK period
§ CLK_2: One ring prescalar clock period defined above. The ring prescalar clock is programmed through the universal timer register DSP_TELE (CTRL). The ring clock is programmed through the universal timer register DSP_TELE (LOAD), with a value larger than zero.

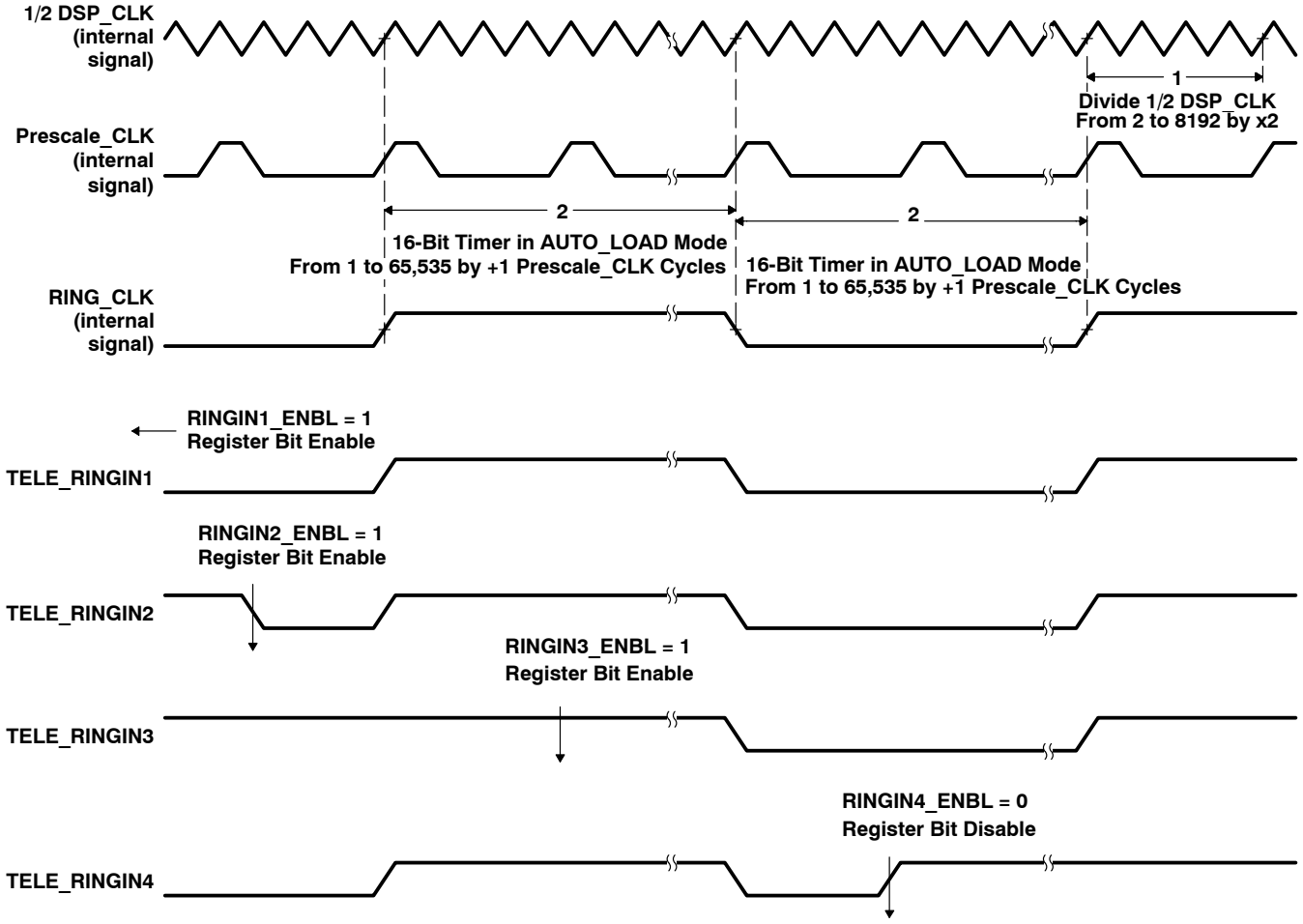


Figure 5–33. Line Codec Interface Ring

5.12 UART Interface Timing

Table 5–32. UART Timing (See Figure 5–34)†

NO.	DESCRIPTION		MIN	MAX	UNIT
	BAUD	BAUD rate‡§	1200	256000	BAUD
	$f_{clock(DIV\_CLK)}$	Clock frequency, DIV_CLK‡¶		82.5	MHz
1	$t_{c(DIV\_CLK)}$	Cycle time, divider clock‡	12.12		ns
2	$t_{d(UART\_TX\_P)}$	Delay time, UART_TX pause between stop and start UART_CTS transfers‡	$t_c \times 0$		ns
3	$t_{d(UART\_CTS\_I)}$	Delay time, UART_CTS↑ to middle of stop bit‡		16	ns
4	$t_{d(UART\_CTS\_A)}$	Delay time, UART_CTS↓ to UART_TX start bit↓‡		$t_c \times 25$	ns
5	$t_{d(UART\_RX\_P)}$	Delay time, UART_RX pause between stop and start UART_RTS transfers‡	$t_c \times 0$		ns
6	$t_{d(UART\_RTS\_I)}$	Delay time, middle of stop bit on UART_RX (RX_FIFO trigger active) to UART_RTS↑‡		$t_c \times 3$	ns
7	$t_{d(UART\_RTS\_A)}$	Delay time, RX FIFO trigger reset to UART_RTS↓‡		$t_c \times 4$	ns

† Auto flow: Through the UART (MODEM_CTRL) register, the UART may be set for auto flow. In auto-flow mode, the UART may transmit data on UART_TX whenever UART_CTS is active. In addition, the UART must be ready to receive data on UART_RX, as long as the UART is holding UART_RTS active.

‡ Specified by design

§ BAUD rate: BAUD rate is created from the DIV_CLK, further divided by the fixed value 16.

¶ Divider clock: This DIV_CLK value is created by dividing the VBUS_CLK frequency by the DLH and DLL values found in the UART (DIV_LATCH_LSB) and UART (DIV_LATCH_MSB) register set.

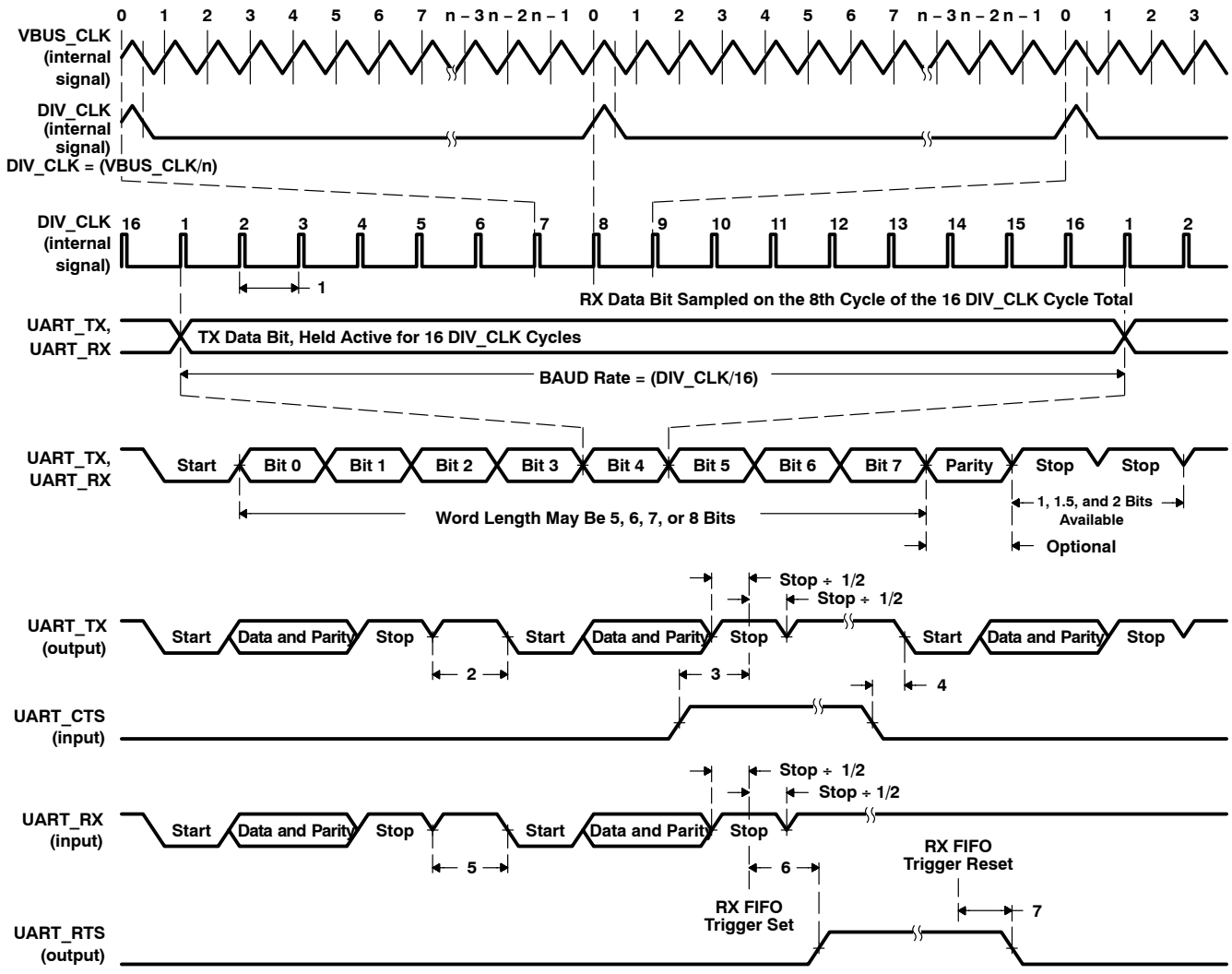


Figure 5–34. UART

5.13 LCD Interface Timing

5.13.1 LCD Interface Display Driver (LIDD Mode)

Each LIDD-mode chip select is provided with a control register that allows individual adjustment of the write timing parameters (W_SU, W_STROBE, and W_HOLD), read timing parameters (R_SU, R_STROBE, and R_HOLD), and chip select delay timing (CS_DELAY).

- E0 provided on LCD_BIAS_E0, register LCD (LIDD_CS0_CONFIG)
- E1 provided on LCD_E1, register LCD (LIDD_CS1_CONFIG)

Table 5–33. LCD LIDD Mode Timing (See Figures 5–35 Through 5–42)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(LIDD\_CLK)}$	Clock frequency, LIDD_CLK†		75	MHz
1	$t_{c(LIDD\_CLK)}$	Cycle time, LIDD_CLK	13.33		ns
2	$t_{w(LIDD\_CLK\_H)}$	Pulse duration, LIDD_CLK high	6		ns
3	$t_{w(LIDD\_CLK\_L)}$	Pulse duration, LIDD_CLK low	6		ns
4	$t_{d(LCD\_D\_V)}$	Delay time, LIDD_CLK↑ to LCD_D[15:0] valid (write)	1	7	ns
5	$t_{d(LCD\_D\_I)}$	Delay time, LIDD_CLK↑ to LCD_D[15:0] invalid (write)	1	7	ns
6	$t_{d(LCD\_E\_A)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_BIAS_E0 or LCD_E1↓‡	1	7	ns
7	$t_{d(LCD\_E\_I)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_BIAS_E0 or LCD_E1↑‡	1	7	ns
8	$t_{d(LCD\_A\_A)}$	Delay time, LIDD_CLK↑ to LCD_VSYNC_A↓	1	7	ns
9	$t_{d(LCD\_A\_I)}$	Delay time, LIDD_CLK↑ to LCD_VSYNC_A↑	1	7	ns
10	$t_{d(LCD\_W\_A)}$	Delay time, LIDD_CLK↑ to $\overline{\text{LCD\_HSYNC\_W}}$↓	1	7	ns
11	$t_{d(LCD\_W\_I)}$	Delay time, LIDD_CLK↑ to $\overline{\text{LCD\_HSYNC\_W}}$↑	1	7	ns
12	$t_{d(LCD\_STRB\_A)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_PIXEL_STRB↑	1	7	ns
13	$t_{d(LCD\_STRB\_I)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_PIXEL_STRB↓	1	7	ns
14	$t_{d(LCD\_D\_Z)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_D[15:0] in 3-state Z	1	7	ns
15	$t_{d(Z\_LCD\_D)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_D[15:0] (valid from 3-state Z)	1	7	ns
16	$t_{su(LCD\_D)}$	Setup time, LCD_D[15:0] valid before LIDD_CLK (LCD_E1)↑	7		ns
17	$t_{h(LCD\_D)}$	Hold time, LCD_D[15:0] valid after LIDD_CLK (LCD_E1)↑	2		ns

† The LIDD clock is available on LCD_E1 when operating the LIDD in 6800 synchronous mode and 8080 synchronous mode, but is not available externally in HD44780 mode. LIDD mode selects are provided in the LCD (LIDD_CTRL) register.

‡ Control signal polarity: The active polarity of the control signals (LCD_BIAS_E0, LCD_E1, LCD_VSYNC_A, $\overline{\text{LCD\_HSYNC\_W}}$, and LCD_PIXEL_STRB) is individually programmable in LIDD mode through the LCD (LIDD_CTRL) register.

5.13.1.1 HD44780 Write

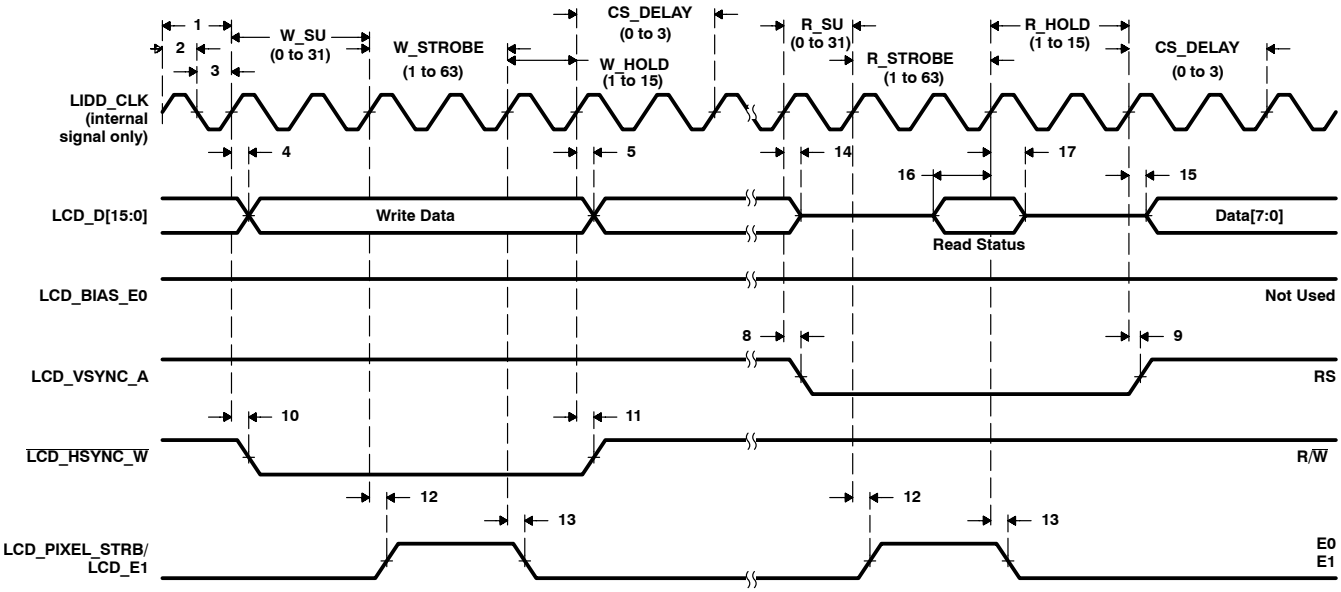


Figure 5–35. Character Display HD44780 Write

5.13.1.2 HD44780 Read

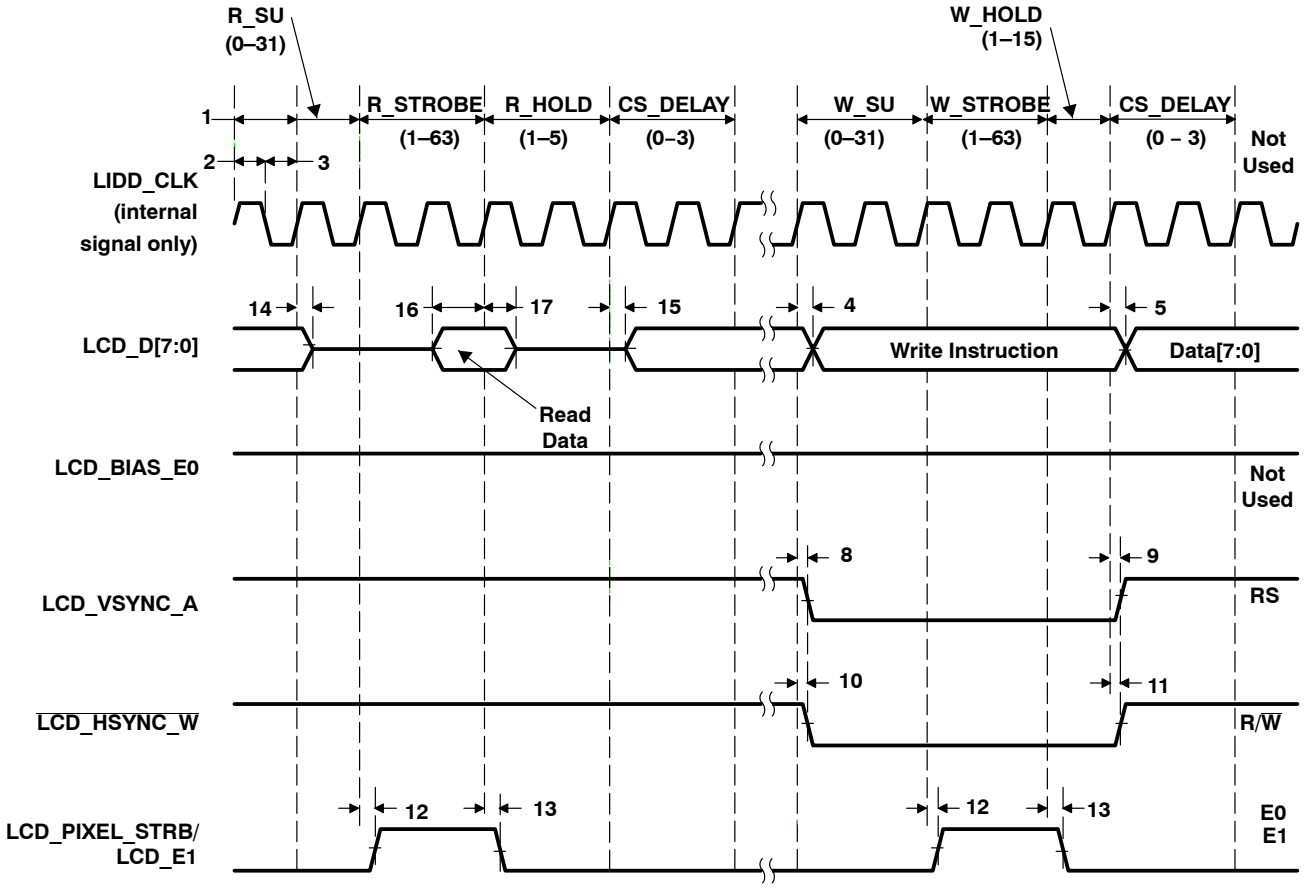


Figure 5–36. Character Display HD44780 Read

5.13.1.3 6800 Write

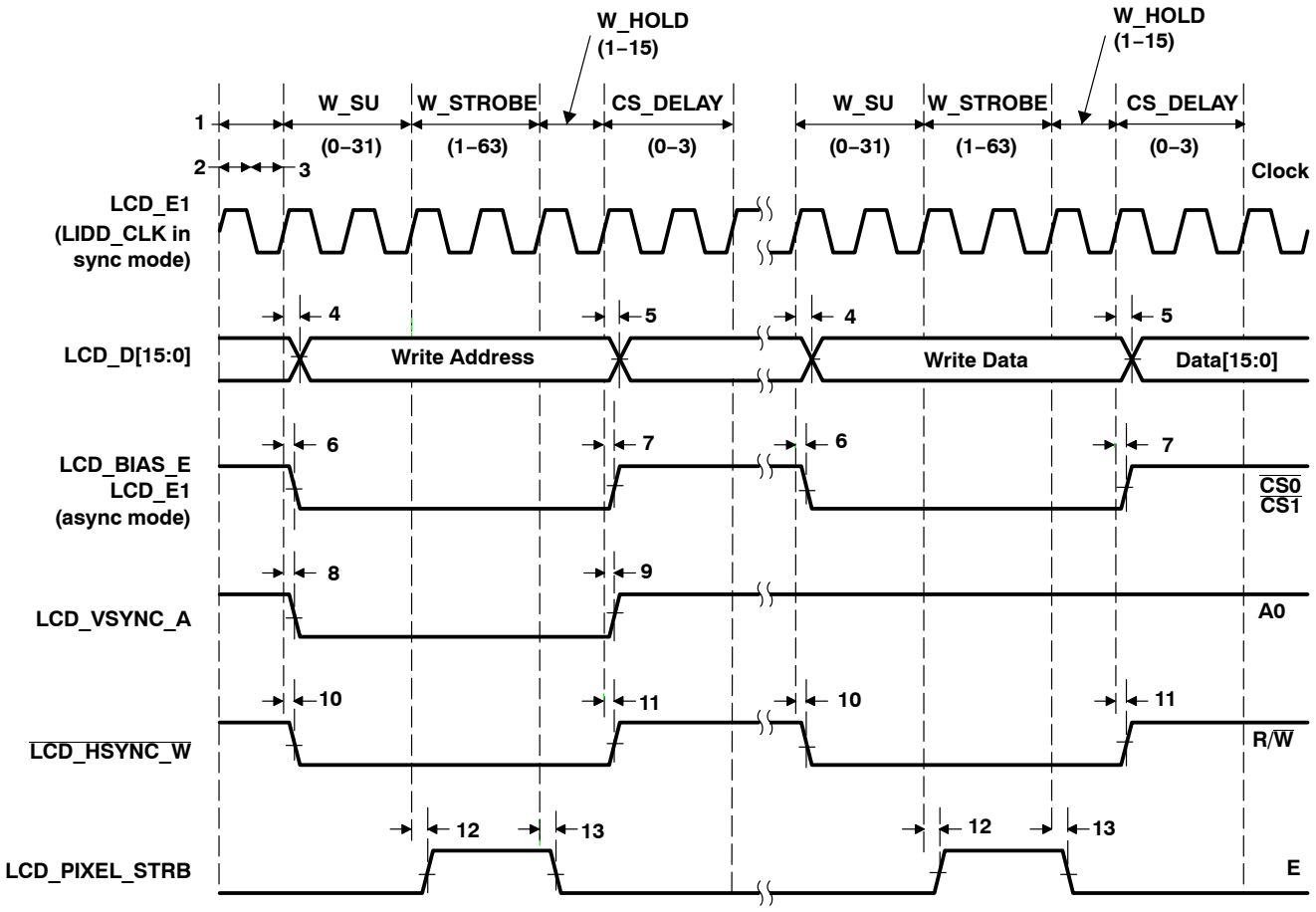


Figure 5–37. Micro-Interface Graphic Display 6800 Write

5.13.1.4 6800 Read

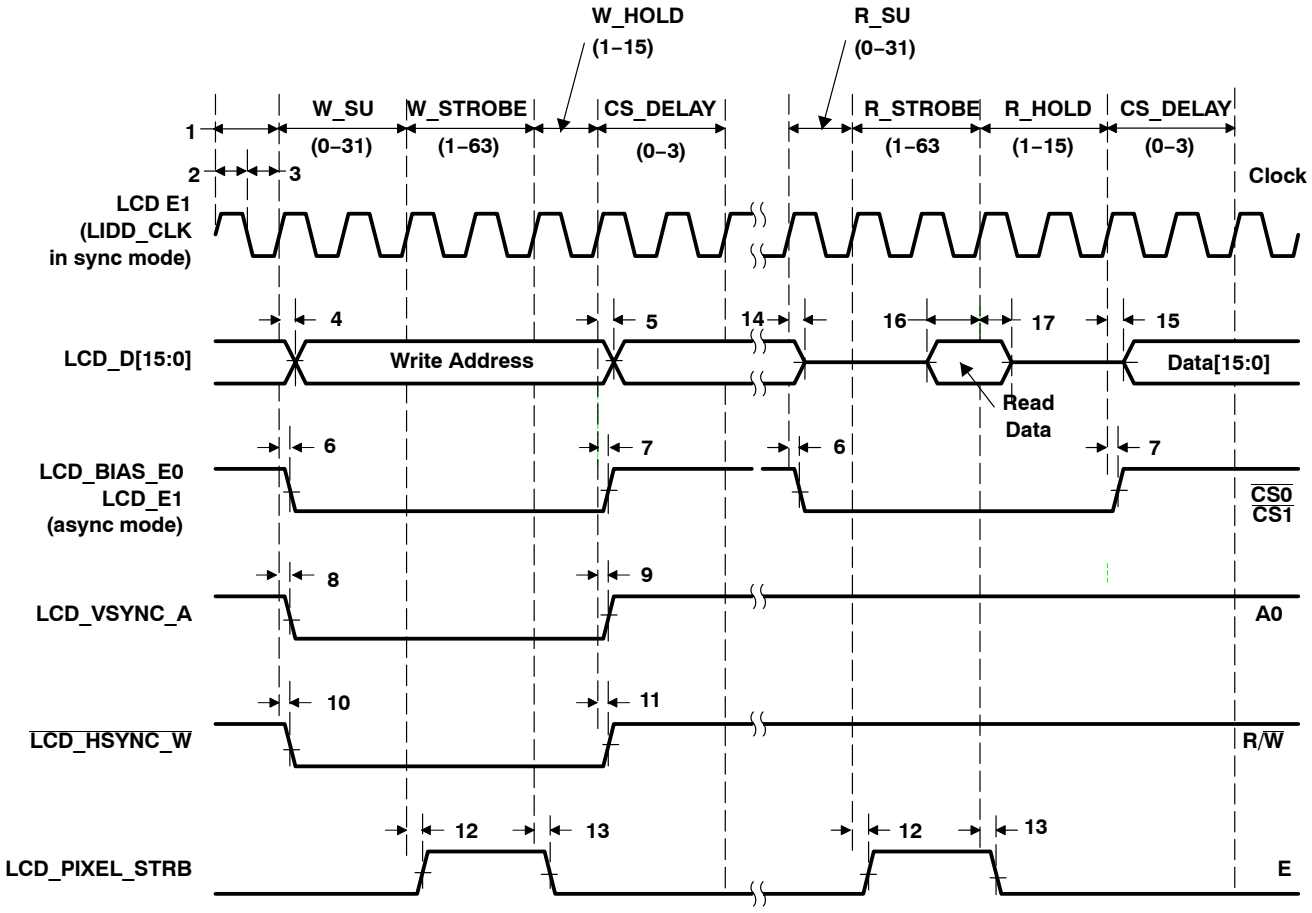


Figure 5–38. Micro-Interface Graphic Display 6800 Read

5.13.1.5 6800 Status

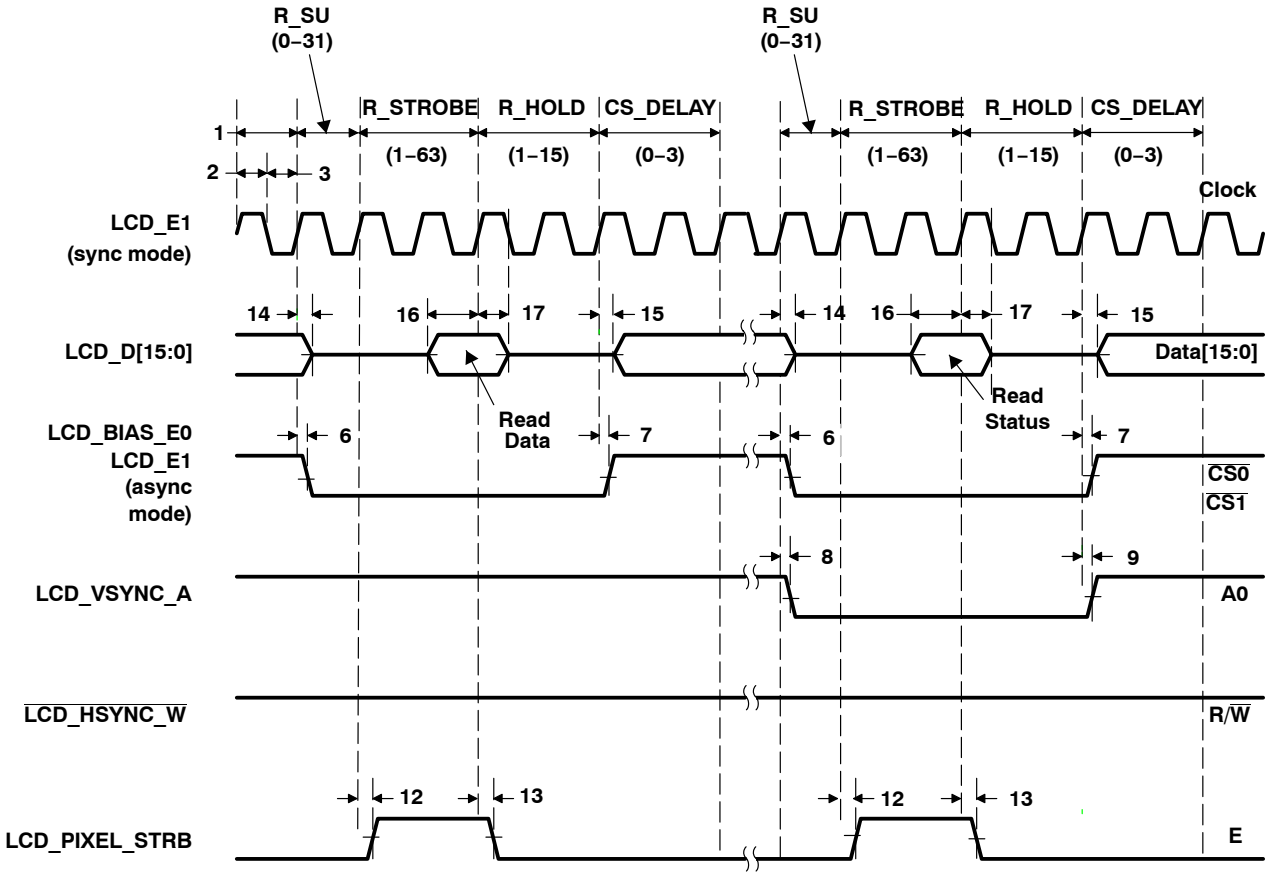


Figure 5–39. Micro-Interface Graphic Display 6800 Status

5.13.1.6 8080 Write

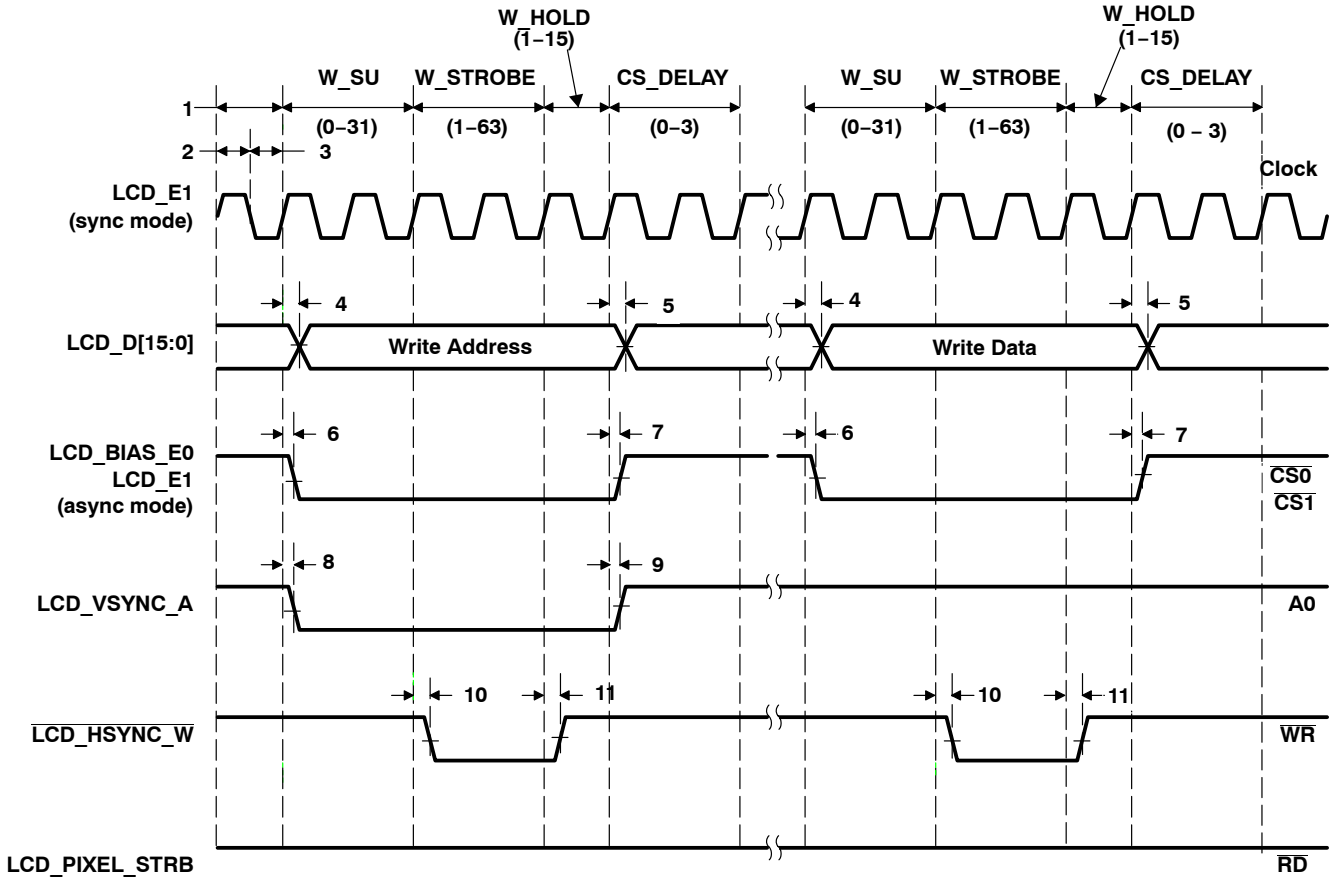


Figure 5–40. Micro-Interface Graphic Display 8080 Write

5.13.1.7 8080 Read

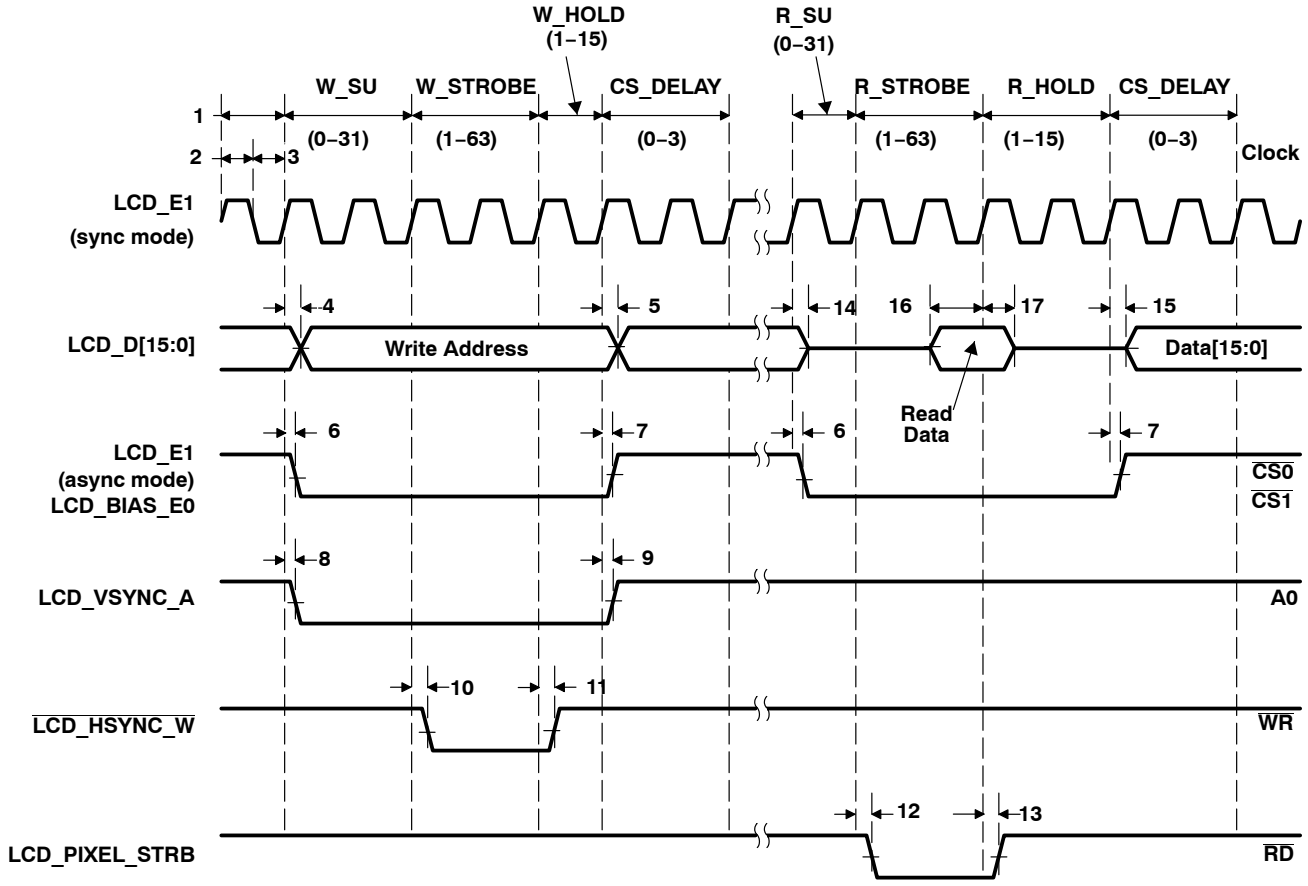


Figure 5–41. Micro-Interface Graphic Display 8080 Read

5.13.1.8 8080 Status

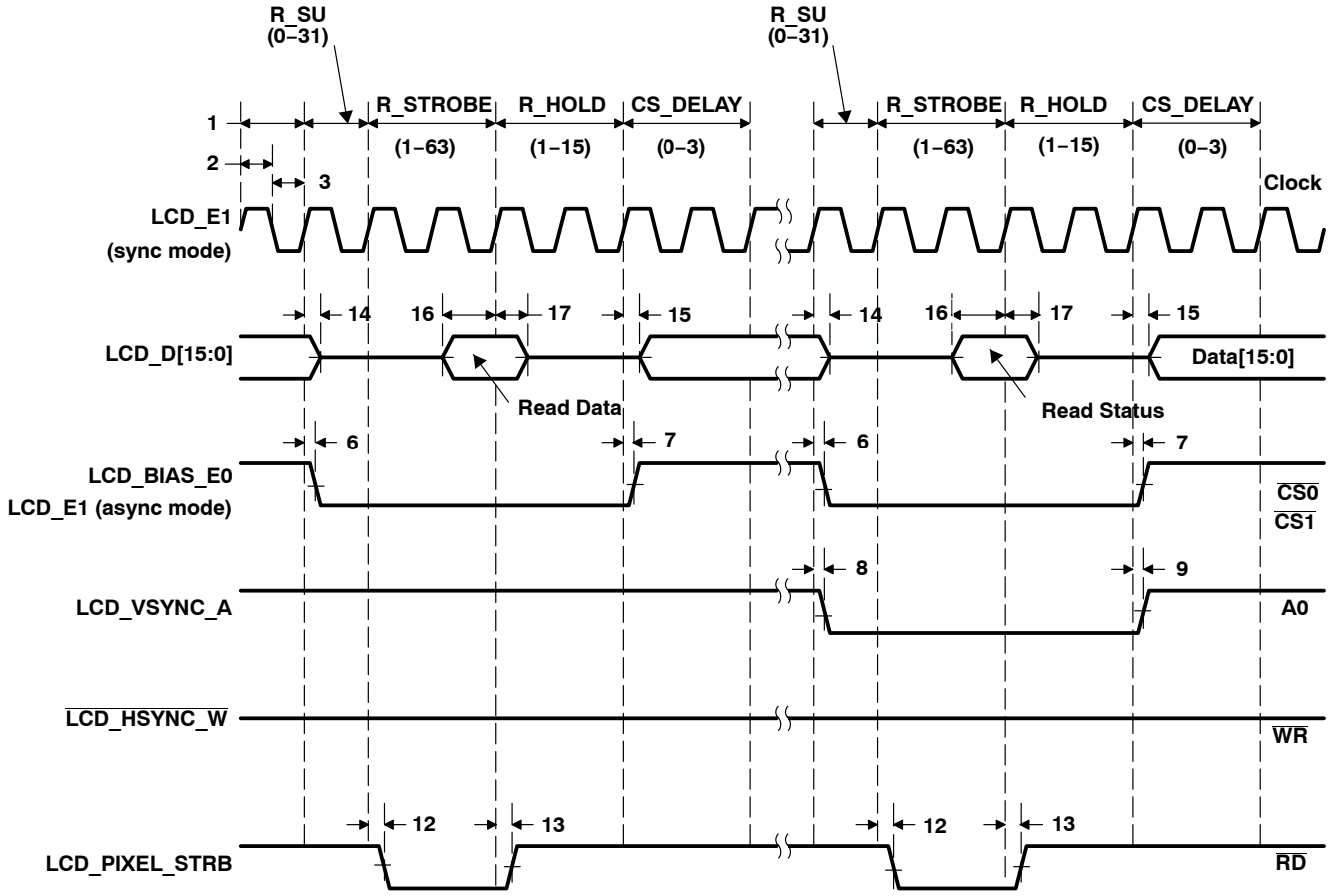


Figure 5–42. Micro-Interface Graphic Display 8080 Status

5.13.2 Raster Mode

Table 5–34. LCD Raster Mode Timing (See Figures 5–43 Through 5–47)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(PIXEL\_CLK)}$	Clock frequency, pixel clock†		37.5	MHz
1	$t_{c(PIXEL\_CLK)}$	Cycle time, pixel clock	26.67		ns
2	$t_{w(PIXEL\_CLK\_H)}$	Pulse duration, pixel clock high‡	10		ns
3	$t_{w(PIXEL\_CLK\_L)}$	Pulse duration, pixel clock low	10		ns
4	$t_{d(LCD\_D\_V)}$	Delay time, LCD_PIXEL_STRB↑ to LCD_D[15:0] valid (write)§	1	7	ns
5	$t_{d(LCD\_D\_IV)}$	Delay time, LCD_PIXEL_STRB↑ to LCD_D[15:0] invalid (write)	1	7	ns
6	$t_{d(LCD\_BIAS\_A)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_BIAS_E0↑	1	7	ns
7	$t_{d(LCD\_BIAS\_I)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_BIAS_E0↓	1	7	ns
8	$t_{d(LCD\_VSYNC\_A)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_VSYNC_A↑	1	7	ns
9	$t_{d(LCD\_VSYNC\_I)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_VSYNC_A↓	1	7	ns
10	$t_{d(LCD\_HSYNC\_A)}$	Delay time, LCD_PIXEL_STRB↑ to $\overline{\text{LCD\_HSYNC\_W}}$↑	1	7	ns
11	$t_{d(LCD\_HSYNC\_I)}$	Delay time, LCD_PIXEL_STRB↑ to $\overline{\text{LCD\_HSYNC\_W}}$↓	1	7	ns

† The pixel clock always is available on LCD_PIXEL_STRB. In addition, the polarity of this clock may be inverted while in raster mode, producing timing delay from the opposite edge of the clock. This may be accomplished through the LCD (RASTER_TIMING_2) register.

‡ The active polarity of the control signals (LCD_BIAS_E0, LCD_VSYNC_A, and $\overline{\text{LCD\_HSYNC\_W}}$) is individually programmable in raster mode through the LCD (RASTER_TIMING_2) register.

§ The activation edge of the control signals LCD_VSYNC_A and $\overline{\text{LCD\_HSYNC\_W}}$ may be programmed to either the rising or falling edge of the pixel clock through the LCD (RASTER_TIMING_2) register. In Figures 5–43 through 5–47, all signal polarity and activation edges are based on the default LCD (RASTER_TIMING_2) register settings.

Frame-to-frame timing is derived through the following parameters in the LCD (RASTER_TIMING_1) register:

- Vertical front porch (VFP)
- Vertical sync pulse width (VSW)
- Vertical back porch (VBP)
- Lines per panel (LPP)

Line-to-line timing is derived through the following parameters in the LCD (RASTER_TIMING_0) register:

- Horizontal front porch (HFP)
- Horizontal sync pulse width (HSW)
- Horizontal back porch (HBP)
- Pixels per panel (PPL)

LCD_BIAS_E0 timing is derived through the following parameter in the LCD (RASTER_TIMING_2) register:

- AC bias frequency (ACB)

5.13.2.1 LCD Format

The display format produced in raster mode is shown in Figure 5–43. An entire frame is delivered one line at a time. The first line delivered starts at data pixel (1, 1) and ends at data pixel (P, 1). The last line delivered starts at data pixel (1, L) and ends at data pixel (P, L). The beginning of each new frame is denoted by the activation of I/O signal LCD_VSYNC_A. The beginning of each new line is denoted by the activation of I/O signal $\overline{\text{LCD\_HSYNC\_W}}$.

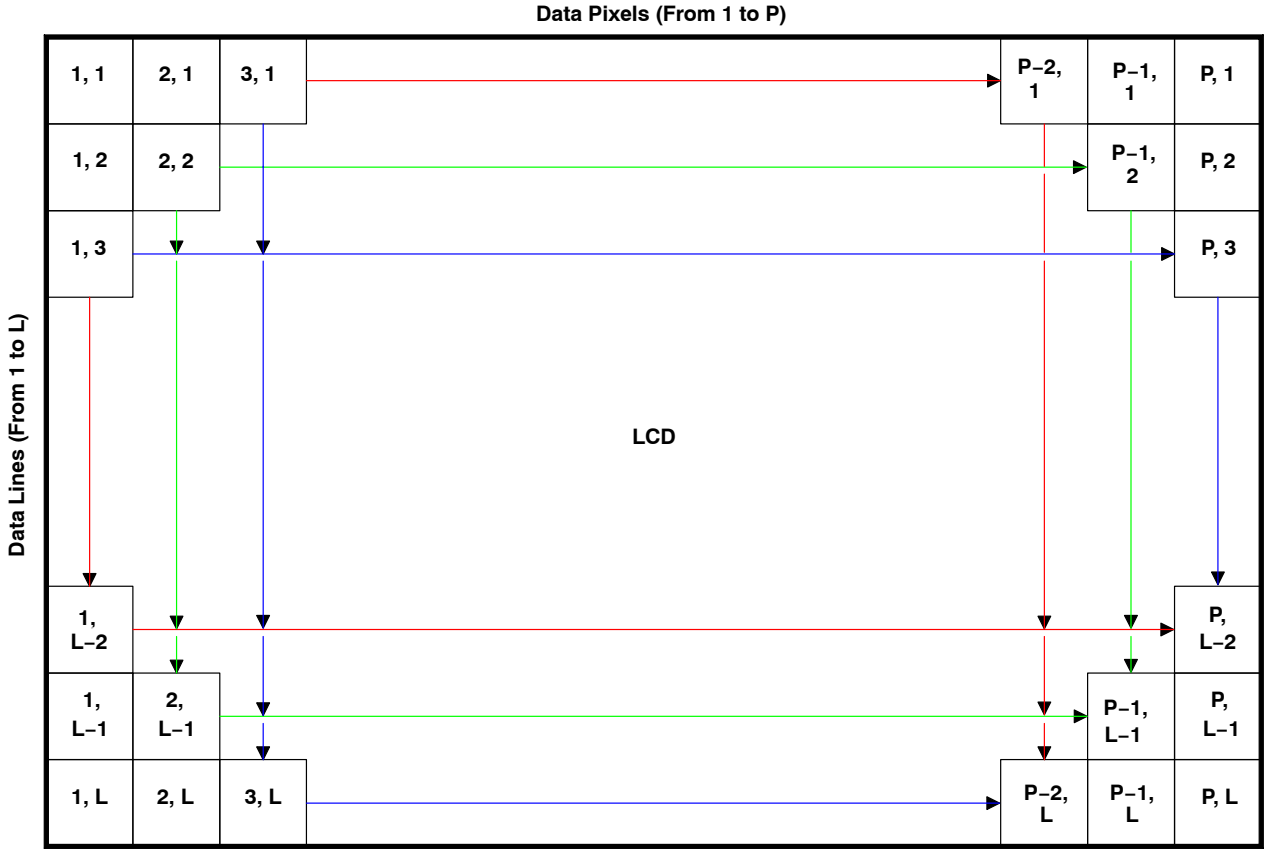


Figure 5–43. LCD Raster-Mode Display Format

5.13.2.2 Active Mode

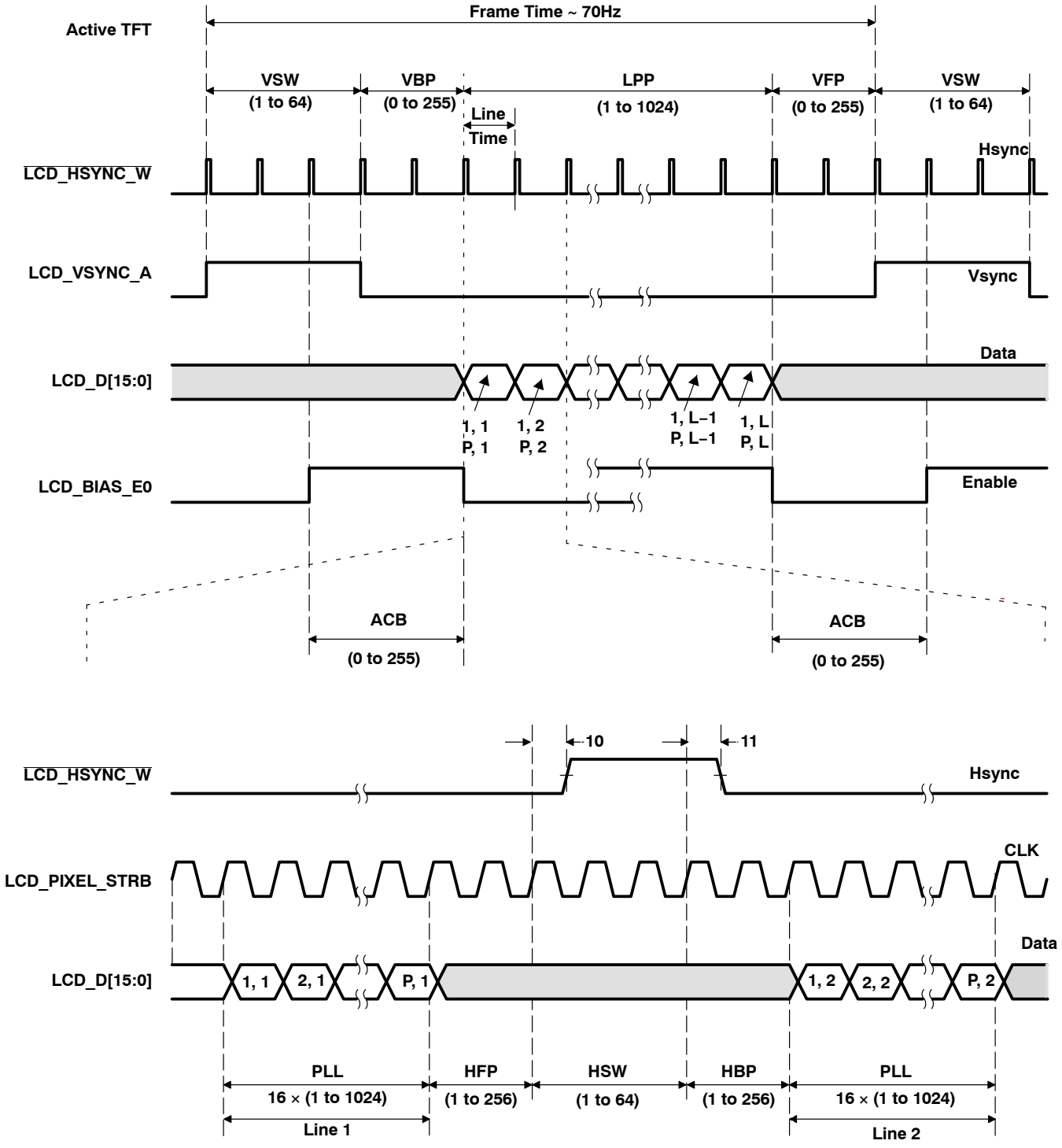


Figure 5–44. LCD Raster-Mode Active

5.13.2.3 Passive Mode

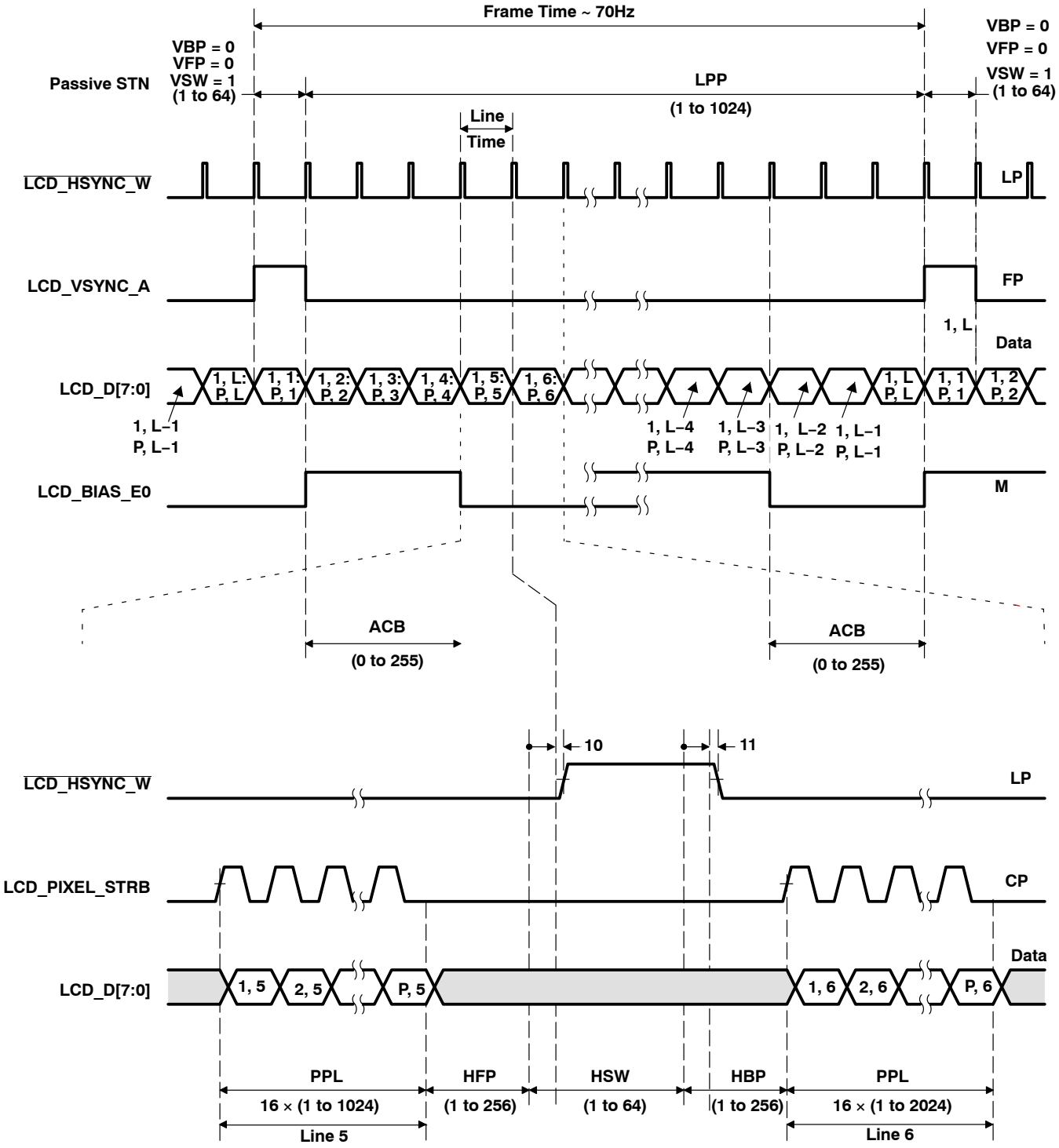


Figure 5–45. LCD Raster-Mode Passive

5.13.2.4 Control Activation

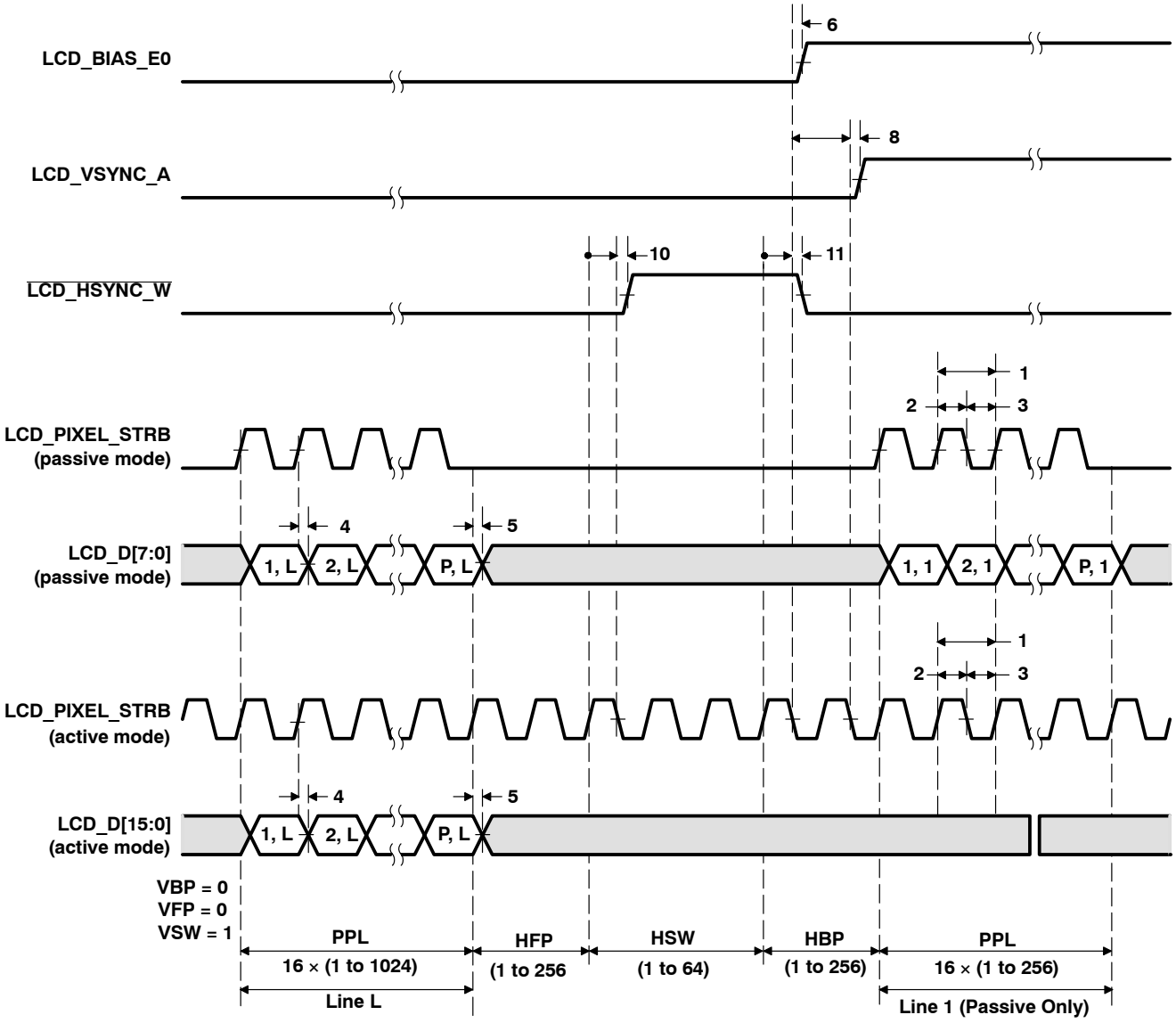


Figure 5–46. LCD Raster-Mode Control Signal Activation

5.13.2.5 Control Deactivation

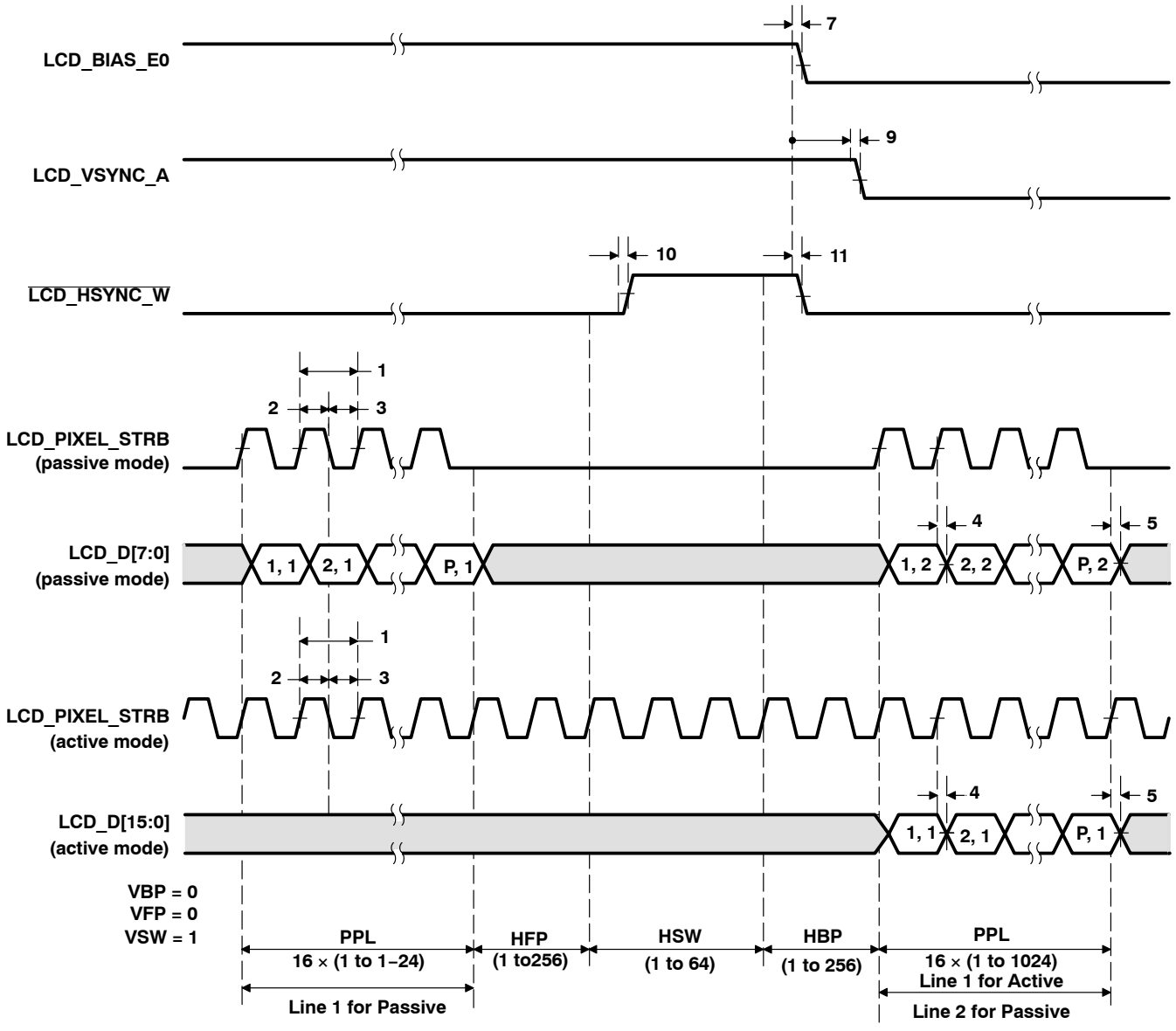


Figure 5–47. LCD Raster-Mode Control Signal Deactivation

5.14 Sequencer Serial Port (SSP) Timing

The SSP unit contains two flexible sequencer engines and five control signals to support a wide variety of serial interfaces. In the following timing diagrams, a simple serial port interface (SPI) is chosen to present the SSP timing. The timing defined by the SPI is identical to any other serial interface type. In addition, the signals SSPx, SSPy, and SSPz may be individually configured to be any one of the five control signals (SSP0, SSP1, SSP2, SSP3, or SSP4).

Table 5–35. SSP Timing (See Figures 5–48 Through 5–51)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(SSP\_CLK)}$	Clock frequency, SSP_CLK†		41.25	MHz
1	$t_{c(SSP\_CLK)}$	Cycle time, SSP_CLK	24.24		ns
2	$t_{w(SSP\_CLK\_H)}$	Pulse duration, SSP_CLK high	12		ns
3	$t_{w(SSP\_CLK\_L)}$	Pulse duration, SSP_CLK low	12		ns
4	$t_{d(SSP\_D\_D)}$	Delay time, SSP_CLK↑↓ to data drive (to valid)‡	1	9	ns
5	$t_{d(SSP\_D\_R)}$	Delay time, SSP_CLK↓ to data release (to invalid)‡	1	9	ns
6	$t_{d(SSP\_DO)}$	Delay time, SSP_CLK↓ to data bit shift out valid‡	1	9	ns
7	$t_{d(SSP\_DI)}$	Delay time, data bit shift in before SSP_CLK↓§	1	9	ns
8	$t_{d(SSP\_DI)}$	Delay time, SSP_CLK↓ to 3-state Z§	1	9	ns
9	$t_{d(SSP\_E\_A)}$	Delay time, SSP_CLK↑ to SSPz↓	8		ns
10	$t_{d(SSP\_E\_I)}$	Delay time, SSP_CLK↑ to SSPz↑	4		ns

† This internal clock signal drives the SSP engine and is created from the VBUS_CLK after being divided by two clock dividers. External visibility of this clock signal is dependent on the sequencer program.

‡ The serial data exiting the TNETV1060 may be configured to delay one VBUS_CLK cycle (see Figure 5–50) through the DELAY_OUT control bit in either the SSP (CONFIG_1_PORT_0) or SSP (CONFIG_1_PORT_1) register.

§ The serial data entering the TNETV1060 may be configured to load into the deserializer 1/2 SSP_CLK cycle early (see Figure 5–51) through the EARLY_IN control bit in either the SSP (CONFIG_1_PORT_0) or SSP (CONFIG_1_PORT_1) register.

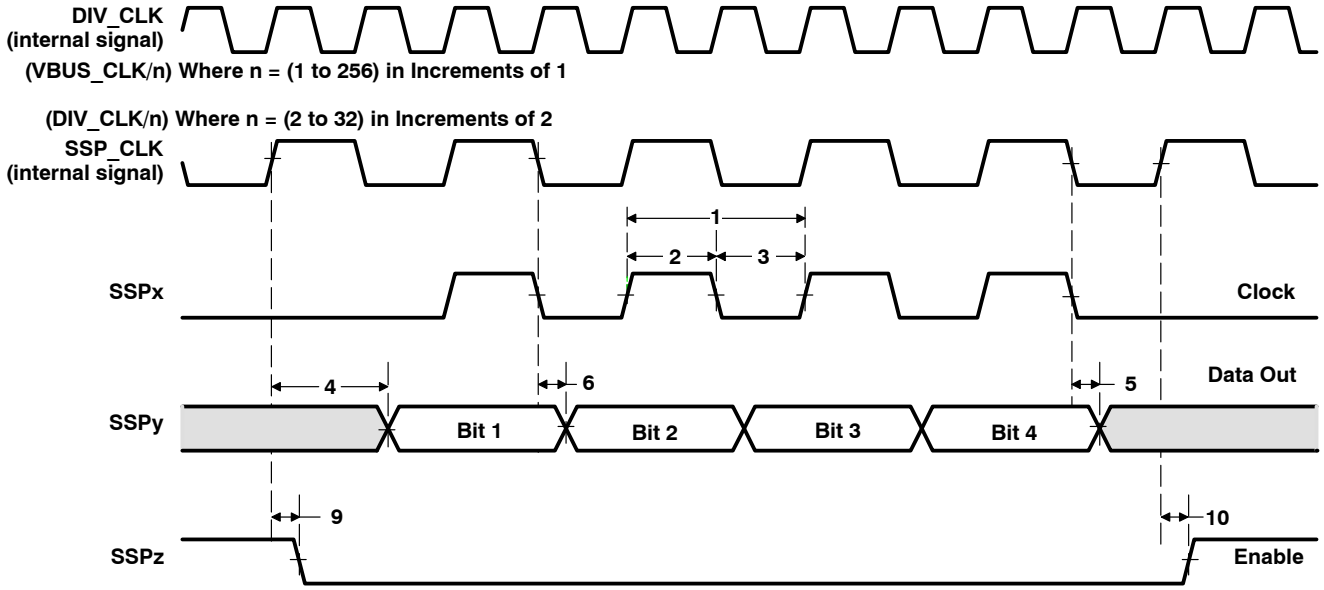


Figure 5–48. Serial Port Data Out

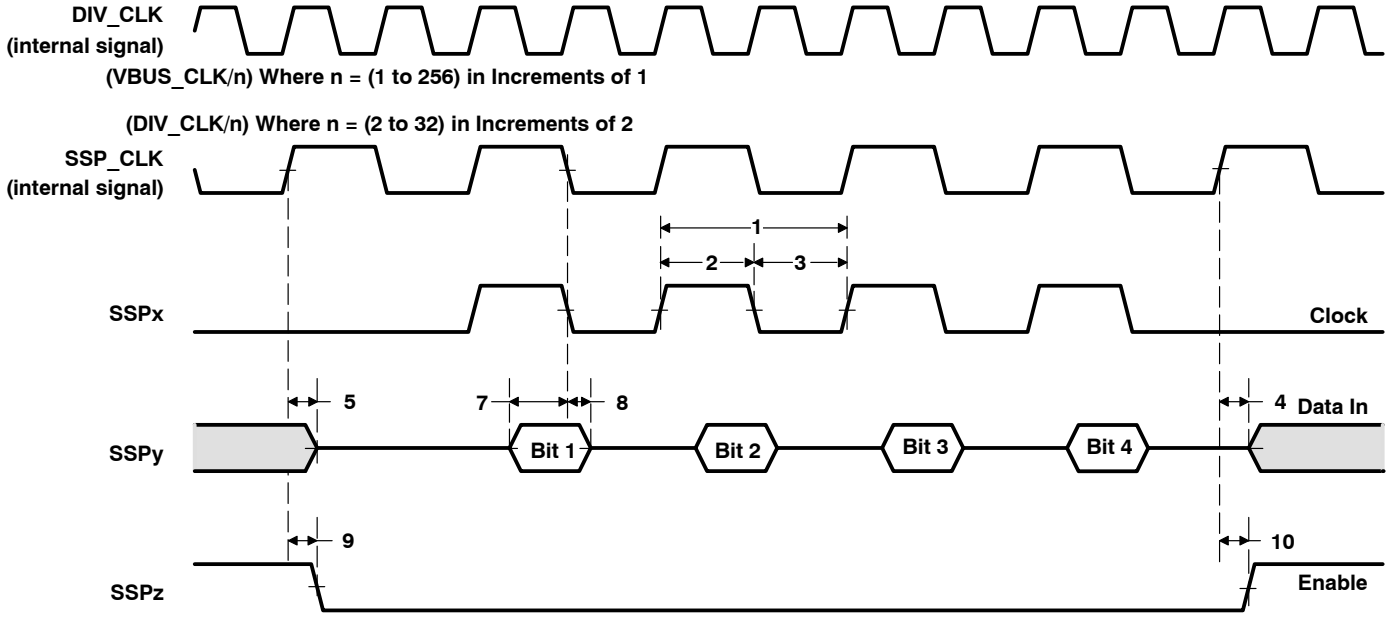


Figure 5–49. Serial Port Data In

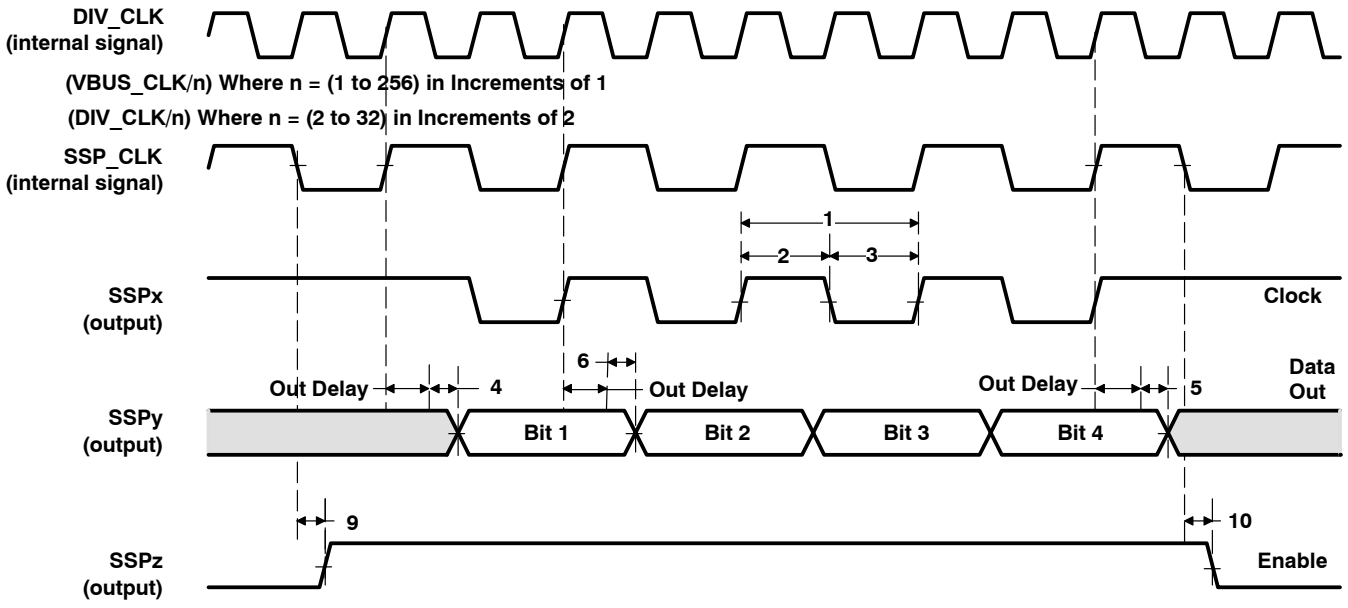


Figure 5–50. Serial Port Data Out Delay

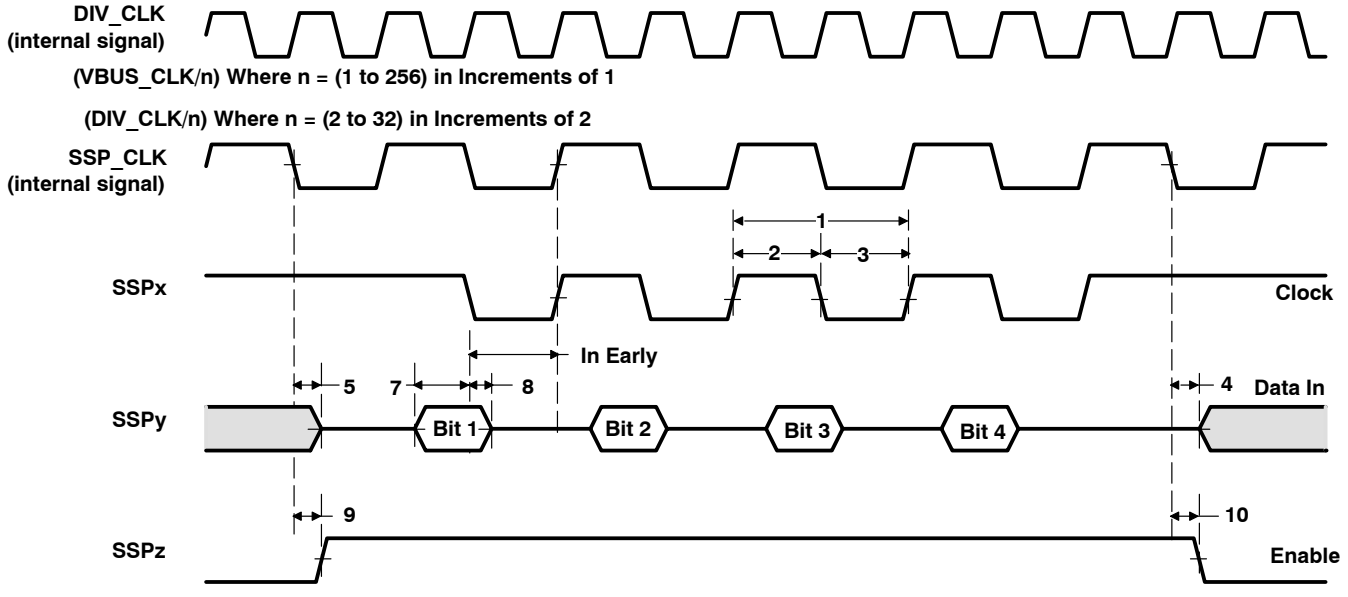


Figure 5–51. Serial Port Data In Early

5.15 VLYNQ™ Interface Timing

There is one five-terminal VLYNQ unit within the TNETV1060.

Table 5–36. VLYNQ Timing Requirements (See Figure 5–52)†‡

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(VLYNQ\_CLK)}$	Clock frequency, VLYNQ_CLK		62.5	MHz
1	$t_{c(VLYNQ\_CLK)}$	Cycle time, VLYNQ_CLK (input mode)	16		ns
2	$t_{w(VLYNQ\_CLK\_H)}$	Pulse duration, VLYNQ_CLK high (input mode)§	3.6		ns
3	$t_{w(VLYNQ\_CLK\_L)}$	Pulse duration, VLYNQ_CLK low (input mode)§	3.6		ns
4	$t_{r(VRCKR)}$	Rise time, RX_D and VYLNQ_CLK (input mode)§		3	ns
5	$t_{f(VRCKF)}$	Fall time, RX_D and VYLNQ_CLK (input mode)§		3	ns
6	$t_{d(VRV-VCKH)}$	Delay time, VLYNQ5_RX_D[1:0] valid to VLYNQ_CLK	1		ns
7	$t_{d(VCKH-VRV)}$	Delay time, VLYNQ_CLK to VLYNQ5_RX_D[1:0]	2		ns

† The VLYNQ clock can be sourced internally or externally through the configuration bit CLK_DIR in the VLYNQ5 (CTRL) register. If sourced internally, this clock is based on the VBUSP_CLK.

‡ See section 4 of Texas Instruments application report SPRA956, *Circuit-Board Design Guidelines for VLYNQ™ Devices,* to determine how to analyze VLYNQ timing.

§ Specified by design

Table 5–37. VLYNQ Switching Characteristics (See Figure 5–52)†‡

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(VLYNQ\_CLK)}$	Clock frequency, VLYNQ_CLK		62.5	MHz
1	$t_{c(VLYNQ\_CLK)}$	Cycle time, VLYNQ_CLK (output mode)	16		ns
	$t_{j(VLYNQ\_CLK)}$	Cycle to cycle jitter, VLYNQ_CLK (output mode)§		250	ps
2	$t_{w(VLYNQ\_CLK\_H)}$	Pulse duration, VLYNQ_CLK high (output mode)§	3.6		ns
3	$t_{w(VLYNQ\_CLK\_L)}$	Pulse duration, VLYNQ_CLK low (output mode)§	3.6		ns
8	$t_{r(VTCKR)}$	Rise time, TX_D and VYLNQ_CLK (output mode)§		3	ns
9	$t_{f(VTCKF)}$	Fall time, TX_D and VYLNQ_CLK (output mode)§		3	ns
10	$t_{d(VCKH-VTH)}$	Delay time, VLYNQ_CLK to VLYNQ5_TX_D[1:0] invalid	2		ns
11	$t_{d(VCKH-VTV)}$	Delay time, VLYNQ_CLK to VLYNQ5_TX_D[1:0] valid		7.55	ns

† The VLYNQ clock can be sourced internally or externally through the configuration bit CLK_DIR in the VLYNQ5 (CTRL) register. If sourced internally, this clock is based on the VBUSP_CLK.

‡ See section 4 of Texas Instruments application report SPRA956, *Circuit-Board Design Guidelines for VLYNQ™ Devices,* to determine how to analyze VLYNQ timing.

§ Specified by design

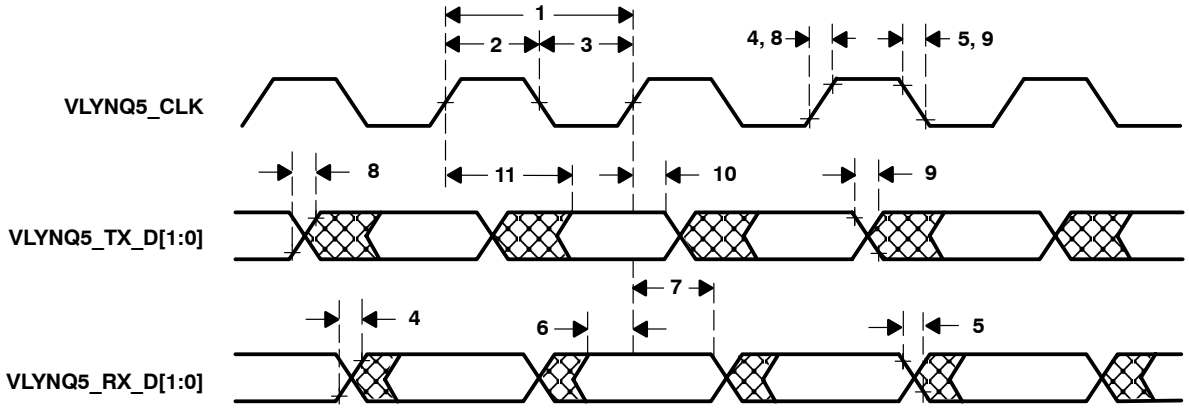


Figure 5–52. VLYNQ Interface

cmd1[7:4] pkttype	cmd1[3:0] adrmsk	cmd2[7:0]	bytecnt[7:0] (1 to 64)d	
0x 0	0x F	not used	USED	Write
0x 1	0x F	not used	USED	Write with Address Increment
0x 2	X	not used	not used	Reserved
0x 3	0x F	not used	not used	Write 32-bit Word with Address Increment
0x 4	0x F	not used	USED	Configuration Write
0x 5	0x F	not used	USED	Configuration Write with Address Increment
0x 6	X	X	X	Reserved for extended command (cmd2)
0x 7	0x F	not used	not used	Interrupt
0x 8	0x F	not used	USED	Read
0x 9	0x F	not used	USED	Read with Address Increment
0x A	X	not used	not used	Reserved
0x B	0x F	not used	not used	Read 32-bit Word with Address Increment
0x C	0x F	not used	USED	Configuration Read
0x D	0x F	not used	USED	Configuration Read with Address Increment
0x E	0x F	not used	USED	Read Response

	Code	8-bit	10-bit-	10-bit+
Flow Control Enable	/P/	0x 1C	0x 0F4	0x 30B
Error Indication	/E/	0x 3C	0x 0F9	0x 306
Flow Control Disable	/C/	0x 5C	0x 0F5	0x 30A
Flowed	/F/	0x 7C	0x 0F3	0x 30C
Initialization 0	/0/	0x 9C	0x 0F2	0x 30D
Idle	/I/	0x BC	0x 0FA	0x 305
Initialization 1	/1/	0x DC	0x 0F6	0x 309
		0x FC	0x 0F8	0x 307
Byte Disable	/M/	0x F7	0x 3A8	0x 057
Start of Packet	/S/	0x FB	0x 368	0x 097
End of Packet	/T/	0x FD	0x 2E8	0x 117
Link	/L/	0x FE	0x 1E8	0x 217

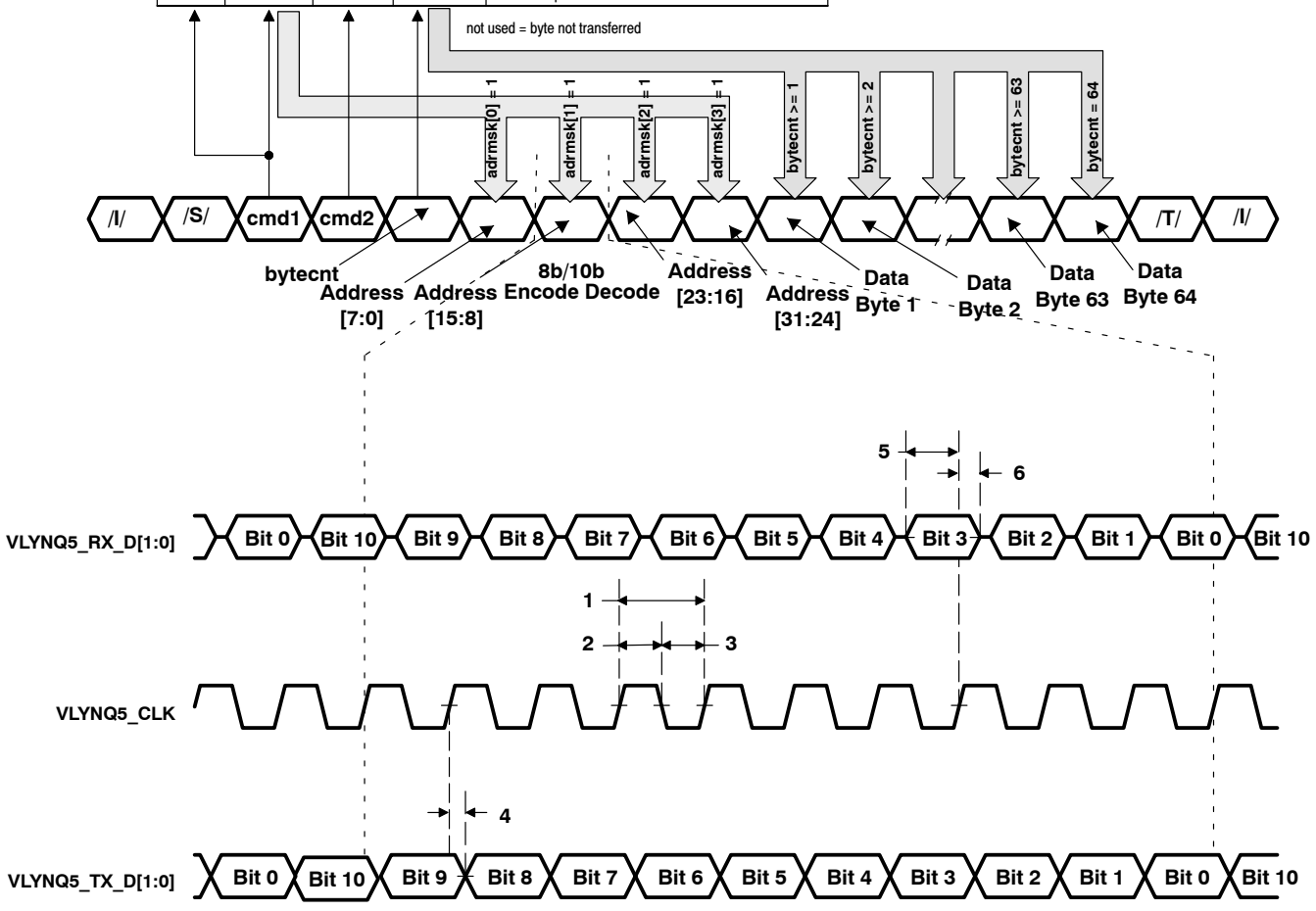


Figure 5–53. VLYNQ Interface (Five Terminal)

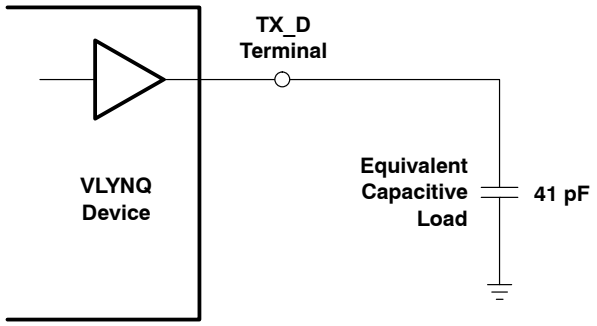


Figure 5–54. Equivalent Load Circuit

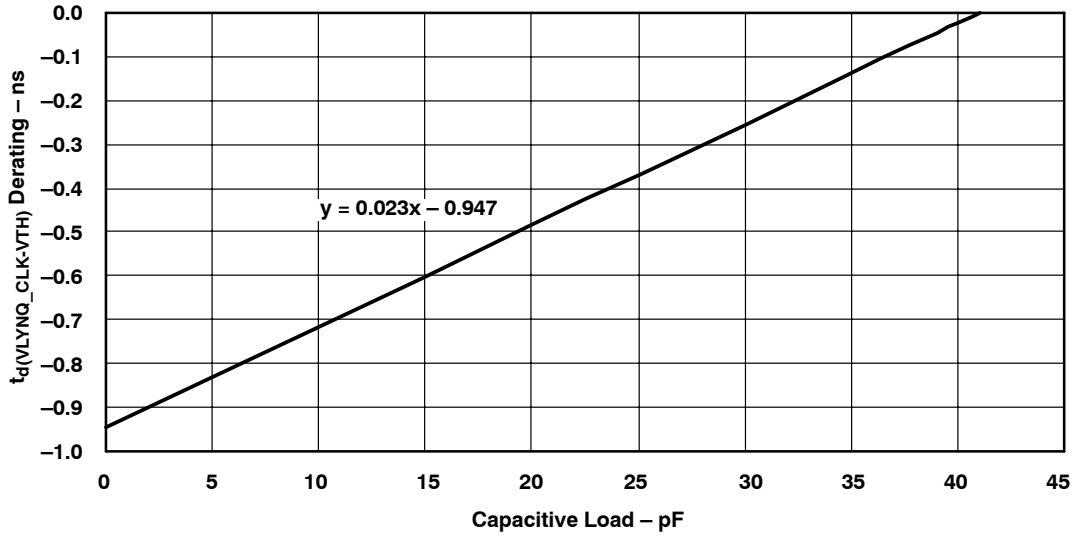


Figure 5–55. Derating Curve for $t_{d(VLYNQ\_CLK-VTH)}$

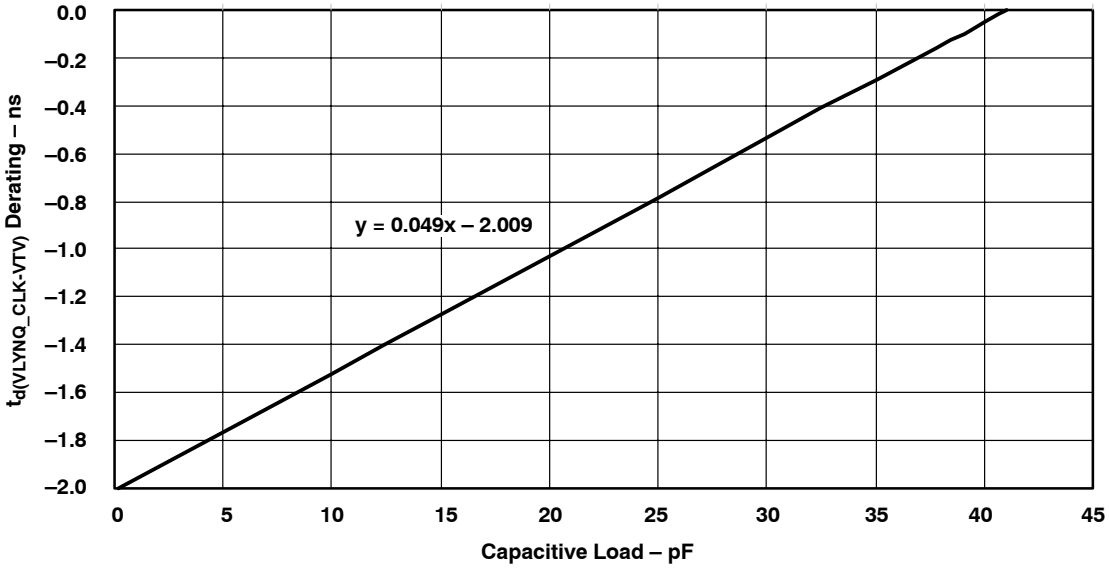


Figure 5–56. Derating Curve for $t_{d(VLYNQ\_CLK-VTV)}$

5.16 GPIO Timing

Table 5–38. GPIO Timing (See Figure 5–57)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(VBUS\_CLK)}$	Clock frequency, VBUS_CLK†		82.5	MHz
1	$t_{c(VBUS\_CLK)}$	Cycle time, VBUS_CLK†	12.12		ns
2	$t_{d(GPIO\_O\_R)}$	Delay time, DATA_OUT register change to GPIO driver†‡		0	ns
3	$t_{d(GPIO\_O)}$	Delay time, through GPIO driver to GPIO[51:0] output change†‡	1	8	ns
4	$t_{d(GPIO\_I)}$	Delay time, GPIO[51:0]↑ (input) to VBUS_CLK↑†‡	$t_c \times 0$		ns
5	$t_{d(GPIO\_I)}$	Delay time, GPIO[51:0]↓ (input) to VBUS_CLK↓†‡	2		ns
6	$t_{d(GPIO\_I\_R)}$	Delay time, GPIO[51:0]↓ to DATA_IN register change (after one clock sync)†‡		0	ns

† Specified by design

‡ The SYS_GPIO (DATA_IN) register contains raw data. This raw data is asynchronous, only having one VBUS_CLK delay, instead of two. In addition, this data is not latched in the register and is free to change when there is a change to the GPIO signal.

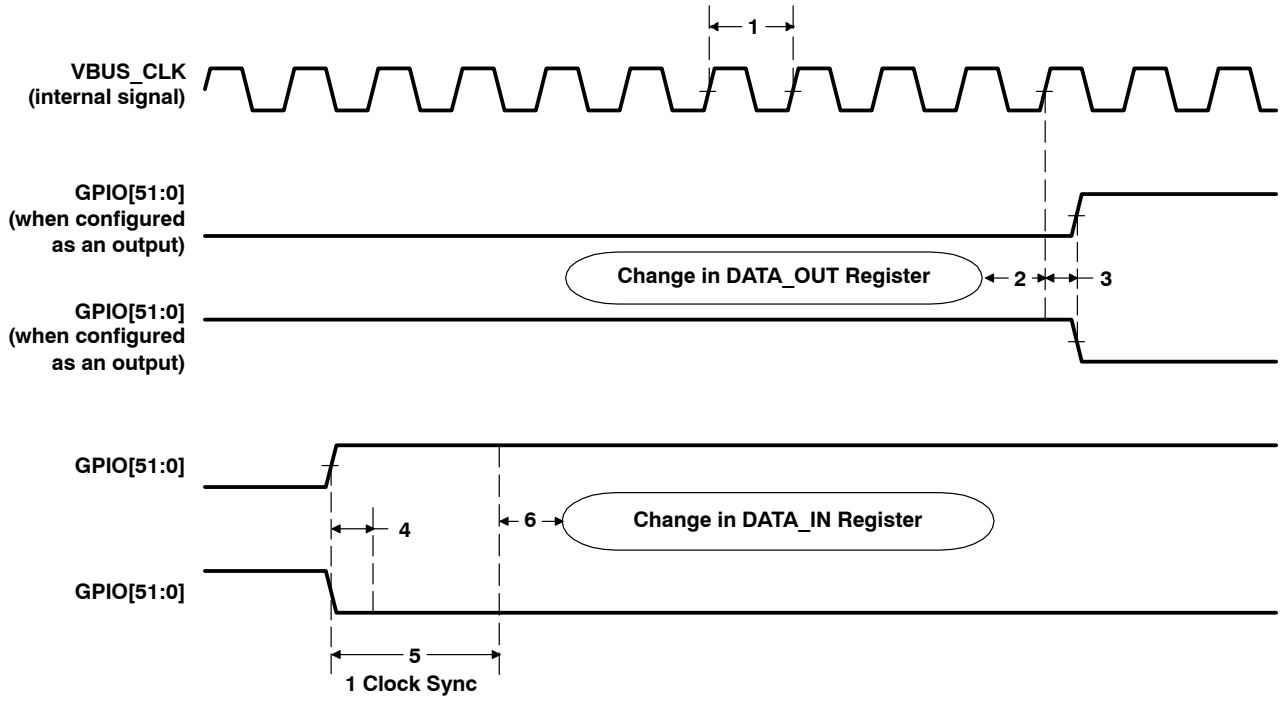


Figure 5–57. GPIO

5.17 Keypad Interface Timing

Table 5–39. Keypad Timing (See Figure 5–58)

NO.	DESCRIPTION†§		MIN	MAX	UNIT
	$f_{clock(VBUS\_CLK)}$	Clock frequency, VBUS_CLK		82.5	MHz
1	$t_{c(VBUS\_CLK)}$	Cycle time, VBUS_CLK	12.12		ns
2	$t_{d(KEYPAD\_O\_R)}$	Delay time, DATA_OUT register to VBUS_CLK↑‡¶		0	Clock
3	$t_{d(KEYPAD\_O)}$	Delay time, VBUS_CLK↑ to KEYPAD(15:0)↑¶	1	8	ns
4	$t_{d(KEYPAD\_I)}$	Delay time, KEYPAD[15:0]↑ input to VBUS_CLK↑¶	0		ns
5	$t_{d(KEYPAD\_I)}$	Delay time, KEYPAD[15:0]↓ input to VBUS_CLK↓¶	$t_c \times 2$		ns
6	$t_{d(KEYPAD\_I\_R)}$	Delay time, VBUSA_CLK↓ to DATA_IN register change after one clock sync¶		0	ns

† The debounce counter can be used to filter keypad activation and deactivation mechanical glitches. The filtered results feed the keypad interrupt to the MIPS. Prior to use, the keypad I/O must be properly enabled and polarized through the KEYPAD (MSK_POLARITY) register. The debounce time is defined in the KEYPAD (CNT) register. Additional control is required in the KEYPAD (CTRL) register.

‡ This value is one VBUS_CLK cycle time.

§ The KEYPAD (DATA_IN) register contains raw data. This raw data is asynchronous, only having one VBUS_CLK delay, instead of two. In addition, this data is not latched in the register and is free to change when there is a change to the KEYPAD signal.

¶ Specified by design

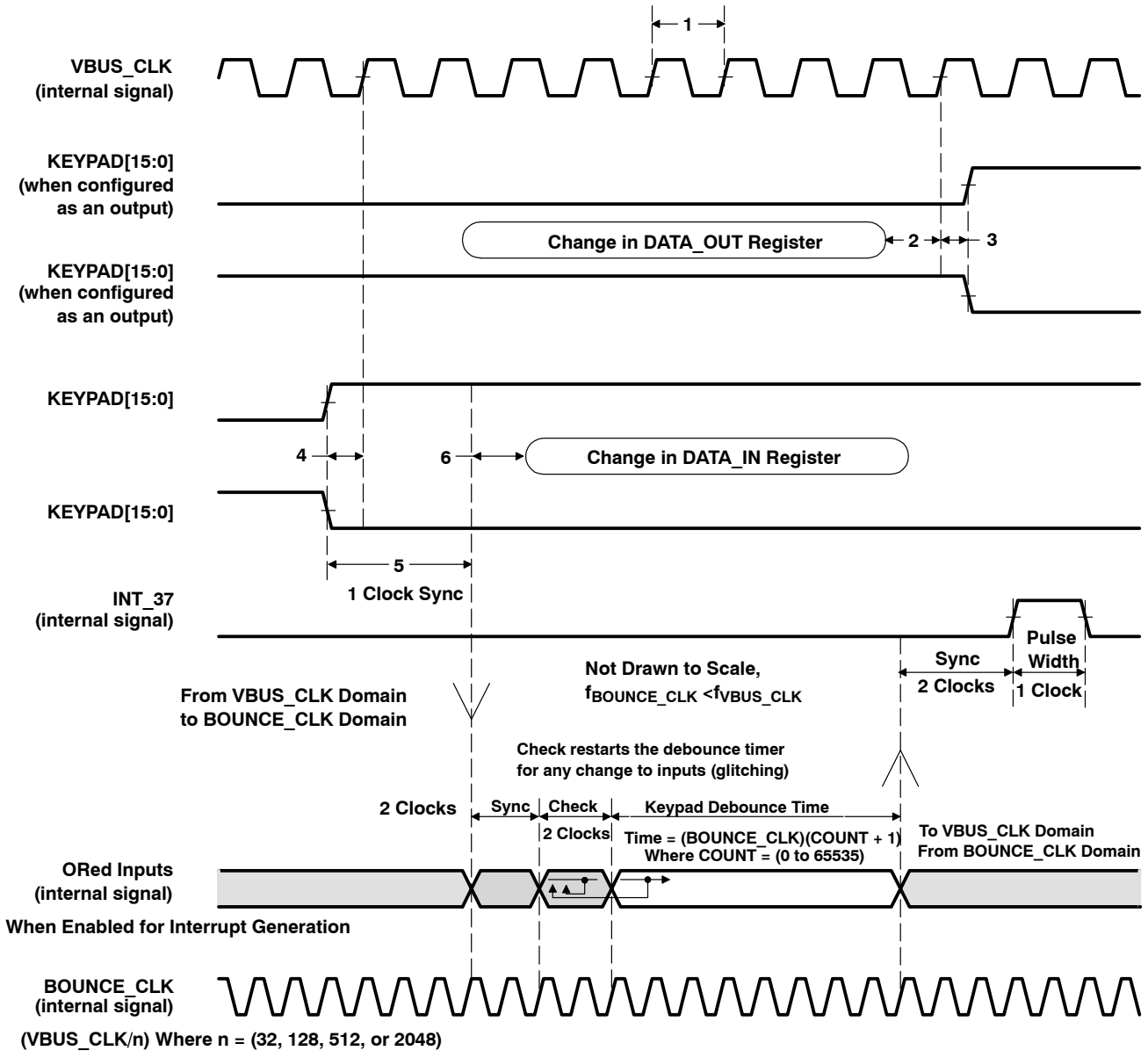


Figure 5–58. Keypad

5.18 MIPS Interrupt Interface Timing

There are five external MIPS interrupt sources. EXT_INT[4:1] enter the MIPS interrupt controller as INT_4 to INT_1, while TELE_INT enters as INT_23.

The MIPS interrupt interface is asynchronous. Input data is synchronized with two VBUSP_CLK cycles upon entry to the TNETV1060.

The SYS_INT (STAT_RAW_1) and SYS_INT (STAT_RAW_2) register set holds the interrupt pending status of all TNETV1060 interrupts destined for the MIPS. To generate a MIPS interrupt, the corresponding bit in the SYS_INT (STAT_MSK_1) or SYS_INT (STAT_MSK_2) register set must also be active.

The polarity (active high or low) may be configured in the SYS_INT (POLARITY_1 and SYS_INT (POLARITY_2) register set. The type (active level or edge) may be configured in the SYS_INT (TYPE_1) and SYS_INT (TYPE_2) register set.

TELE_INT is the only external DSP interrupt source.

The DSP interrupt interface is asynchronous. Input data is synchronized with two DSP_CLK cycles upon entry to the TNETV1060 DSP subsystem.

The DSP_INT (IFR0) and DSP_INT (IFR1) register set holds the interrupt pending status of all TNETV1060 interrupts destined for the DSP. To generate a DSP interrupt, the corresponding bit in the DSP_INT (IER0) or DSP_INT (IER1) register set also must be active.

The input polarity is a fixed active high, and the input type is a fixed active edge.

Table 5–40. MIPS Interrupt Timing (See Figure 5–59)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(VBUSP\_CLK)}$	Clock frequency, VBUSP_CLK		125	MHz
1	$t_{c(VBUSP\_CLK)}$	Cycle time, VBUSP_CLK	8		ns
2	$t_{d(INT)}$	Delay time, EXT_INT[4:1]/TELE_INT↑ to VBUSP_CLK↑†	0		ns
3	$t_{d(INT\_E)}$	Delay time, VBUSP_CLK↑ to EXT_INT[4:1]/TELE_INT edge (↑/↓)†	$3 \times t_c$		ns
4	$t_{d(INT\_L)}$	Delay time, VBUSP_CLK↑ to EXT_INT[4:1]/TELE_INT level (H/L)†	$3 \times t_c$		ns
5	$t_{d(INT\_R)}$	Delay time, MIPS interrupt (after synchronization) to active status in STAT_RAW register	$1 \times t_c$		ns

† Specified by design

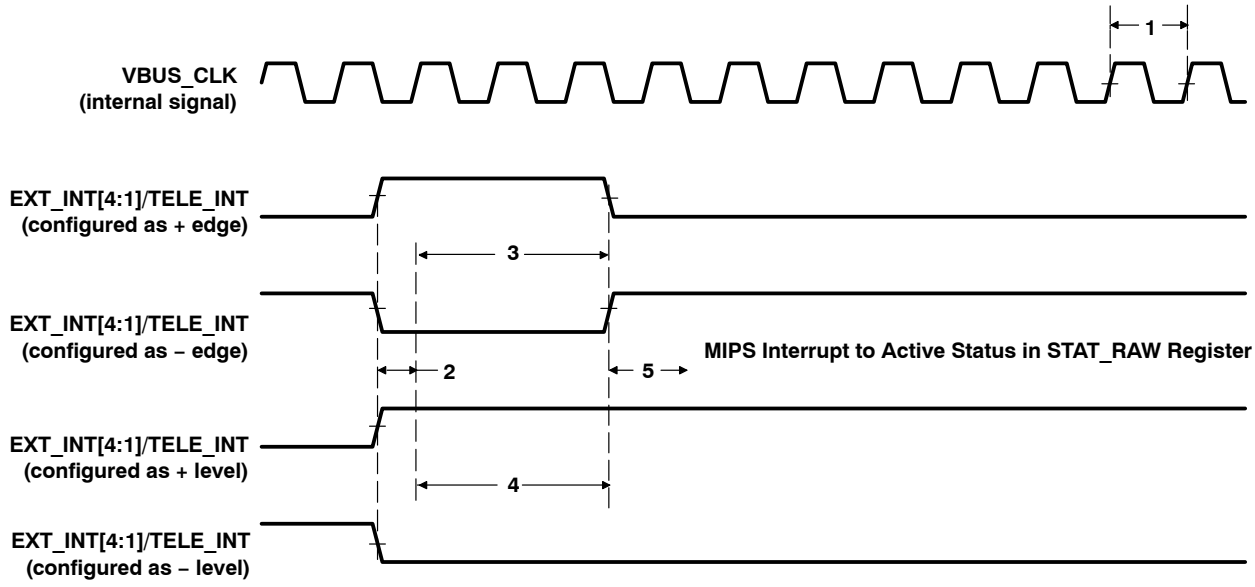


Figure 5–59. MIPS Interrupt

Table 5–41. DSP Interrupt Timing (See Figure 5–60)

NO.	DESCRIPTION		MIN	MAX	UNIT
	$f_{clock(DSP\_CLK)}$	Clock frequency, DSP_CLK		125	MHz
1	$t_{c(DSP\_CLK)}$	Cycle time, DSP_CLK	8		ns
2	$t_{d(DSP\_INT)}$	Delay time, TELE_INT↑ to DSP_CLK↓†	0		ns
3	$t_{d(DSP\_INT\_E)}$	Delay time, DSP_CLK↓ to TELE_INT↓†	$t_c \times 3$		ns
5	$t_{d(DSP\_INT\_R)}$	Delay time, DSP interrupt (after synchronization) to active status in DSP_INT register†	$t_c \times 1$		ns

† Specified by design

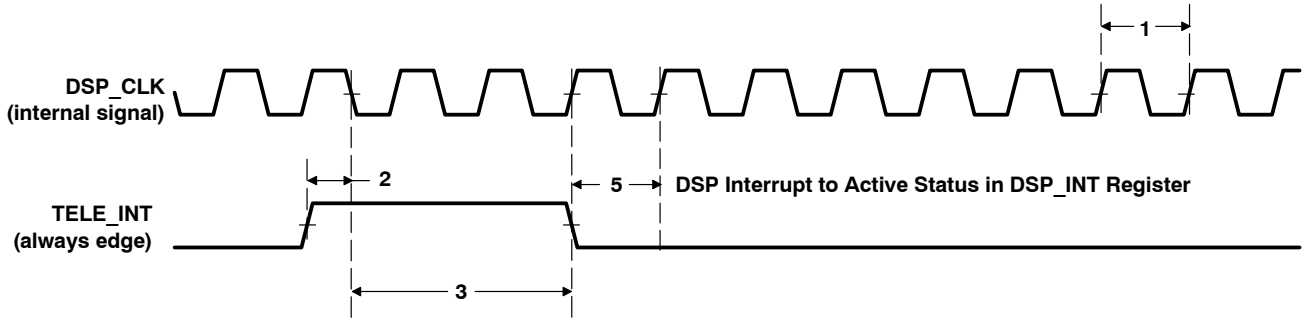
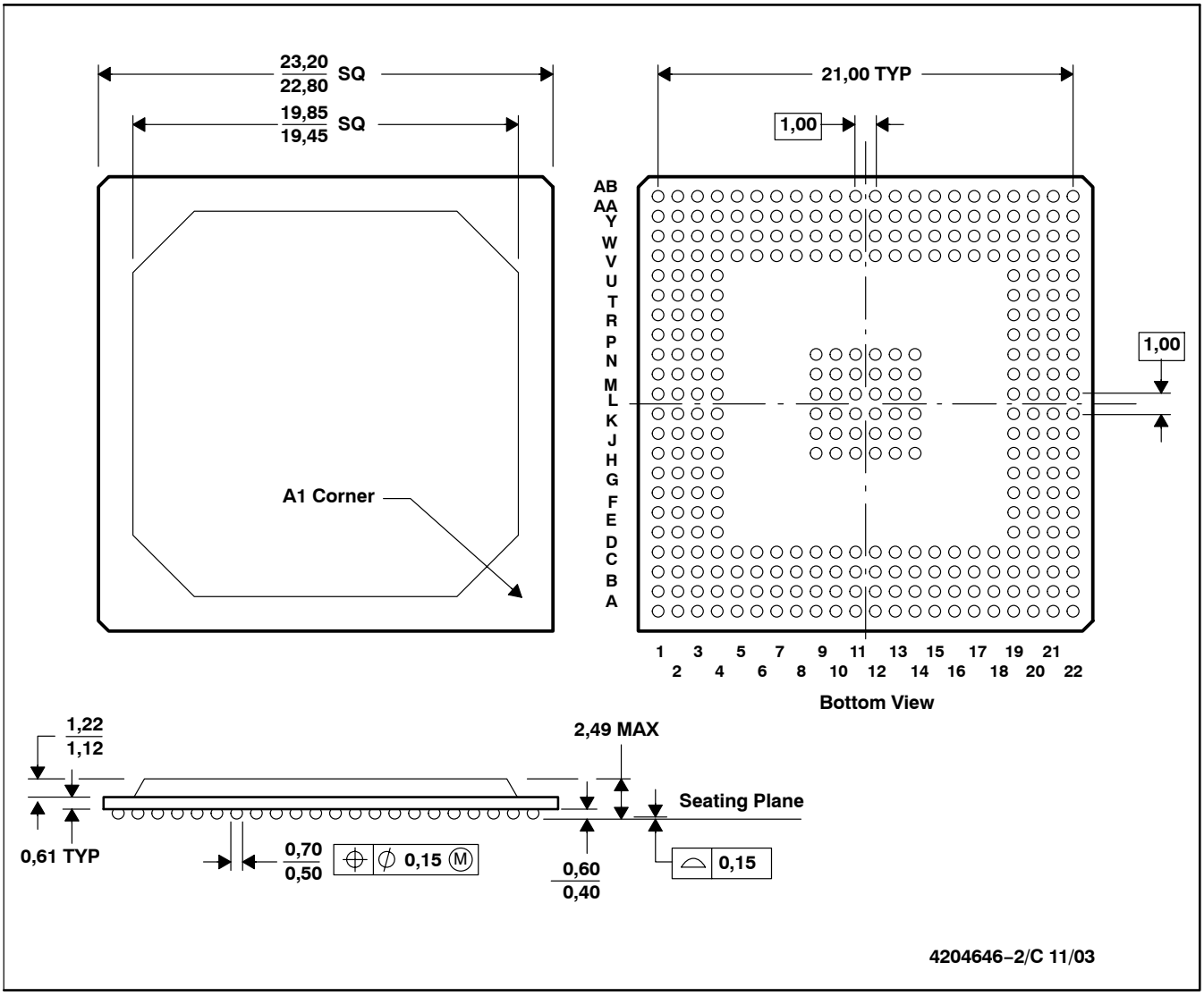


Figure 5–60. DSP Interrupt

6 Mechanical Specification



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–151

Figure 6–1. GDW (S–PBGA–N324) Plastic Ball Grid Array

7 Documentation Support

Table 7–1. Documentation

NAME DESCRIPTION	LITERATURE NUMBER	LOCATION	V1060 FUNCTION
TNETV1060 Data Manual TNETV1060 features, I/O, hardware overview, and electrical specification	SPRS255	Contact TI	All
TNETV1050 User's Guide TNETV1050/1055/1060 feature detail including register description	SPRU799	Contact TI	All
TMS320C55x™ DSP Functional Overview Basic overview of TMS320 C55x™ DSP core	SPRU312	www.ti.com	DSP
TMS320C55x™ DSP CPU Reference Guide Detailed description of C55x CPU architecture, registers, memory, stack, interrupts and addressing	SPRU371	www.ti.com	DSP
TMS320C55x™ DSP Peripherals Reference Guide Detailed description of C55x peripherals, including the McBSP	SPRU317	www.ti.com	DSP
TMS320C55x™ DSP Programmer's Guide Explanation and examples of Assembly and C code optimization (including DSPLIB), fixed-point arithmetic, and bit-reversed addressing for the C55x	SPRU376	www.ti.com	DSP
TMS320C55x™ DSP Mnemonic Instruction Set Reference Guide Summary, description, and opcodes for the mnemonic form of the C55x instruction set	SPRU374	www.ti.com	DSP
TMS320C55x™ DSP Algebraic Instruction Set Reference Guide Summary, description, and opcodes for the algebraic form of the C55x instruction set	SPRU375	www.ti.com	DSP
TMS320C55x™ Optimizing C Compiler User's Guide Detailed explanation of how to use the compiler, optimizer, interlist utility, library-build utility, and C++ name demangler for the C55x DSP	SPRU281	www.ti.com	DSP
TMS320C55x™ Assembly Language Tools User's Guide	SPRU280	www.ti.com	DSP
TMS320C55x™ DSP Library Programmer's Reference Detailed explanation of the C55x DSP library (DSPLIB) and its use	SPRU422	www.ti.com	DSP
Code Composer Studio™ User's Guide Explanation of how to use Code Composer Studio to develop and debug real-time software applications	SPRU393	www.ti.com	DSP
TMS320C55x™ DSP Technical Overview Detailed overview of the C55x DSP core	SPRU328	www.ti.com	DSP
MIPS32™ 4KE™ Processor Core Family Software User's Manual Description of the MIPS32 4KE processor and functions necessary for coding	MD00103	www.mips.com	MIPS Processor
MIPS32™ 4KE™ Processor Core Family Integrator's Guide Targeted for the ASIC designer who is integrating the MIPS32 4KE processor core into the system ASIC	MD00104	www.mips.com	MIPS Processor
MIPS32™ 4KEc™ Processor Core Data Sheet MIPS32 4KEc features, I/O, hardware overview, and electrical specification	MD00111	www.mips.com	MIPS Processor
ECt Interface Specification Describes the ECt interface designed for microprocessor cores	MD00052	www.mips.com	MIPS Processor
Core Coprocessor Interface Specification Describes the coprocessor interface standard supported by MIPS32 processor core	MD00068	www.mips.com	MIPS Processor
EJTAG Specification Describes the behavior and organization of on-chip EJTAG hardware resources as seen by software and by external agents	MD00047	www.mips.com	MIPS JTAG

Table 7–1. Documentation (Continued)

NAME DESCRIPTION	LITERATURE NUMBER	LOCATION	V1060 FUNCTION
EJTAG Implementation Application Note Practical guide to assist in achieving the maximum possible performance in terms of speed and reliability over the JTAG serial link	MD00071	www.mips.com	MIPS JTAG
EJTAG Trace Control Block Specification Detailed explanation of tracing logic within the MIPS32 4KEc JTAG	MD00148	www.mips.com	MIPS JTAG
MIPS32™ Architecture for Programmers, Volume III: The MIPS32™ Privileged Resource Architecture Describes the MIPS32 Privileged Resource Architecture, which defines and governs the behavior of the privileged resources included in a MIPS32 processor implementation	MD00090	www.mips.com	MIPS
TLV320AIC20 Data Manual Register-level description of the TLV320AIC20 CDEC (not exact implementation for TNETV1060)	SLAS363A	www.ti.com	AIC20 Codec
MystiPHY™ 110 10/100 Base-TX/FX Ethernet PHY Core Product Brief Short description of PHY features and structure	MystiPHY110	www.mysticom.com	PHY