VLSI Design Review 1

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1 Block Diagram

Figure 1 is a simplified diagram of our SRAM memory block. It shows every input and output of each component, as well as bus widths, giving a general sense of the design of our memory.

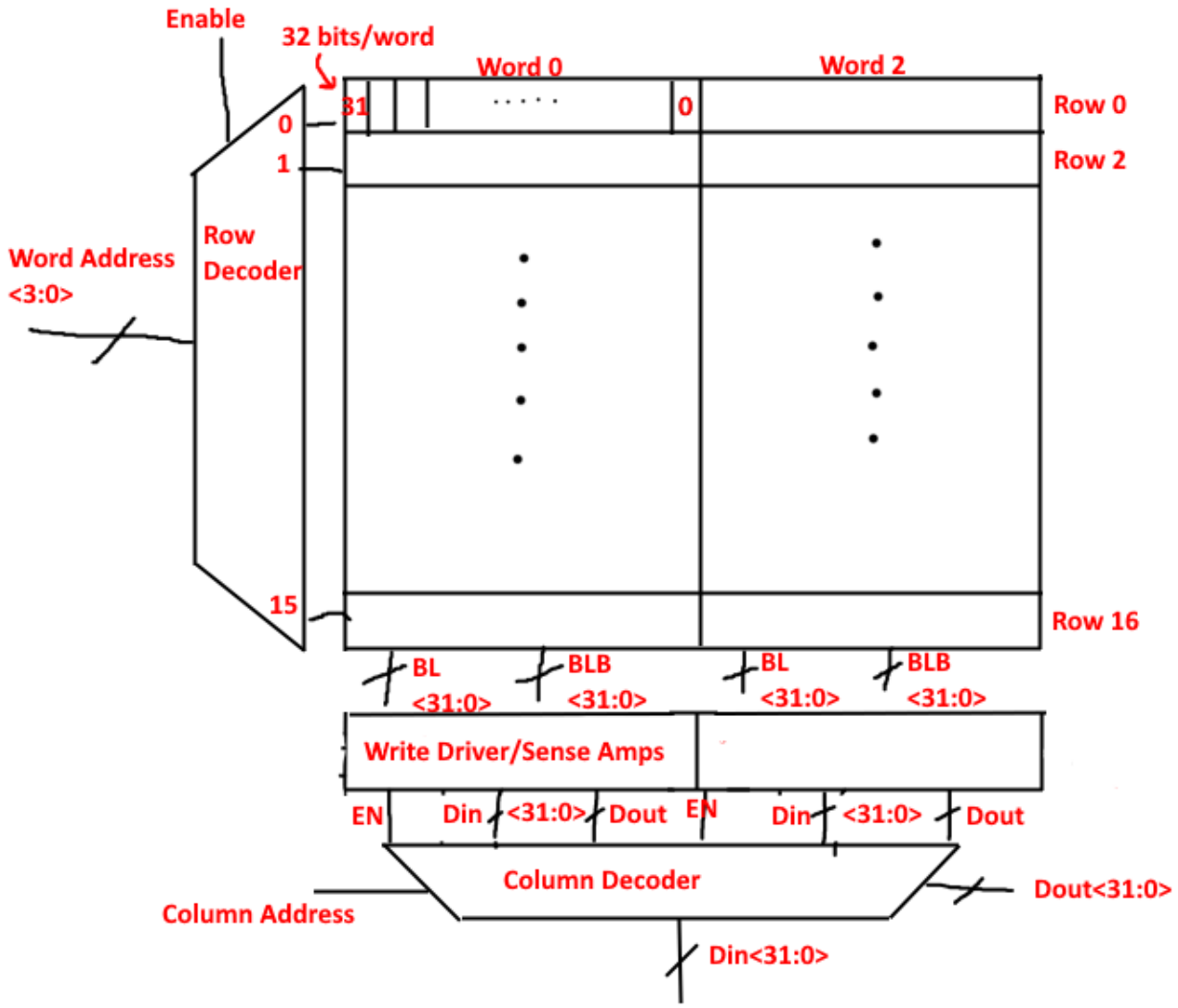


Figure 1: Block Diagram

2 Cadence schematics

Figures 2 through 6 show the hierarchical schematics for the entire array, from the top level down to the word level (the bitcell schematic is shown in Section 4). We heavily utilized wire and device buses to simplify the schematic.

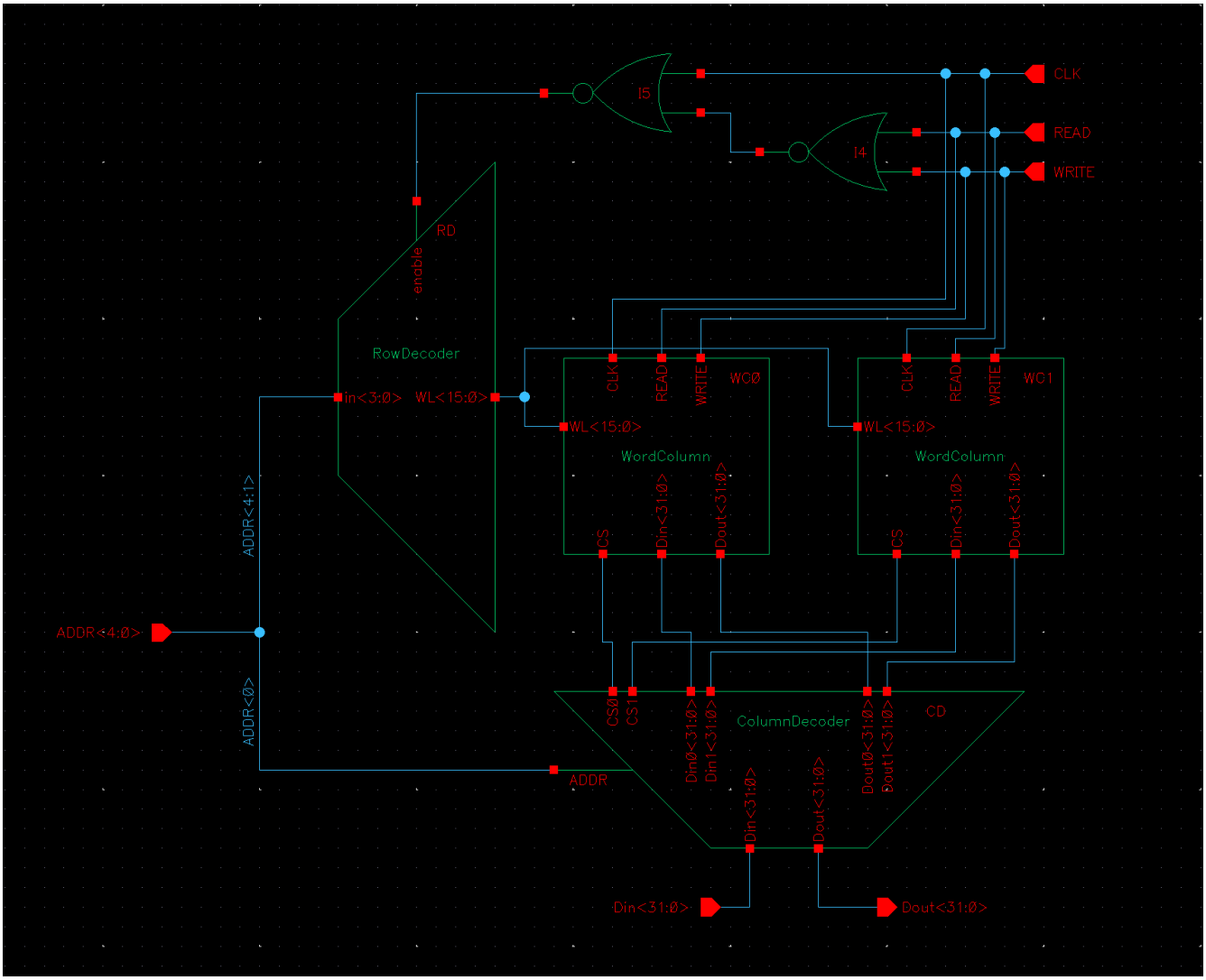


Figure 2: Top-Level Schematic

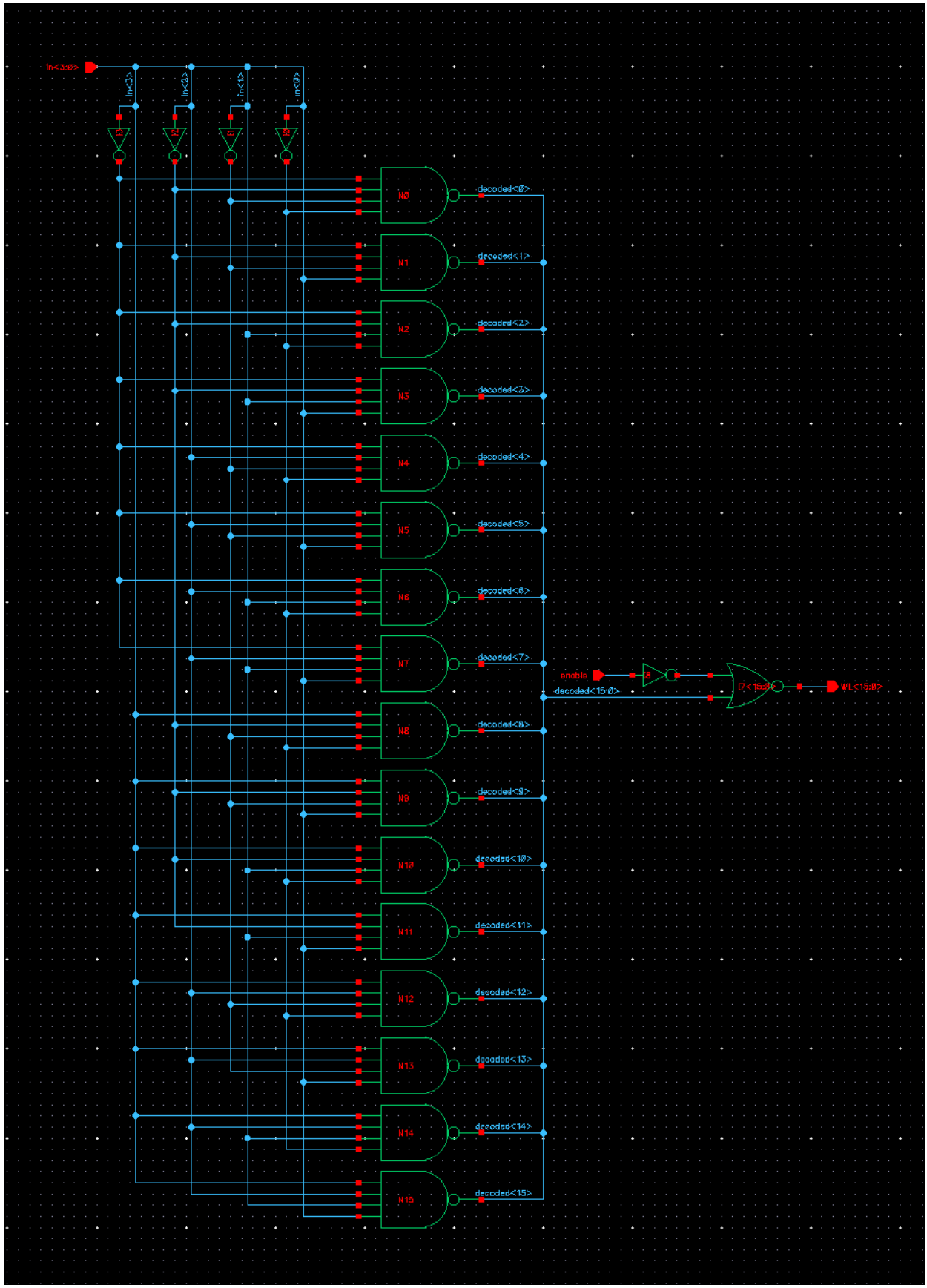


Figure 3: Row Decoder Schematic

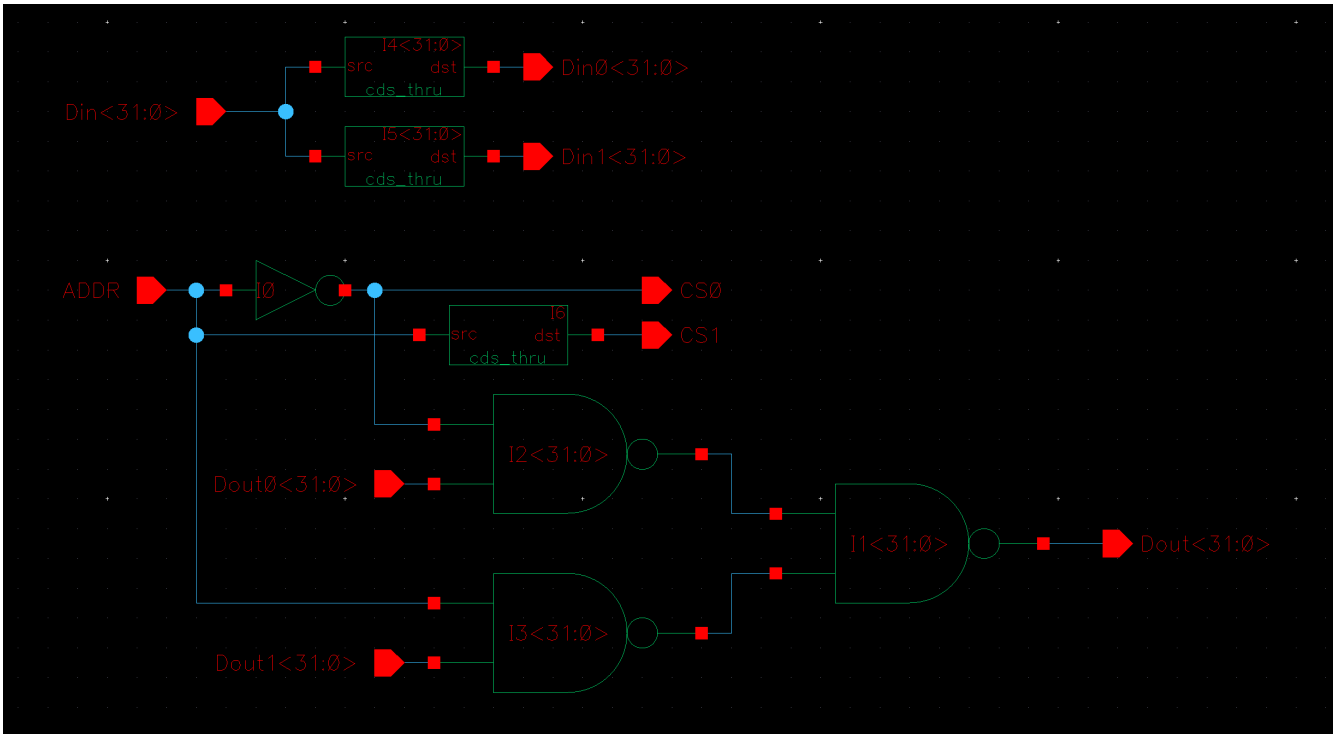


Figure 4: Column Decoder Schematic

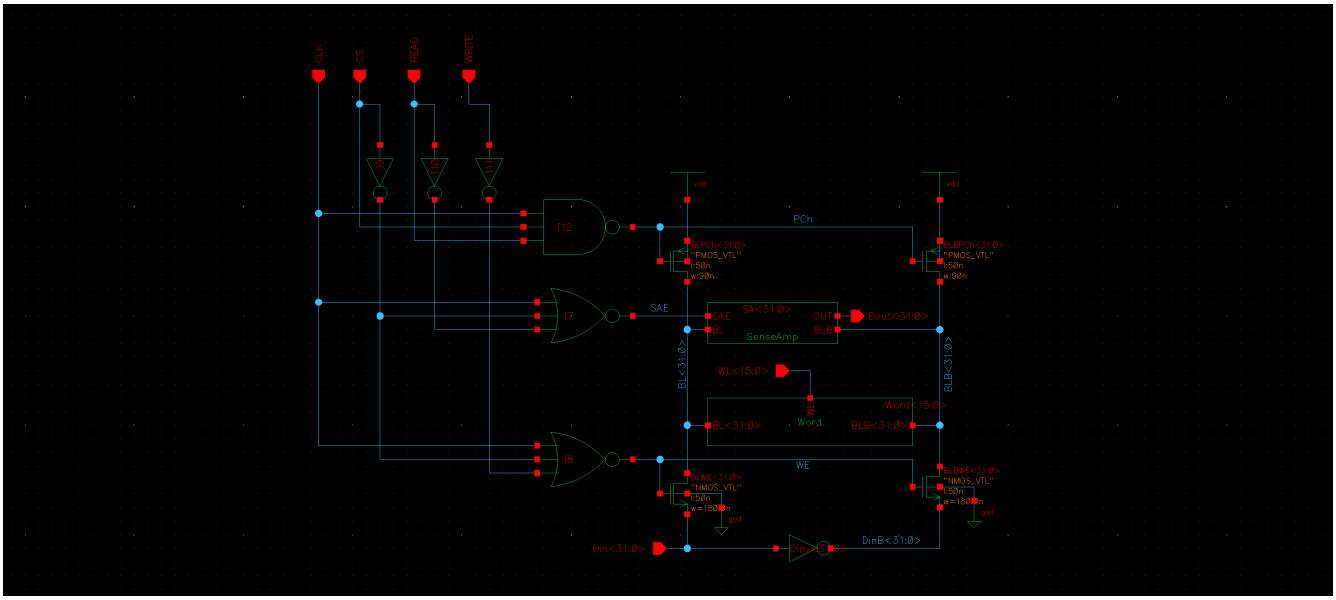


Figure 5: Word-Column Schematic

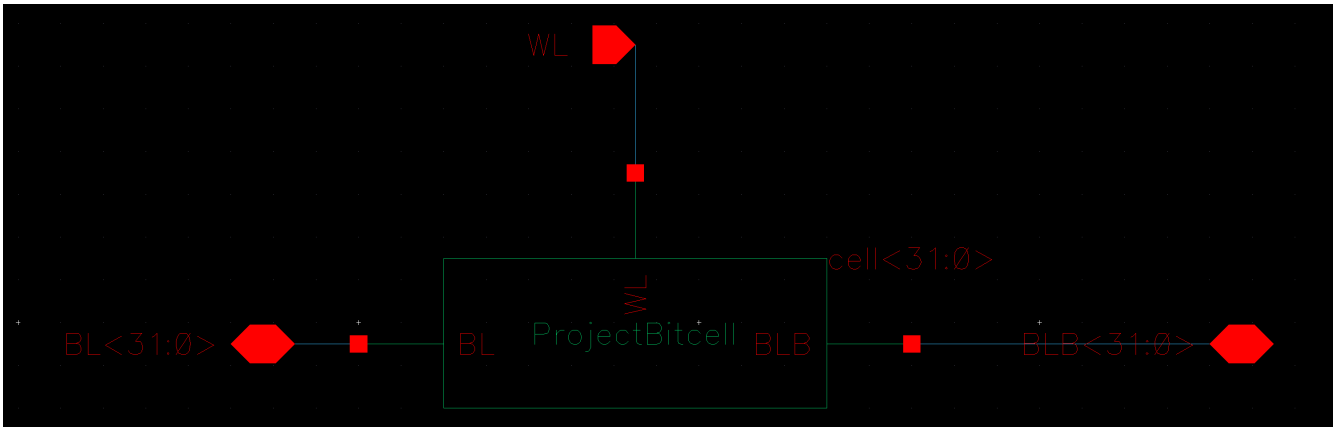


Figure 6: 32-bit Word Schematic

3 Timing Diagram

Figure 7 demonstrates the timing needed for various signals external and internal to the SRAM we've designed.

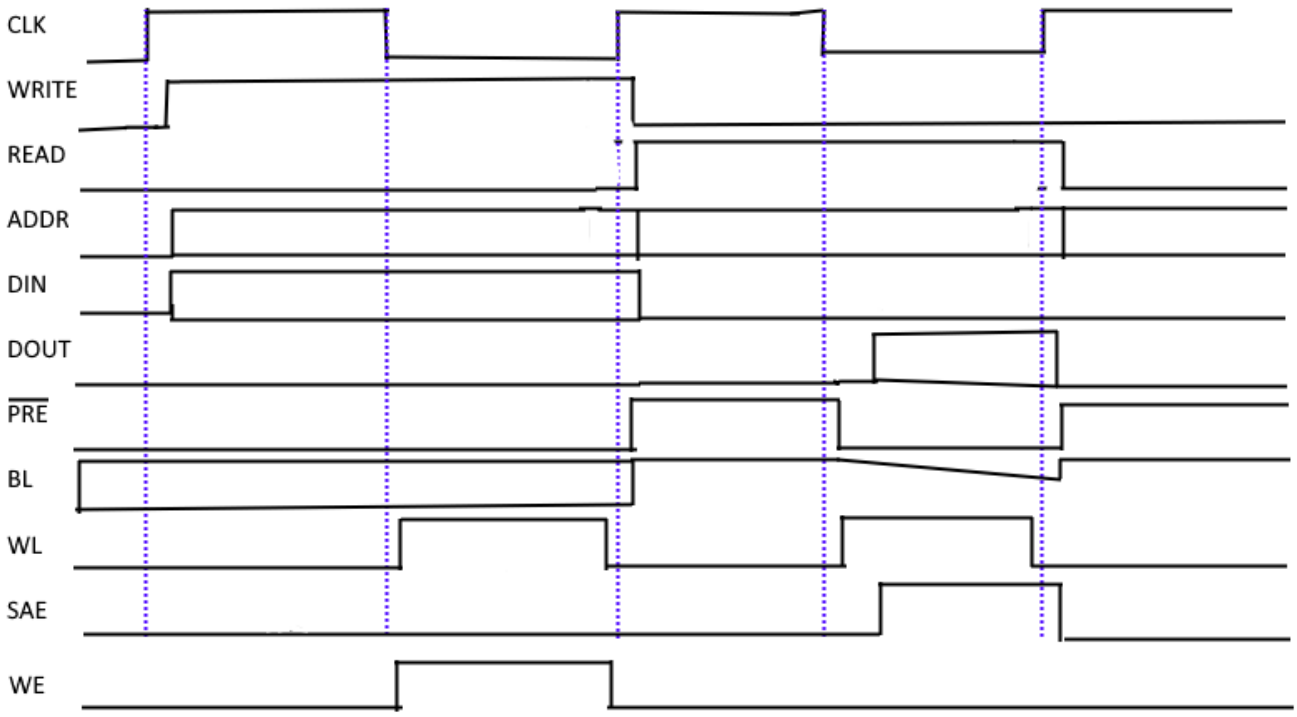


Figure 7: Timing Diagram

4 Bitcell Schematic

Figure 8 shows the bitcell schematic. We used widths of 90 nm for the pull-up and access transistors and 140 nm for the pull-down transistors.

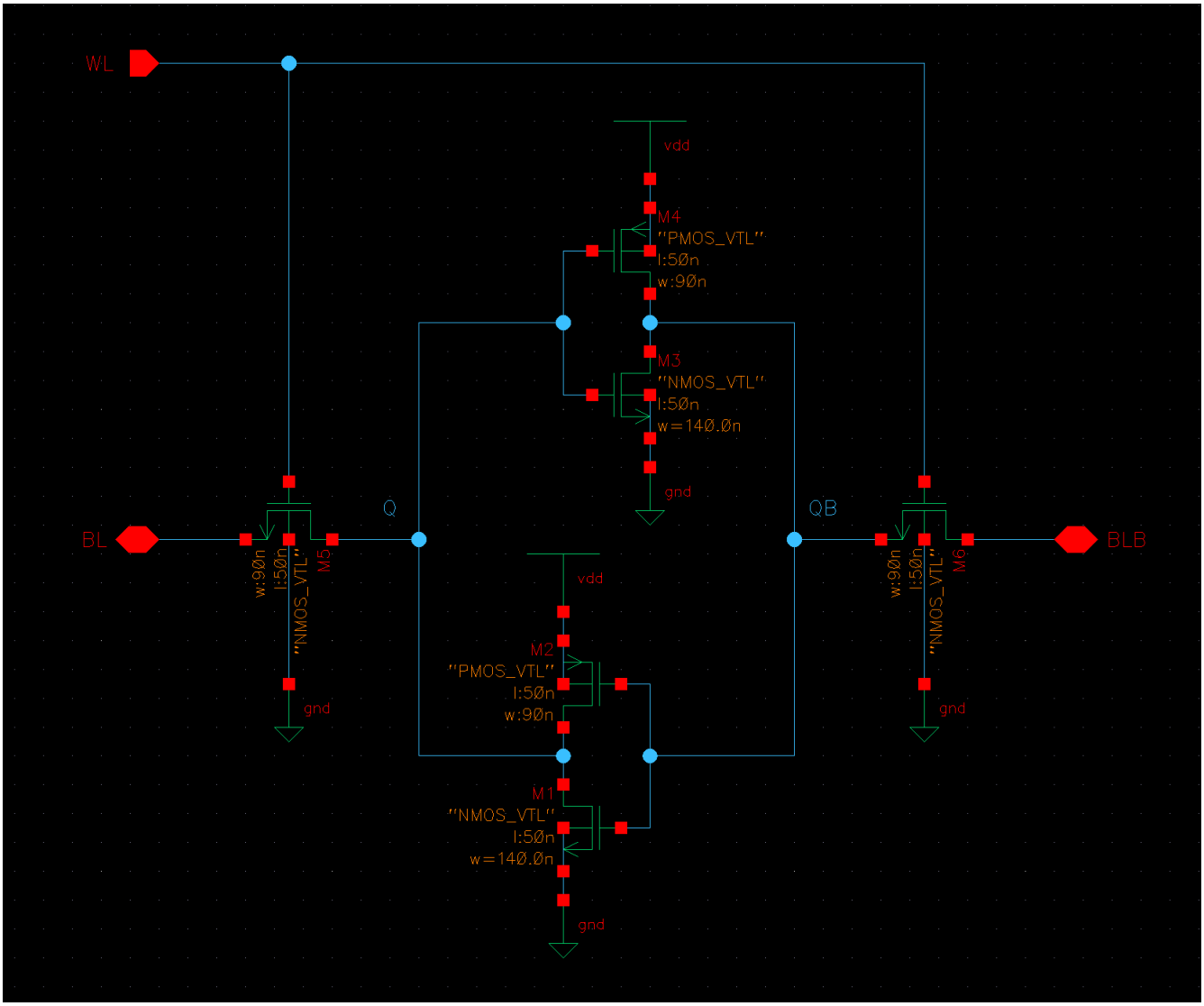
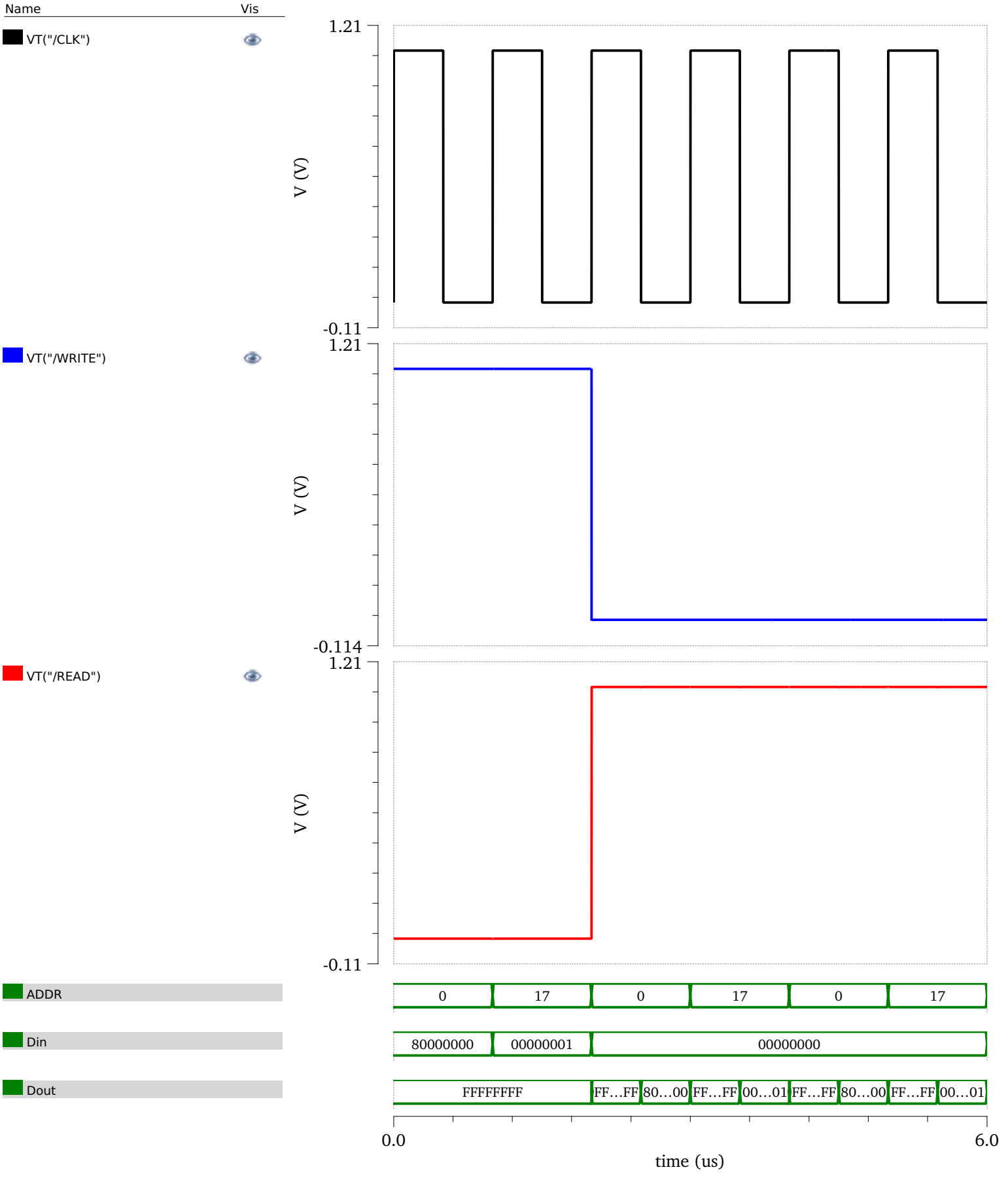


Figure 8: Bitcell Schematic

5 Simulation Printouts

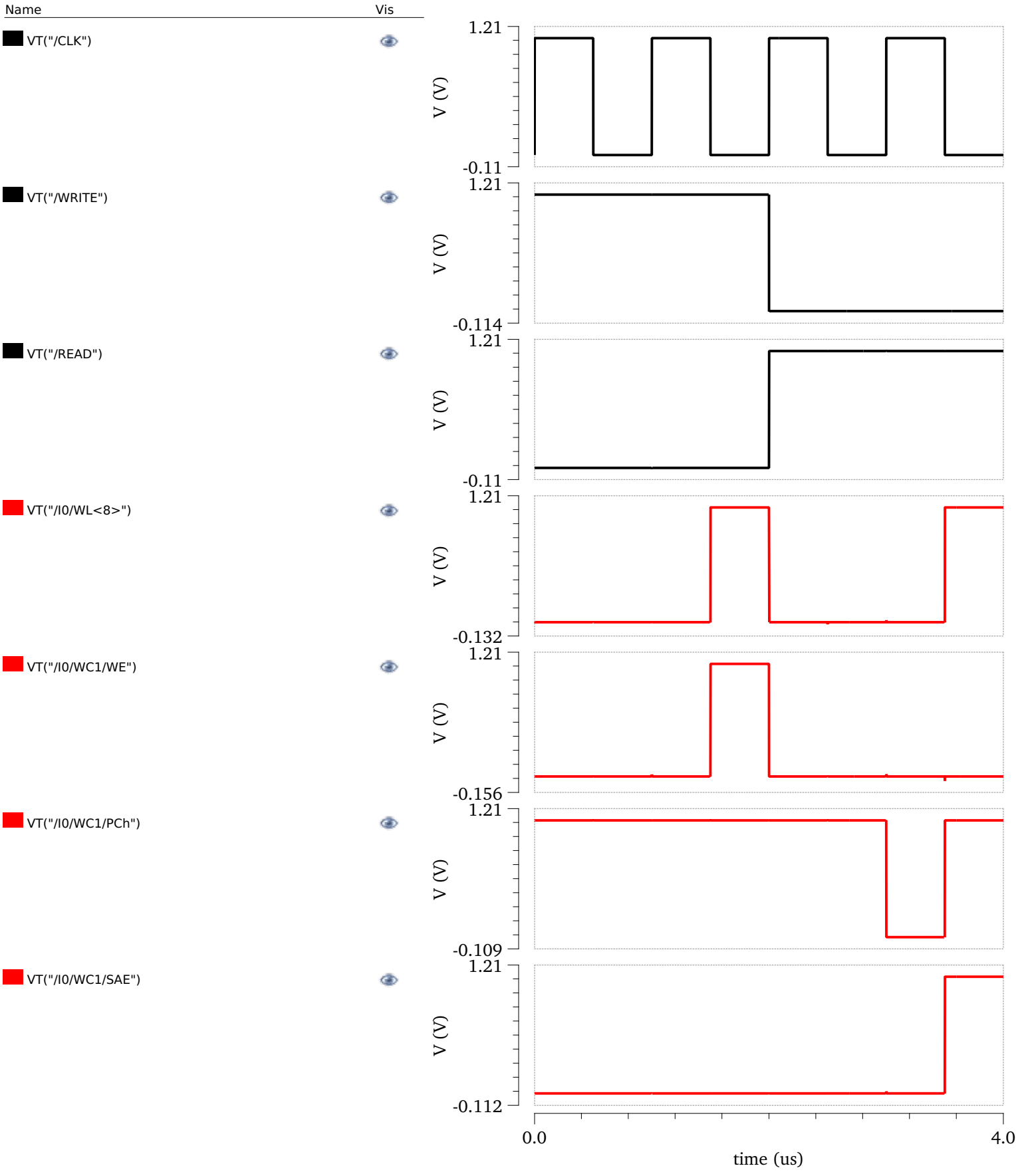
The next page shows a simulation printout of the top-level IO for basic write and read operations. The values `0x8000 0000` and `0x0000 0001` are written to two different addresses, and then read to demonstrate the memory can receive a value written to it, hold its state, and return it when read. Finally, both addresses are read once more to demonstrate the read operation does not destroy the data.

Transient Response

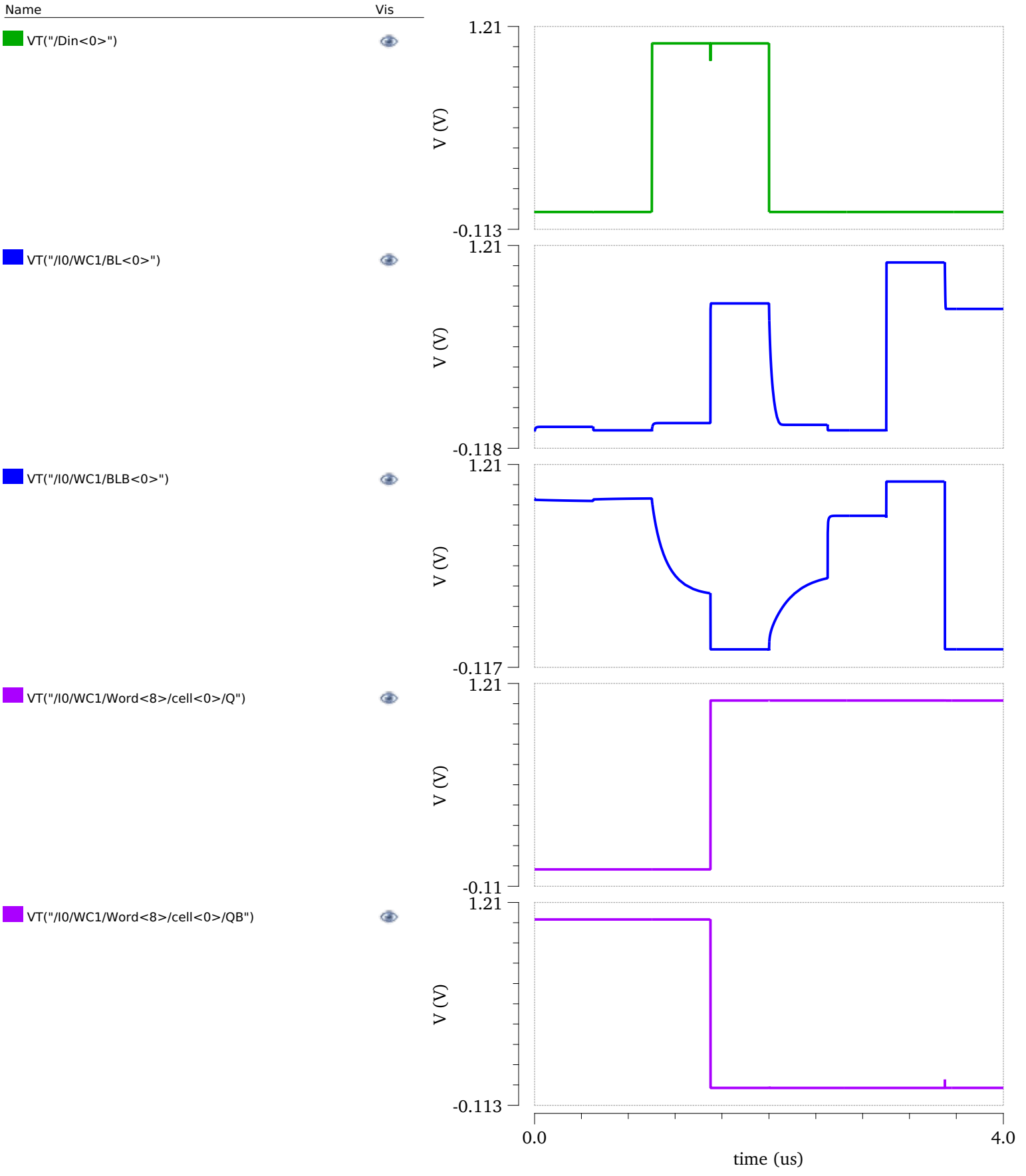


The next two pages show detailed traces for a single bit, which is first written from 0 to 1, then read.

Transient Response



Transient Response



The next page shows a simulation printout of the VTC for the inverter used in the SRAM bitcell. To produce a butterfly plot, the raw data was exported and reflected to produce Figure 9 below.

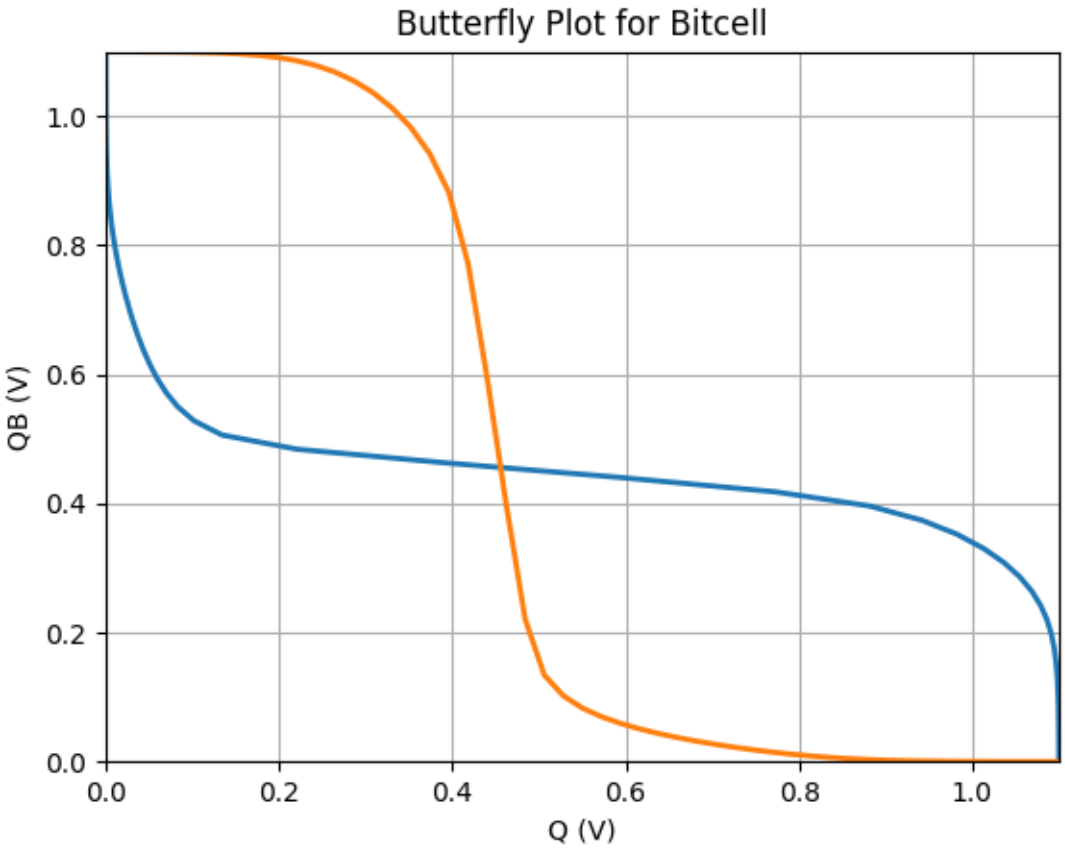
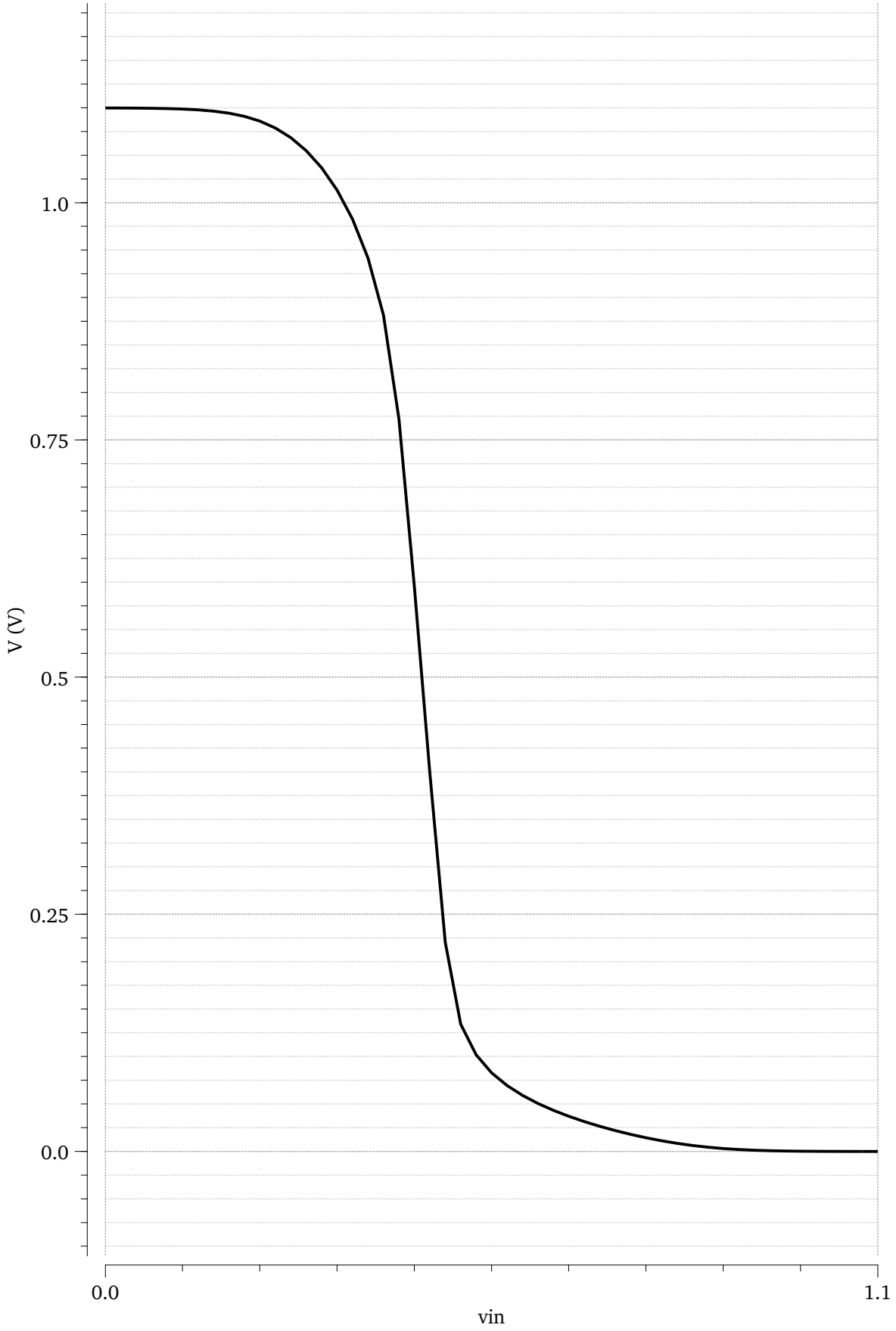


Figure 9: Butterfly Plot for the SRAM Bitcell

DC Response

Name	Vis
VS("/QB")	



Completed Tasks

As of now, we've designed the entire structure of the SRAM block. The block contains sixteen rows of two words, with each word comprised of 32 bitcells. It also contains the row and column decoders, write drivers, and sense amplifiers. The transistors within both the bitcells and sense amps have been sized to allow them to function correctly. We've ran simulations to verify the functionality of the read and write operations, and confirmed that the SRAM block does indeed function properly.

Remaining Tasks

In general, the next steps are to increase the size of our memory and improve performance across speed, area, and power metrics. Achieving this may involve expanding the SRAM to multiple blocks, increasing the number of rows or columns within each block, and resizing the transistors to the optimal level for increased performance speed and decreased power consumption. Expanding the size of the SRAM should be quite simple, only involving adding more blocks and a block decoder; and decreasing power consumption or increasing speed will require more thought.