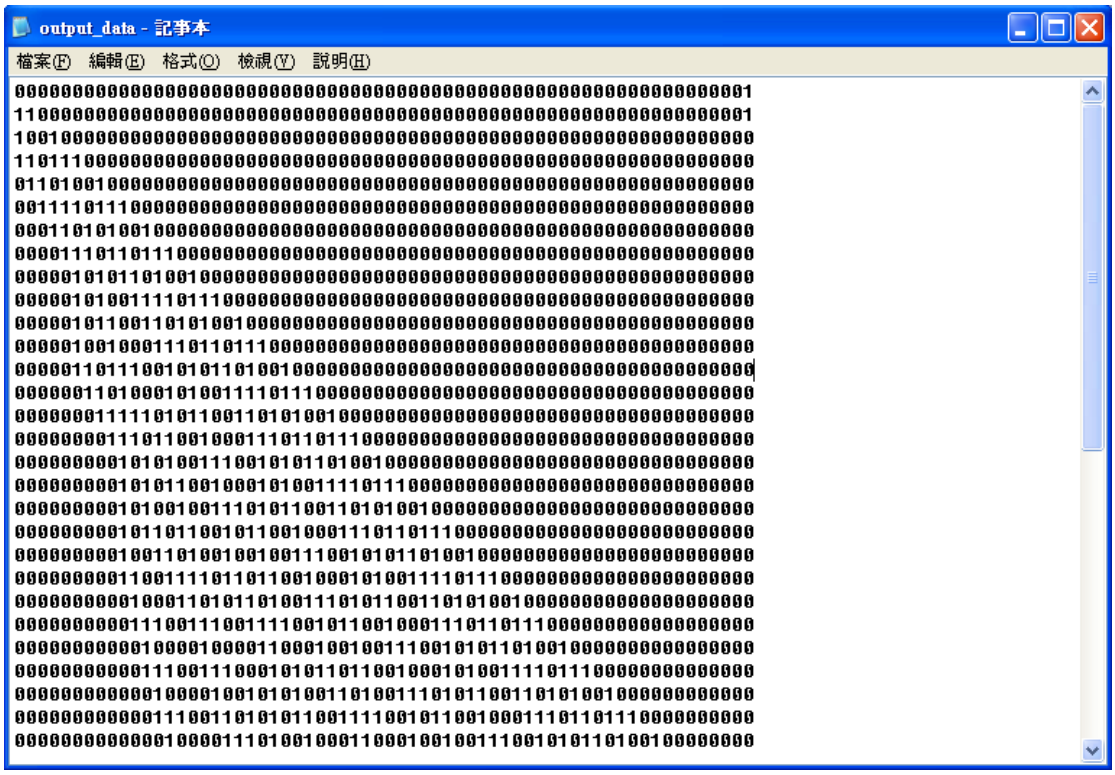
Homework 4
Due Day 12/31

Implement and simulate the 64-bit random number generator (RNG) circuit at **RTL level** introduced in Chapter 9 using Modelsim. In the simulation, **please DO NOT use the same initial seed value shown in Chapter 9 for the observation of output**. The implementation of 1D cell array with 64 cells is required.

Your project report should include the following items.

1. the Modelsim project file containing the VHDL code of the system,
2. the ppt or word files containing the simulation results and the corresponding discussions.

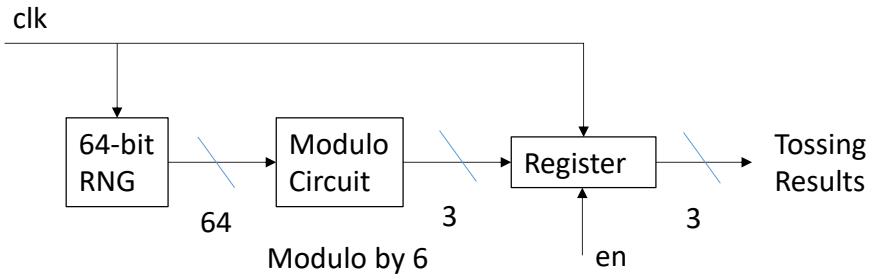
Please show your output as a textfile shown below.



Optional:

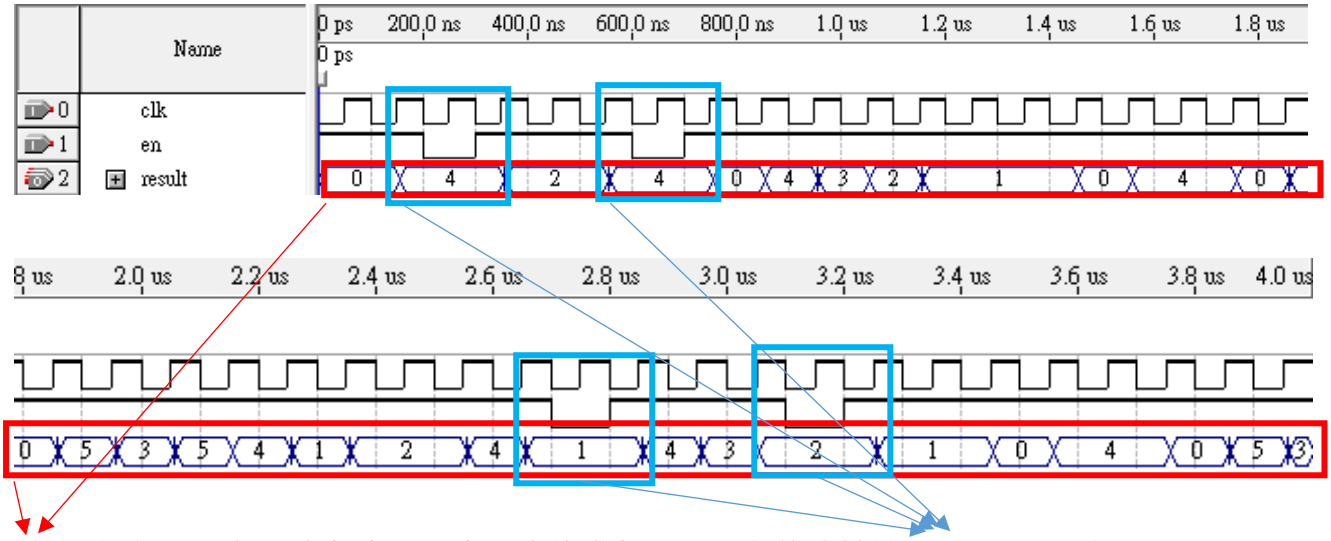
Extra credits (**40 points**) will be granted if you have successfully applied the circuit for the applications such as electronic die tossing.

As shown in the following figure, the electronic die tossing circuit is based on 64-bit RNG and a modulo-by-6 circuit.



You can implement the modulo circuit by modulo operator (i.e., mod) in VHDL.

Vector waveform:



可以看到 result 都是亂數產生器產生出的亂數 mod 6 之後的結果，且 en = ‘0’時輸出不變。

RTL viewer(參考用):