VLSI Homework #3
Due Day: 12/17/2021

The goal of this homework is to design a traffic light control circuit as shown below. As shown in Figure 1, the circuit consists of a controller and a counter.

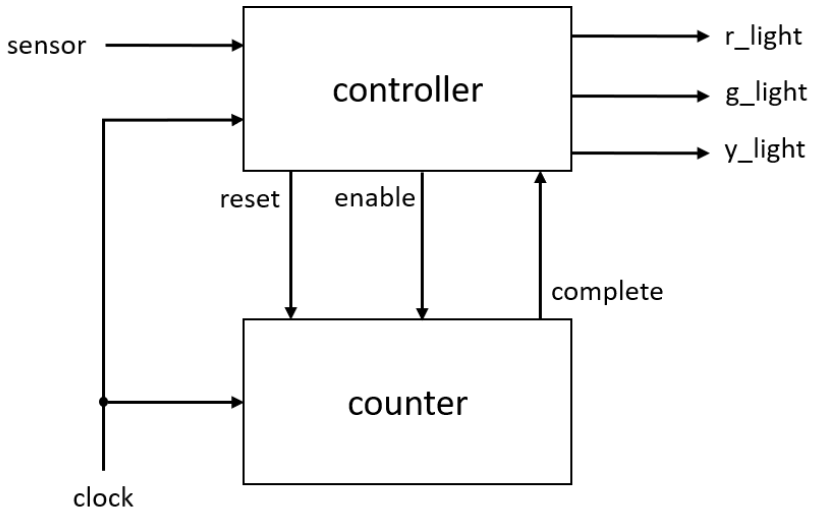


Figure 1. The architecture of the traffic light control circuit.

The ASM chart of the controller is shown in Figure 2. The controller has four states: **green**, **red**, **yellow1** and **yellow2**. When the controller in **green** state, it turns on g_light (g_light=1), and resets the counter (reset=1). The controller stays in the **green** state until sensor input becomes 1. After that, the controller enters the **yellow1** state, where the yellow light is on. After the **yellow1** state, the controller is in the **red** state. Note that, in red state, the counter is activated (enable=1). After the counting operation is completed (complete=1), the controller then enters **yellow2** state. In the **yellow2** state, the controller turns on y_light (y_light=1) again, and then returns to **green** state.

The counter performs up counting operations. It will be reset as 0 when reset=1. When reset=0 and enable=1, the counter will increase its counting value by 1 on the rising edge of the clock. When counting value reaches the maximum value, the complete=1.

Implement the traffic light controller by VHDL. Your project report should

include the Quartus II project file containing the codes of the system.

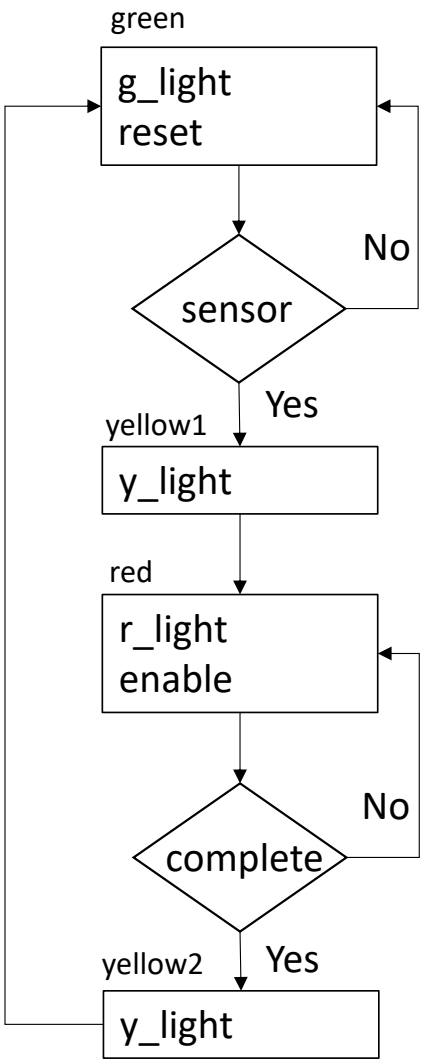
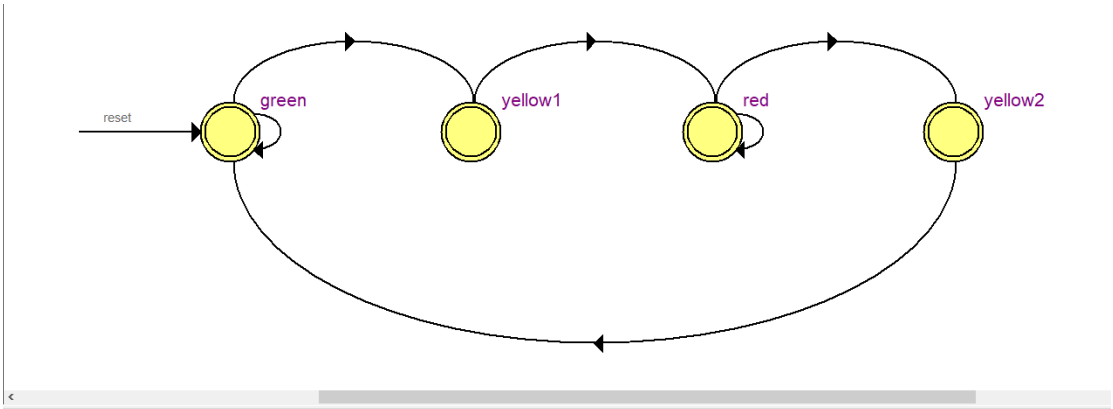


Figure 2. The ASM chart of the controller.

State Machine viewer:



	Source State	Destination State	Condition
1	green	green	(!sensor)
2	green	yellow1	(sensor)
3	yellow1	red	
4	red	red	(!complete)
5	red	yellow2	(complete)
6	yellow2	green	

Reference output:

(此為範例測資，同學可自行調整輸入內容)