

# FSP Example Project Usage Guide

User's Manual

Renesas RA Family

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## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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## Renesas RA Family

# FSP Example Project Usage Guide

## Contents

1. Introduction.....	1
1.1 Prerequisites.....	1
2. Hardware and Software Requirements .....	2
3. Tool Installation .....	2
3.1 FSP and tools installation.....	2
3.2 JFlashLite and JLink RTTViewer Installation .....	2
4. Importing and Running the Project .....	2
4.1 Downloading the Project .....	2
4.1.1 Downloading the Project from GitHub.....	2
4.1.2 Downloading the Project from Renesas.com.....	2
4.2 Running the project .....	2
4.2.1 Flashing pre-built binary .....	3
4.2.2 Importing the project into e2studio, Keil MDK and IAR.....	5
4.2.3 Running the Project.....	6
5. References .....	8
Appendix .....	9
Revision History .....	11

## 1. Introduction

This Example Project Usage Guide provides steps for running FSP example projects.

### 1.1 Prerequisites

1. Tool experience: It is assumed that the user has prior experience working with integrated development environments, such as e<sup>2</sup> studio, Segger RTT Viewer and terminal emulation programs, such as Tera Term.
2. Subject knowledge: It is assumed that the user has basic knowledge about microcontrollers, embedded systems, and FSP to modify the example projects. First time users must refer to FSP User Manual for Tutorial on *Starting Development*, paying special attention to sections *First RA MCU Project – Blinky*, *Importing an Existing Project into e2 studio*, and Tutorial on *Using HAL Drivers – Programming the WDT*. When working with Microcontrollers which have support for Arm® TrustZone® refer to section *Primer: TrustZone Project Development*.
3. Prior to running the example projects or programming the kits, default jumper settings must be used. Refer to the kits' user's manual for the default jumper settings.
4. The screen shots provided throughout this document are for reference. The actual screen content may differ depending on the version of software and development tools used.

## 2. Hardware and Software Requirements

This document provides general, high-level requirements for running the projects.

Refer to the readme.txt file in the specific module folder of `/example_projects` folder for additional hardware and software requirements for running the projects.

### Note:

1. Some projects may require external hardware as mentioned in the respective readme.txt files
2. Some pin numbers are printed on the back of the board.

### Software Requirements

- Windows® 10 operating system
- FSP v1.3.0 or later
- e<sup>2</sup> studio v2020-07 or later
- Keil MDK v5.31 or later
- IAR Embedded Workbench v.8.50.5 or later
- SEGGER J-Link RTTViewer v6.82d or later
- SEGGER J-Flash Lite v6.82d or later

## 3. Tool Installation

### 3.1 FSP and tools installation

Download and install the latest version of FSP and tools from FSP GitHub repository.

1. Open FSP GitHub repository: <https://github.com/renesas/fsp>
2. Go to the **Releases** section of Git and navigate to latest FSP section.
3. Follow the instructions on installing and using FSP and e<sup>2</sup> studio, Keil MDK and IAR.

### 3.2 JFlashLite and JLink RTTViewer Installation

Download and install SEGGER J-Link Software for Windows from

<https://www.segger.com/downloads/jlink#J-LinkSoftwareAndDocumentationPack>.

Default download path is C:\Program Files\SEGGER\JLink.

Note: Select version 6.82d or later from the drop-down menu in Version tab.

## 4. Importing and Running the Project

### 4.1 Downloading the Project

#### 4.1.1 Downloading the Project from GitHub

1. Open FSP Examples Repository: <https://github.com/renesas/ra-fsp-examples/releases>.
2. Navigate to **Assets** section of Examples for FSP v1.3.0.
3. Download the project files for specific kit.

#### 4.1.2 Downloading the Project from Renesas.com

1. Download the example project bundle for the specific kit from <https://www.renesas.com/us/en/products/software-tools/software-os-middleware-driver/software-package/ra-fsp.html#downloads>

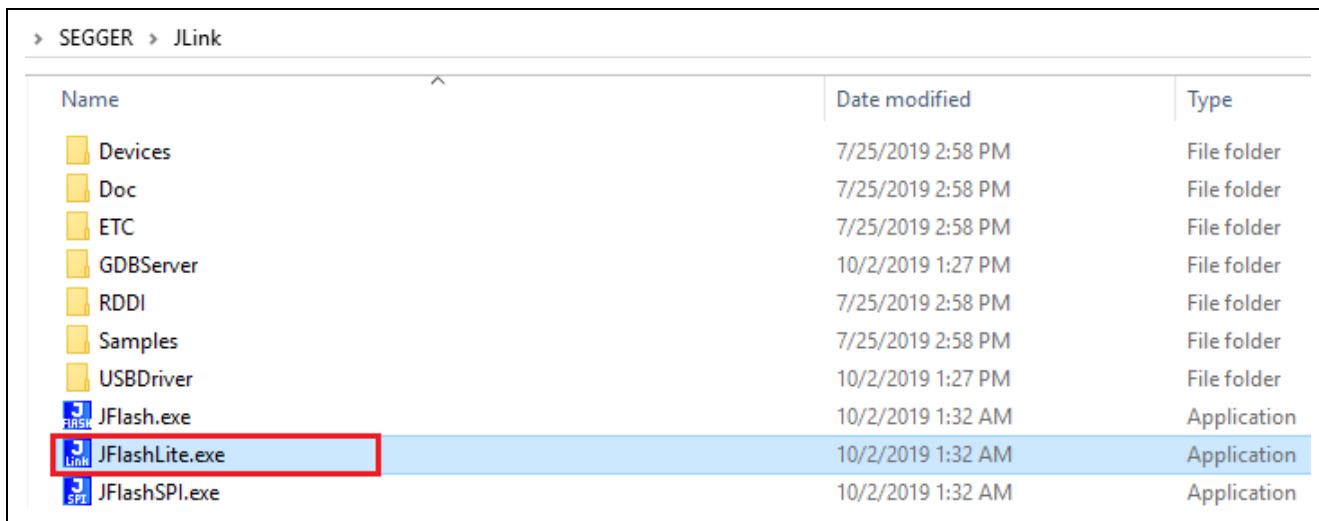
### 4.2 Running the project

There are two ways of running the project:

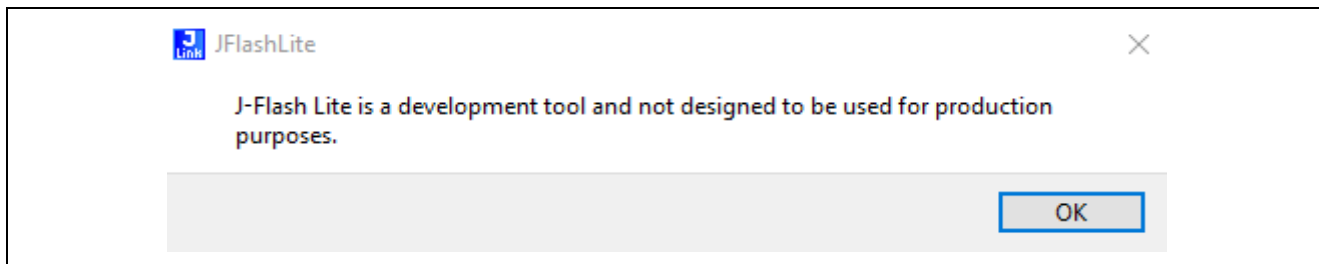
- Flashing the pre-built binary (.hex file) and running the project as explained in section 4.2.1.
- Importing the project into e<sup>2</sup> studio, building, loading and running the project as explained in section 4.2.2.

### 4.2.1 Flashing pre-built binary

1. In the **e2studio** folder of the module folders, a **.hex** file included.
2. Navigate to the downloaded /Segger/JLink folder and open JFlash Lite by double clicking on JFlashLite.exe.



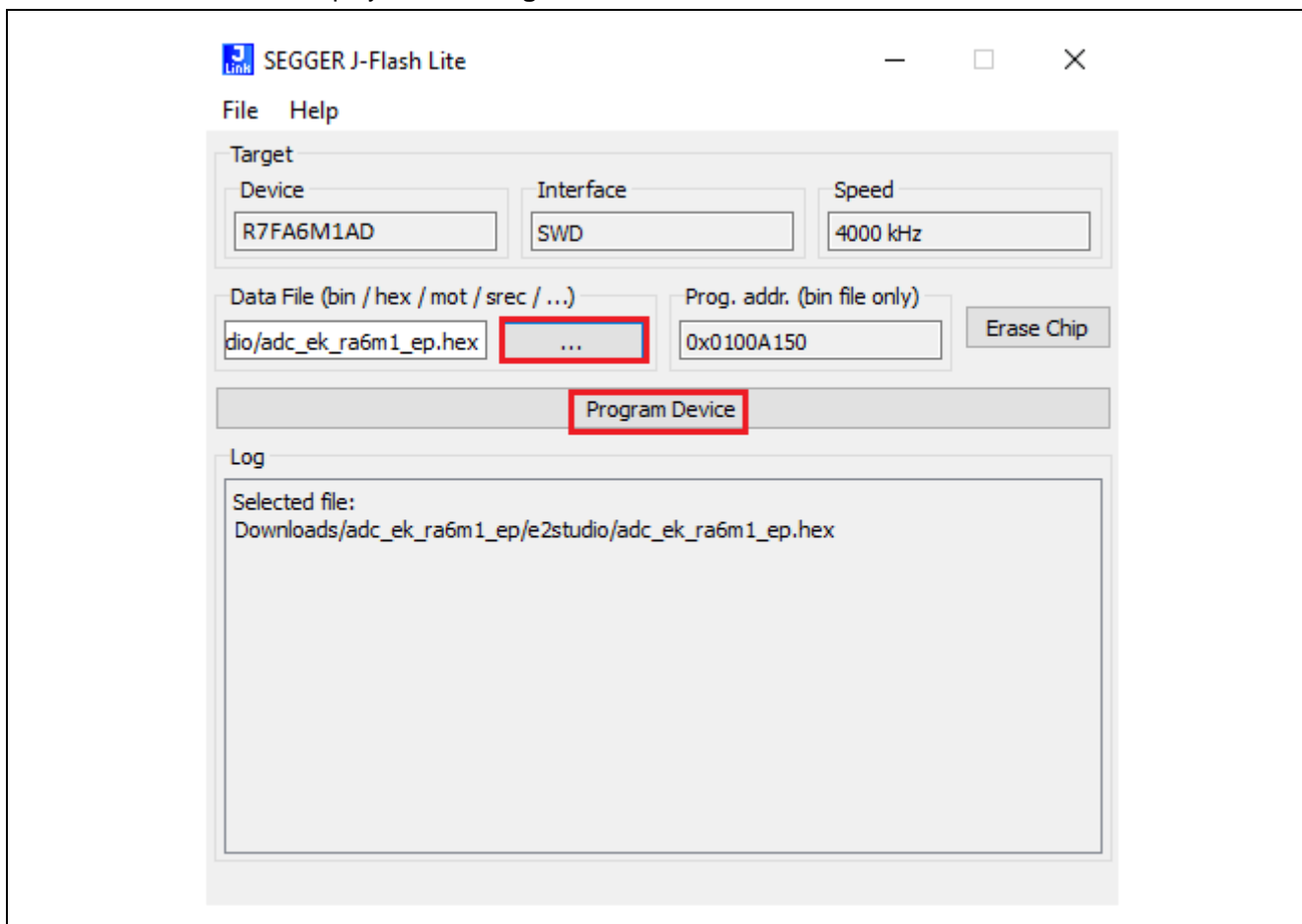
3. Click **OK** to get past the warnings.



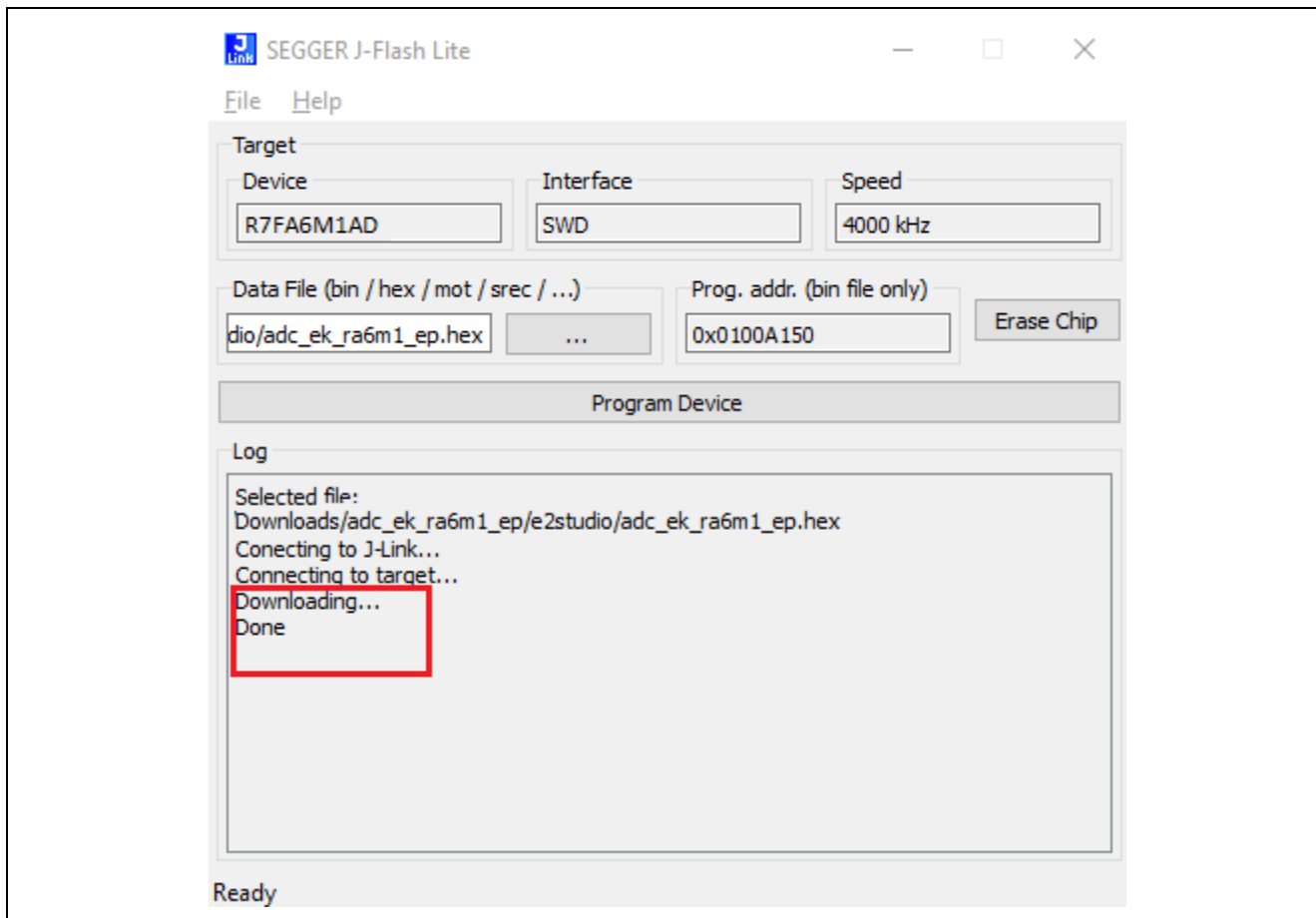
4. Click on the  tab for the list of supported devices and choose Renesas RA device. Click **OK**.



5. Browse to the location of the .hex file using the  tab and click on the **Program Device** tab. The selected file will be displayed in the **Log** section.



6. When downloading is complete, the status will be displayed as shown in the following figure.



7. Skip to section 4.2.3 for steps on running the project.

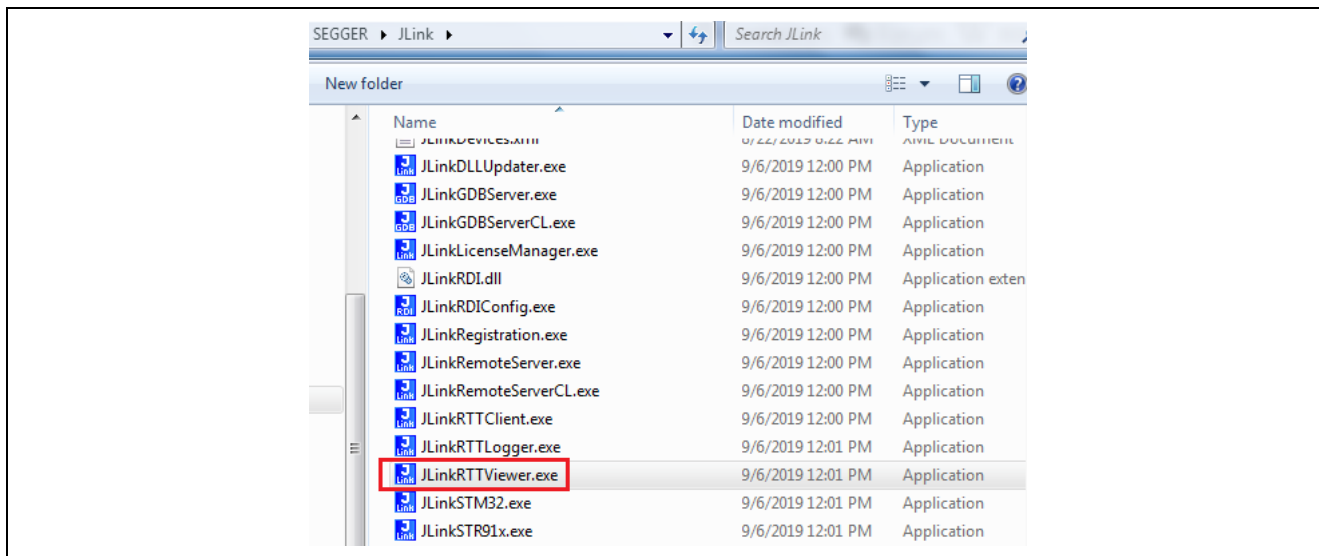
#### 4.2.2 Importing the project into e2studio, Keil MDK and IAR


Refer to FSP User Manual for steps on importing a project:

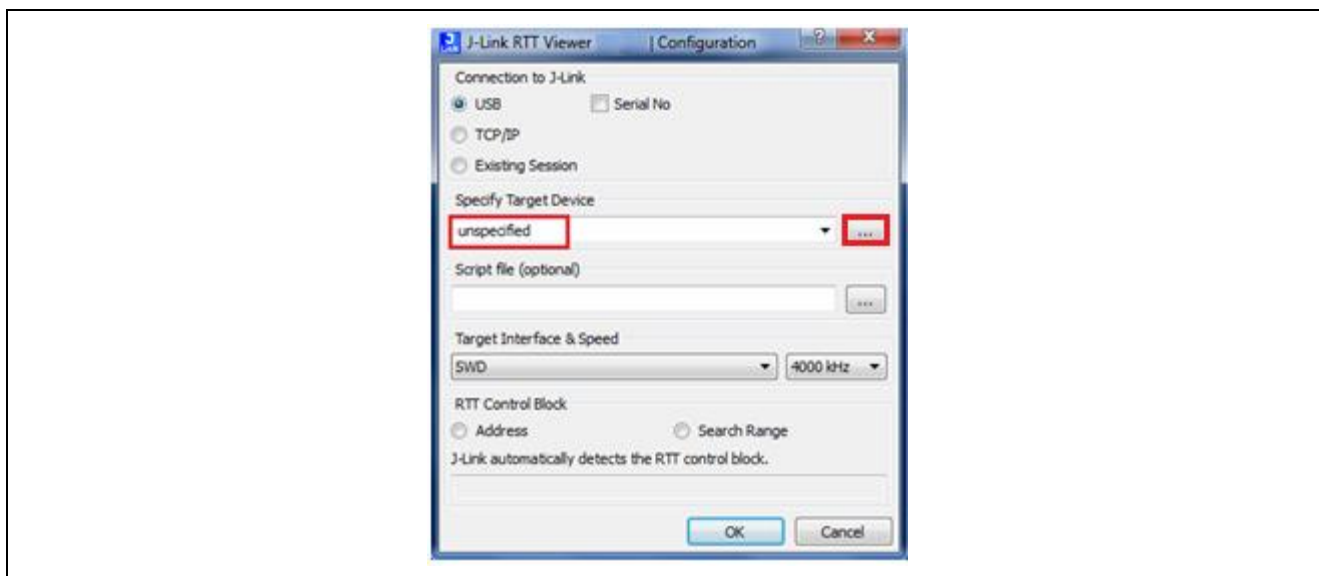
- Importing an existing project
- Generating Project content
- Building the project
- Downloading the project image to the board

### 4.2.3 Running the Project

1. Open RTT Viewer by double clicking `JLinkRTTViewer.exe` in the downloaded /Segger/JLink folder.



2. On opening, the field **Specify Target Device** shows up as **unspecified**. Click on the  tab to select the Renesas RA device.

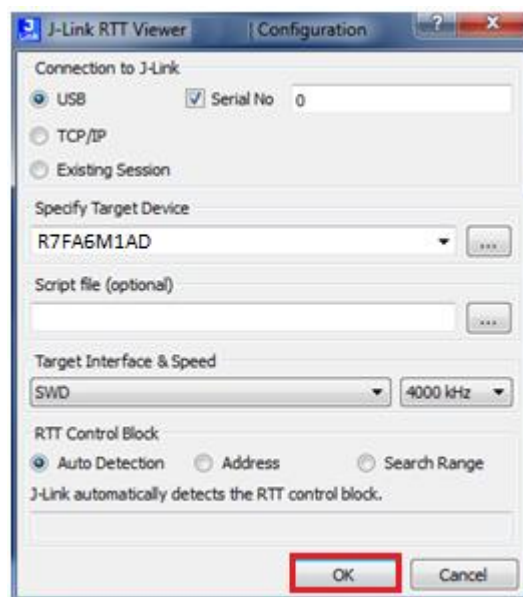




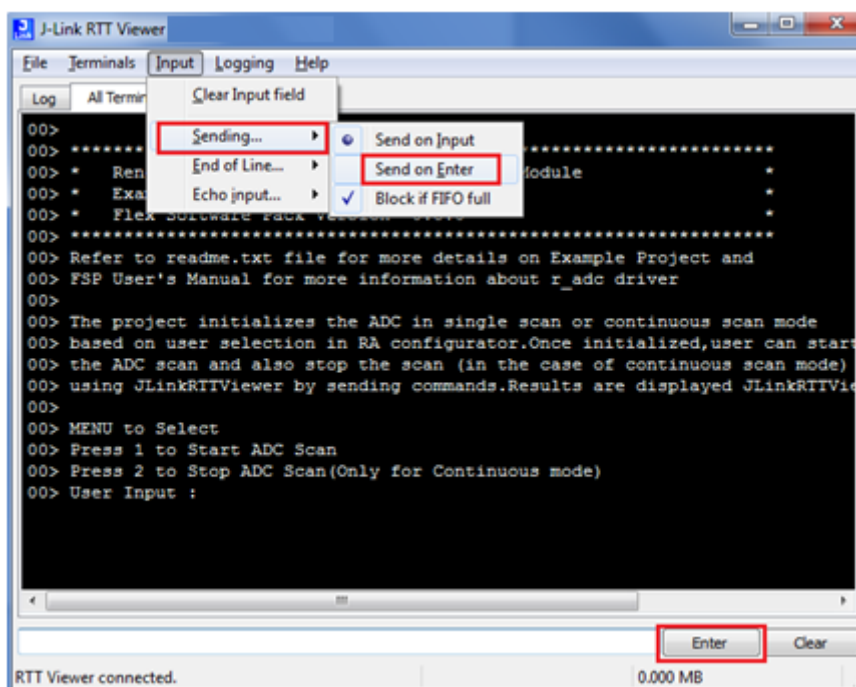
3. If multiple kits are connected to the PC, make sure to choose the corresponding serial number. The default is 0.



4. Click **OK**. (Refer Appendix).



5. Click on the **Input** tab and change **Sending** option to **Send on Enter**. Every time input is entered, you must either press the **Enter** or **Enter** tab on the RTT viewer.



6. Follow the instructions displayed on the RTT Viewer as shown above. Also refer to `readme.txt` file in the project folder (downloaded.zip file or in <https://github.com/renesas/ra-fsp>) to run the project.

**Note:**

1. Example Projects do not support floating point or special characters or any non-numeric characters.
2. Example projects do not handle cases where the user input is greater than the expected input array size.

## 5. References

FSP GitHub: <https://github.com/renesas/fsp>  
 FSP User Manual: [www.renesas.com/fsp#documents](http://www.renesas.com/fsp#documents)  
 FSP Example Projects: <https://github.com/renesas/ra-fsp-examples>  
 Evaluation Kit Manuals:

[www.renesas.com/ra/ek-ra6m3g](http://www.renesas.com/ra/ek-ra6m3g)  
[www.renesas.com/ra/ek-ra6m3](http://www.renesas.com/ra/ek-ra6m3)  
[www.renesas.com/ra/ek-ra6m2](http://www.renesas.com/ra/ek-ra6m2)  
[www.renesas.com/ra/ek-ra6m1](http://www.renesas.com/ra/ek-ra6m1)  
[www.renesas.com/ra/ek-ra4m1](http://www.renesas.com/ra/ek-ra4m1)  
[www.renesas.com/ra/ek-ra2a1](http://www.renesas.com/ra/ek-ra2a1)

Knowledge Base:

[Creating an RA Project with ARM Compiler 6 \(AC6\) in e2 studio](#)  
[Creating a Custom Board Support Package \(BSP\) for FSP](#)  
[www.keil.com/appnotes/docs/apnt\\_330.asp](http://www.keil.com/appnotes/docs/apnt_330.asp)

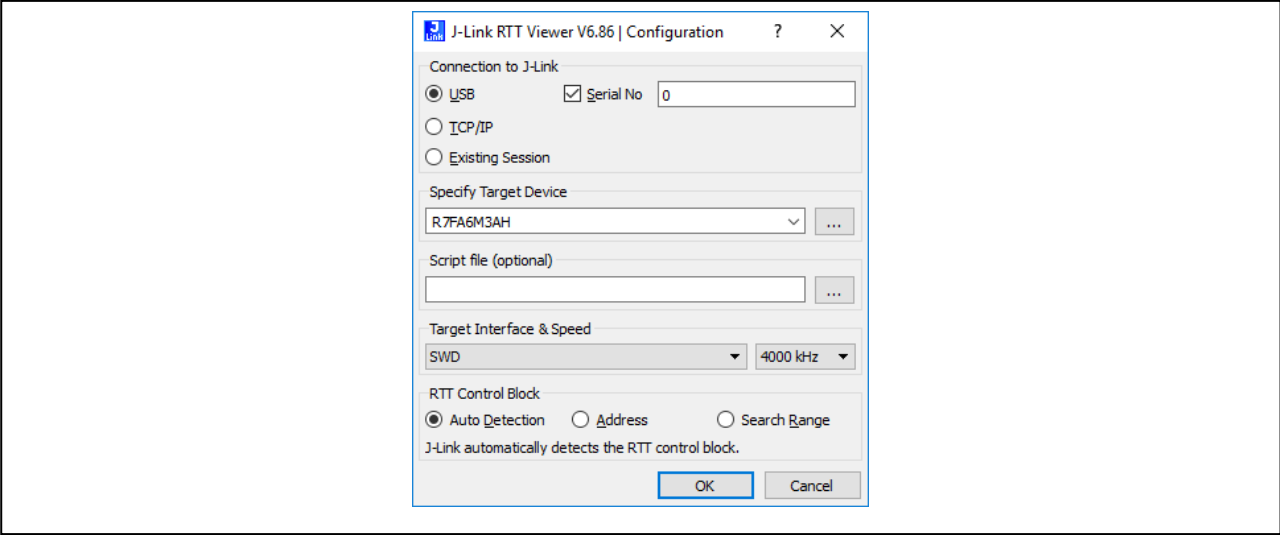
Support System:

[www.renesas.com/ra/support](http://www.renesas.com/ra/support)

Appendix

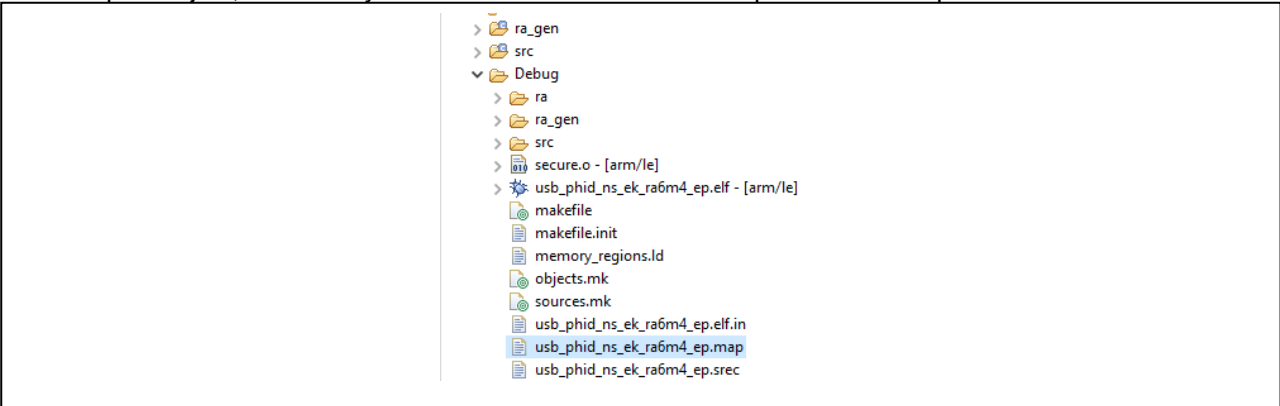
Limitations in connecting with J-Link RTT Viewer v6.86

When using Auto Detection option for the RTT Control Block, J-Link RTT Viewer may not be able to find the `SEGGER_RTT` variable in RAM memory. If the RTT Control Block cannot be found by RTT Viewer, then output from an Example Project may not be visible in the RTT Viewer Console.



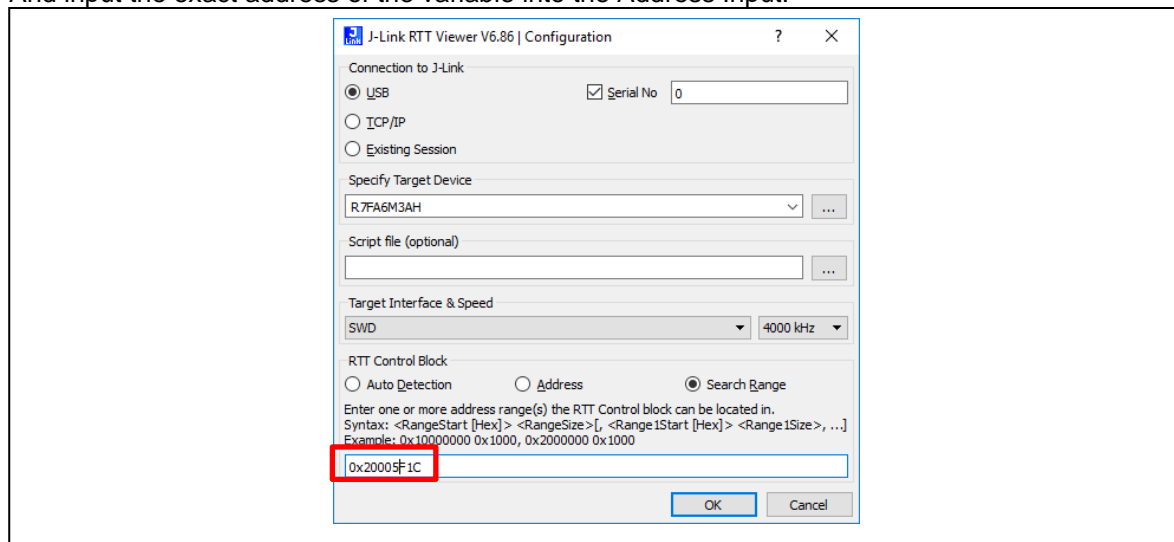
To circumvent this situation, you may use any one of the following approaches:

1. Search `_SEGGER_RTT` variable in the map file, generated upon successfully building a configuration of an Example Project, which is by default located in the address space for On-chip SRAM.

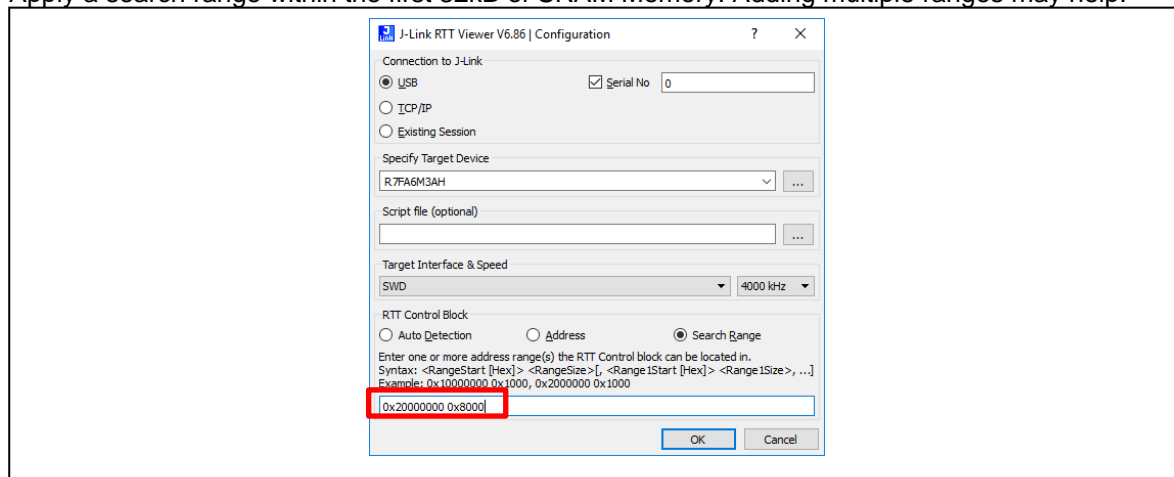


COMMON	0x20005f1c	0xa8	./src/SEGGER_RTT/SEGGER_RTT.o
	0x20005f1c		SEGGER_RTT
COMMON	0x20005fc4	0x51	./ra_gen/main.o
	0x20005fc4		g_fsp_common_initialized_semaphore_memory
	0x2000600c		g_fsp_common_thread_count

And input the exact address of the variable into the Address Input.



2. Apply a search range within the first 32kB of SRAM Memory. Adding multiple ranges may help.



**Revision History**

Rev.	Date	Description	
		Page	Summary
1.00	Oct.03.19	—	Initial release
1.01	May.26.20	—	Support for IAR, EK-RA4W1
1.02	Jul.08.20	—	Updates for FSP v1.2.0
1.03	Aug.27.20	—	Support for FSP v1.3.0
1.04	Oct.02.20	—	Support for FSP v2.0.0. Appendix for known limitations.

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