Virtual memory & MMU I CompSys304 – Computer Architecture

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Content

Principle

Address translation

Virtual memory

Motivation or problems solved

- Safe and efficient sharing of memory among multiple programs
 - Secure sharing
- ② Burden of programming for small, limited memories
 - Programs can exceed size of physical memory

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- Virtual address address used by CPU
- Physical address address in main memory
- Address translation mapping virtual to physical address

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OK, but why here, why not in OS course?

- Address translation done in CPU hardware (Memory Management Unit – MMU) and software
- Impact on CPU performance

Concepts

- Each program gets own address space (i.e. area)
 - Virtual memory exists in abundance
 - No other program is allowed to access this address space
 - ⇒ Protection of program's code and data from other programs

Concepts

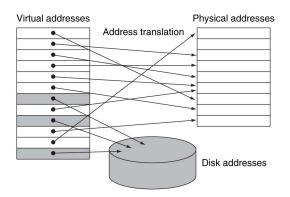
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- Main memory becomes cache of secondary memory (disks)
 - Indeed very similar to cache concept
- Virtual address has usually more bits than physical address
 - Idea of concept!
 - But less is also possible (32-bit CPU with more than 4GB RAM)

Principle of address translation

- Virtual address can be mapped to any physical address or disk location
- Address translation is process of doing this



Features

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Possible:

- 2 different virtual addresses can map to same physical address
 - To share code between programs

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Address translation

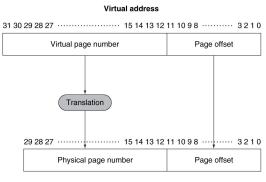
Address translation notation

- Page smallest block handled by virtual memory
 - Corresponds to cache line
- Page offset $f 2^f$ is size of page (in bytes)
 - On x86 CPUs (all?) $f = 12 \rightarrow \text{page size 4KByte}$
 - Support for 2/4MB pages on x86
- Page number number referencing page, index of page
- Page hit page is in main memory
 - Translation handled by MMU
- Page fault page is not in main memory
 - Virtual memory miss
 - Corresponds to cache miss
- Page fault handler function to handle a page miss
 - SW: part of OS kernel



Address translation

• Virtual address 32 bits, physical address 30 bits, page offset 12 bits



Physical address

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- Page faults can be handled by software
 - Disk access slow anyway, hardware not necessary
 - Advantage, clever placement algorithms can reduce page fault rate

Placement and retrieval

- Reduce page fault rate
 - ⇒ Fully associative placement of pages in memory
 - Virtual page can go into any physical page
- But, locating a page must be fast
- Use indexed table

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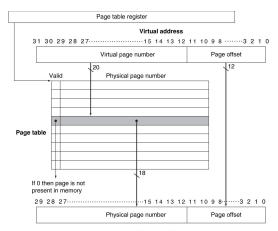
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Page table

- In main memory
- Every program (process) has own page table
- Virtual-physical pairs
 - also entries for not in memory (valid bit is false)
- Indexed with page number of virtual address
 - No searching necessary
- Page table register
 - MMU register: points to start of page table

Page table

- Table indexed by page number
 - $2^{20} = 1M$ entries, 4 bytes each $\Rightarrow 4MB$



Physical address

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- On 32-bit system, page table would require 4 MB
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 - or . . .
- Not discussed here
- ⇒ studied in Operating System design



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Approximation

- Use reference bit (ref bit)
 - Set when page is accessed
 - Periodically reset
 - Software takes snapshots before reset
 - Can build set of recently used pages
 - Evict page to swap space whose ref bit has not been set for some time