Time Report Project Week 3

Group 2

Finished tasks during the week:

- Design specification version 2.0
- Project plan version 2.0

Planned tasks for the coming week:

- VHDL coding for project
    - Dividing the block diagram so that 2 people per block are responsible for the code for the block.

Individual worked hours:

Student	Worked last week	Worked so far	Tasks done this week
Kebba Jeng	5	15	Address comments from supervisor; work on design specification and project plan version 2.0
Hannes Fröberg	5	15	Work on designspecification within decode. Started looking into the code for decode.
Ghady Al Haddad	5	15	Work on the settings block and a bit here and there with the required documents. Started looking into the code and testing a few options.
Martin Bildhjerd	5	15	Ports for the sig- gen is pretty much done. Also some analysing from labb4 documents, and some preliminary code have been added to the sig- gen part.
Aidin Jamshidi	5	15	Further work on GitLab. Research for VGA-, sig-gen- and settings-module. Some “pre” coding to test some features in mux.

How do this follow the time plan (in the project plan document)?

Everything is progressing according to schedule.