UNIVERSITY OF LAGOS
QUALITY ASSURANCE AND SERVICOM UNIT
OFFICE OF THE VICE CHANCELLOR
TEACHING WORKPLAN

Faculty:	Science
Department:	Computer Science
Session:	2017/2018
Semester:	First
Course Code:	CSC303
Title of Course:	Analysis and Design of Logic Circuits
Course Units:	3 units
Course Lecturers:	Dr. Ebun Phillip Fasina (EPF) Dr. B. A. Sawyerr (BAS)
Teaching Schedule:	Monday 10 a.m. - 12 noon
Venue:	Faculty Lecture Rm. E303

COURSE DESCRIPTION

In this course students are introduced to Boolean algebra and its application to logic gate design, minimization of Boolean functions and the design of combinational and sequential circuits. Various procedures and algorithms are introduced to simplify the design of digital circuits. Students are encouraged throughout the course to conceptualize and design logic circuits with useful applications.

LEARNING OUTCOMES

1. Understand the basic concepts of Boolean Algebra
2. Minimize digital functions using various approaches - Boolean algebra, K-maps and the Quine-McCluskey algorithm
3. Understand how to implement logic circuits with logic gates
4. Understand the function performed by standard combinational circuits such as adders, decoders, encoders, multiplexers, demultiplexers, comparators, subtractors, etc.
5. Formulate and solve problems using combinational circuits
6. Solve problems with SSI, MSI, LSI and VLSI logic circuits.
7. Understand the operation of latches and flip-flops
8. Understand the problems of sequential circuit design: State reduction and state assignment
9. Formulate and solve problems using sequential circuits
10. Recognize variants of registers and counters and understand how they function
11. Formulate and design registers and counters
12. Solve problems with registers and counters
13. Distinguish between ROM and RAM and understand their roles in logic circuit design
14. Understand ROM and RAM architectures
15. Design logic circuits using programmable logic arrays, programmable array logic and sequential programmable devices

COURSE RESOURCES

Required Textbook (On Reserve at the Main Library)

Mano, Morris M. and Michael D. Ciletti (2013) Digital Design: With an Introduction to the Verilog HDL, 5th Edition, Pearson Education, Inc., Prentice Hall, New Jersey 07458

Additional Textbooks

1 Hayes, John P. (1993) Introduction to Digital Logic Design, 1st Edition, Addison-Wesley

2 Perlman, David E., and James E. Palmer (1993) Schaum's Outline of Introduction to Digital Systems, 1st Edition, McGraw-Hill Education

3 Gajski, Daniel D. (1997) Principles of Digital Design, 1st Edition, Prentice Hall

COURSE CONTENT

WEEK	TOPIC	LECTURER(S)	REMARKS
1	**Digital Systems and Binary Numbers** Binary, Octal and Hexadecimal Numbers, Number-Base Conversions, Complement of Numbers, Binary Number Representation, Binary Codes, Binary Logic, Storage and Registers	BAS	
2	**Boolean Algebra** Basic Definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems of Boolean Algebra, Properties of Boolean Algebra,	BAS	
3	**Boolean Functions, Logic Gates and Logic Circuits** Boolean Functions, Canonical and Standard Forms, Logic Operations, Digital Logic Gates, Integrated Circuits	BAS	
4	**Gate-Level Minimization I** The Map Method (Sum-of-Products Simplification), Four-, Five- and Six-Variable K-Maps, Product-of-Sums Simplification, Don't-Care Conditions	BAS	
5	**Continuous Assessment** I – MCQ Test **Tutorial**	BAS	
6	**Gate-Level Minimization II** Quine-McCluskey Minimization Algorithm	BAS	
7	**Combinational Logic** Combinational Circuits, Analysis Procedure, Design Procedure, Binary Adder-Subtractor, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Priority Encoders, Multiplexers	EPF	
8	**Storage Elements** Asynchronous and Synchronous SR and D Latches, JK and T Flip-flops	EPF	
9	**Sequential Circuits** Analysis of Clocked Sequential Circuits, State Reduction, State Assignment, Design of Synchronous Sequential Circuits	EPF	
10	**Continuous Assessment** II – MCQ Test **Tutorial**	EPF	
11	**Registers** Registers, Shift Registers	EPF	
12	**Counters** Binary and BCD Ripple Counters, Binary and BCD Synchronous Counters, Counters with Unused States, Ring Counters, Johnson Counters	EPF	
13	**Memory** Read-Only Memory, Random Access Memory, Memory Decoding	EPF	

14	**Programmable Logic** Programmable Logic Array, Programmable Array Logic, Sequential Programmable Devices	EPF	
15	**Revision**	EPF/BAS	
16	**Examination**	EPF/BAS	
17	**Examination**	EPF/BAS	

COURSE AND UNIVERSITY POLICIES:

Attendance

Students enrolled in each course are expected to make **65% attendance** at lectures in order to be eligible for examination.

Evaluation

Continuous Assessment:	**Subtotal**	**40 marks**
MCQ Test I (1 hour)		15 marks
MCQ Test II (1 hour)		15 marks
Term Project – Implementation of the Quine-McCluskey Exact Logic Minimizer with Java or C# (2 weeks)		10 marks
Examinations:	**Subtotal**	**60 marks**
Examination (2 hours) – Answer 3 questions (40 minutes each) from 5 questions		
Final Marks:	**Total**	**100 marks**

Signature of Lecturers

Dr. B. A. Sawyerr

Dr. E. P. Fasina

Head of Department

Dr. B. A. Sawyerr