Department of Electrical Engineering

Faculty Member: MISS RAFIA **Dated: 25 – 02 - 25**

Semester: 2ND **Section:BS DS 02A**

Group No.:

EE-221: Digital Logic Design

Lab 5: Minimization of Boolean Functions

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance** **5 Marks**	**Analysis of data in Lab Report** **5 Marks**	**Modern Tool Usage** **5 Marks**	**Ethics and Safety** **5 Marks**	**Individual and Team Work** **5 Marks**	**Total marks Obtained** **25 Marks**
AILYA ZAINAB	**523506**						
IMAN NAEEM	**525378**						
LAIBA NASIR	**510419**						
LUQMAN SHEHZAD	**507599**						

Lab 5: Minimization of Boolean Functions

This Lab has been divided into two parts.

The first part is the hardware implementation of a Boolean function given to you. But you have to first minimize the Boolean functions to minimum number of literals.

In next part you will simulate the same circuit using Verilog.

Objectives:

- ✓ Understand Minimization of Boolean Functions
- ✓ Simulate Basic Circuits using Verilog
- ✓ Hardware Implementation of Basic Logic Circuits

Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation. Alternately each group to upload completed lab report on LMS for grading.
- ✓ The students will start lab task and demonstrate design steps separately for step-wise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab
- ✓ There are related questions at the end of this activity. Give complete answers.

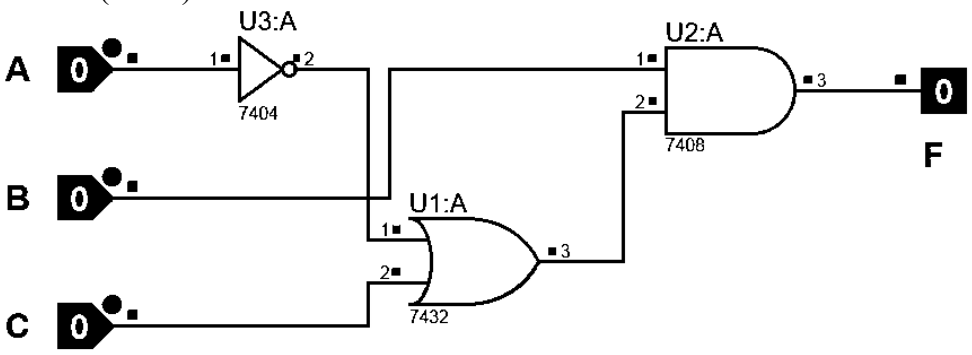
.

Pre-Lab Tasks (2 marks)

1. Write the Boolean expression of the following two functions. Simplify the expression using algebraic manipulation and draw the **logic diagram**.

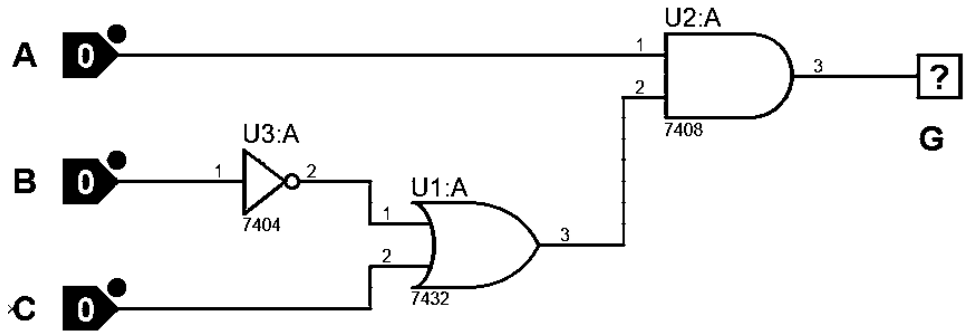
F (A, B, C) = ∑ (2, 3, 7)

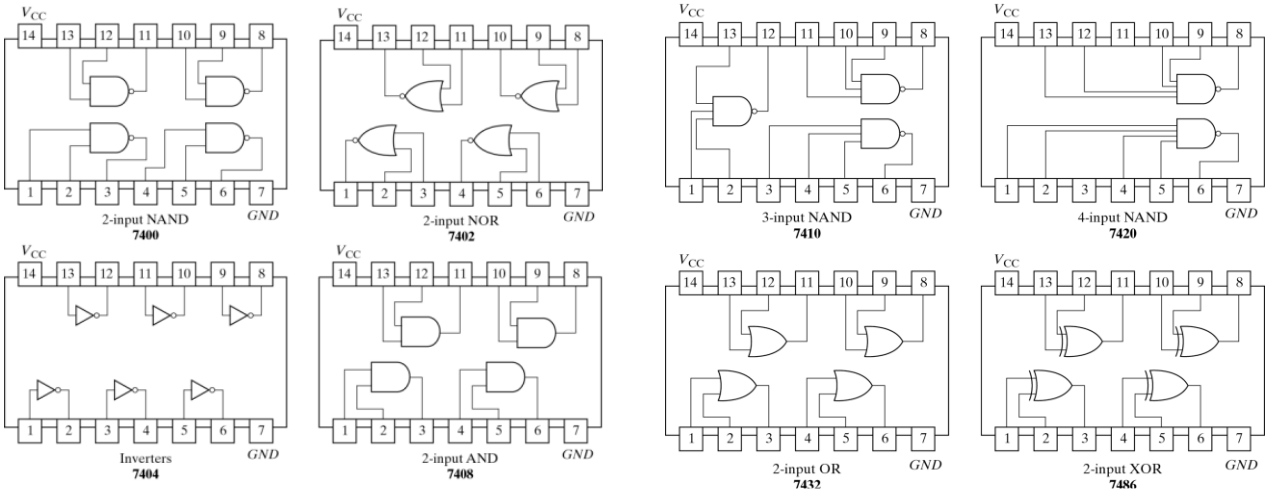
⇒ A'BC' + A'BC + ABC
⇒ A'BC' + BC(A + A')
⇒ A'BC' + BC(1)
⇒ A'BC' + BC
⇒ B(A'C'+C)
⇒ B(A'+C)
⇒ A'B+BC
⇒ B(A'+C)



G (A, B, C) = ∑ (4, 5, 7)

⇒ AB'C' + AB'C + ABC
⇒ AB'C' + AC(B'+B)
⇒ AB'C' + AC(1)
⇒ AB'C' + AC
⇒ A(B'C'+C)
⇒ A(B'+C)
⇒ AB'+AC
⇒ **A(B'+C)**


A
0
B
0
C
0
U3:A
1
2
7404
U1:A
1
2
3
7432
U2:A
1
2
3
7408
?
G



Lab Tasks (8 marks)

Lab Task 1: (5)

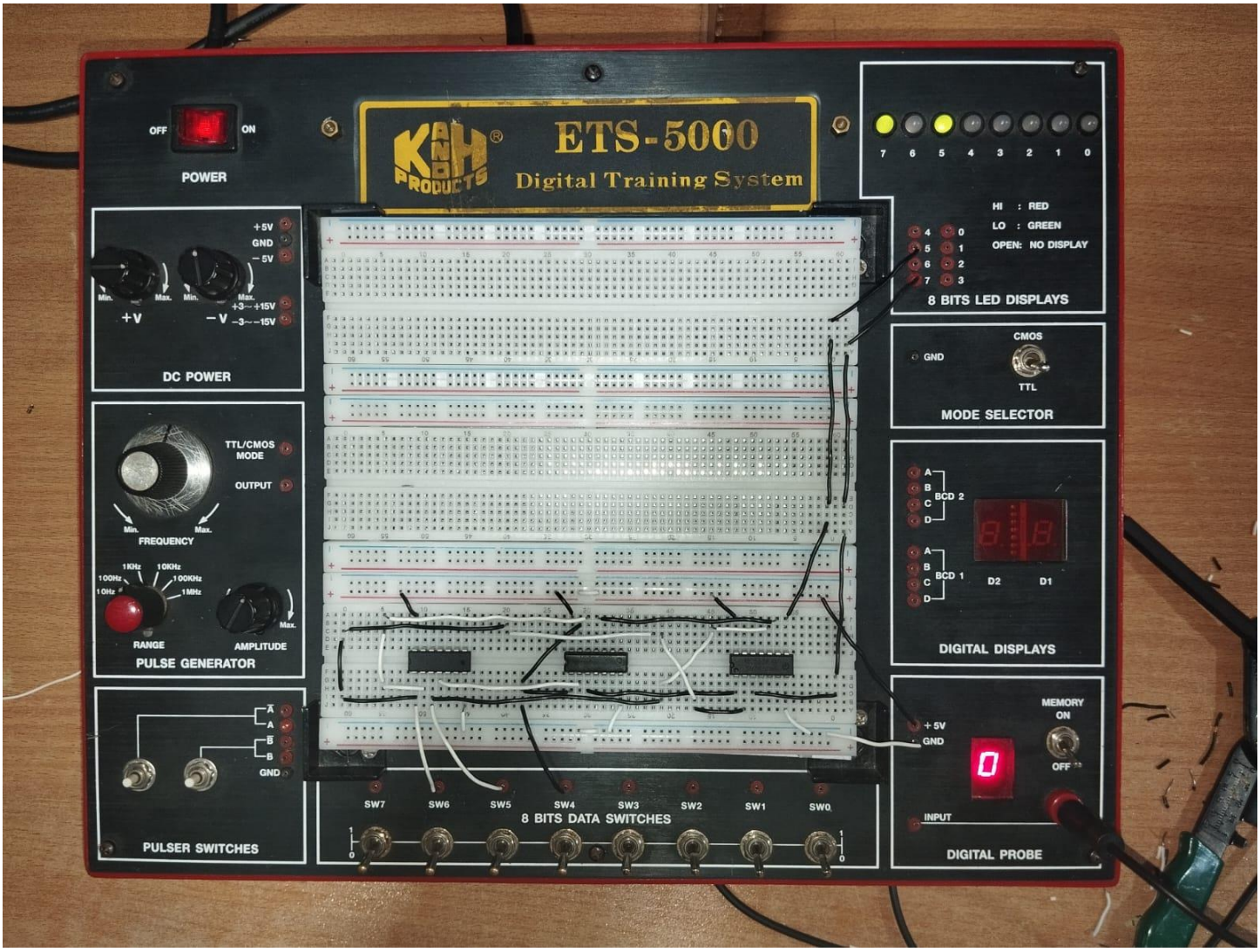
Implement the Boolean functions in hardware you simplified in your Pre-Lab Task. Make truth table and run the simulation in Proteus. Mention what and how many gates you would be using?

Truth Table:

A	B	C	G
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Hardware SS (3)



INPUT: 000

OUTPUT: 00

INPUT: 001

OUTPUT: 00

INPUT: 010

OUTPUT: 10

INPUT: 011

OUTPUT: 10

INPUT: 100

OUTPUT: 10


ETS-5000
Digital Training System
KANDI PRODUCTS
POWER
OFF
ON
DC POWER
+5V
GND
−5V
+V
−V
8 BITS LED DISPLAYS
HI : RED
LO : GREEN
OPEN: NO DISPLAY
MODE SELECTOR
CMOS
TTL
GND
PULSE GENERATOR
TTL/CMOS MODE
OUTPUT
FREQUENCY
RANGE
AMPLITUDE
DIGITAL DISPLAYS
BCD 2
BCD 1
D2
D1
PULSER SWITCHES
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
DIGITAL PROBE
MEMORY ON
INPUT

INPUT: 101

OUTPUT: 10


ETS-5000
Digital Training System
KNOBIT PRODUCTS
POWER
OFF
ON
DC POWER
+5V
GND
−5V
+V
−V
+3~+15V
−3~−15V
PULSE GENERATOR
TTL/CMOS MODE
OUTPUT
FREQUENCY
RANGE
AMPLITUDE
PULSER SWITCHES
GND
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
8 BITS LED DISPLAYS
HI : RED
LO : GREEN
OPEN: NO DISPLAY
MODE SELECTOR
CMOS
TTL
GND
DIGITAL DISPLAYS
BCD 2
BCD 1
D2
D1
DIGITAL PROBE
MEMORY ON
OFF
INPUT

INPUT: 100

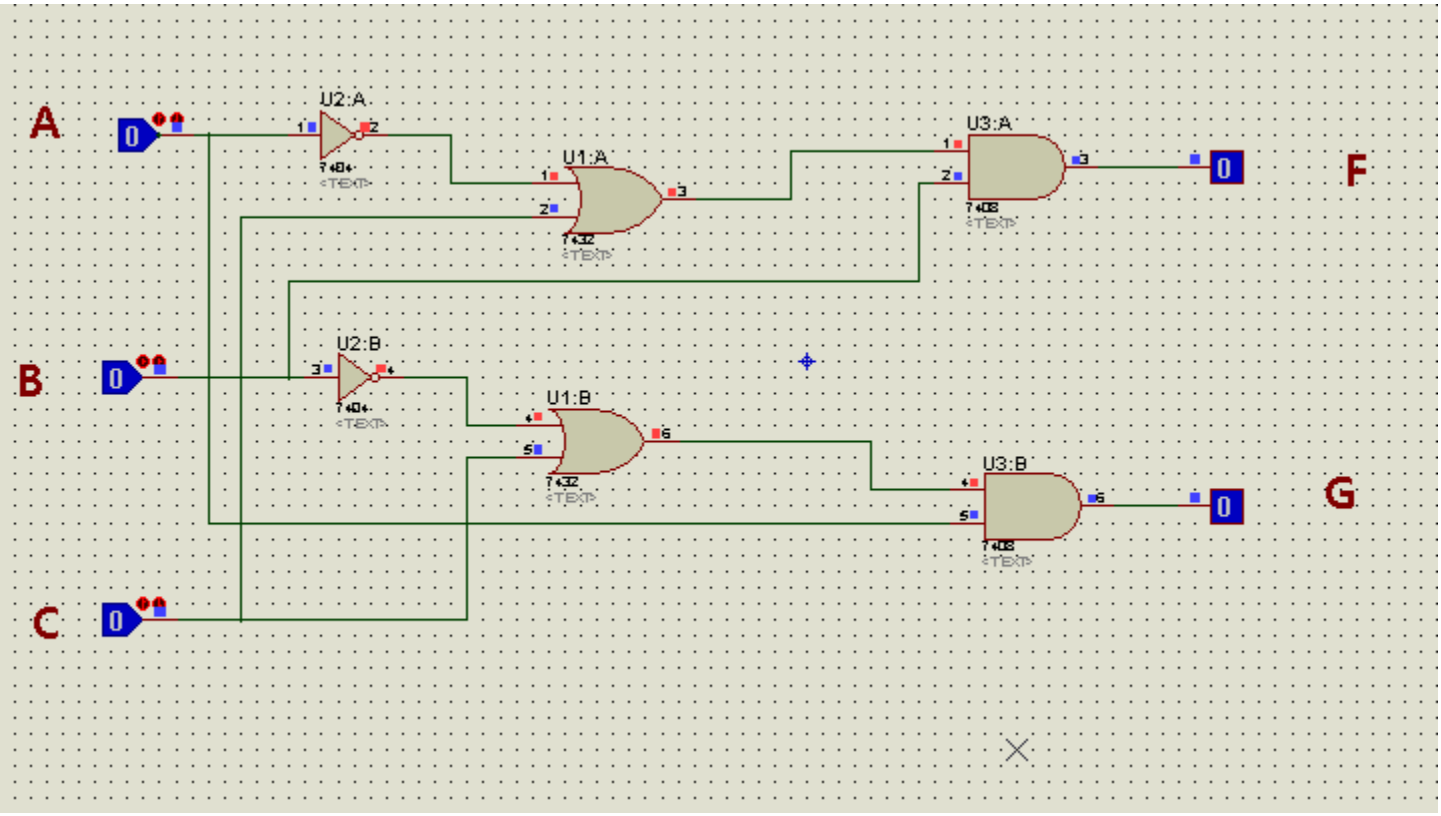
OUTPUT: 00

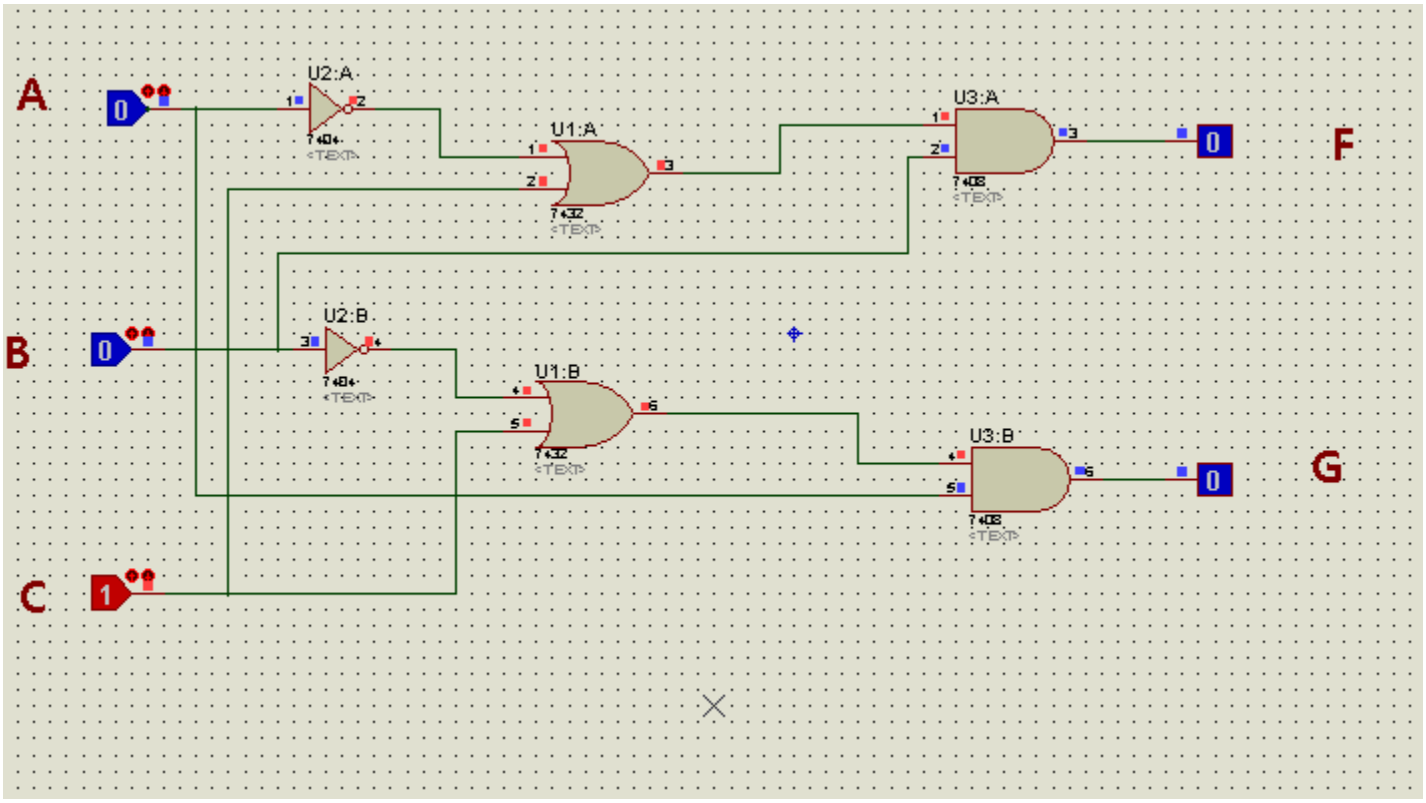

ETS-5000
Digital Training System
KANDH PRODUCTS
POWER
OFF
ON
DC POWER
+5V
GND
−5V
+3~+15V
−3~−15V
PULSE GENERATOR
TTL/CMOS MODE
OUTPUT
FREQUENCY
RANGE
AMPLITUDE
PULSER SWITCHES
GND
8 BITS LED DISPLAYS
HI : RED
LO : GREEN
OPEN: NO DISPLAY
MODE SELECTOR
CMOS
TTL
DIGITAL DISPLAYS
BCD 2
BCD 1
D2
D1
DIGITAL PROBE
MEMORY ON
INPUT
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0

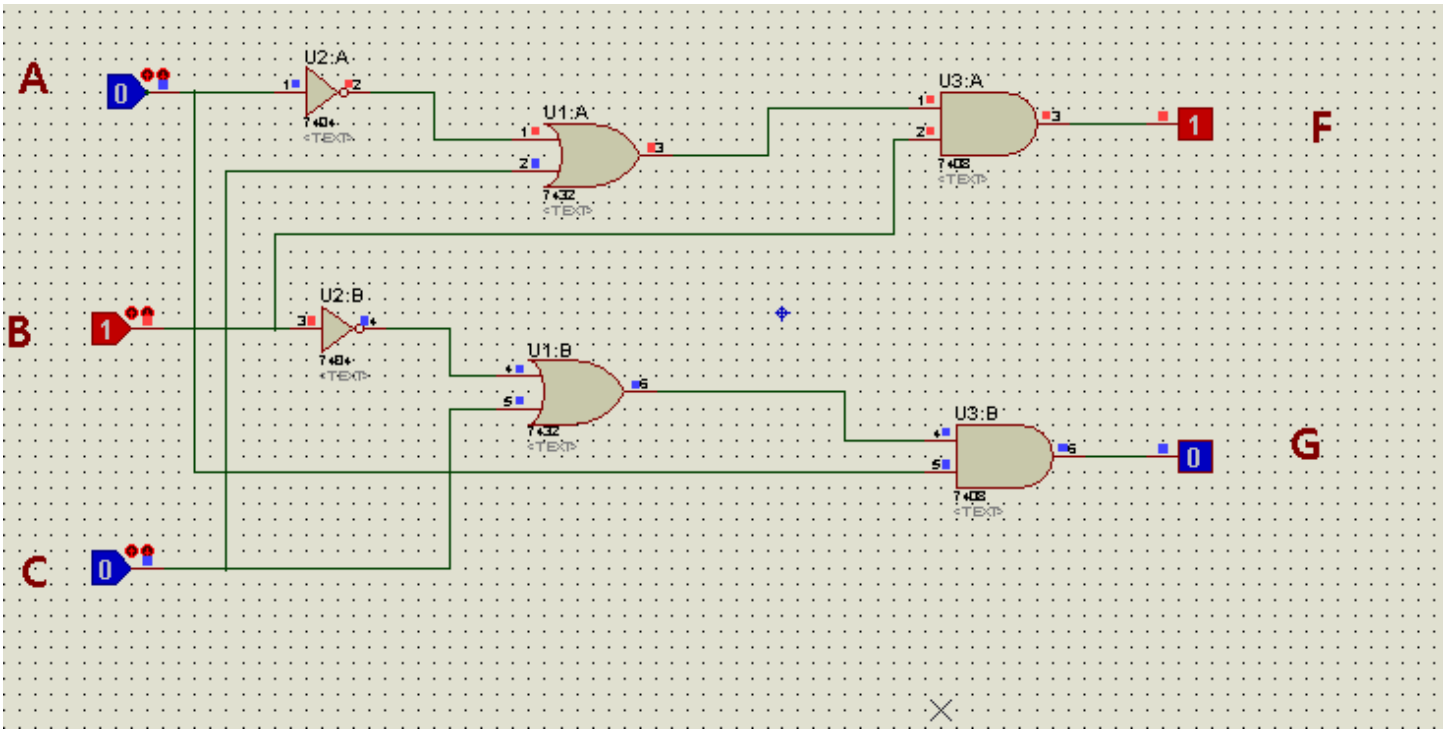
INPUT: 111

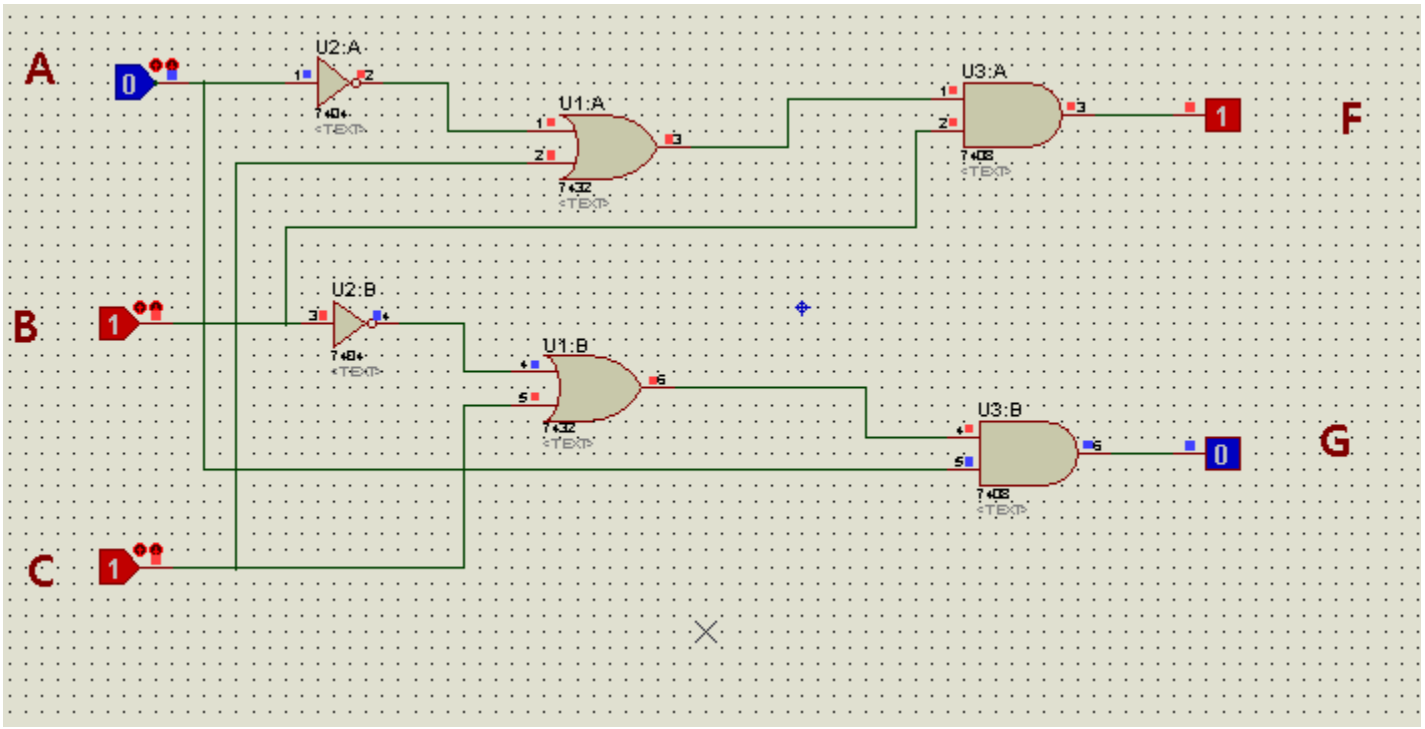
OUTPUT: 11

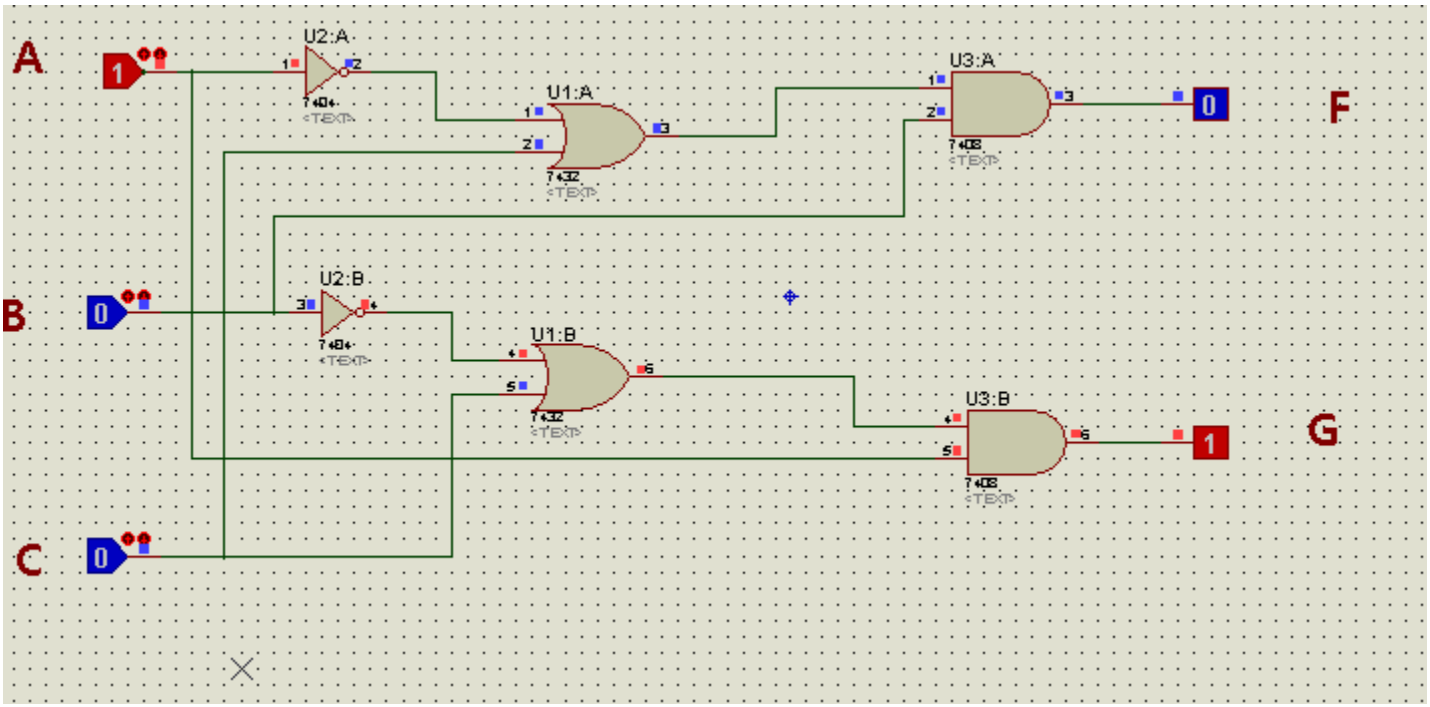
Proteus Simulation (2)

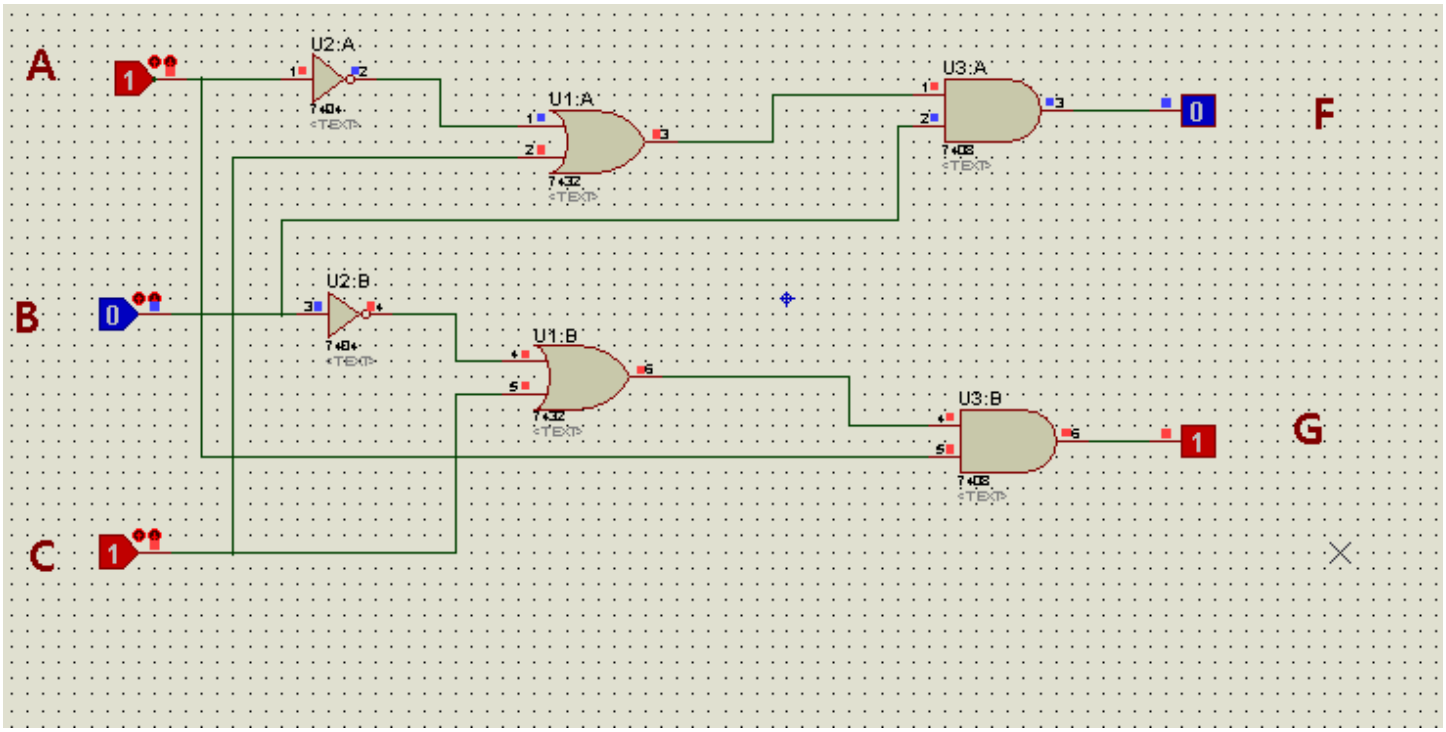


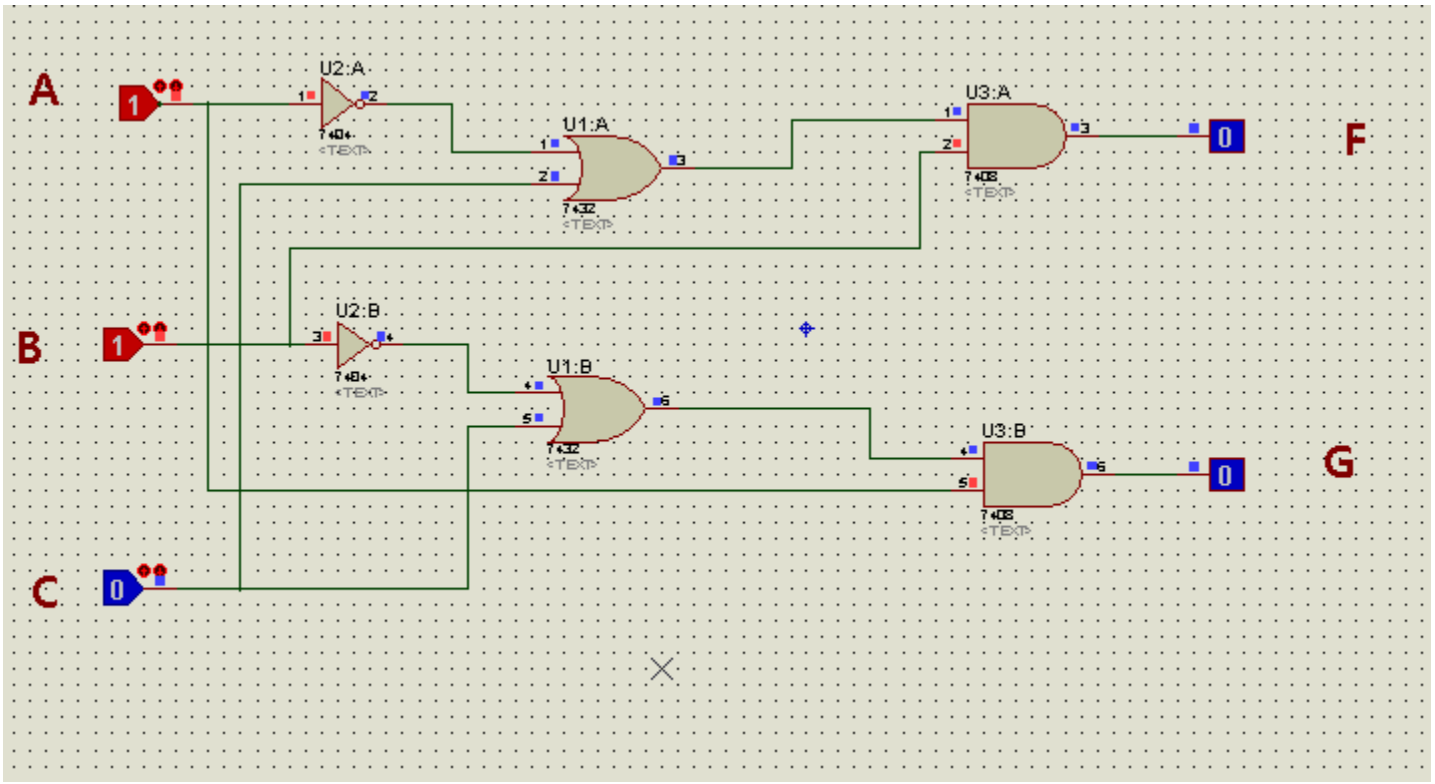

A
B
C
F
G
U2:A
U2:B
U1:A
U1:B
U3:A
U3:B
7404
7432
7408
<TEXT>
0
1

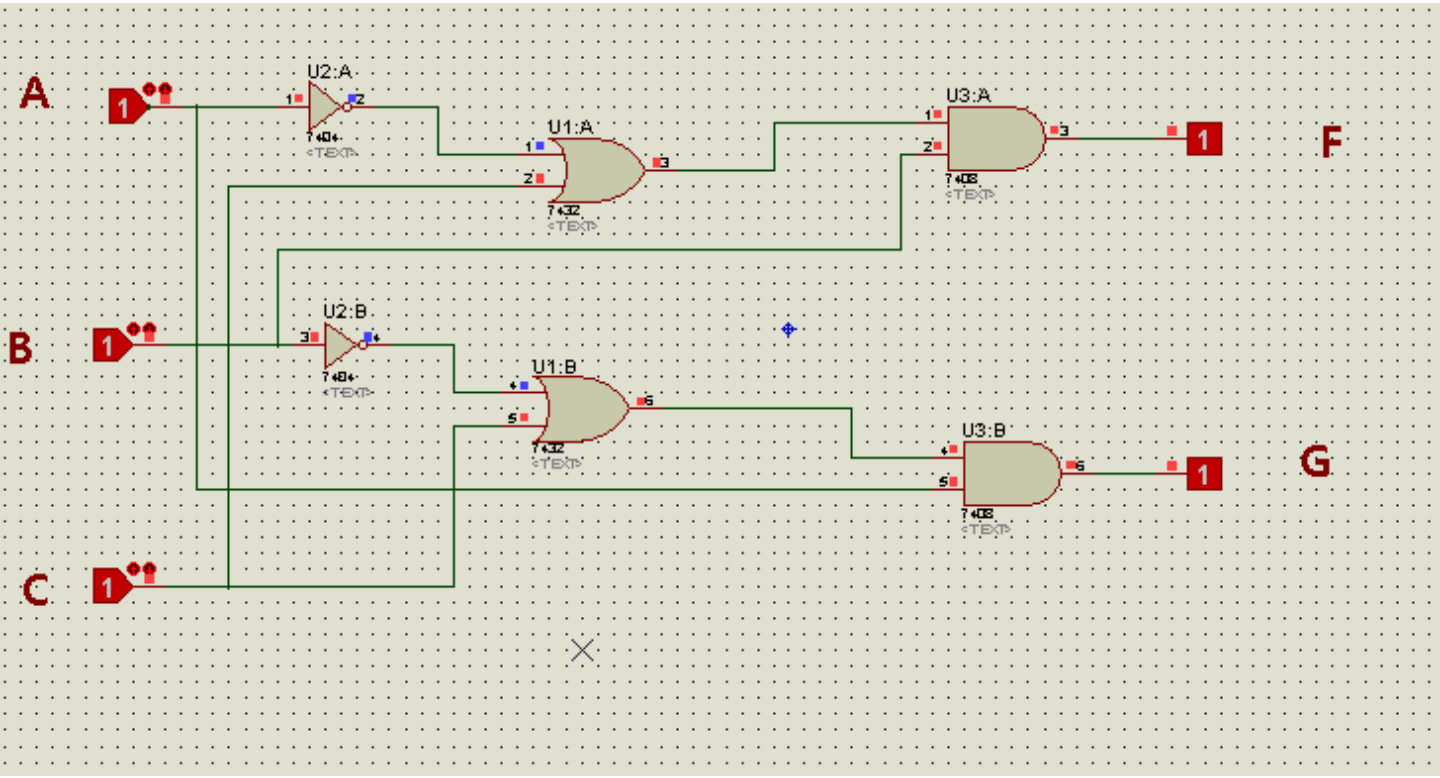

A
B
C
F
G
U2:A
U2:B
U1:A
U1:B
U3:A
U3:B
7404
7432
7408
<TEXT>
0
1


A
B
C
F
G
U2:A
U1:A
U3:A
U2:B
U1:B
U3:B
7404
7432
7408
<TEXT>
0
1


A
B
C
F
G
U2:A
U1:A
U3:A
U2:B
U1:B
U3:B
7404
7432
7408
<TEXT>
0
1


A
B
C
F
G
U2:A
U1:A
U3:A
U2:B
U1:B
U3:B
7404
7432
7408
<TEXT>


A
B
C
F
G
U2:A
U1:A
U3:A
U2:B
U1:B
U3:B
7404
7432
7408
<TEXT>



Lab Task 2: (3)

Write Verilog code for the minimized functions at gate-level and perform simulation. Attach the relevant snapshots below.

CODE IN VERILOG

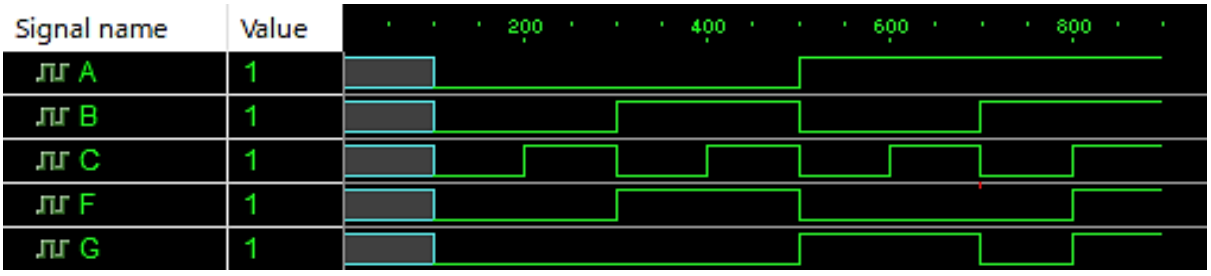
```
module task01(A, B, C, F);
```

```
input A, B, C;
output F;
wire w1, w2;
not n1(w1, A);
or o1(w2, w1, C);
and a1(F, w2, B);
endmodule

module testTask01;


reg a, b, c;
wire f, g;
taskLab05 t1(a, b, c, f);
taskLab05 t2(b, a, c, g);
initial
begin
a=1'b0; b=1'b0; c=1'b0;
#100 a=1'b0; b=1'b0; c=1'b1;
#100 a=1'b0; b=1'b1; c=1'b0;
#100 a=1'b0; b=1'b1; c=1'b1;
#100 a=1'b1; b=1'b0; c=1'b0;
#100 a=1'b1; b=1'b0; c=1'b1;
#100 a=1'b1; b=1'b1; c=1'b0;
#100 a=1'b1; b=1'b1; c=1'b1;
end
endmodule
```

VERILOG CODE:

```
 1 module task01(A, B, C, F);
 2 input A, B, C;
 3 output F;
 4 wire w1, w2;
 5 not n1(w1, A);
 6 or o1(w2, w1, C);
 7 and a1(F, w2, B);
 8 endmodule
 9
10 module testTask01;
11 reg a, b, c;
12 wire f, g;
13 taskLab05 t1(a, b, c, f);
14 taskLab05 t2(b, a, c, g);
15 initial
16 begin
17 a=1'b0; b=1'b0; c=1'b0;
18 #100 a=1'b0; b=1'b0; c=1'b1;
19 #100 a=1'b0; b=1'b1; c=1'b0;
20 #100 a=1'b0; b=1'b1; c=1'b1;
21 #100 a=1'b1; b=1'b0; c=1'b0;
22 #100 a=1'b1; b=1'b0; c=1'b1;
23 #100 a=1'b1; b=1'b1; c=1'b0;
24 #100 a=1'b1; b=1'b1; c=1'b1;
25 end
26 endmodule
```

WAVE OUTPUT:



Observations/Comments:

In this lab, we implemented a logical circuit that is more optimal than its original counterpart, i.e. we simplified the sum of **standard minterms** to reduce and minimize the use of gates, essentially making it both efficient and cost effective.

We have also confirmed/verified the circuit's output as it conforms to the truth table laid out in the Pre – lab and that it serves the purpose for what it was designed conclusively.
