Department of Electrical Engineering

Faculty Member:_____ **Dated:** _____

Semester:_____ **Section:** _____

Group No.:

EE-221: Digital Logic Design

Lab 9: 2-bit binary Adder and Subtractor

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance** **5 Marks**	**Analysis of data in Lab Report** **5 Marks**	**Modern Tool Usage** **5 Marks**	**Ethics and Safety** **5 Marks**	**Individual and Team Work** **5 Marks**	**Total marks Obtained** **25 Marks**
AILYA ZAINAB	**523506**						
IMAN NAEEM	**525378**						
LAIBA NASIR	**510419**						
LUQMAN SHEHZAD	**507599**						

Lab 9: 2-bit binary Adder and Subtractor

This Lab Activity has been designed to familiarize the students with design and working of binary adders using basic logic gates.

Objectives:

- ✓ Design and Implementation of Half Adder
- ✓ Design and Implementation of a Full Adder using Half Adders
- ✓ Extending the design to add 2-bit binary numbers
- ✓ Verification of 4-bit adder IC
- ✓ Gate-Level Verilog code for 4-bit adder

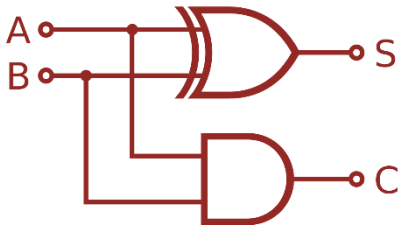
Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation. Alternately each group to upload completed lab report on LMS for grading.
- ✓ The students will start lab task and demonstrate design steps separately for step-wise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ **The Total duration for the lab is 3 hrs.**
- ✓ **A lab with in-complete lab tasks will not be accepted.**
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
- ✓ There are related questions at the end of this activity. Give complete answers.

Lab Tasks (10)

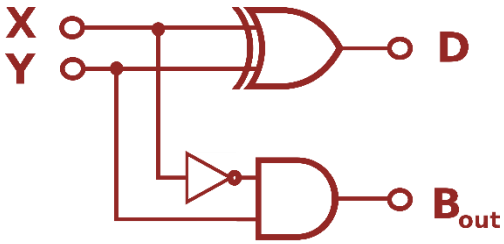
1. Give the truth table and circuit for half adder and half subtractor. (0.5)

HALF ADDER:



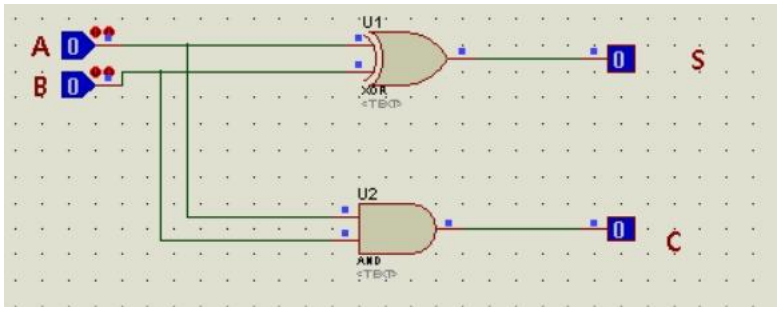
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

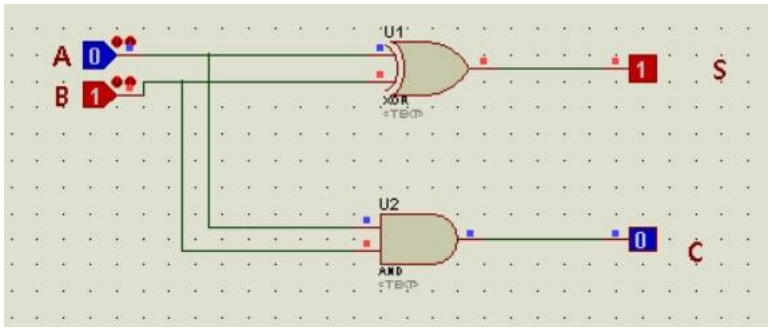
HALF SUBTRACTOR:

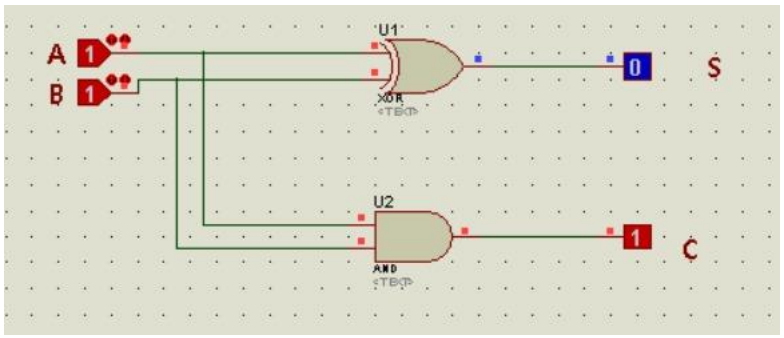


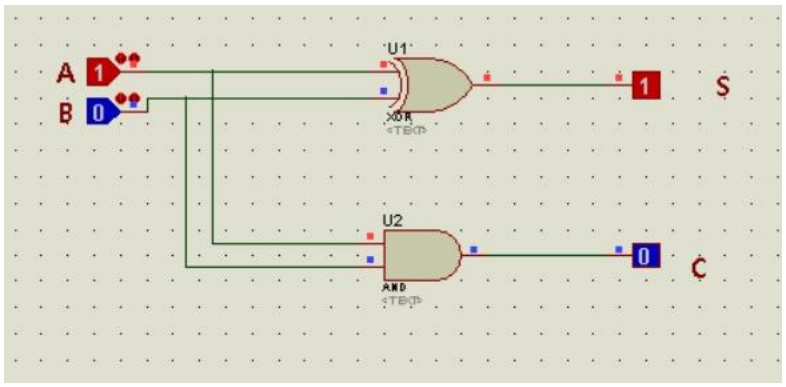
X	Y	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

HALF ADDER

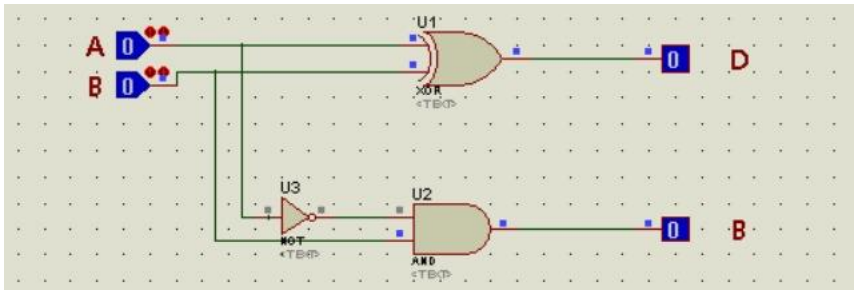


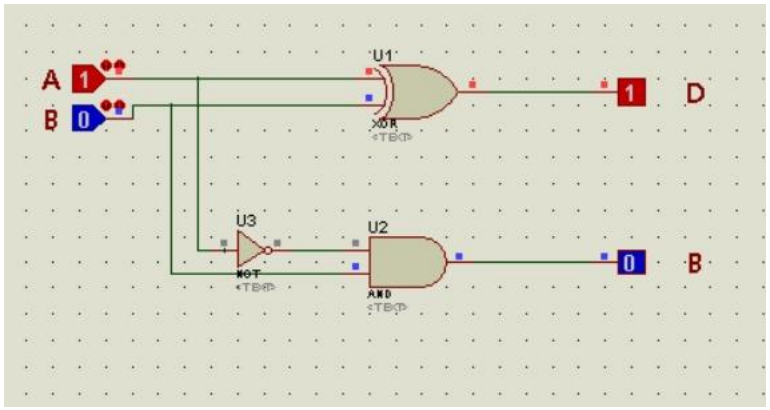




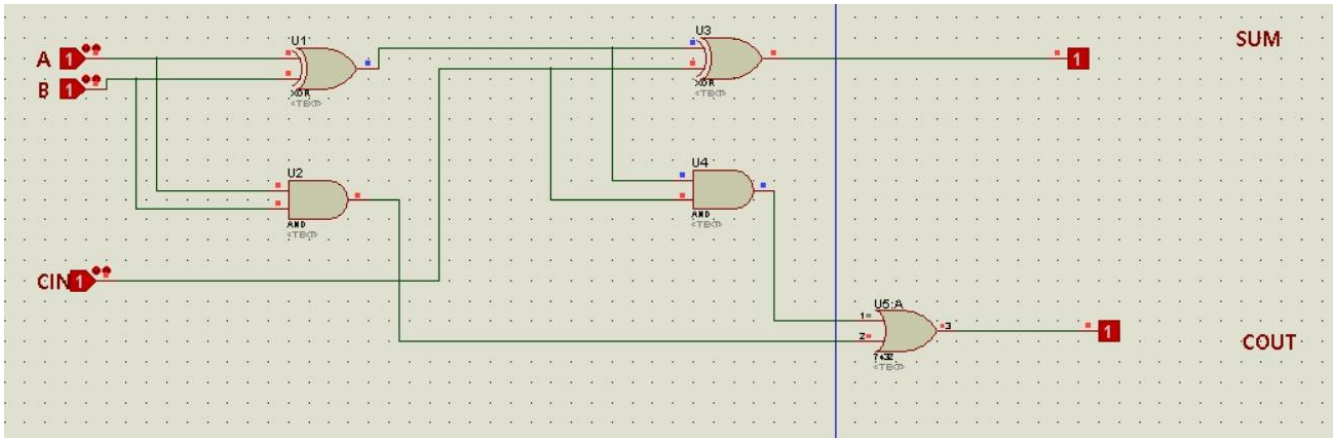


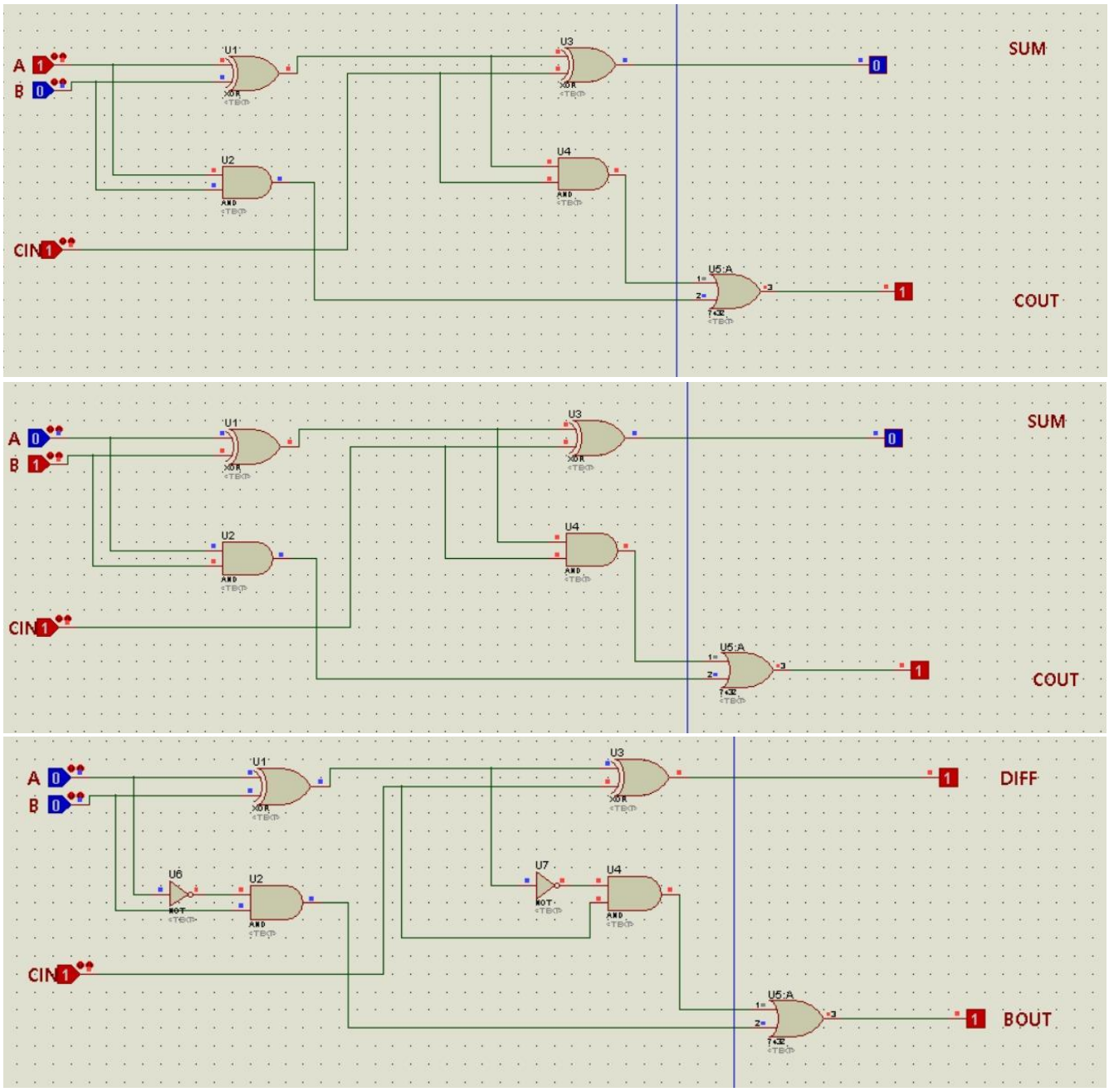
HALF SUBTRACTOR:

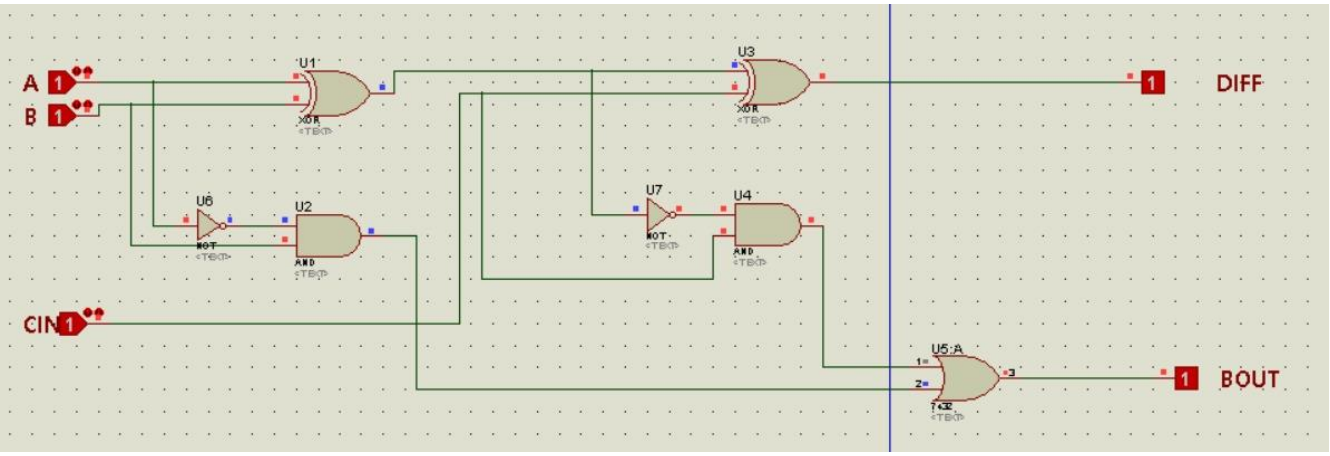




2. Design a full adder and full subtractor using the above designed half adder and half subtractor. Simulate in Proteus only. (1.5)

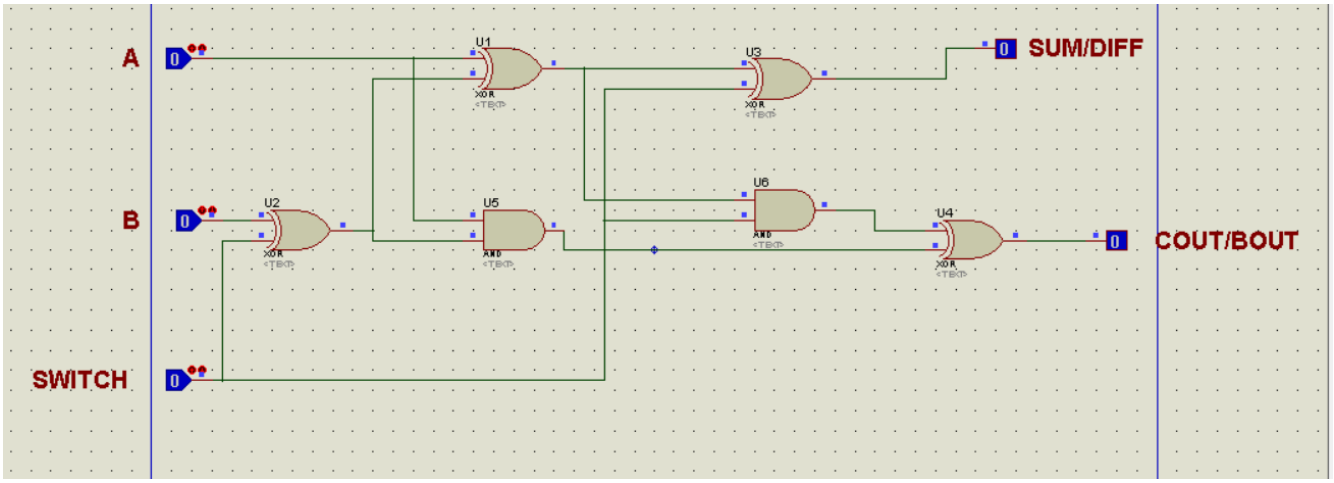


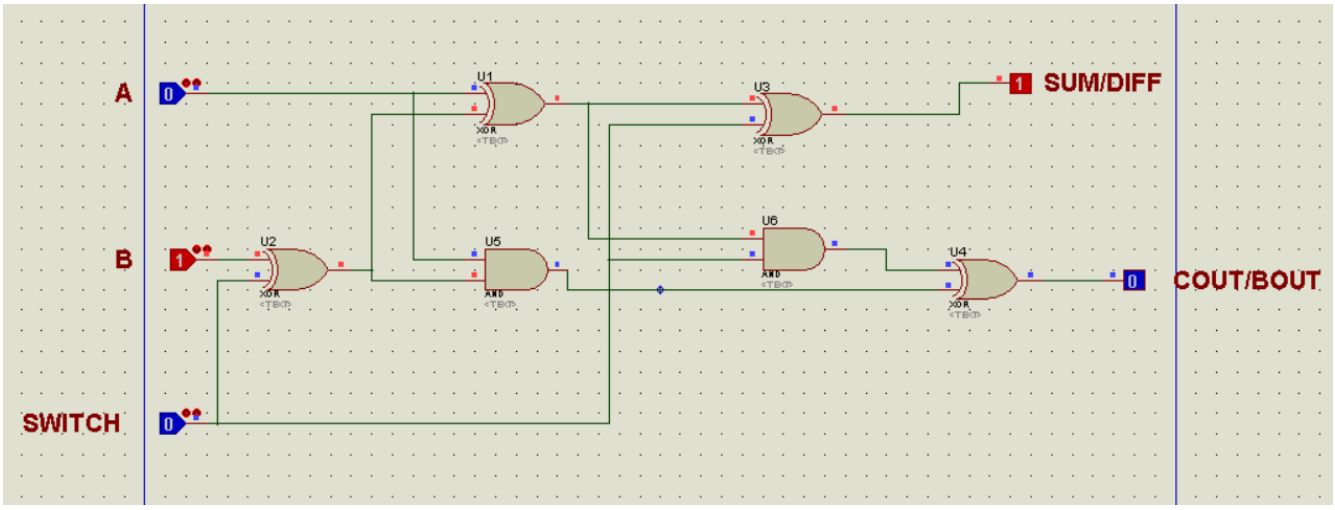

A
B
CIN
U1
U2
U3
U4
U5:A
SUM
COUT
A
B
CIN
U1
U2
U3
U4
U5:A
SUM
COUT
A
B
CIN
U1
U2
U3
U4
U6
U7
U5:A
DIFF
BOUT

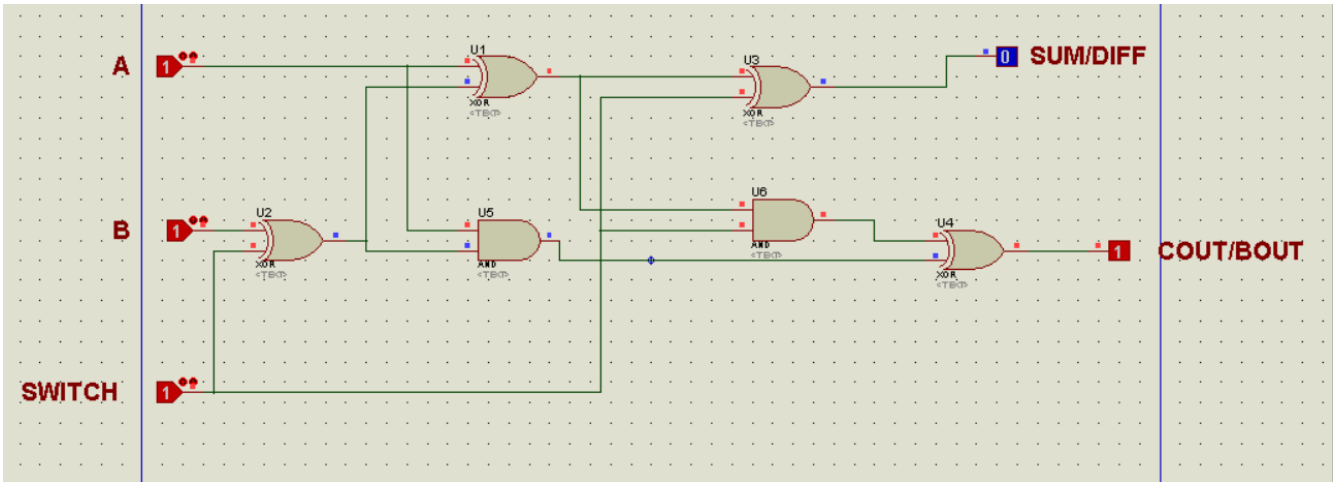


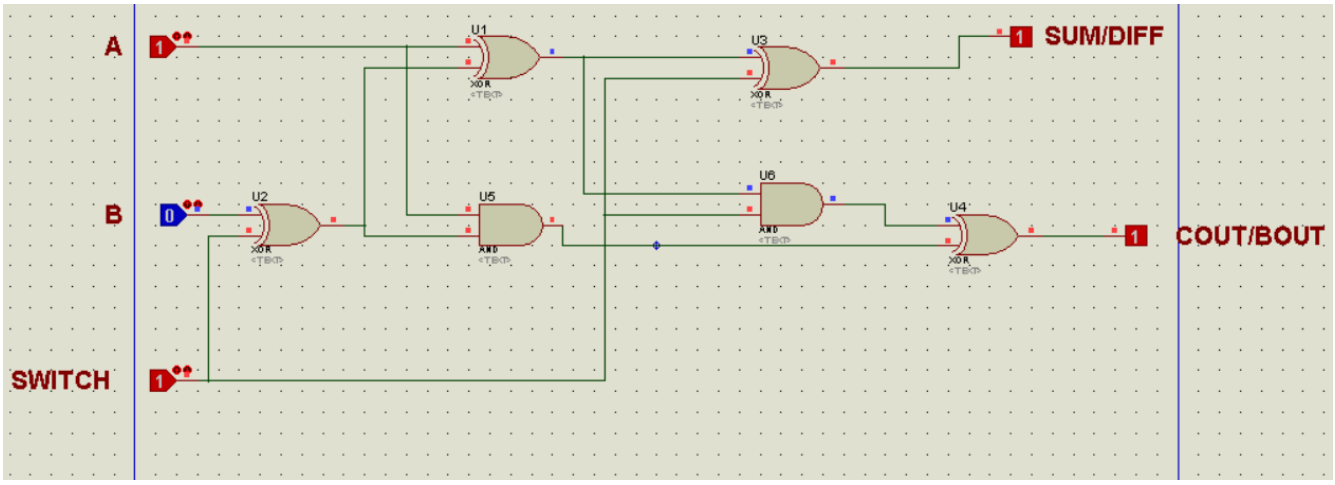
3. Now add the subtraction option in your full adder design and show the logic diagram of full adder with subtractor. Simulate in Proteus & implement it in hardware as well. (4)

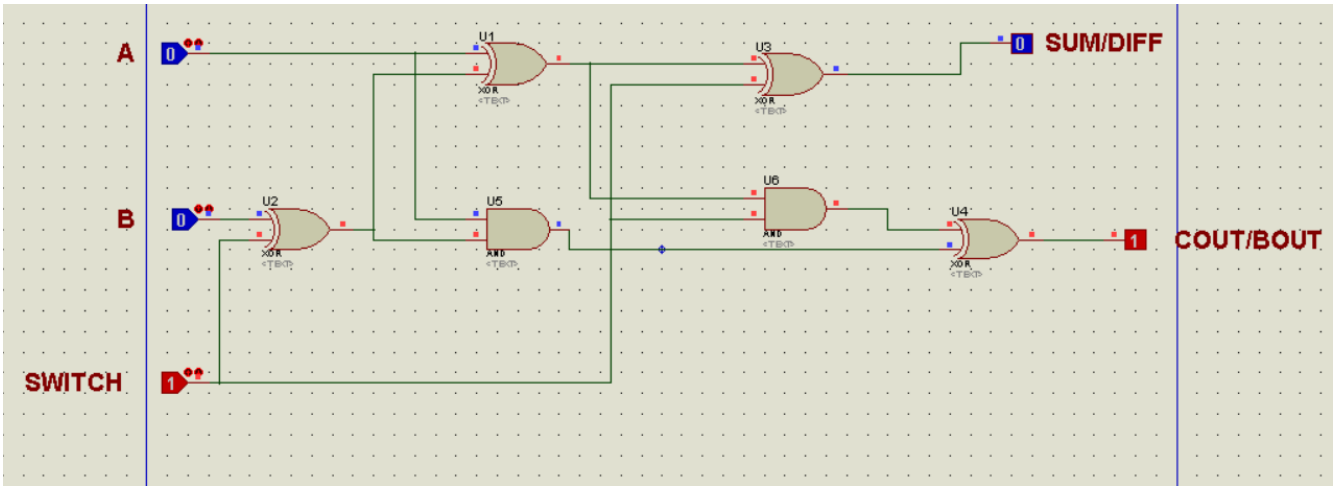
Proteus SS





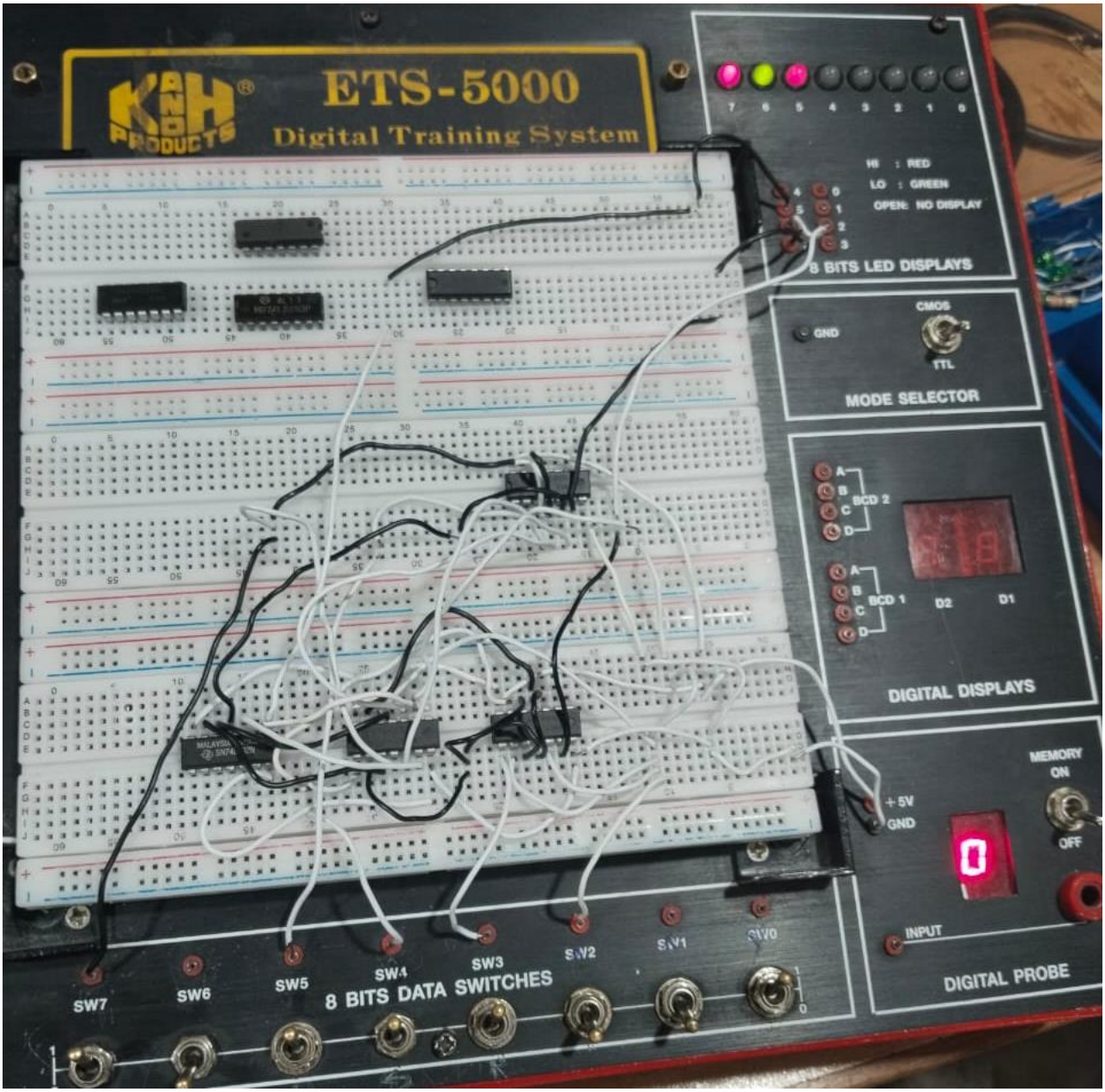

A
B
SWITCH
U1
U2
U3
U4
U5
U6
SUM/DIFF
COUT/BOUT

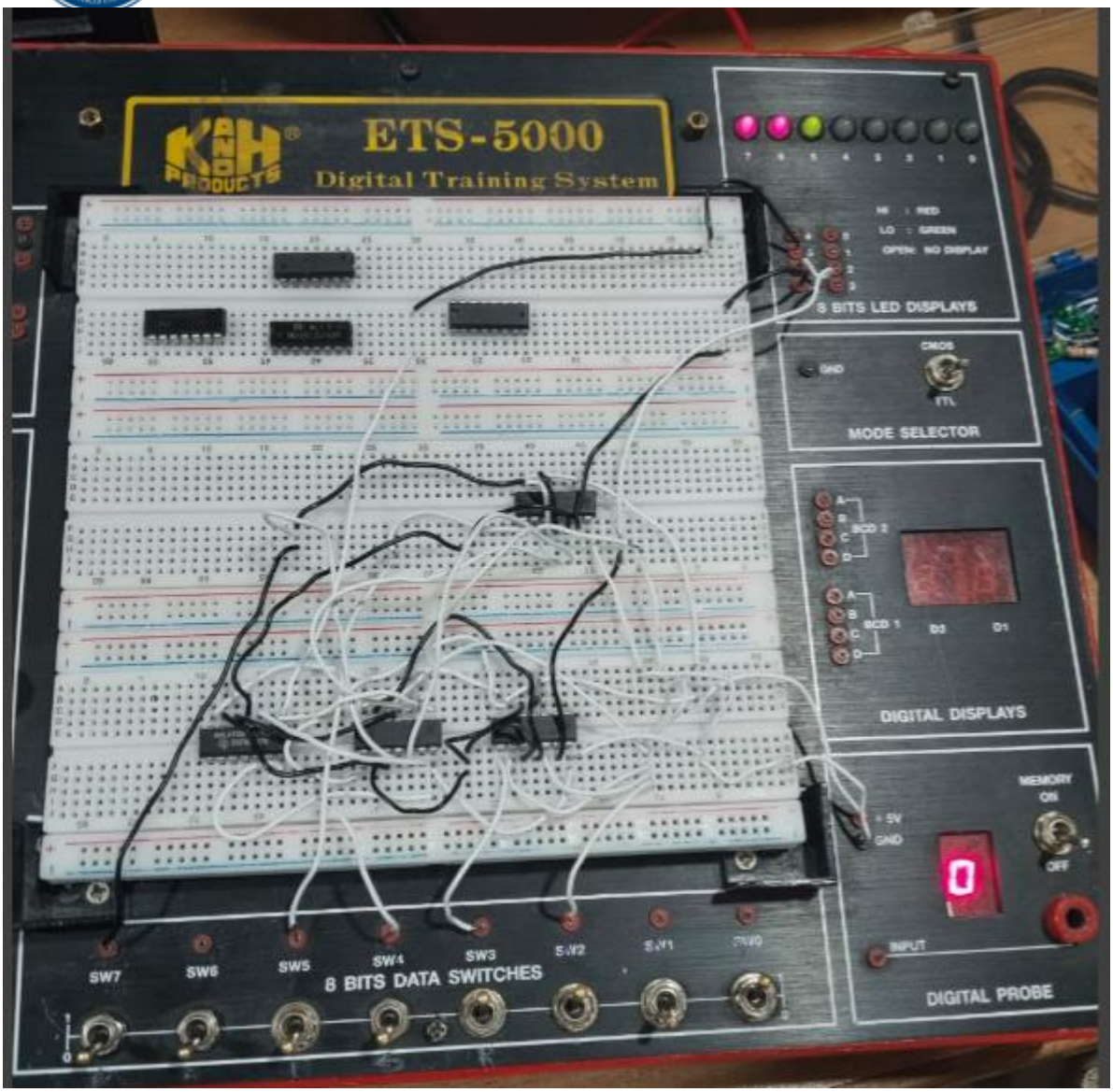

A
B
SWITCH
U1
U2
U3
U4
U5
U6
SUM/DIFF
COUT/BOUT

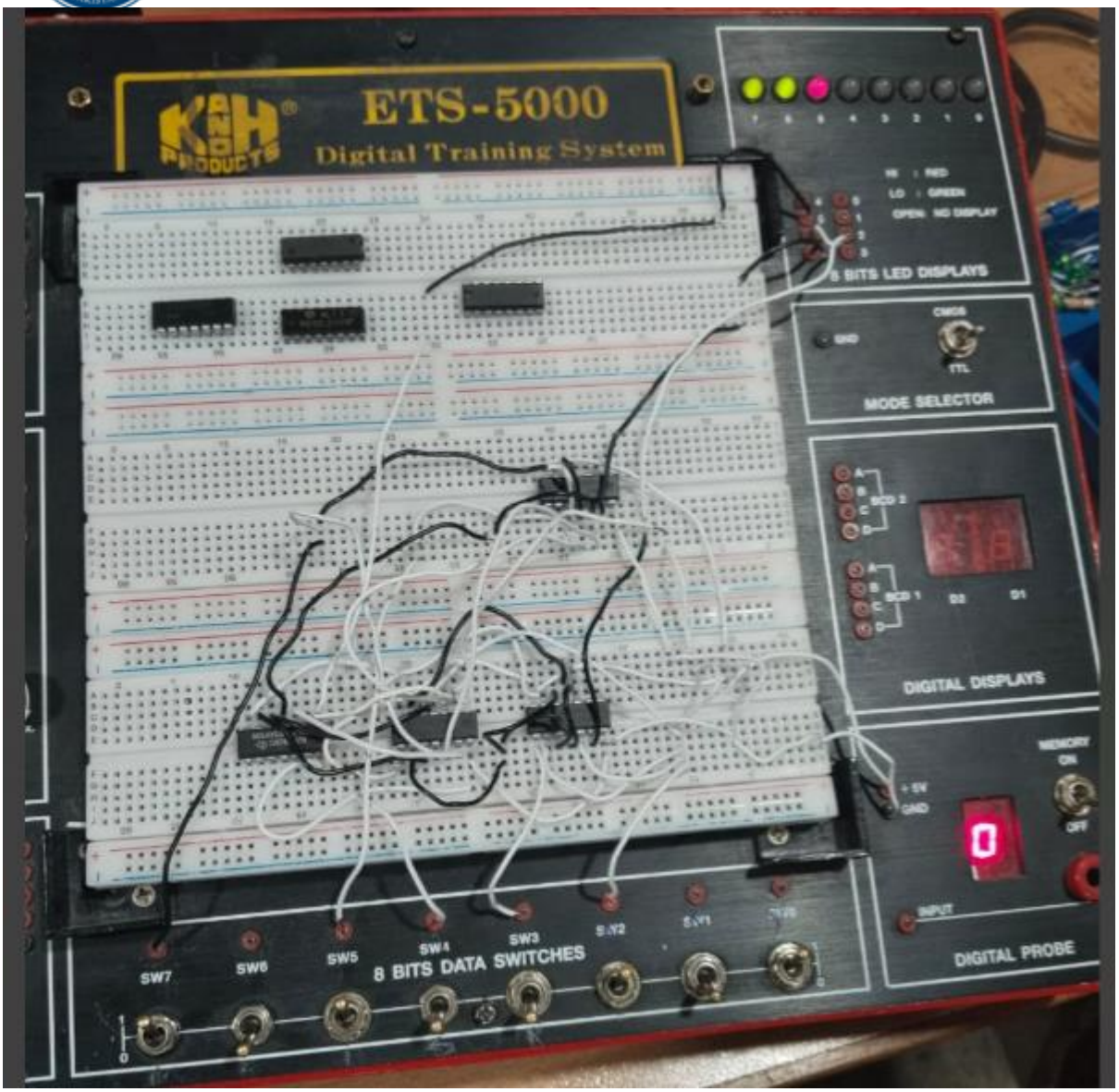

A
B
SWITCH
U1
U2
U3
U4
U5
U6
SUM/DIFF
COUT/BOUT

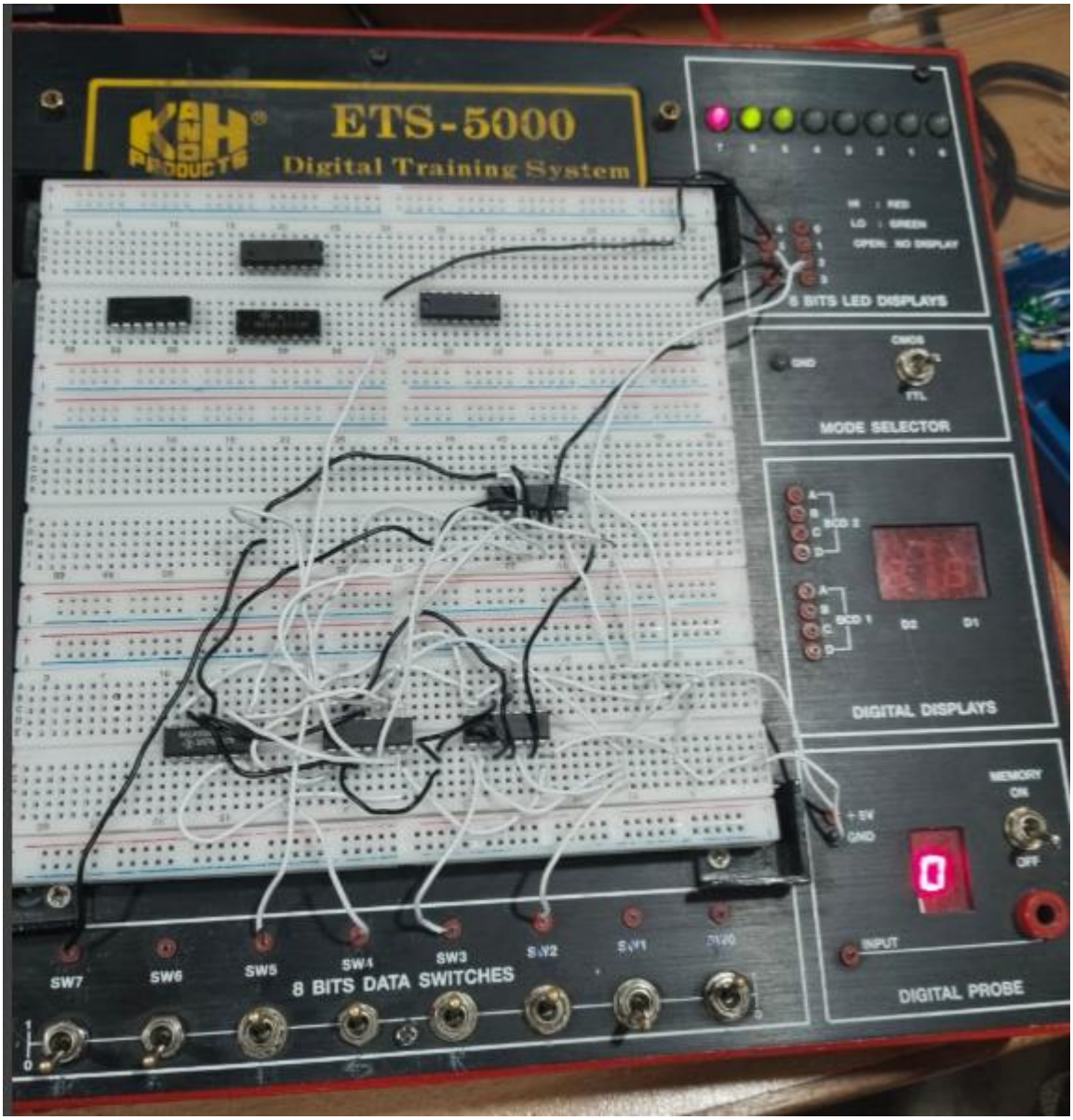
Hardware SS

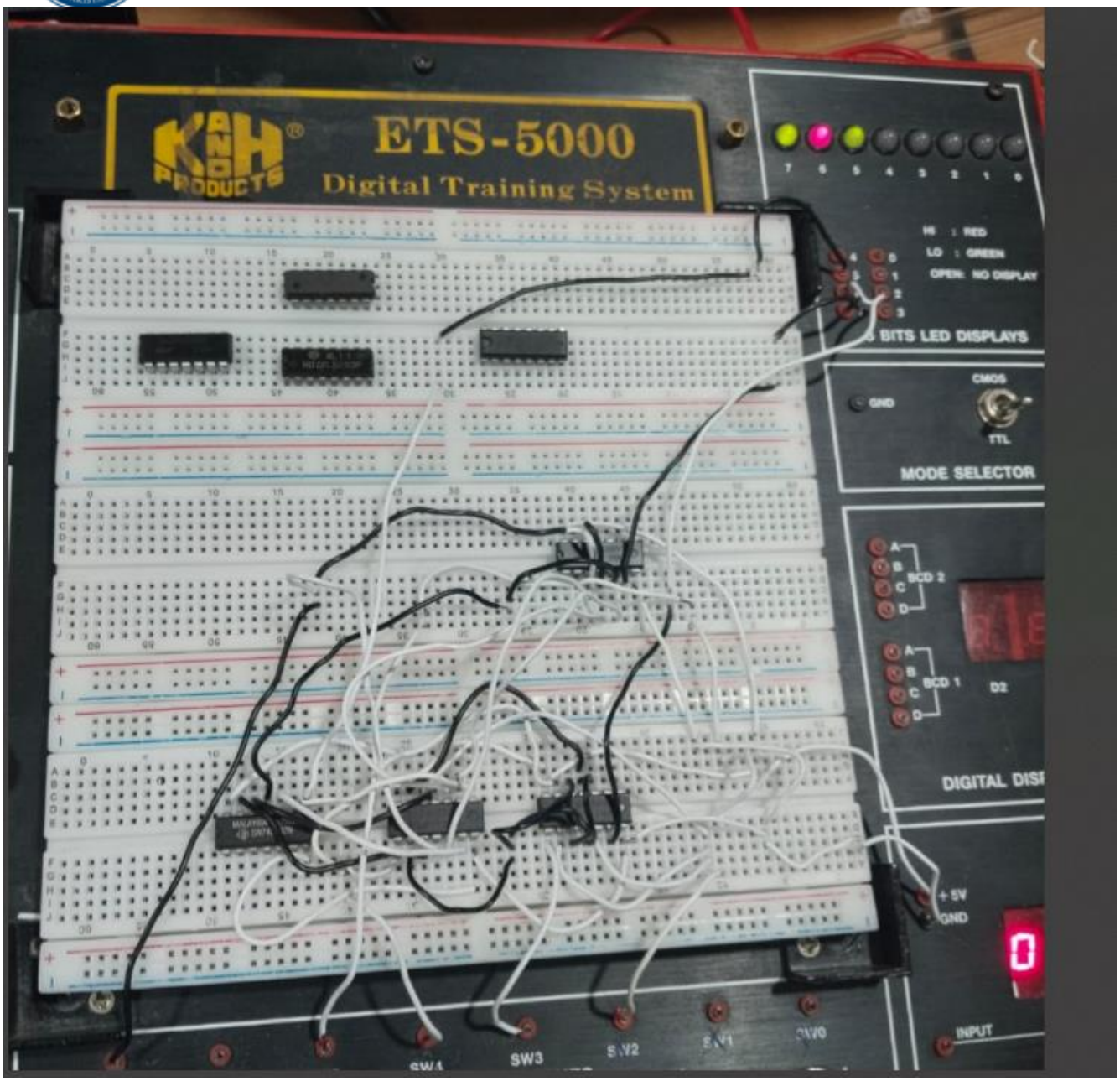
A_1	A_0	B_1	B_0	C_{IN}	$Carry_{OUT}$	S_1	S_0
0	0	0	0	0	**0**	**0**	**0**
0	0	0	0	1	**0**	**0**	**1**
0	0	0	1	0	**0**	**0**	**1**
0	0	0	1	1	**0**	**1**	**0**
0	0	1	0	0	**0**	**1**	**0**
0	0	1	0	1	**0**	**1**	**1**
0	0	1	1	0	**0**	**1**	**1**
0	0	1	1	1	**1**	**0**	**0**
0	1	0	0	0	**0**	**0**	**1**
0	1	0	0	1	**0**	**1**	**0**
0	1	0	1	0	**0**	**1**	**0**
0	1	0	1	1	**0**	**1**	**1**
0	1	1	0	0	**0**	**1**	**1**
0	1	1	0	1	**1**	**0**	**0**
0	1	1	1	0	**1**	**0**	**0**
0	1	1	1	1	**1**	**0**	**1**
1	0	0	0	0	**0**	**1**	**0**
1	0	0	0	1	**0**	**1**	**1**
1	0	0	1	0	**0**	**1**	**1**
1	0	0	1	1	**1**	**0**	**0**
1	0	1	0	0	**1**	**0**	**0**
1	0	1	0	1	**1**	**0**	**1**
1	0	1	1	0	**1**	**0**	**1**
1	0	1	1	1	**1**	**1**	**0**
1	1	0	0	0	**0**	**1**	**1**
1	1	0	0	1	**1**	**0**	**0**
1	1	0	1	0	**1**	**0**	**0**
1	1	0	1	1	**1**	**0**	**1**
1	1	1	0	0	**1**	**0**	**1**
1	1	1	0	1	**1**	**1**	**0**
1	1	1	1	0	**1**	**1**	**0**
1	1	1	1	1	**1**	**1**	**1**

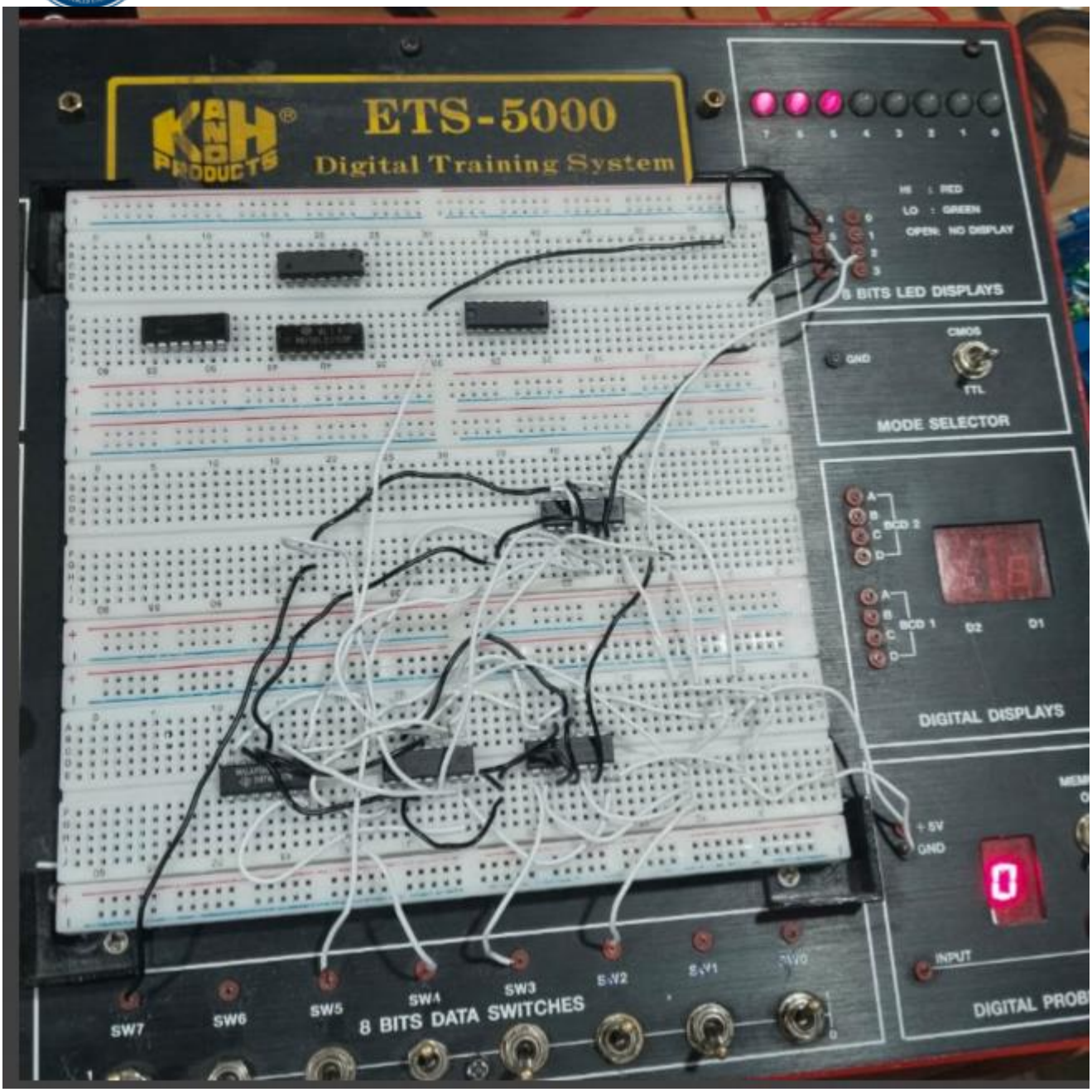

ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
CMOS
TTL
GND
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
MEMORY
ON
OFF
+5V
GND
INPUT
DIGITAL PROBE
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
8 BITS DATA SWITCHES

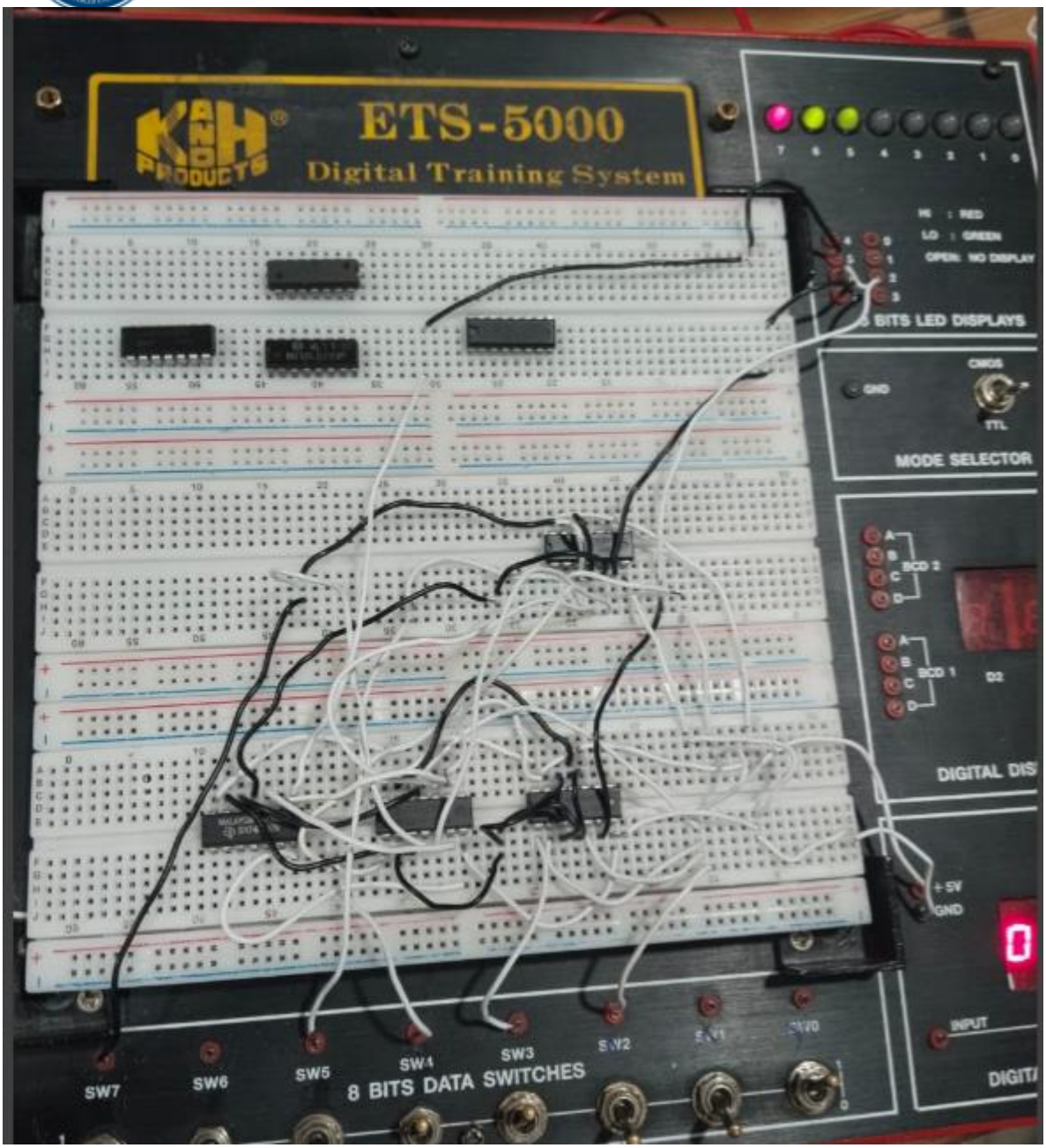

ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3

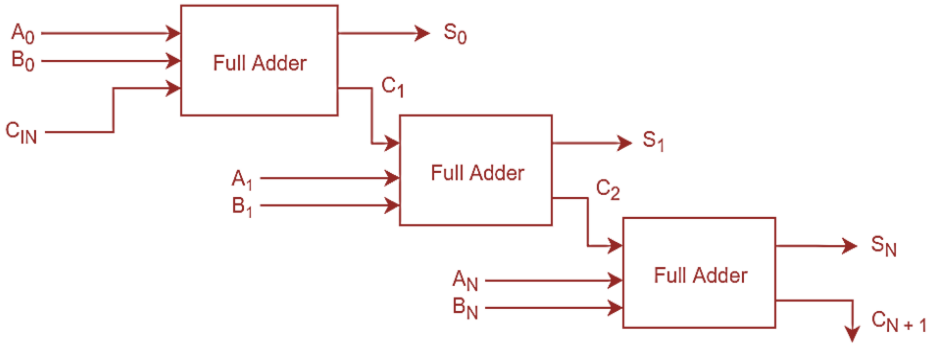

ETS-5000
Digital Training System
BITS LED DISPLAYS
MODE SELECTOR
BCD 2
BCD 1
+5V
GND
INPUT
SW3


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
CMOS
TTL
GND
DIGITAL DISPLAYS
BCD 2
BCD 1
D2
D1
+5V
GND
INPUT
DIGITAL PROB
SW7
SW6
SW5
SW4
SW3
8 BITS DATA SWITCHES



4. Extend your design to N-bit binary adder and subtractor. Draw block diagram only. (0.5)

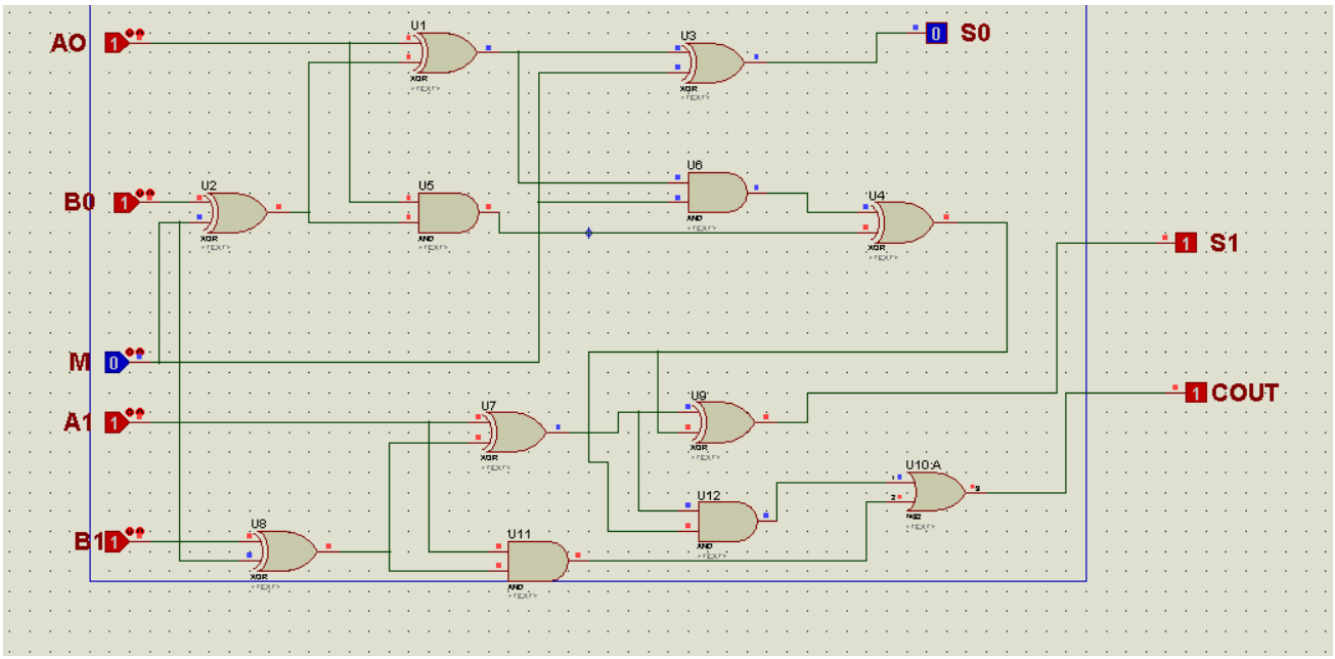
Full Adder for N – Bit Binary Addition

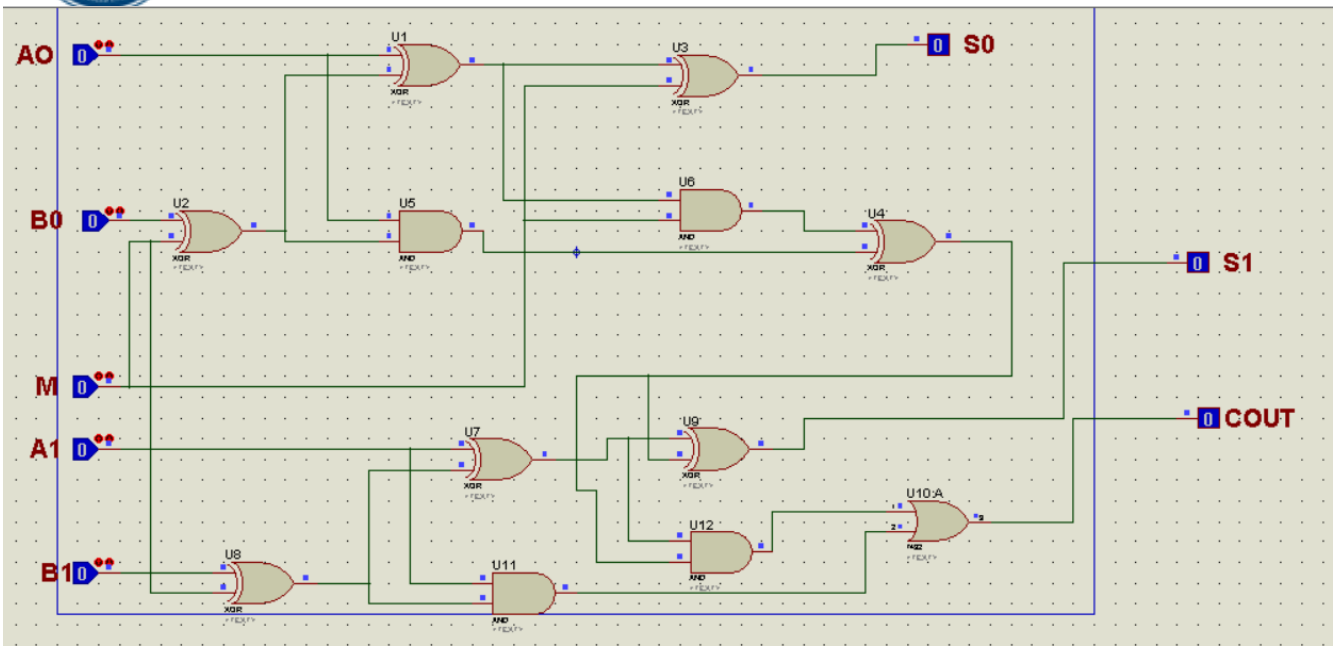


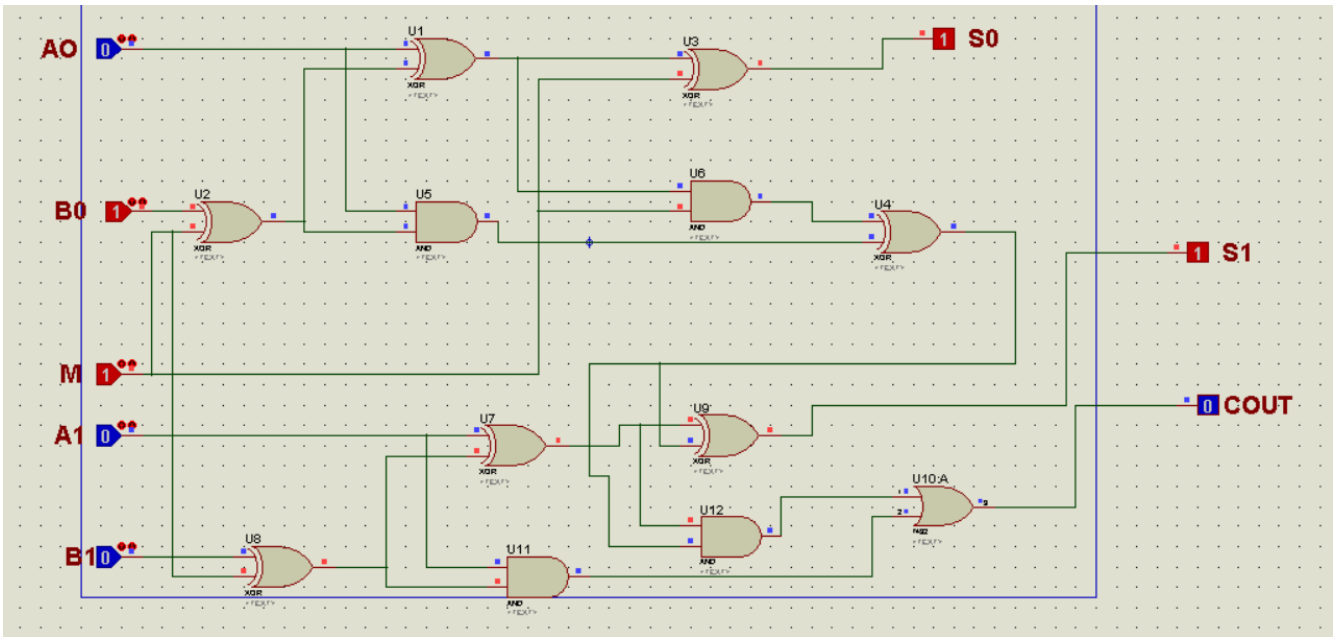
The input carry in each full adder has to propagate through an AND gate and an XOR gate, yielding two level gate implementation. For n – bits, there is a propagation delay of 2n; inferring that addition is drastically slow for a high number of bits.

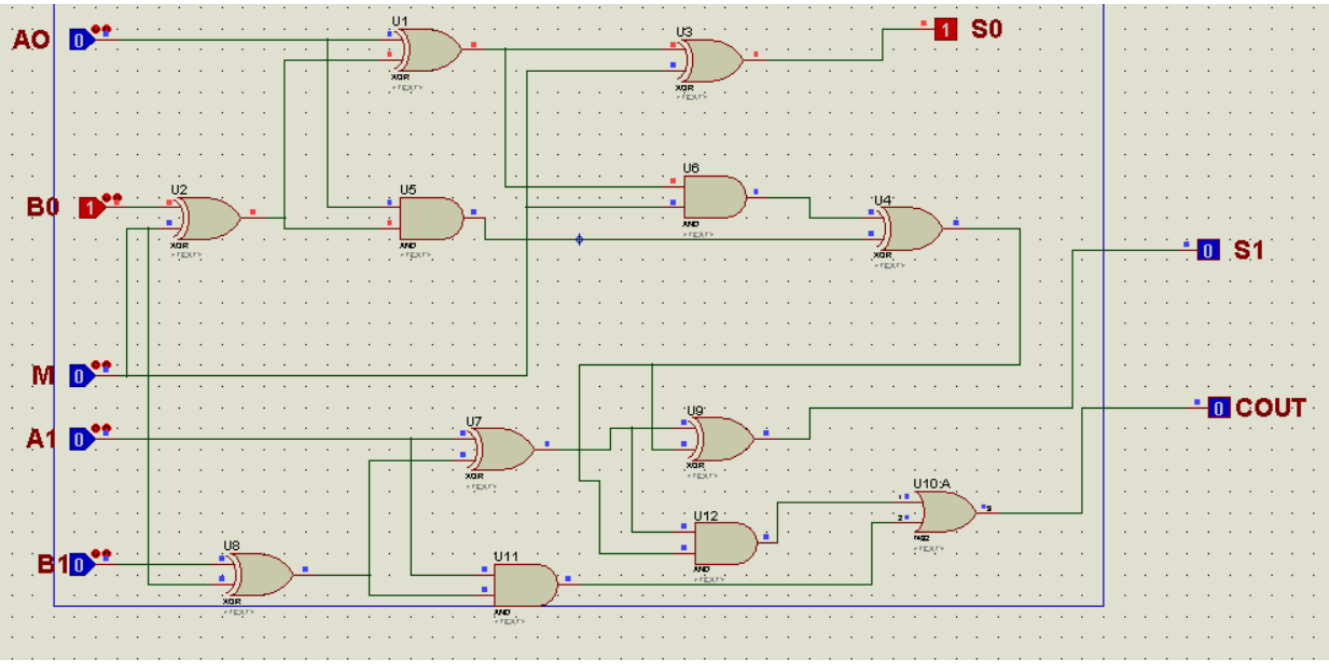
Such a delay can be mitigated by using a Carry – Look Ahead Generator where each carry is propagated depending only the input carry C_{IN}.

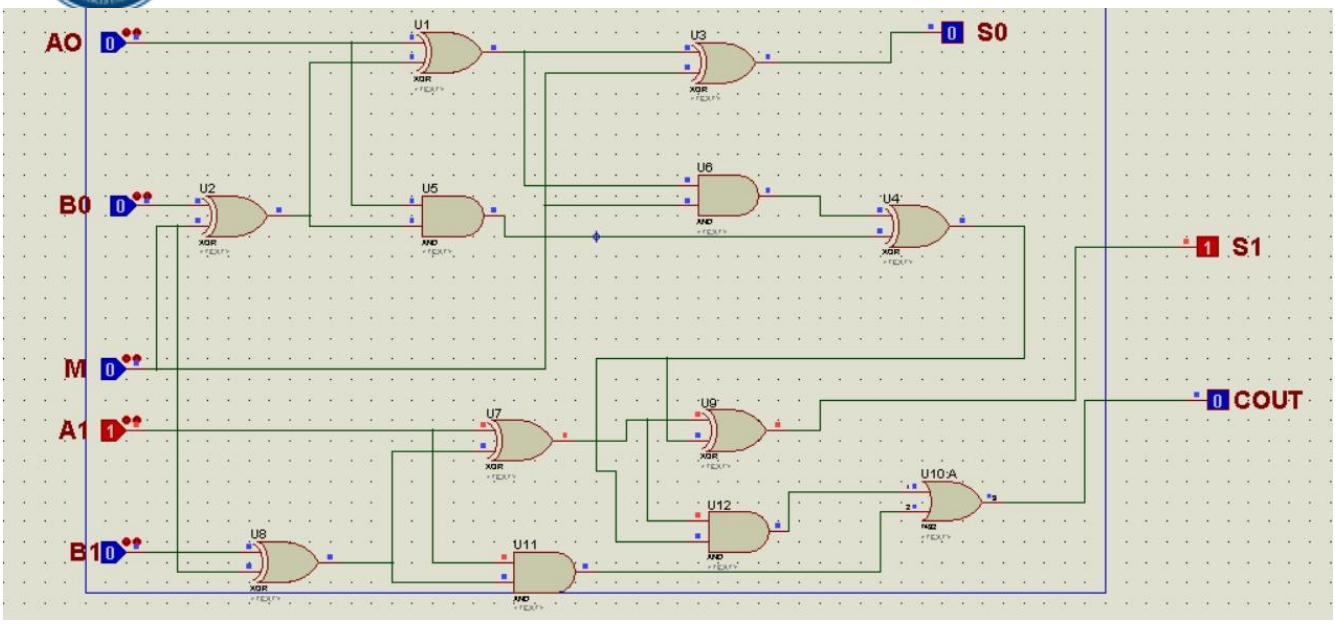
5. Extend your design to 2-bit binary adder and subtractor. Simulate the 2-bit adder subtractor circuit in Proteus only. (2)




AO
B0
M
A1
B1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10:A
U11
U12
S0
S1
COUT

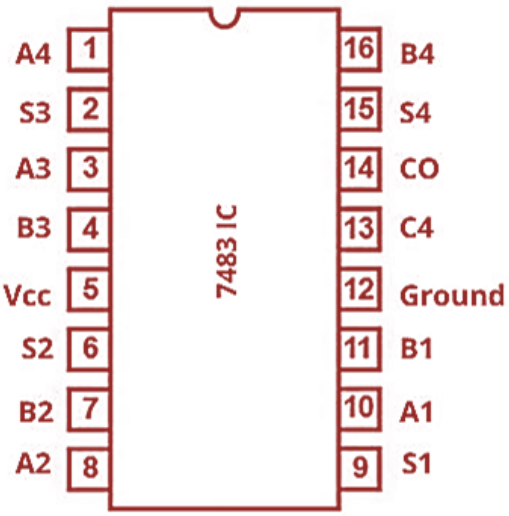

AO
B0
M
A1
B1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10:A
U11
U12
S0
S1
COUT


AO
B0
M
A1
B1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10:A
U11
U12
S0
S1
COUT

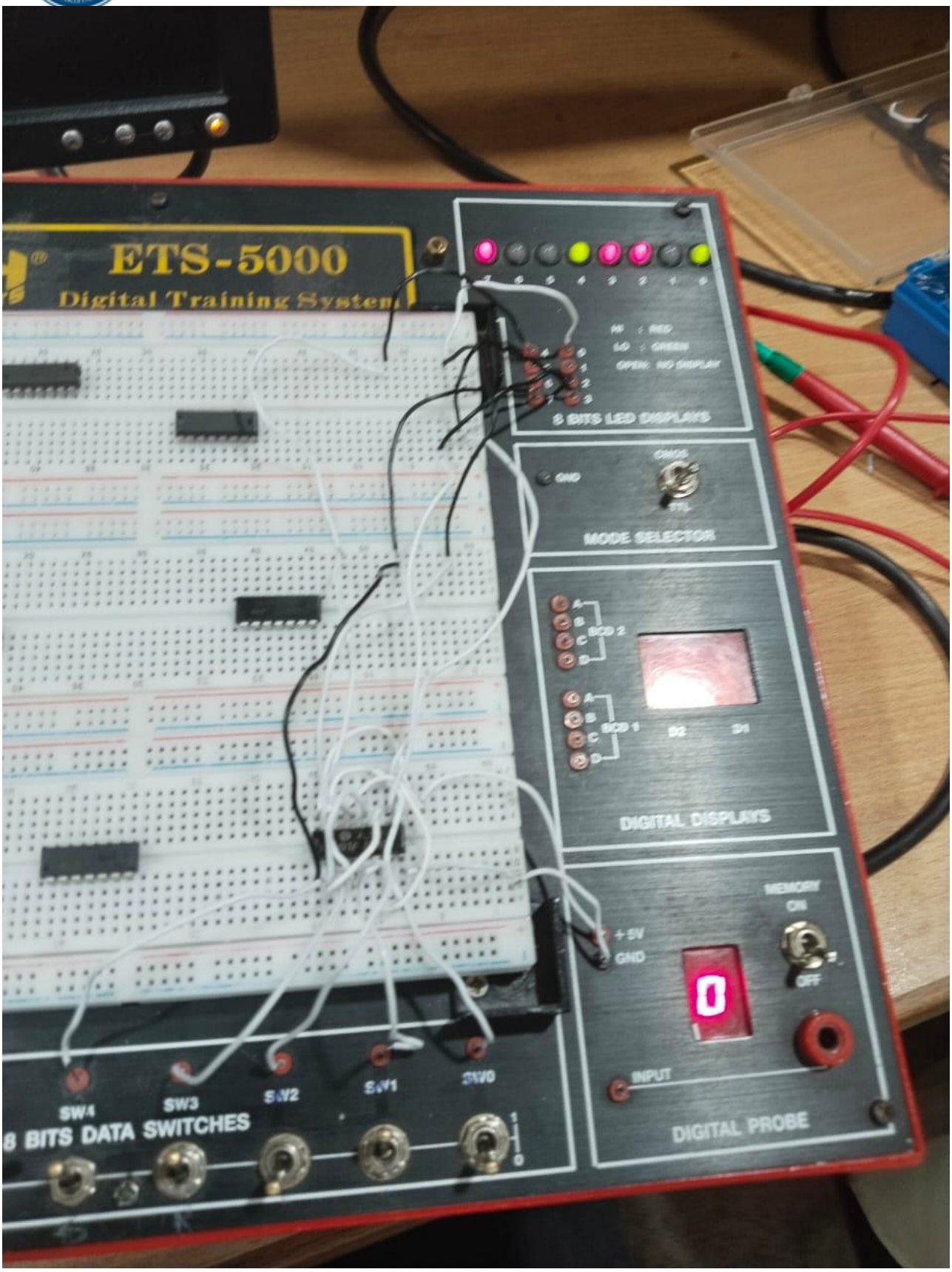


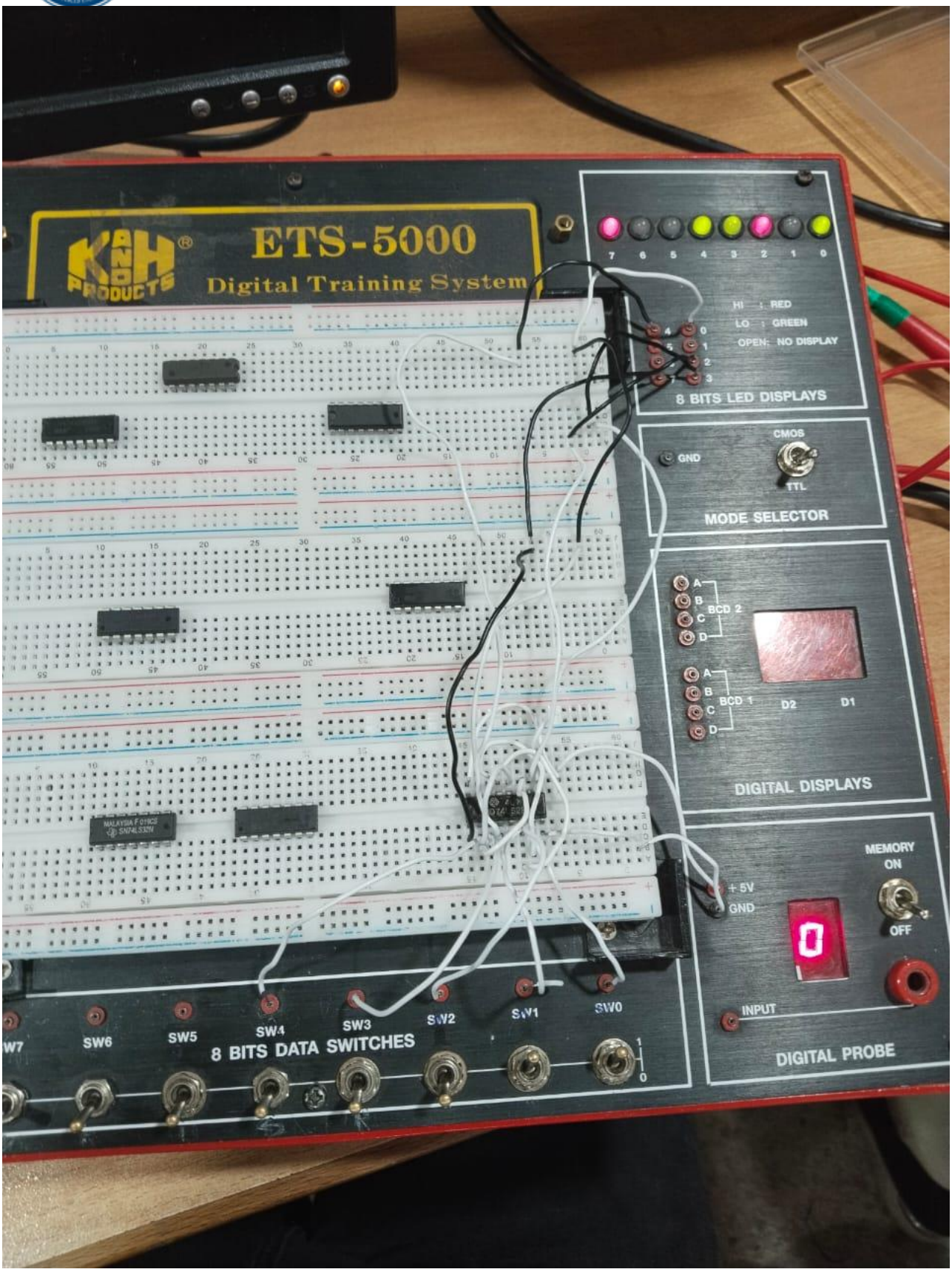
6. Get the 4-bit binary adder IC from the lab and verify its functionality in hardware. Give IC number and pin-layout. Show the result for at least 8 input combinations. (1.5)

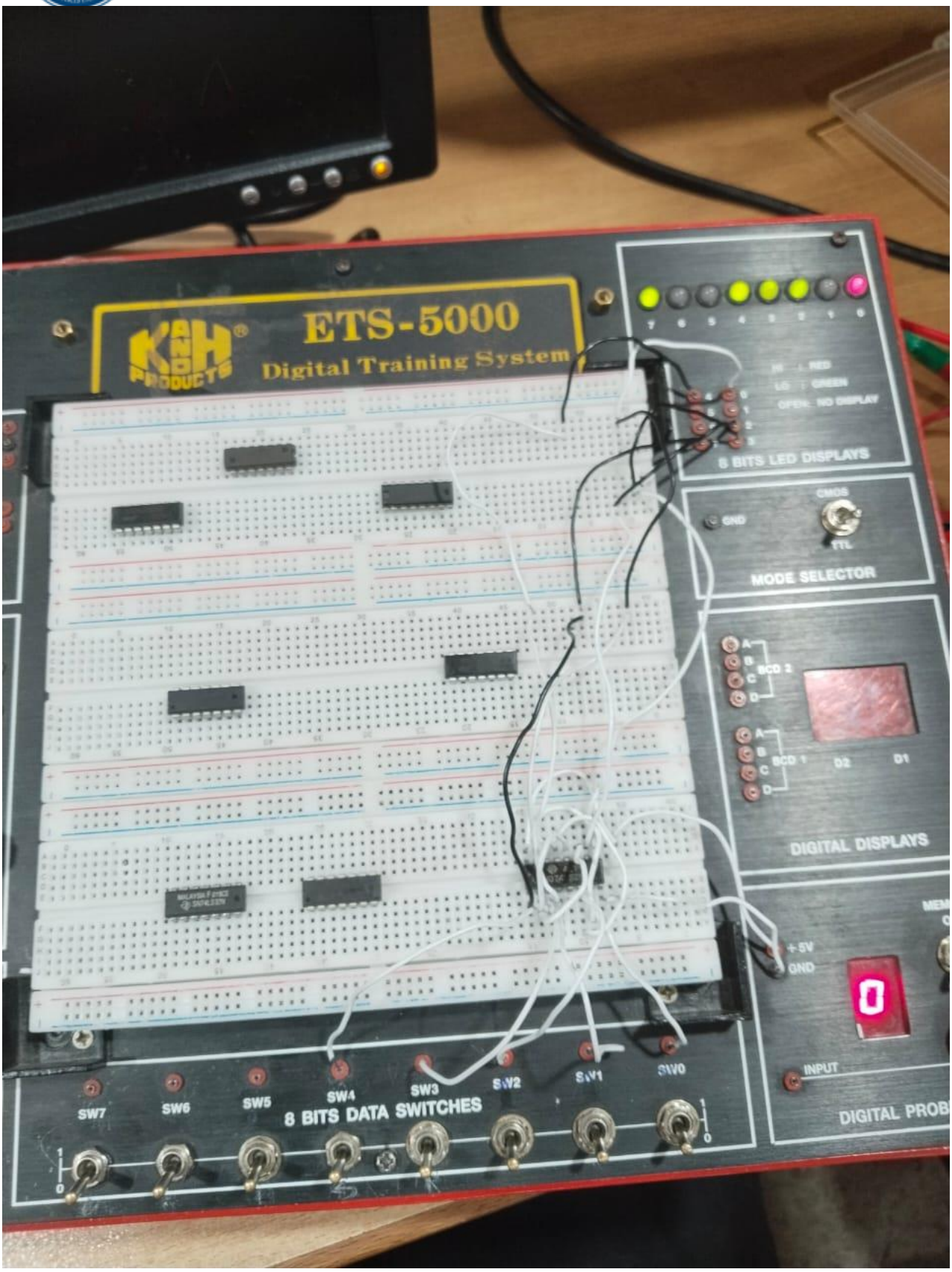
A1, A2, A3, A4: First 4 bit Input
B1, B2, B3, B4: Second 4 bit input
S1, S2, S3, S4: 4 bit output
CO: Carry input
C4: Carry output

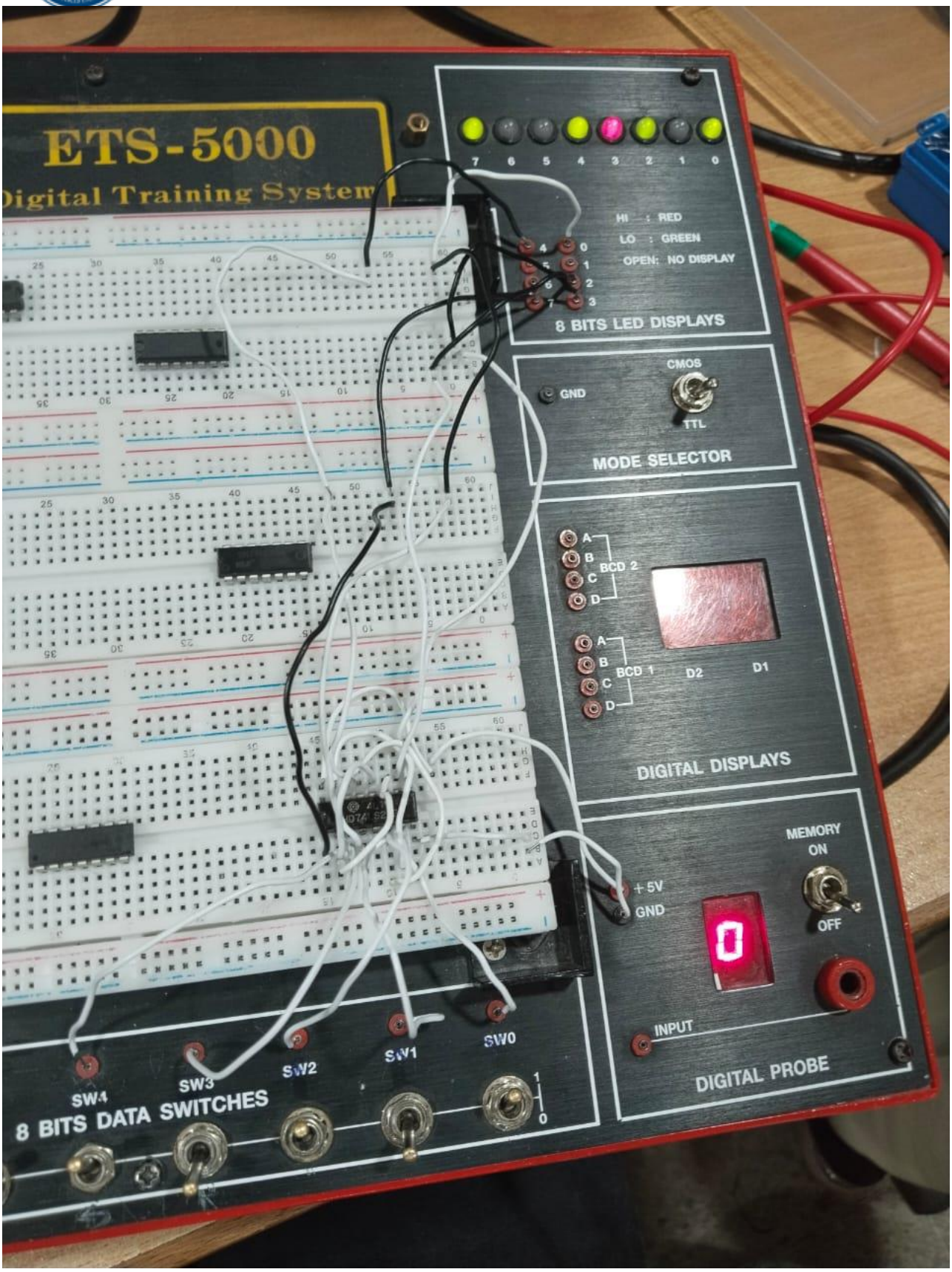


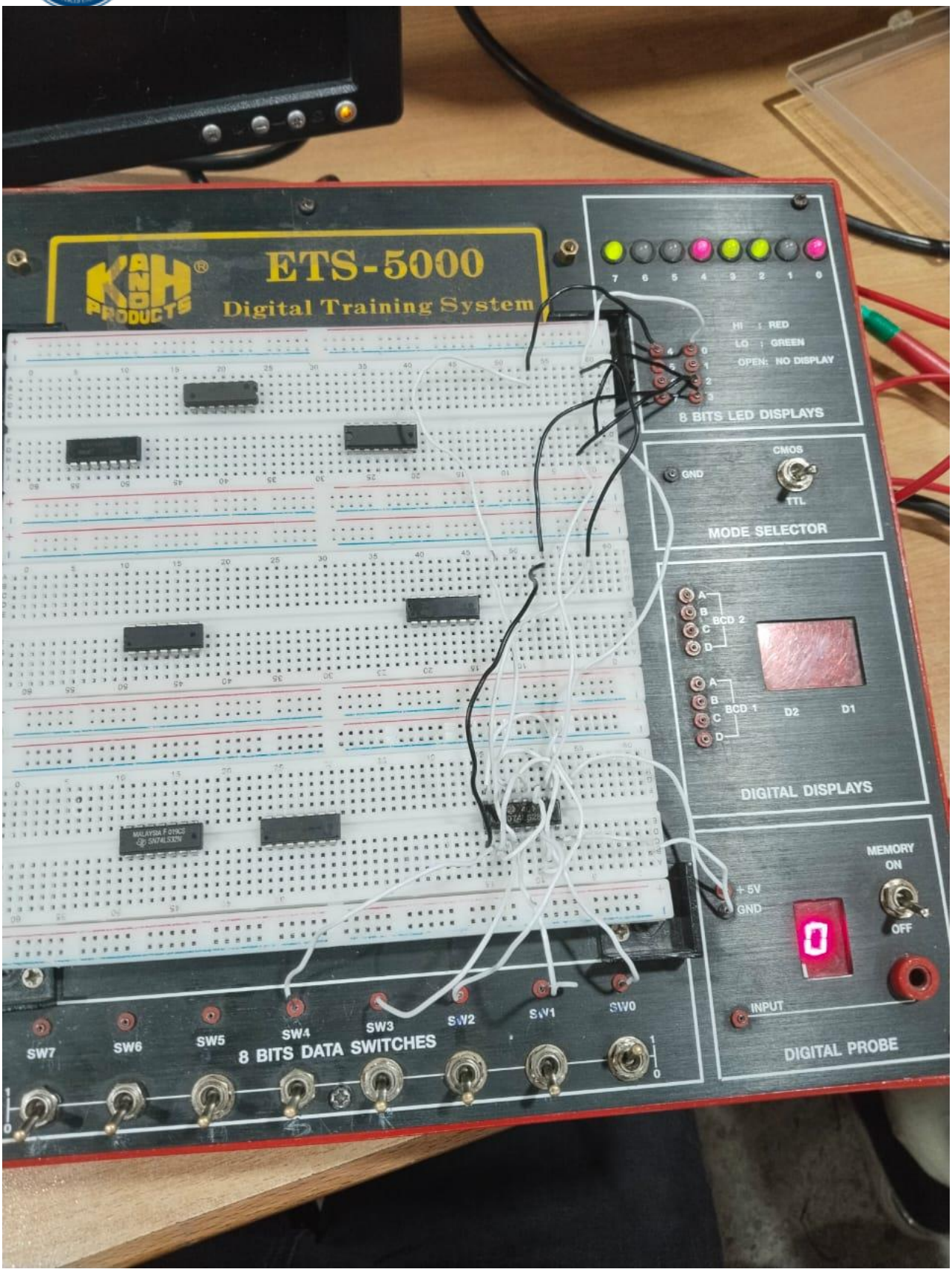
HARDWARE SS:

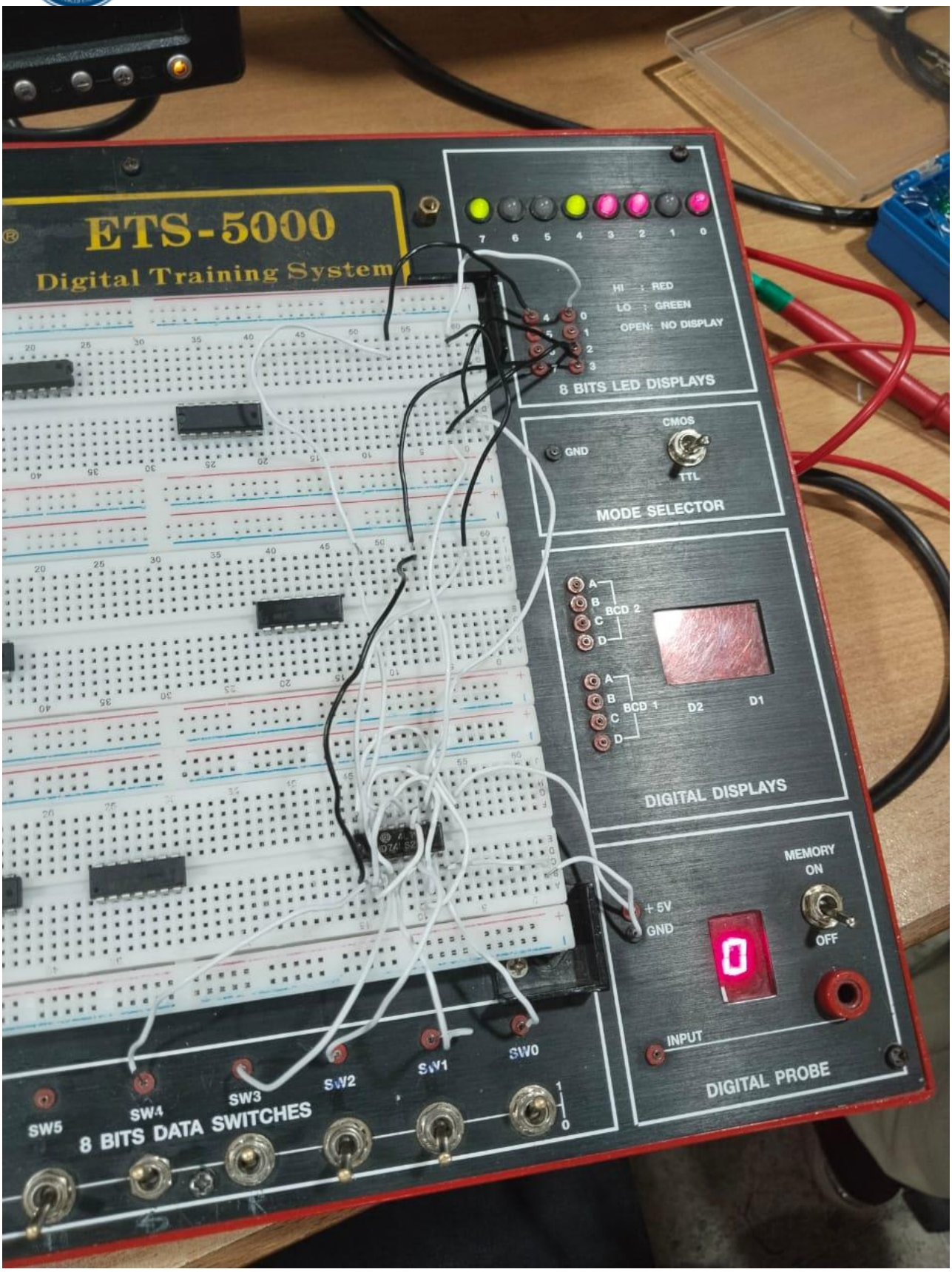

ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW4
SW3
SW2
SW1
SW0
MEMORY
ON
OFF
+5V
GND
INPUT

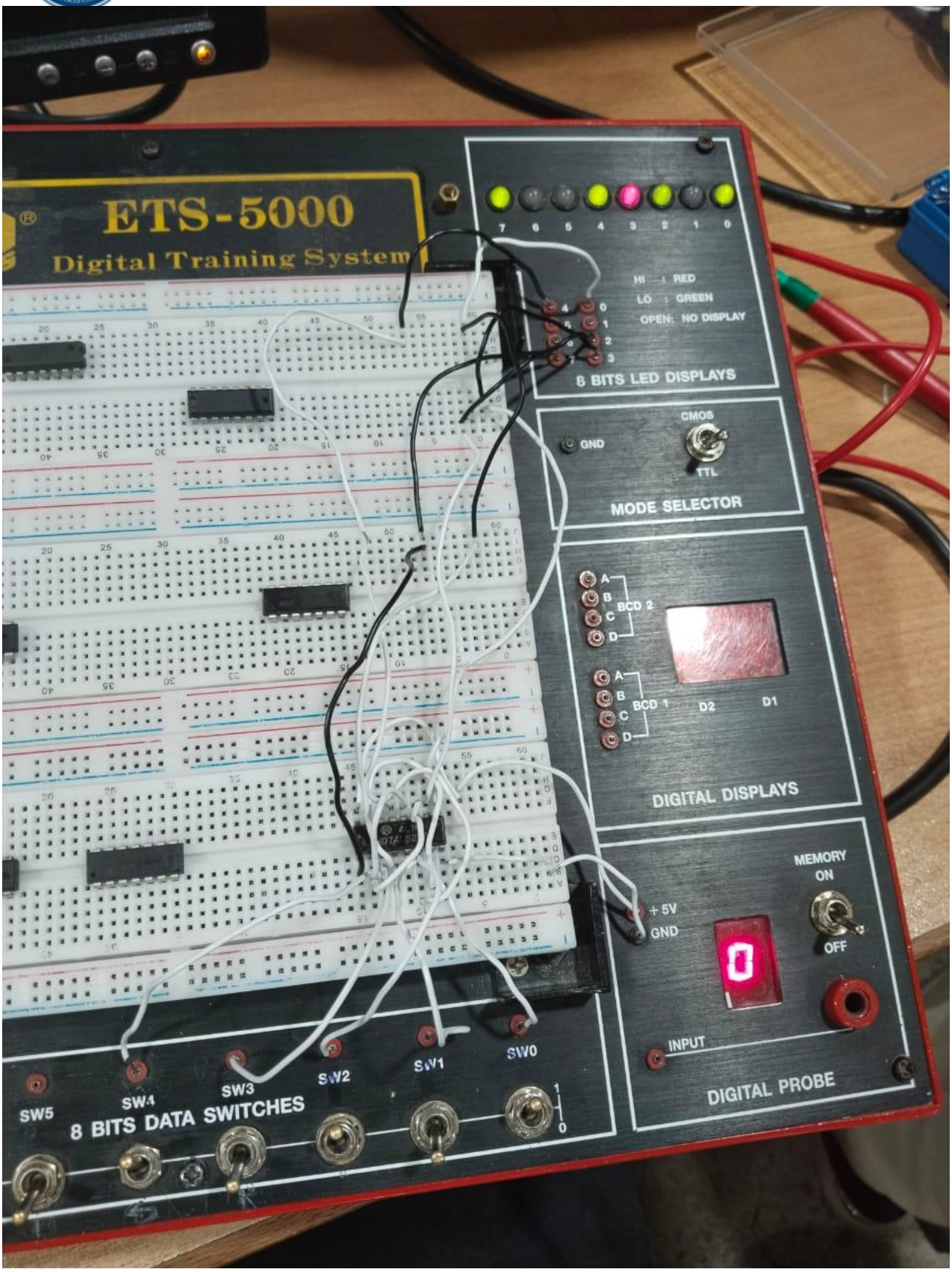

ETS-5000
Digital Training System
KANDO PRODUCTS
7 6 5 4 3 2 1 0
HI : RED
LO : GREEN
OPEN: NO DISPLAY
8 BITS LED DISPLAYS
GND
CMOS
TTL
MODE SELECTOR
A
B
C
D
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
MEMORY
ON
OFF
+5V
GND
INPUT
DIGITAL PROBE
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
8 BITS DATA SWITCHES

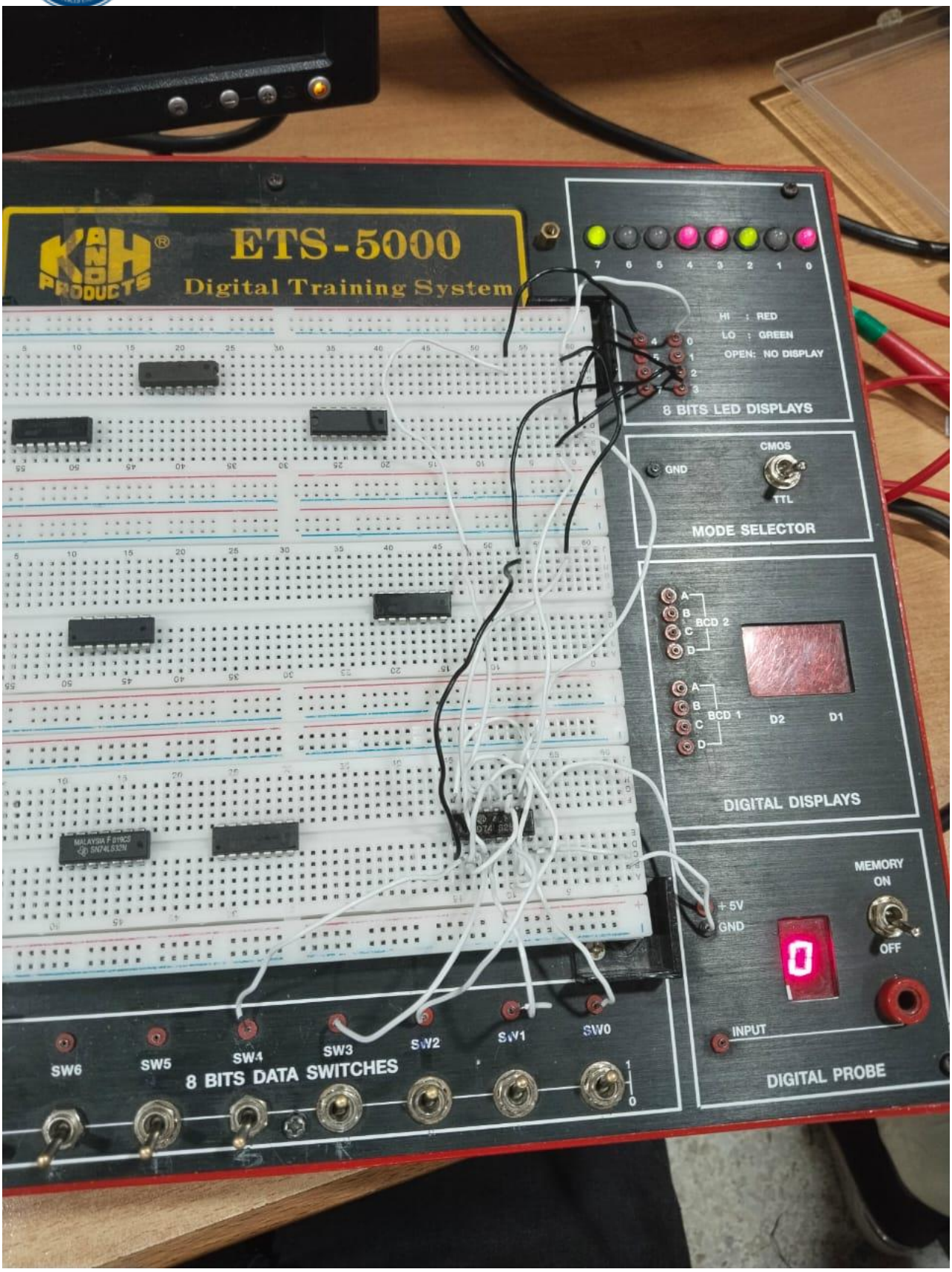

ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
INPUT

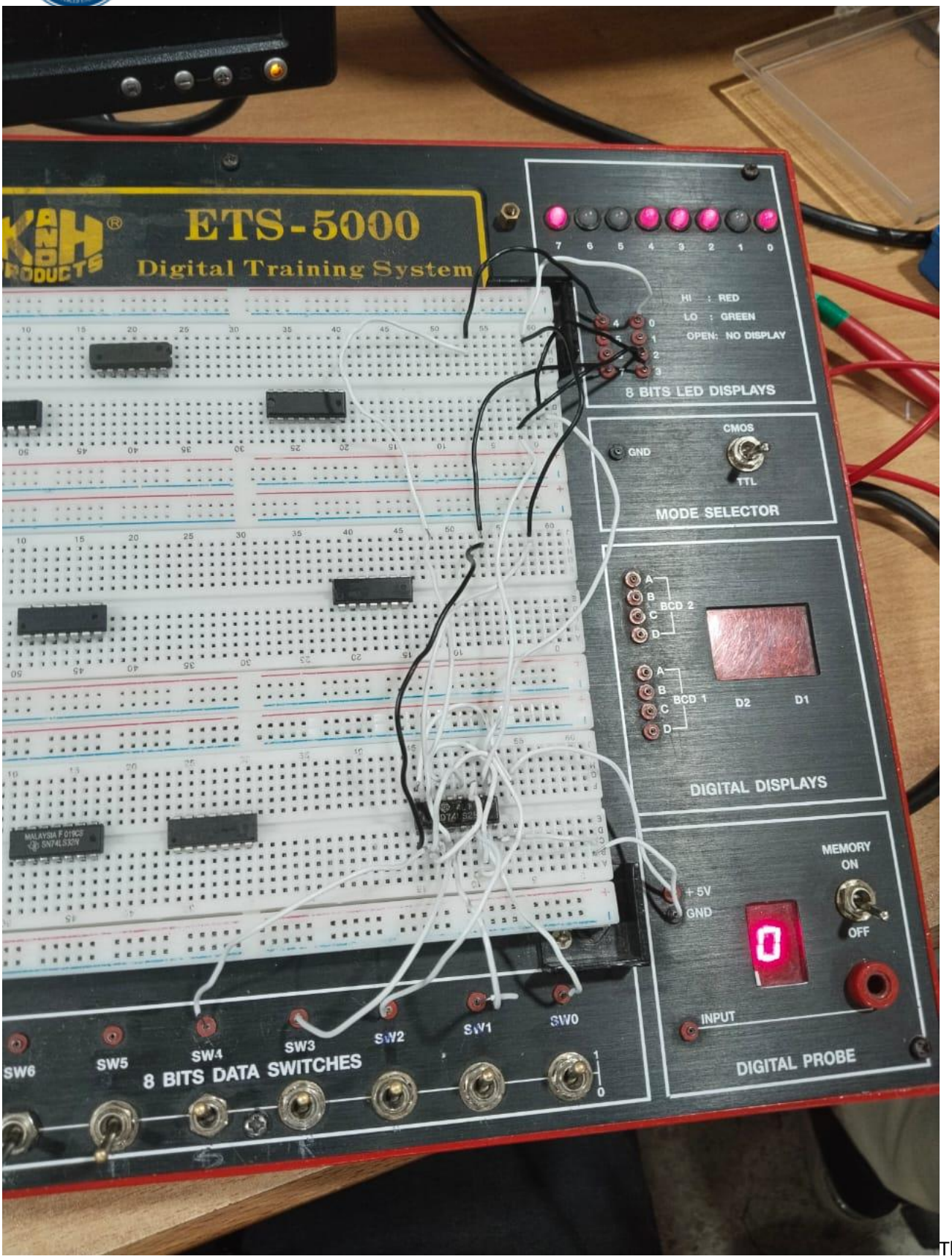

ETS-5000
Digital Training System
7 6 5 4 3 2 1 0
HI : RED
LO : GREEN
OPEN: NO DISPLAY
8 BITS LED DISPLAYS
GND
CMOS
TTL
MODE SELECTOR
A
B
C
D
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
MEMORY
ON
OFF
+5V
GND
INPUT
DIGITAL PROBE
SW4
SW3
SW2
SW1
SW0
8 BITS DATA SWITCHES


ETS-5000
Digital Training System
KANDO PRODUCTS
7 6 5 4 3 2 1 0
HI : RED
LO : GREEN
OPEN: NO DISPLAY
8 BITS LED DISPLAYS
GND
CMOS
TTL
MODE SELECTOR
A
B
C
D
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
+ 5V
GND
MEMORY
ON
OFF
INPUT
DIGITAL PROBE
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
8 BITS DATA SWITCHES


ETS-5000
Digital Training System
7 6 5 4 3 2 1 0
HI : RED
LO : GREEN
OPEN: NO DISPLAY
8 BITS LED DISPLAYS
GND
CMOS
TTL
MODE SELECTOR
A
B
C
D
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
MEMORY
ON
OFF
+5V
GND
INPUT
DIGITAL PROBE
SW5
SW4
SW3
SW2
SW1
SW0
8 BITS DATA SWITCHES


ETS-5000
Digital Training System
7 6 5 4 3 2 1 0
HI : RED
LO : GREEN
OPEN: NO DISPLAY
8 BITS LED DISPLAYS
GND
CMOS
TTL
MODE SELECTOR
A
B
C
D
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
MEMORY
ON
OFF
+5V
GND
INPUT
DIGITAL PROBE
SW5
SW4
SW3
SW2
SW1
SW0
8 BITS DATA SWITCHES
1
0


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
HI : RED
LO : GREEN
OPEN: NO DISPLAY
MODE SELECTOR
CMOS
TTL
GND
DIGITAL DISPLAYS
BCD 2
BCD 1
D2
D1
DIGITAL PROBE
MEMORY
ON
OFF
+5V
GND
INPUT
8 BITS DATA SWITCHES
SW6
SW5
SW4
SW3
SW2
SW1
SW0



The IC performed the 4 – bit binary addition and also verified the functional truth table;

FUNCTIONAL TRUTH TABLE

C (n–1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally