Department of Electrical Engineering

Faculty Member:_____ **Dated:** _____

Semester:_____ **Section:** _____

Group No.:

EE-221: Digital Logic Design

Lab 08: Magnitude Comparator

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance**	**Analysis of data in Lab Report**	**Modern Tool Usage**	**Ethics and Safety**	**Individual and Team Work**	**Total marks Obtained**
		5 Marks	**5 Marks**	**5 Marks**	**5 Marks**	**5 Marks**	**25 Marks**
AILYA ZAINAB	**523506**						
IMAN NAEEM	**525378**						
LAIBA NASIR	**510419**						
LUQMAN SHEHZAD	**507599**						

Lab 8: Magnitude Comparator

This Lab Activity has been designed to familiarize students with design and working of combinational circuits using basic logic gates.

Objectives:

- ✓ Design and Implementation of 2-bit magnitude comparator using classical design method learned in the class.
- ✓ Design of a 4-bit magnitude comparator using a 4-bit adder IC and logic gates
- ✓ Verification of 4 bit comparator IC
- ✓ Dataflow modeling in Verilog HDL

Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
- ✓ The students will start lab task and demonstrate design steps separately for step-wise evaluation(course instructor/lab engineer will sign each step after ascertaining functional verification)
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
- ✓ There are related questions at the end of this activity. Give complete answers.

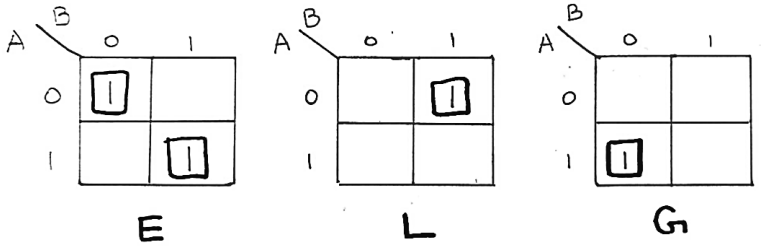
Pre-Lab Tasks (2)

1. What do you mean by a comparator circuit? Draw the truth table for a 1 bit magnitude comparator. The comparator has 2 inputs (A and B) and 3 outputs E, L and G for (A=B), (A<B) and (A>B) respectively. For example, one combination is filled in below example, for your guidance.

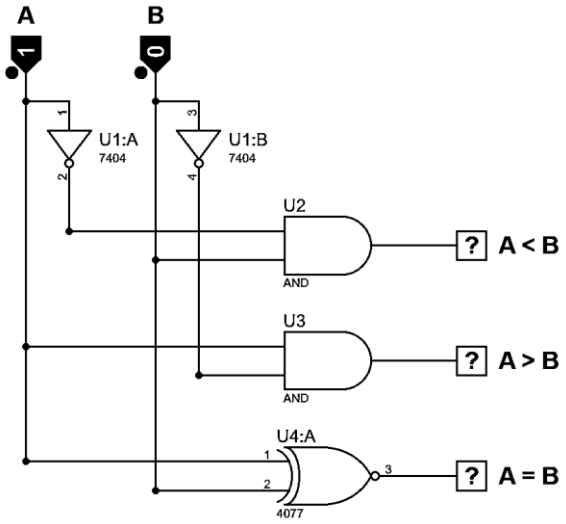
A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

A	B	E (A=B)	G (A>B)	L (A<B)
0	0	**1**	**0**	**0**
0	1	**0**	**1**	**0**
1	0	**0**	**0**	**1**
1	1	**1**	**0**	**0**

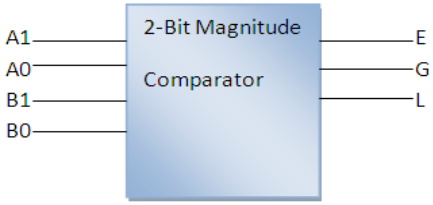
2. Simplify the functions E, G and L and give their Logic diagrams.



Function	Expression
E	A'B' + AB
L	A'B
G	AB'



3. Design a 2-bit magnitude comparator. The Block diagram is shown below.

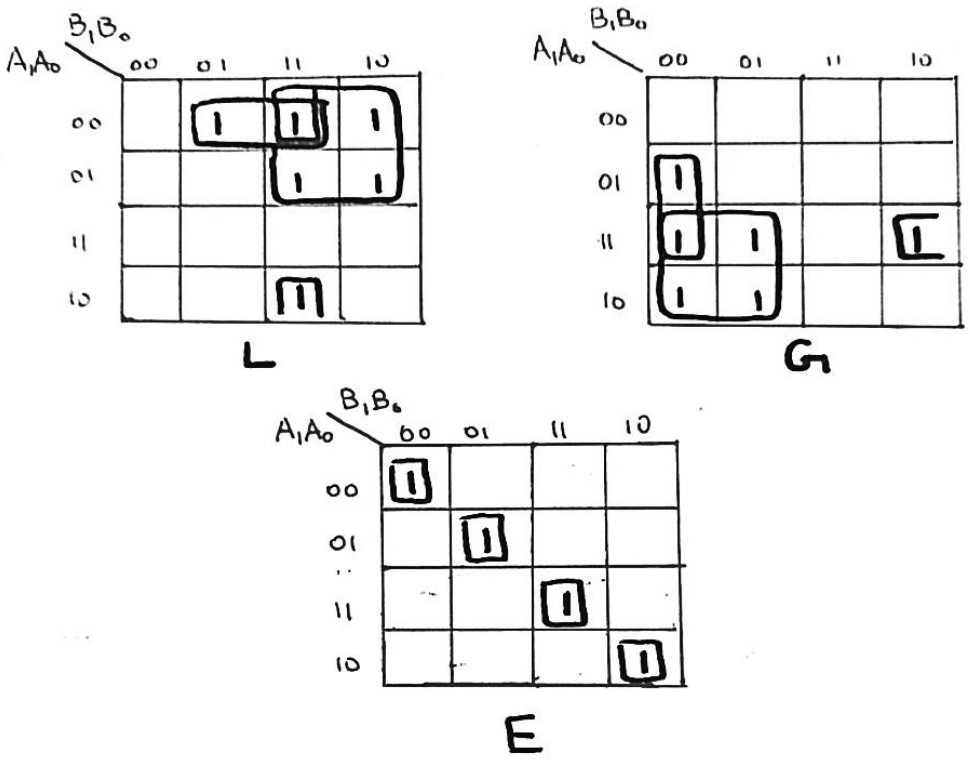


a) List the truth table.

Inputs				Outputs		
A1	A0	B1	B0	L (A<B)	E (A=B)	G (A>B)
0	0	0	0	**0**	**1**	**0**
0	0	0	1	**1**	**0**	**0**
0	0	1	0	**1**	**0**	**0**
0	0	1	1	**1**	**0**	**0**
0	1	0	0	**0**	**0**	**1**
0	1	0	1	**0**	**1**	**0**
0	1	1	0	**1**	**0**	**0**
0	1	1	1	**1**	**0**	**0**
1	0	0	0	**0**	**0**	**1**
1	0	0	1	**0**	**0**	**1**
1	0	1	0	**0**	**1**	**0**
1	0	1	1	**1**	**0**	**0**
1	1	0	0	**0**	**0**	**1**
1	1	0	1	**0**	**0**	**1**
1	1	1	0	**0**	**0**	**1**

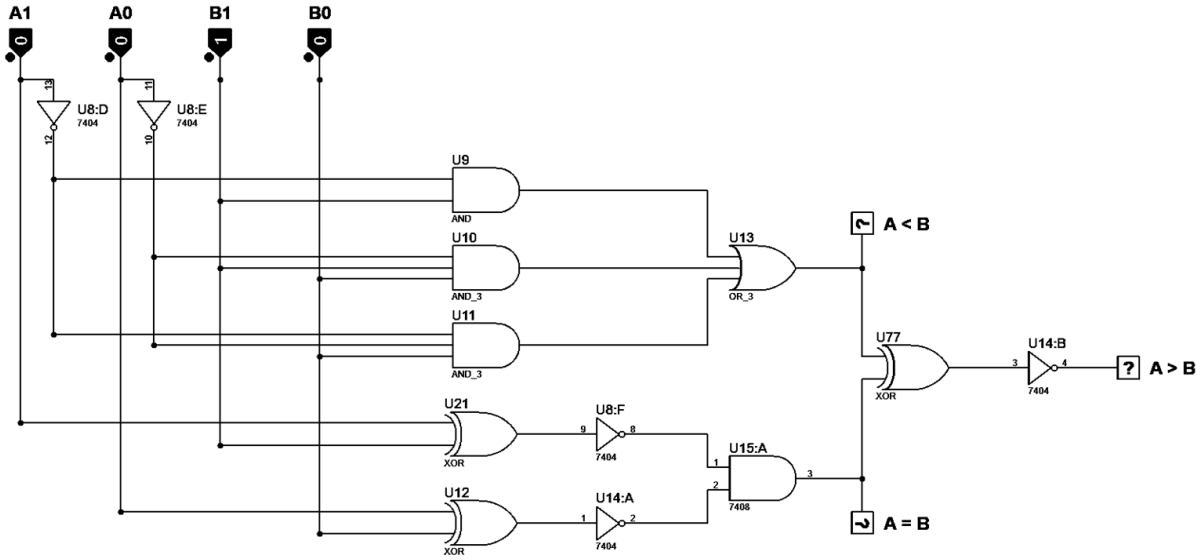
1	1	1	1	**0**	**1**	**0**

b) Find expressions for the functions E, G and L using k maps**.**



Simplified expressions:

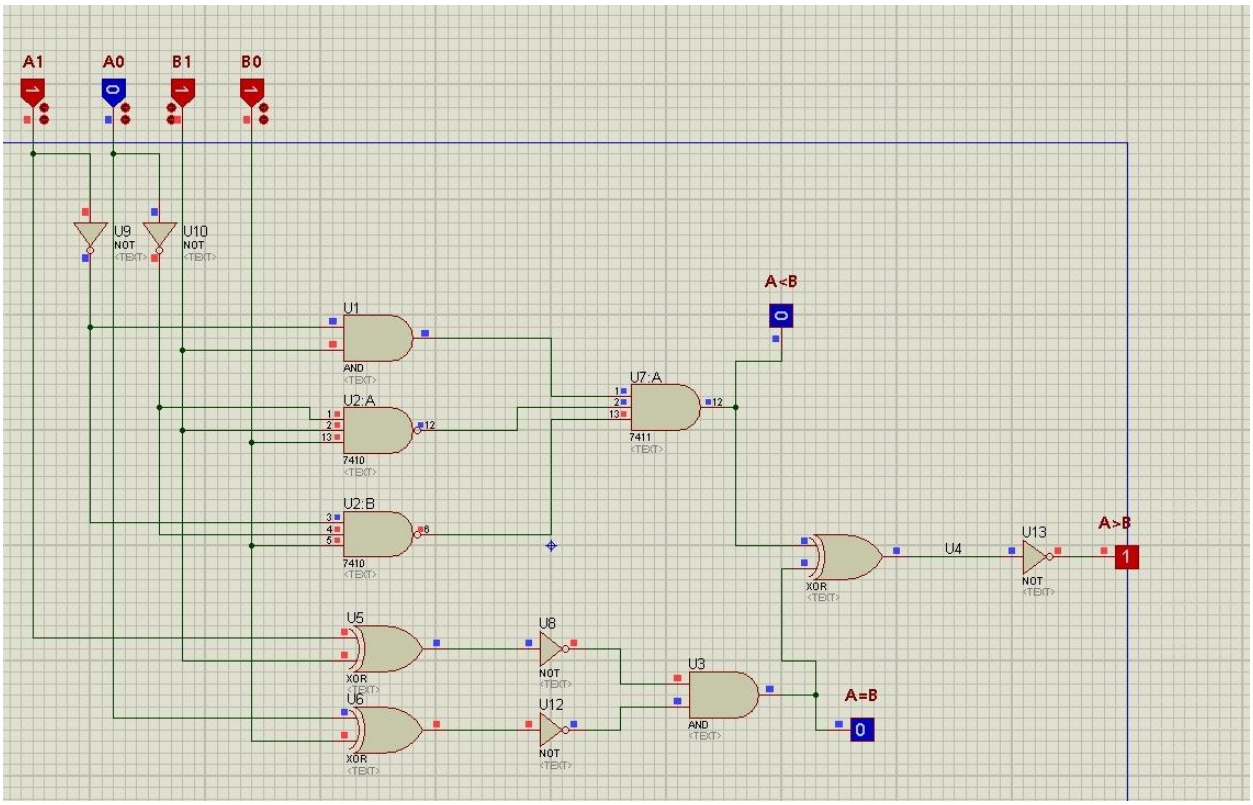
Function	Expression	Simplified
E	A1'A0'B1'B0' + A1'A0B1'B0 + A1A0B1B0 + A1A0'B1B0'	(A1⊙B1)(A0⊙B0)
L	A1'B1 + A0'B1B0 + A1'A0'B0	N/A
G	A1B1' + A0B1'B0' + A1A0B0'	N/A

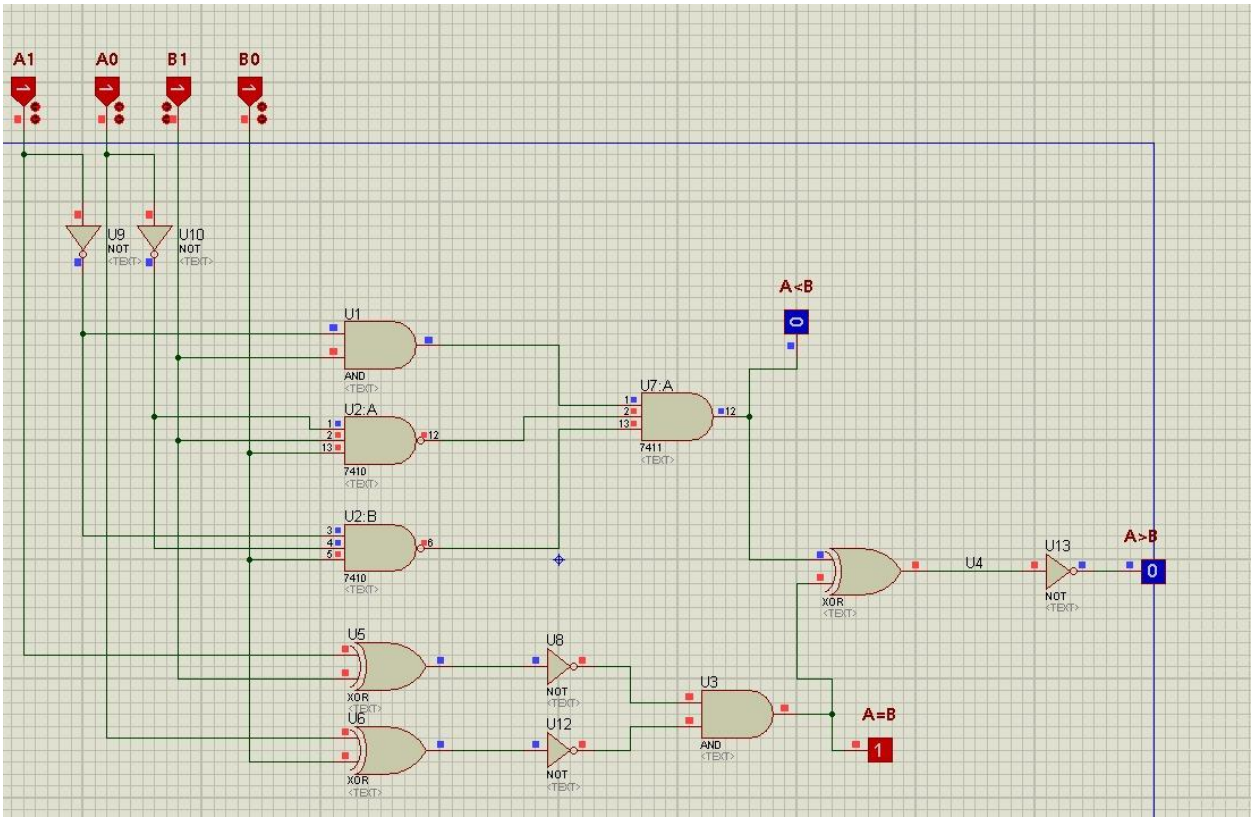


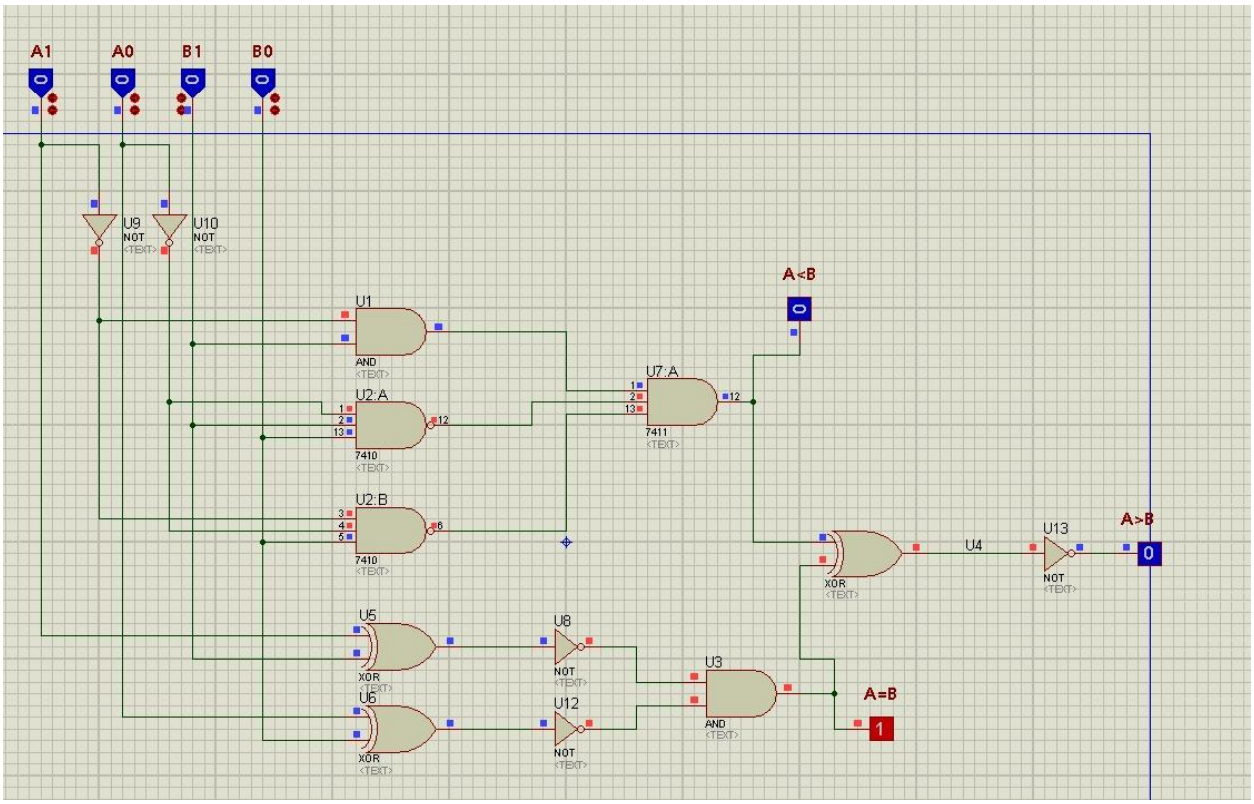
Lab Tasks

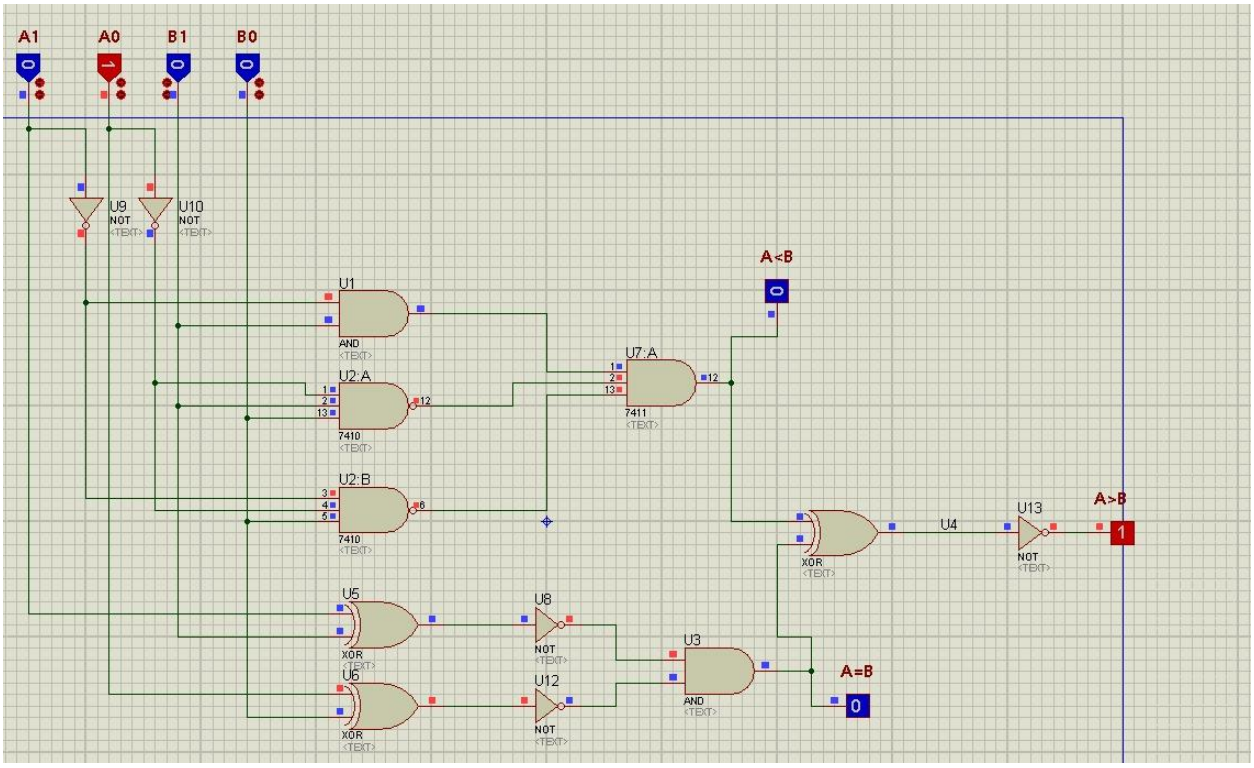
1. Implement the 2-bit Comparator circuit you arrived in your Pre-lab Task in Proteus and hardware. (4)

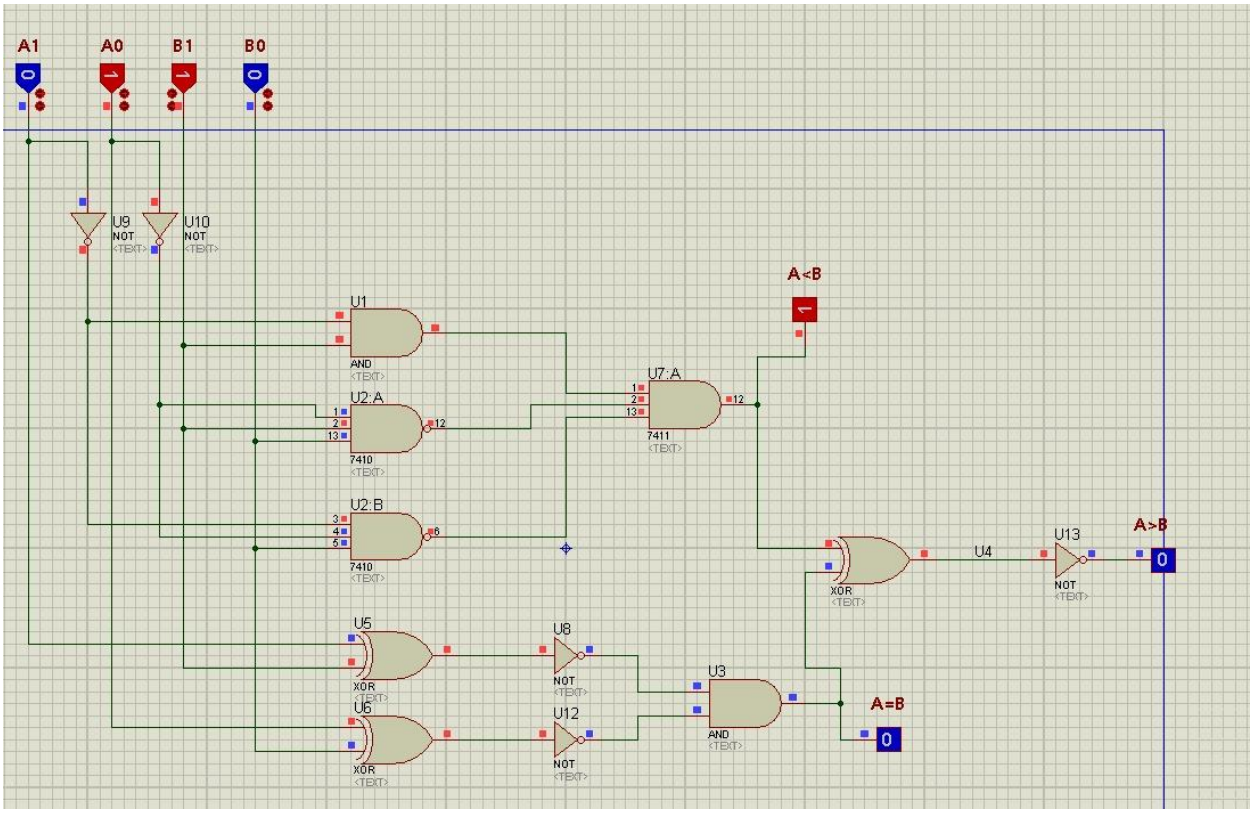
Proteus:

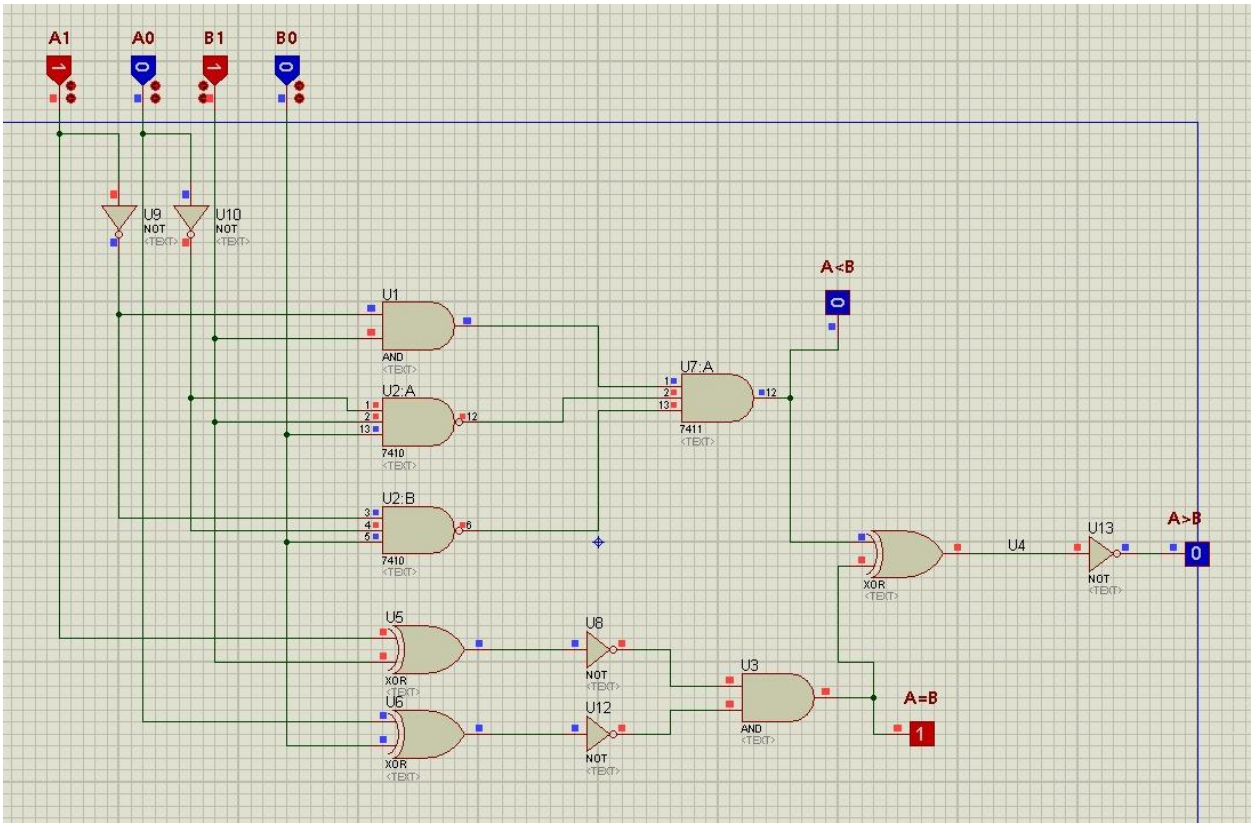


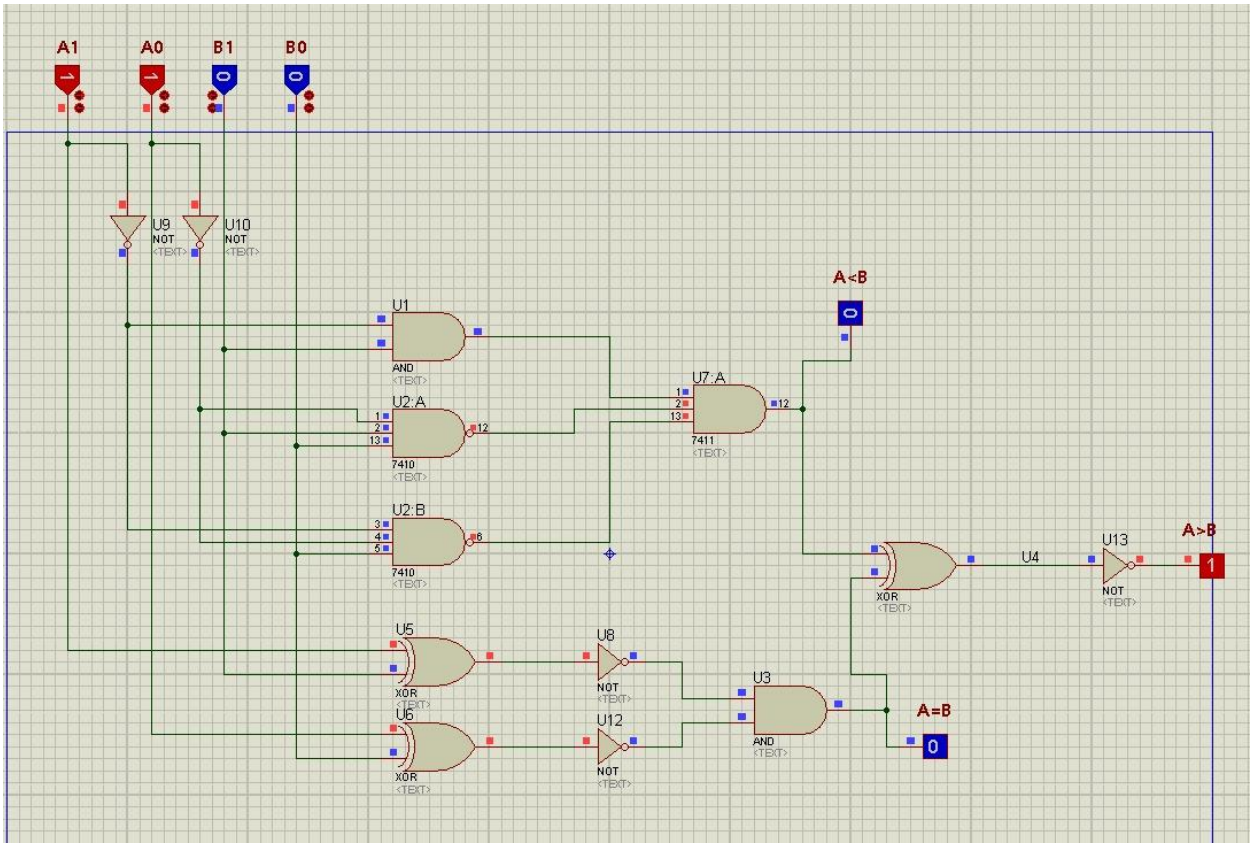

A1
A0
B1
B0
U9
NOT
U10
NOT
U1
AND
U2:A
7410
U2:B
7410
U7:A
7411
A<B
0
U4
XOR
U13
NOT
A>B
0
U5
XOR
U6
XOR
U8
NOT
U12
NOT
U3
AND
A=B
1


A1
A0
B1
B0
U9
NOT
U10
NOT
U1
AND
U2:A
7410
U2:B
7410
U7:A
7411
A<B
0
U4
XOR
U13
NOT
A>B
0
U5
XOR
U6
XOR
U8
NOT
U12
NOT
U3
AND
A=B
1


A1
A0
B1
B0
U9
NOT
U10
NOT
U1
AND
U2:A
7410
U2:B
7410
U7:A
7411
A<B
U4
XOR
U13
NOT
A>B
U5
XOR
U6
XOR
U8
NOT
U12
NOT
U3
AND
A=B

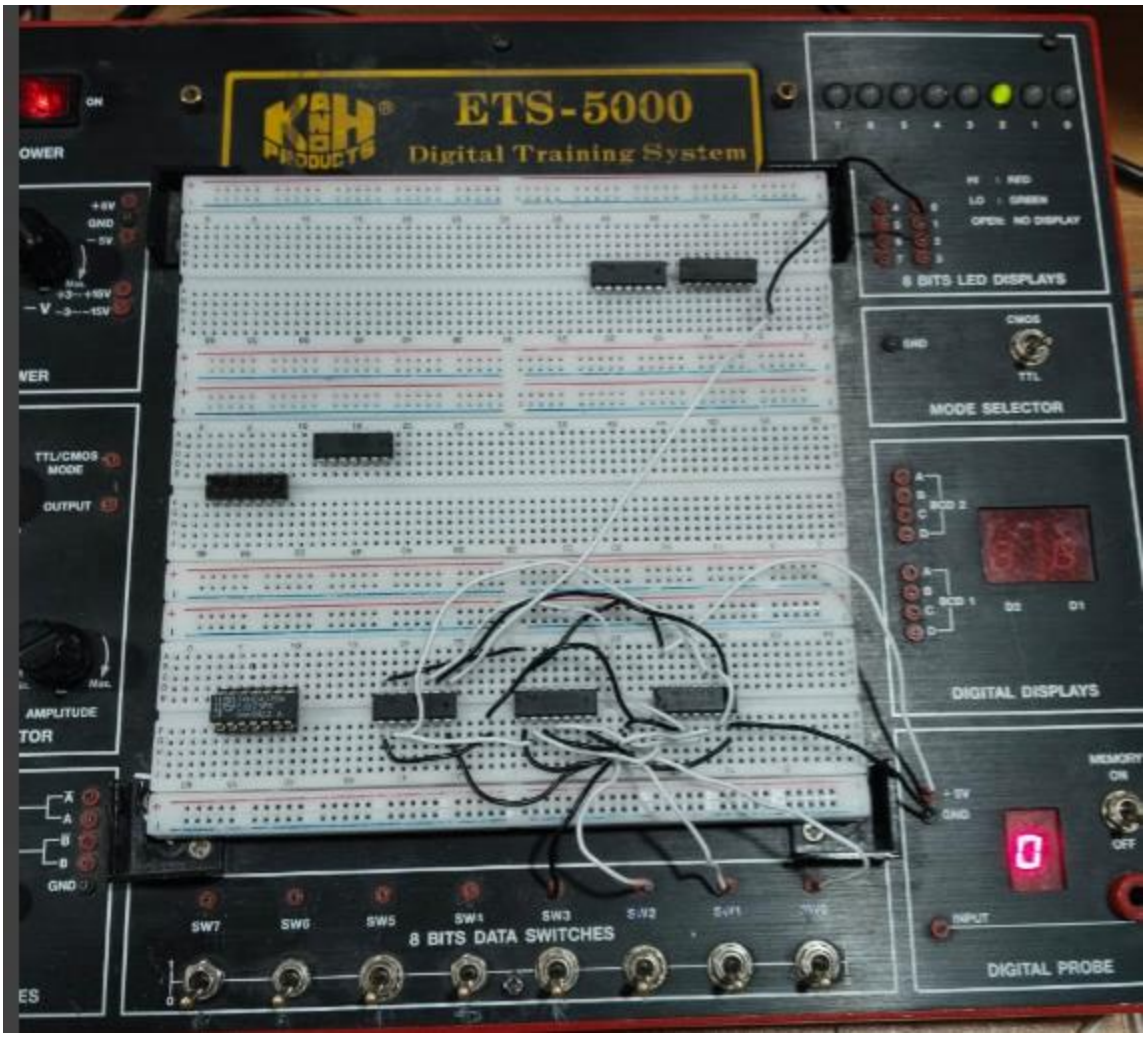

A1
A0
B1
B0
U9
NOT
U10
NOT
U1
AND
U2:A
7410
U2:B
7410
U7:A
7411
A<B
U4
XOR
U13
NOT
A>B
U5
XOR
U6
XOR
U8
NOT
U12
NOT
U3
AND
A=B


A1
A0
B1
B0
U9
NOT
U10
NOT
U1
AND
U2:A
7410
U2:B
7410
U7:A
7411
A<B
0
U4
XOR
U13
NOT
A>B
0
U5
XOR
U6
XOR
U8
NOT
U12
NOT
U3
AND
A=B
1


A1
A0
B1
B0
U9
NOT
U10
NOT
U1
AND
U2:A
7410
U2:B
7410
U7:A
7411
A<B
0
U4
XOR
U13
NOT
A>B
1
U5
XOR
U6
XOR
U8
NOT
U12
NOT
U3
AND
A=B
0

Hardware:


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
TTL/CMOS MODE
OUTPUT
AMPLITUDE
GND

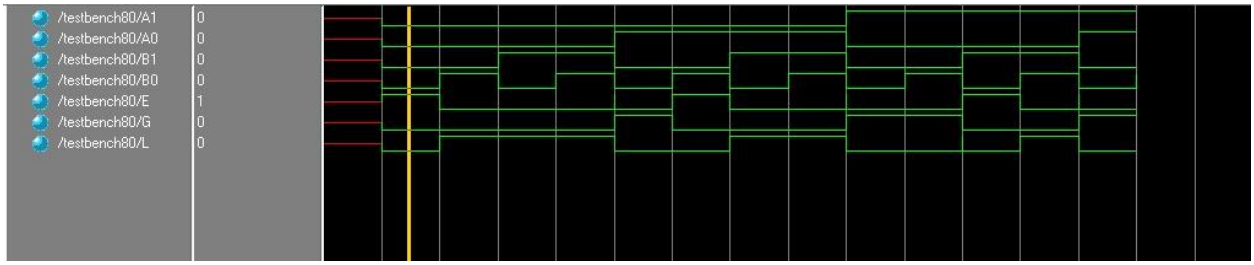

ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
8 BITS DATA SWITCHES
DIGITAL PROBE


ETS-5000
Digital Training System
8 BITS LED DISPLAYS
MODE SELECTOR
DIGITAL DISPLAYS
DIGITAL PROBE
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0

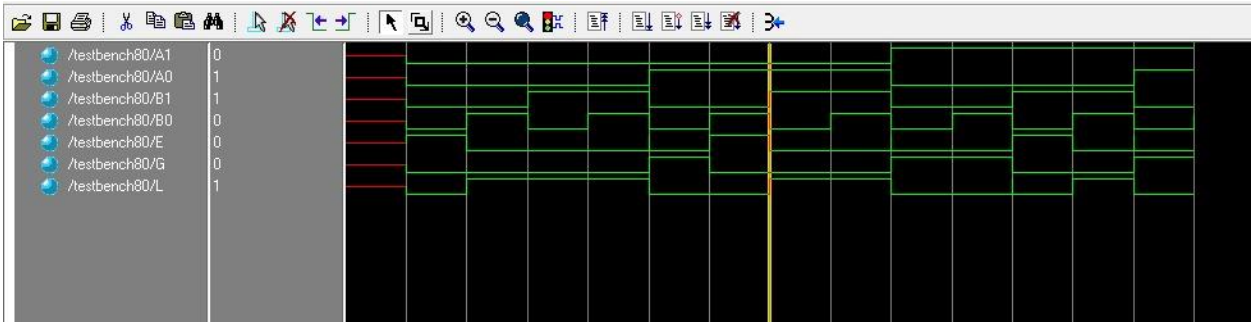
2. Write Verilog code of 2 bit comparator using dataflow modeling. (2)

```
module comparator(e, g , l, a1, a0, b1, b0);

    input a1, a0, b1, b0;
    output e, g , l;

    assign e = (a0 ^~ b0) & (a1 ^~ b1);
    assign g = (a1 & ~b1) | (a0 & ~b1 & ~b0) | (a1 & a0 & ~b0);
    assign l = (~a1 & b1) | (~a0 & b1 & b0) | (~a1 & ~a0 & b0);

endmodule

module testbench80;

    reg A1, A0, B1, B0;
    wire E, G, L;

    comparator t1(E, G, L, A1, A0, B1, B0);

    initial begin
        #100 A1 = 0; A0 = 0; B1 = 0; B0 = 0;
        #100 A1 = 0; A0 = 0; B1 = 0; B0 = 1;
        #100 A1 = 0; A0 = 0; B1 = 1; B0 = 0;
        #100 A1 = 0; A0 = 0; B1 = 1; B0 = 1;
        #100 A1 = 0; A0 = 1; B1 = 0; B0 = 0;
        #100 A1 = 0; A0 = 1; B1 = 0; B0 = 1;
        #100 A1 = 0; A0 = 1; B1 = 1; B0 = 0;
        #100 A1 = 0; A0 = 1; B1 = 1; B0 = 1;
        #100 A1 = 1; A0 = 0; B1 = 0; B0 = 0;
        #100 A1 = 1; A0 = 0; B1 = 0; B0 = 1;
        #100 A1 = 1; A0 = 0; B1 = 1; B0 = 0;
        #100 A1 = 1; A0 = 0; B1 = 1; B0 = 1;
        #100 A1 = 1; A0 = 1; B1 = 0; B0 = 0;
        #100 A1 = 1; A0 = 1; B1 = 0; B0 = 1;
        #100 A1 = 1; A0 = 1; B1 = 1; B0 = 0;
        #100 A1 = 1; A0 = 1; B1 = 1; B0 = 1;
    end

endmodule
```

Wave form:

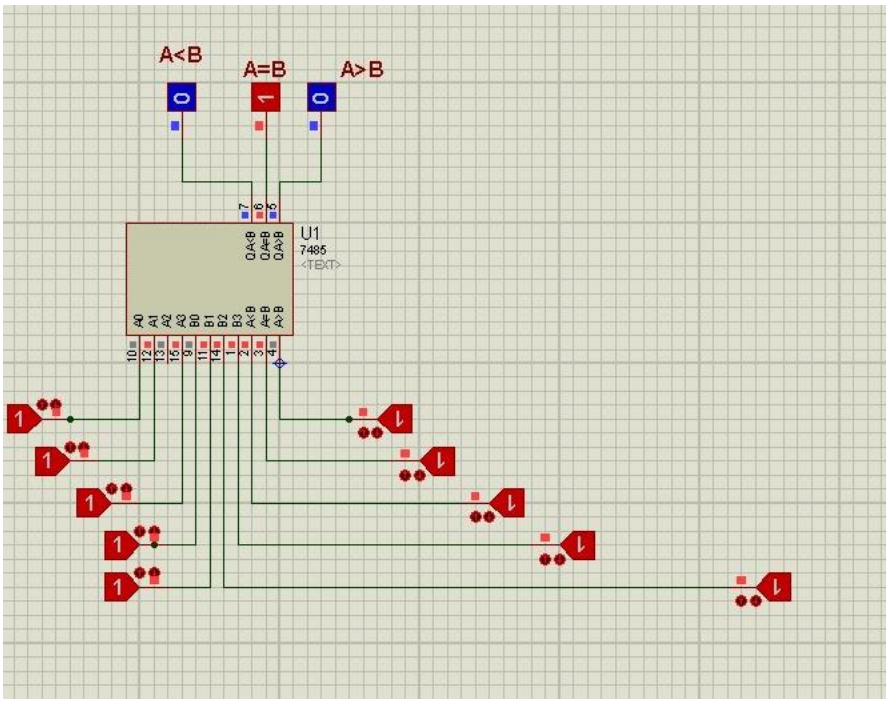


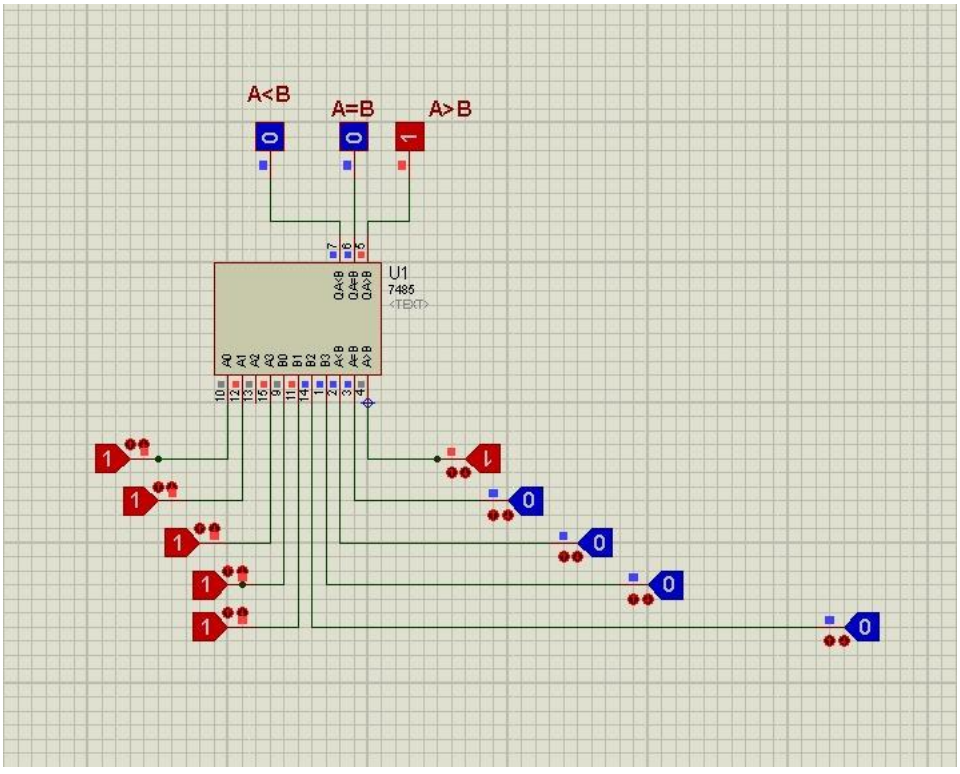
2.



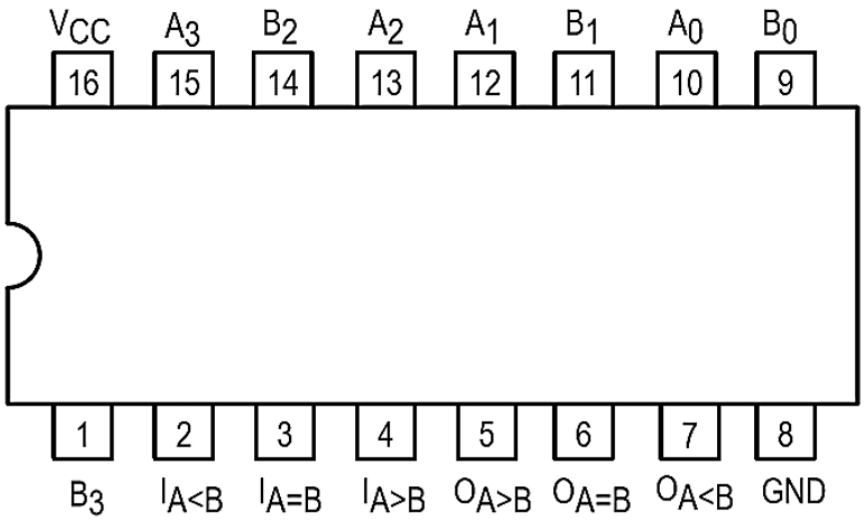
3. Simulate the 4-bit magnitude comparator IC (7485) in Proteus. Give its function table, Pin Layout and show its Proteus. (2)

Proteus:





Pin layout:



Pin Layout of 7485

Function Table:

A3	A2	A1	A0	B3	B2	B1	B0	E (A=B)	G (A>B)	L (A<B)
0	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	1	1	0	1	0
0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	1	0	0	1
0	1	0	0	0	1	0	0	1	0	0
0	1	0	1	0	0	1	1	0	0	1
0	1	1	0	0	1	0	1	0	0	1
0	1	1	1	1	0	0	1	0	1	0
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1	1	1	0	1	1	1	1	0	1	0
1	1	1	1	1	1	1	1	1	0	0