**Department of Electrical Engineering**

**Faculty Member: Miss Rafia Dated: 17-02-2025**

**Semester: 2nd Section: BSDS-2A**

*Group No.:*

**EE-221: Digital Logic Design**

**Lab 4: Design and Implementation of Simple Practical Circuits with Full Adder**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **PLO4/CLO4** | **PLO4/CLO4** | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |  |
| **Name** | **Reg. No** | **Viva / Lab Performance** | **Analysis of data in Lab Report** | **Modern Tool Usage** | **Ethics and Safety** | **Individual and Team Work** | **Total marks Obtained** |
|  |  | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **25 Marks** |
| **AILYA ZAINAB** | **523506** |  |  |  |  |  |  |
| **IMAN NAEEM** | **525378** |  |  |  |  |  |  |
| **LAIBA NASIR** | **510419** |  |  |  |  |  |  |
| **LUQMAN SHEHZAD** | **507599** |  |  |  |  |  |  |

**Lab 4: Design and Implementation of Simple Practical Circuits**

This Lab has been divided into two parts.

In first part you are required to design and implement simple practical circuits.

In the second part you are required to write Verilog code for the practical circuit

**Objectives:**

* Design the Simple practical circuits using digital logic
* Hardware Implementation of Basic Logic Circuits
* Verilog coding of the practical circuit

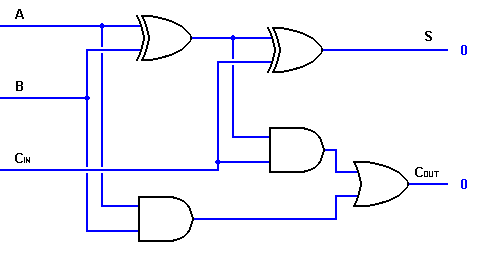
**Lab Instructions**

* This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
* The lab report will be uploaded on LMS three days before scheduled lab date. The students will complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
* The students will start lab task and demonstrate design steps separately for step-wise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
* Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
* After the lab, students are expected to unwire the circuit and deposit back components before leaving.
* The students will complete lab task and submit complete report to Lab Engineer before leaving lab
* There are related questions at the end of this activity. Give complete answers.

.

**Lab Task 1:** (5 Marks)

Implement the Full Adder Circuit given below, make its truth table and run the circuit on Proteus.

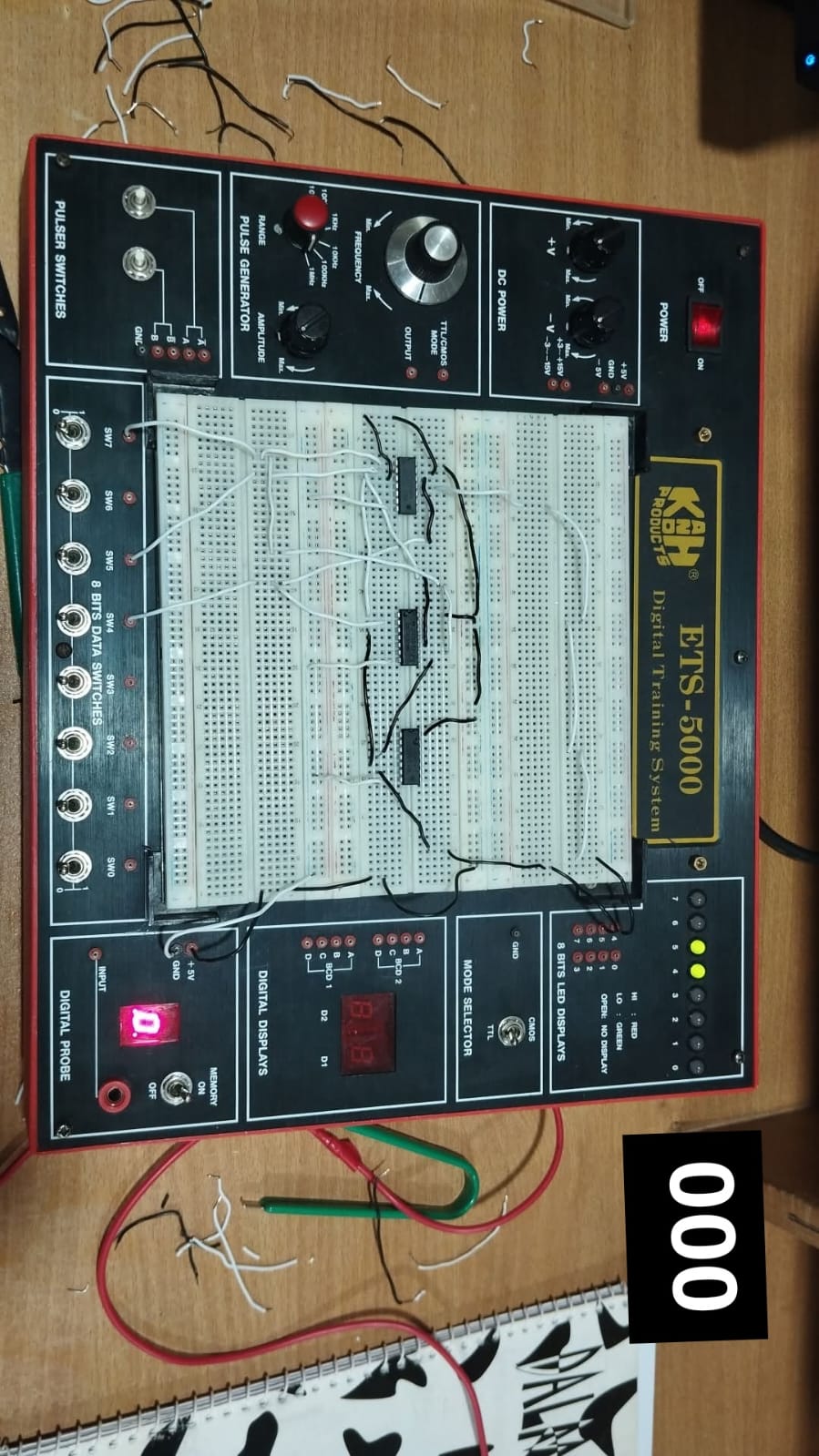


**Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Cin** | **Cout** | **S** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** | **1** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **1** | **1** |

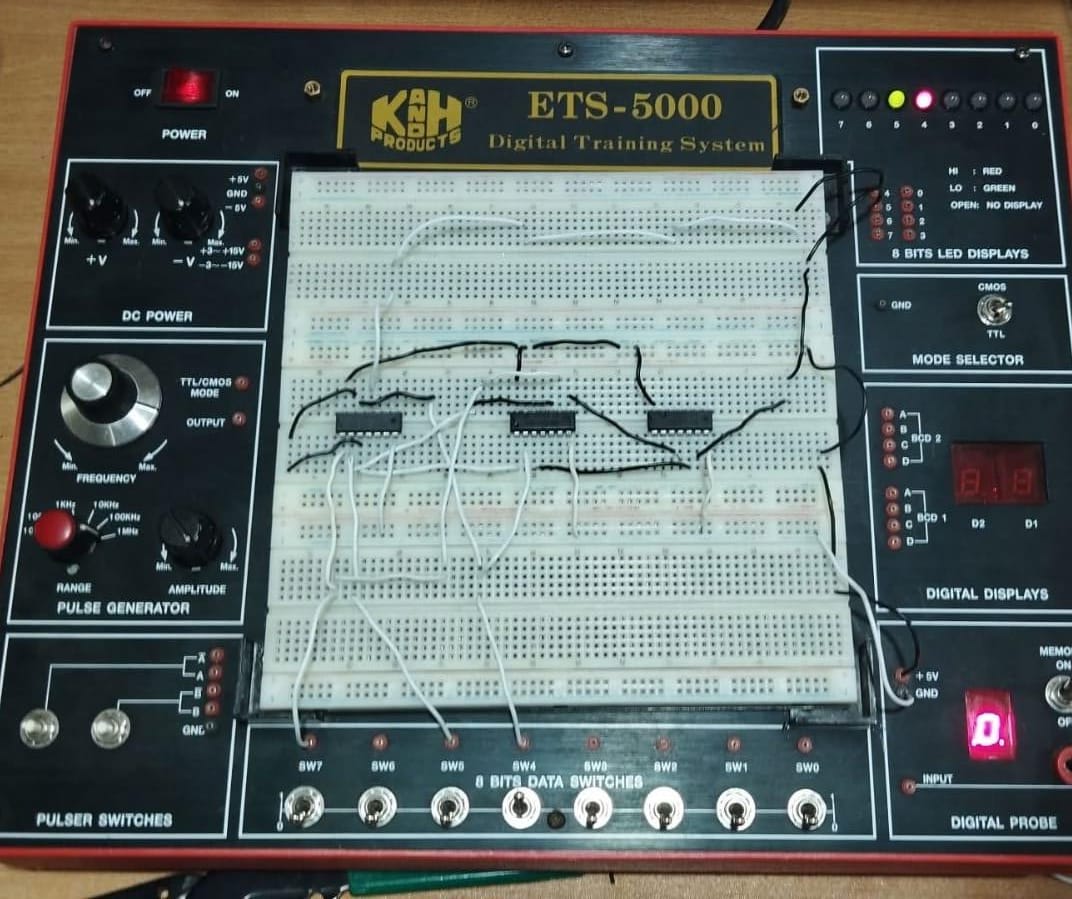
Which are the results we would expect from a FULL ADDER circuit, and to ensure integrity, we have implemented the given schematic on Proteus as well

**Hardware Implementation:**

****

**INPUT: 000**

**OUTPUT: 00**

****

**INPUT: 001**

**OUTPUT: 01**

****

**INPUT: 010**

**OUTPUT: 01**

****

**INPUT: 011**

**OUTPUT: 10**

****

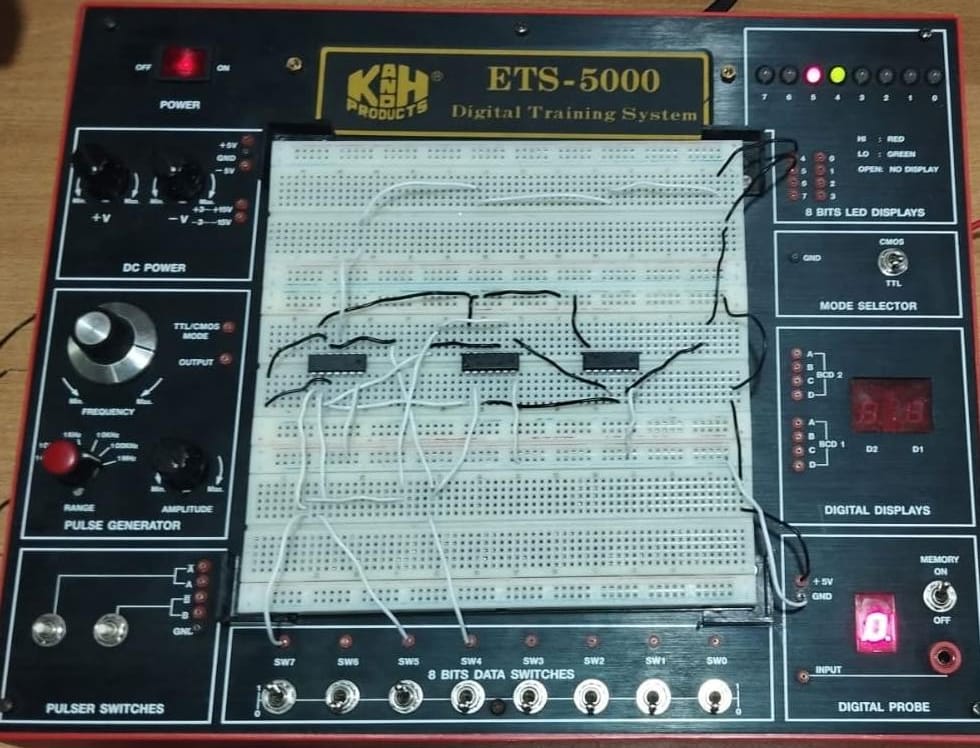
**INPUT: 100**

**OUTPUT: 01**

****

**INPUT: 101**

**OUTPUT: 10**

****

**INPUT: 110**

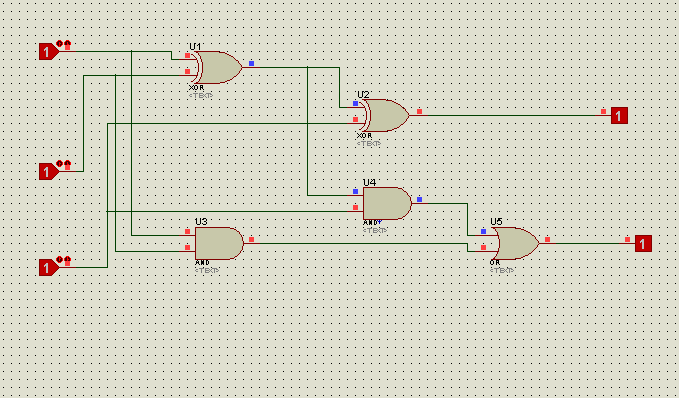
**OUTPUT: 10**

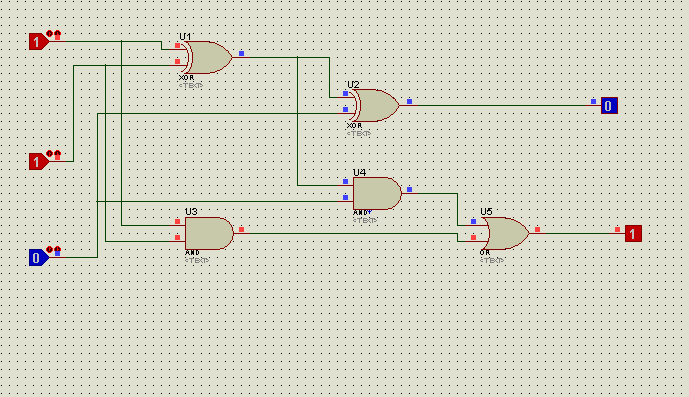
****

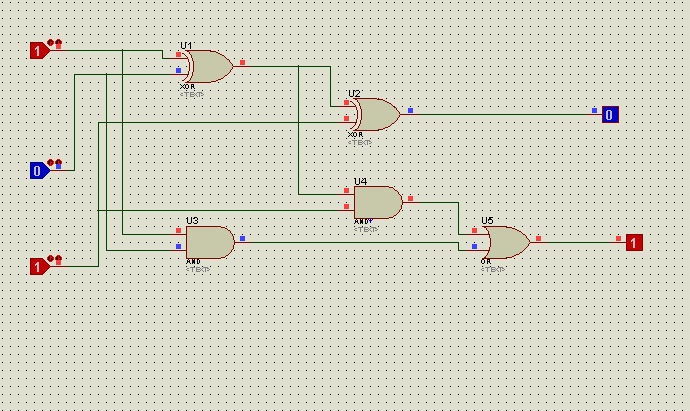
**INPUT: 111**

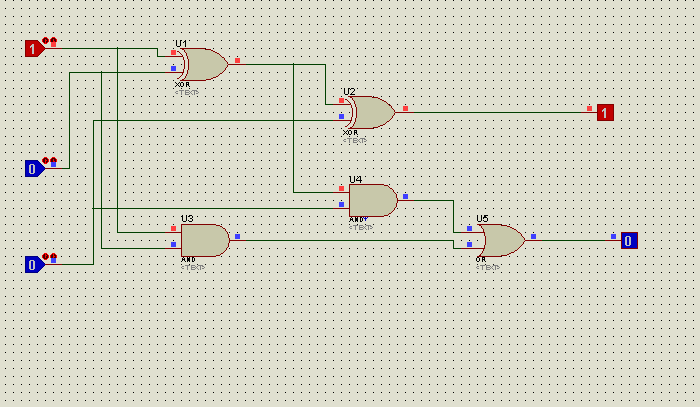
**OUTPUT: 11**

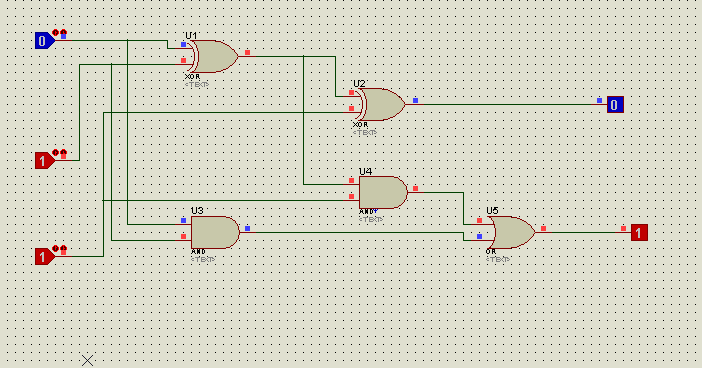
**Proteus Simulation:**

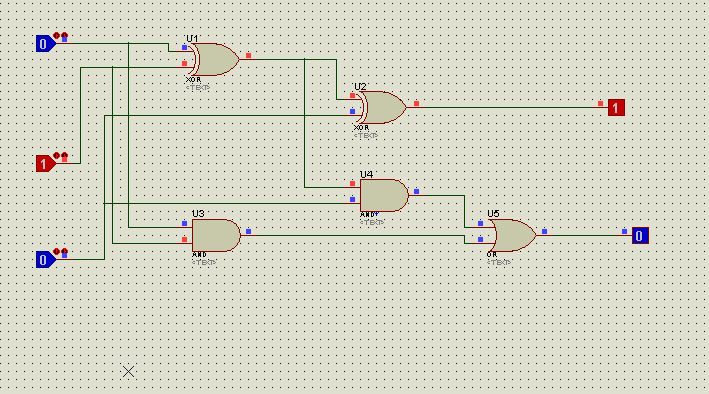
****

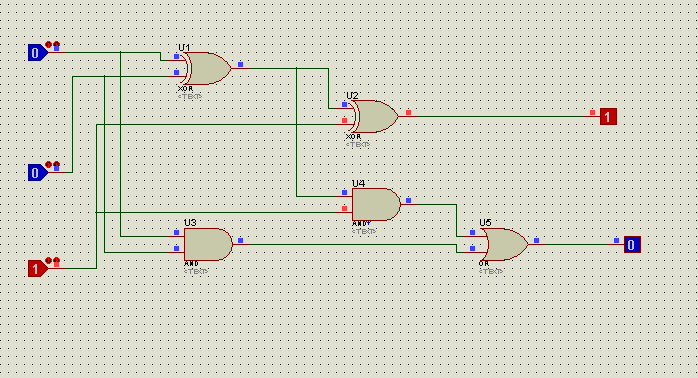
****

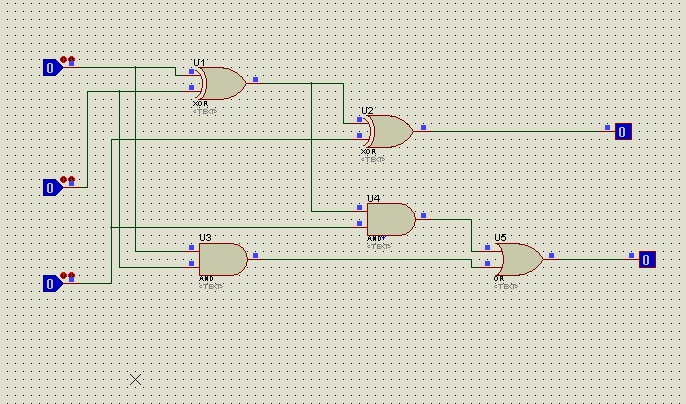
****











**Lab Task 2:** (2.5 Marks)

Simulate the gate-level model of the circuit you patched in task 1. Give the code and resulted waveform in the space provided below.

CODE:

module task1(sum, carry, a, b, c);

input a, b, c;

output sum, carry;

wire w1, w2, w3;

xor x1(w1, a, b);

xor x2(sum, w1, c);

and a1(w2, a, b);

and a2(w3, w1, c);

or o1 (carry, w3, w2);

endmodule

module testbench22;

reg A, B, C;

wire SUM, CARRY;

task1 t22(SUM, CARRY, A, B, C);

initial

begin

#100 A=1'b0; B=1'b0; C=1'b0;

#100 A=1'b0; B=1'b0; C=1'b1;

#100 A=1'b0; B=1'b1; C=1'b0;

#100 A=1'b0; B=1'b1; C=1'b1;

#100 A=1'b1; B=1'b0; C=1'b0;

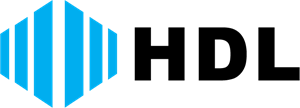
#100 A=1'b1; B=1'b0; C=1'b1;

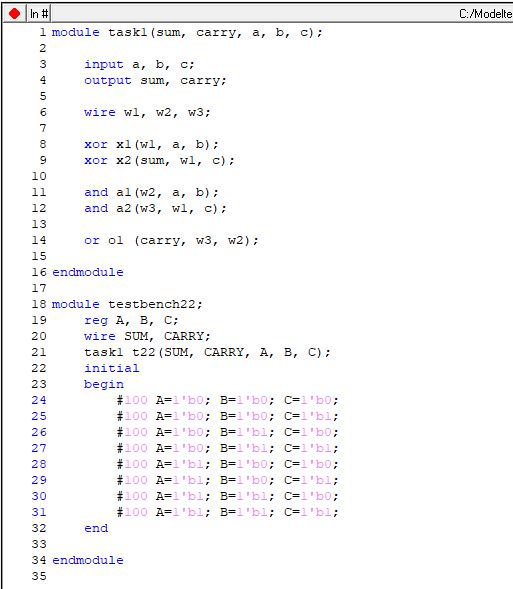
#100 A=1'b1; B=1'b1; C=1'b0;

#100 A=1'b1; B=1'b1; C=1'b1;

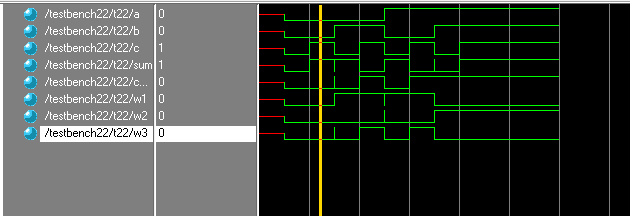
end

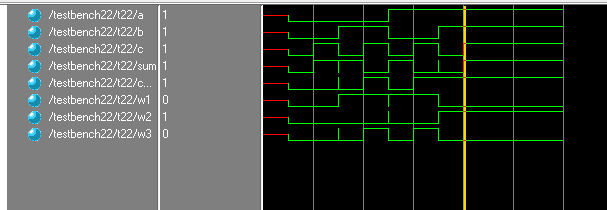
Endmodule





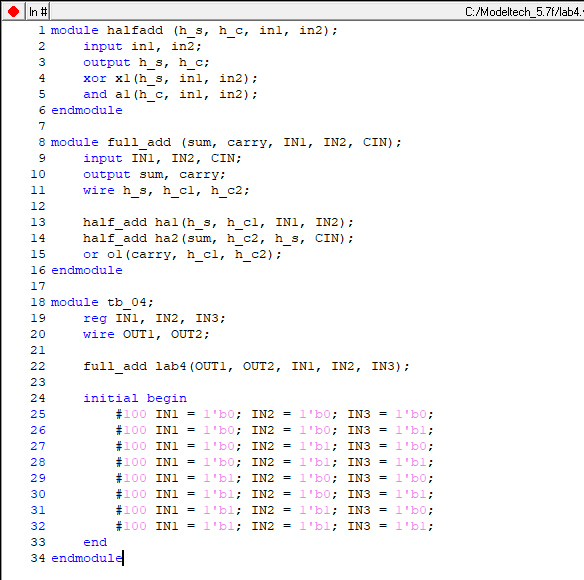
OUTPUT:



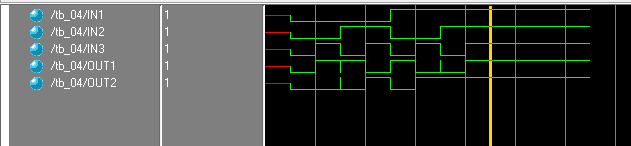


**Lab Task 3:** (2.5 Marks)

Write Verilog code to implement full adder using two half adder circuits.



OUTPUT:



**Observations/Comments:**

In this lab, we deployed the concepts learned in Lab 2, *Implementation of a Half Adder circuit*, to implement a Full Adder. Two Half Adders concatenated together and through use of an additional OR gate give us a Full Adder circuit, essentially implying that:

**Full Adder = Half Adder + Half Adder**

We have also confirmed/verified the circuit’s output as it conforms to the truth table laid out in the Pre – lab and that it serves the purpose for what it was designed conclusively.