# OPEN ENDED EXPERIMENT 2

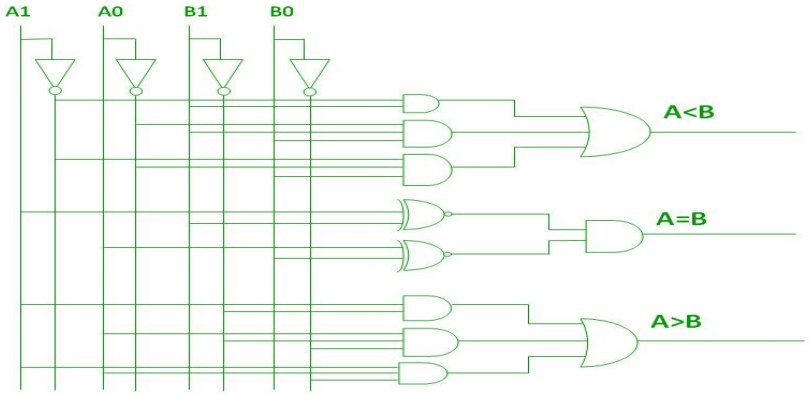
**AIM :** Simulation of 2 bit Magnitude comparator using Verilog HDL in EDA Playground.
Design and Verification of 2 bit Magnitude comparator circuit in TinkerCAD.

## Component/Software Used :

| Component/Software | Specifications |
|---|---|
| ICs | 74HC04,74HC08, 74HC32, 74HC86 |
| Bread Board, Power supply, LEDs, Resistors, Switches, Push button for manual clock, Connecting wires | - |
| Software(s) Used | TinkerCAD, EDA Playground |

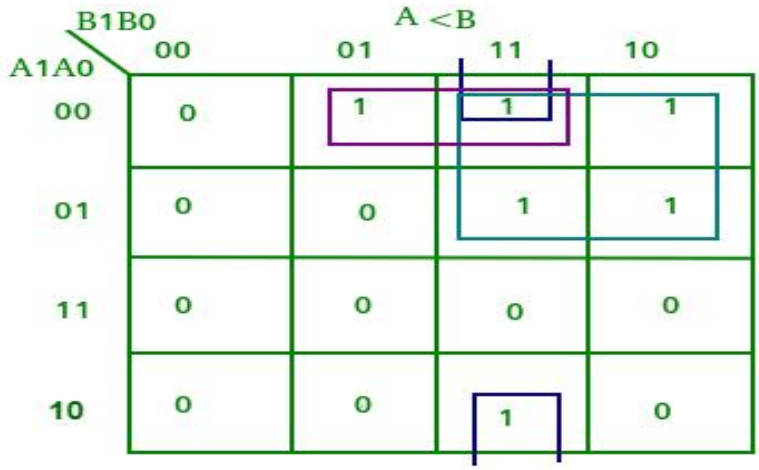
## Theory :

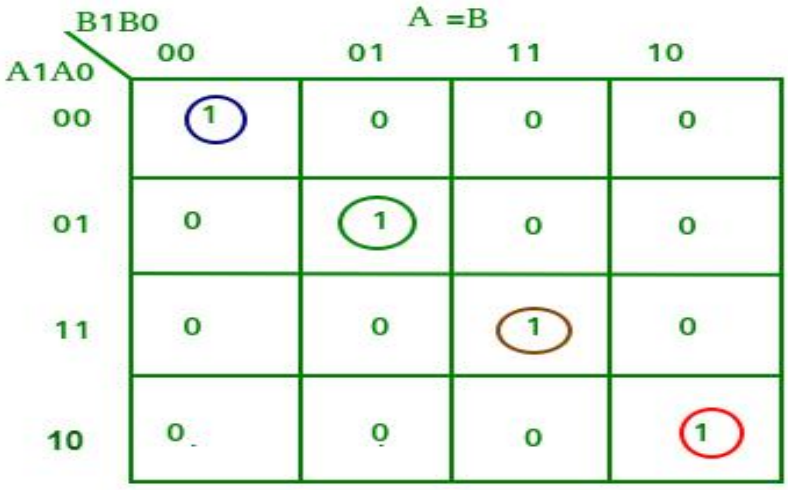
A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

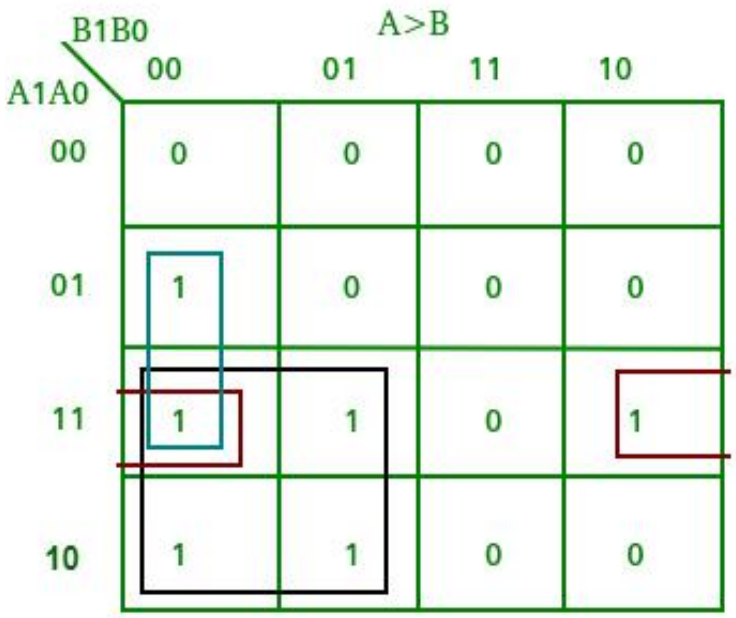


| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| A1 | A0 | B1 | B0 | A<B | A=B | A>B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

# K-Map for 2 bit comparator






A>B:- A1B1’ + A0B1’B0’ + A1A0B0’
A=B:- A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0B1B0 + A1A0’B1B0’
= A1’B1’ (A0’B0’ + A0B0) + A1B1 (A0B0 + A0’B0’)
= (A0B0 + A0’B0’) (A1B1 + A1’B1’)
= (A0 Ex-Nor B0) (A1 Ex-Nor B1)
A<B:- A1’B1 + A0’B1B0 + A1’A0’B0

**Verilog codes and Testbench codes:**

**https://www.edaplayground.com/x/tiC6**

**Testbench :**

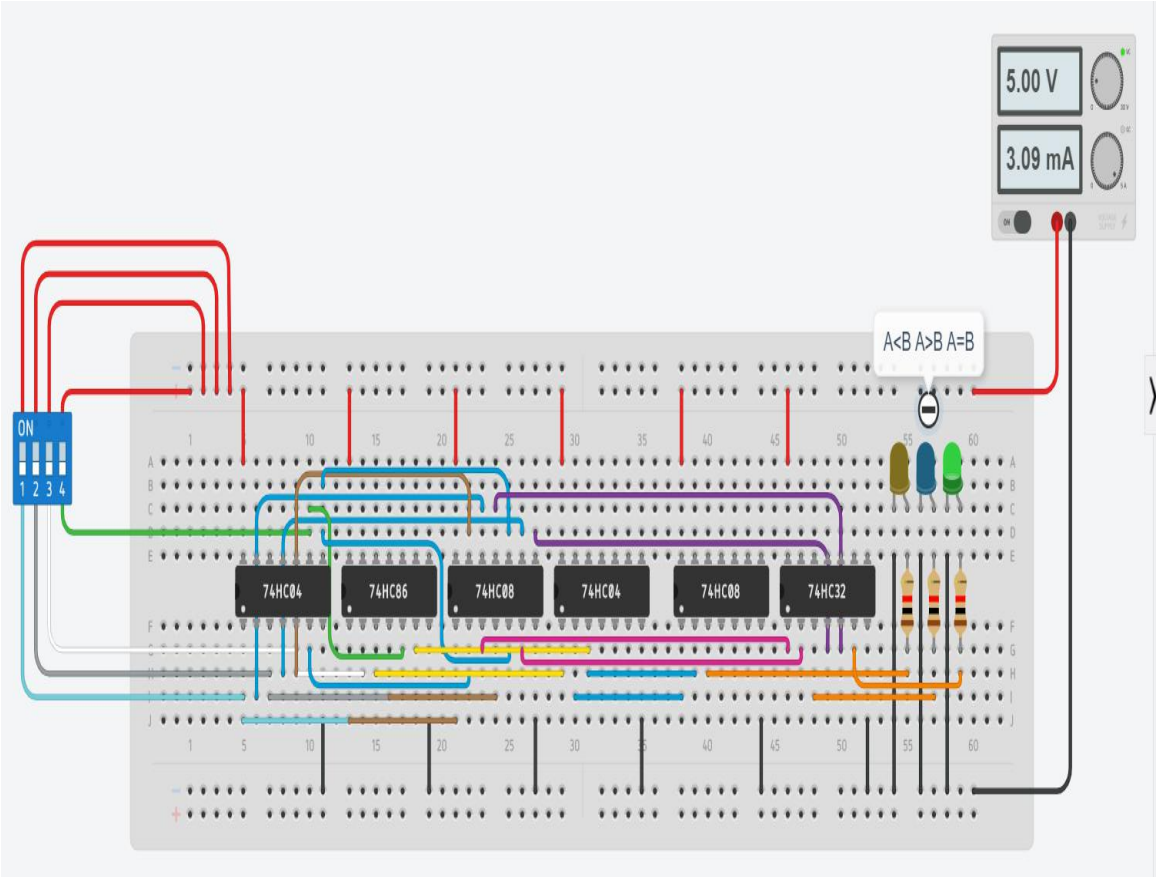
```
module comparator_tb();

  reg [1:0] x;
  reg [1:0] y;
  reg xltyin;
  reg xgtyin;
  wire xgty,xlty,xety;
```

```
initial
  begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end
 initial
  begin
    x = 2'b0;
    y = 2'b0;
    xltyin = 1'b0;
    xgtyin = 1'b0;

    #10 x = 2'b01;
    #10 y = 2'b10;
    #10 xgtyin = 1'b1;
    #10 xgtyin = 1'b0;
        x = 2'b10;
    #10 xltyin = 1'b1;
    #10 x = 2'b11;
    #10 $finish;

  end

twobitcomparator u_dut(
  .xgtyin(xgtyin),
  .xltyin(xltyin),
  .x(x),
  .y(y),
  .xgty(xgty),
  .xlty(xlty),
  .xety(xety)
);
  endmodule
```

**Design :**

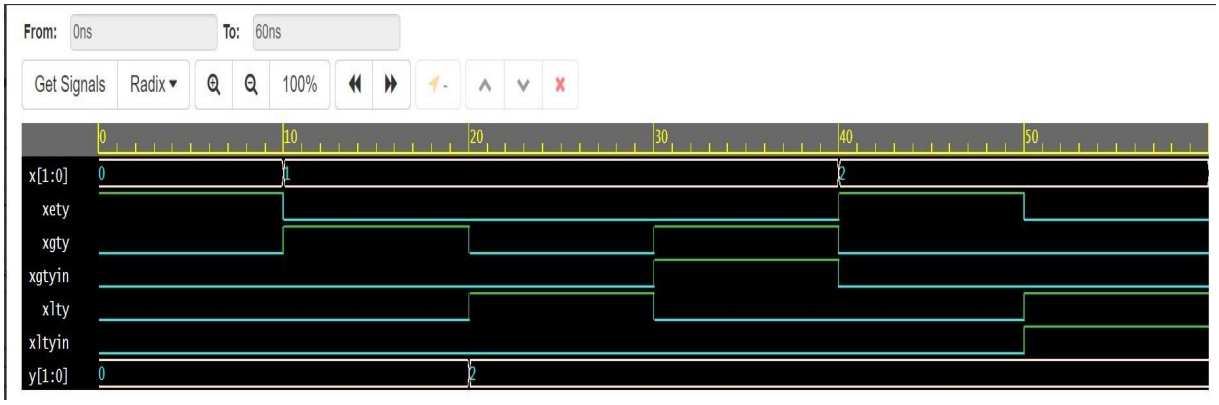
```
module
twobitcomparator(xgtyin,xltyin,x,y,xgty,xlty,xety);
    //I/O
  output xgty, xety, xlty;
  input  xgtyin, xltyin;
  input [1:0] x,y;

  assign xgty = xgtyin | (~xltyin & ((x[1] > y[1]) | ((x[1]
== y[1]) & (x[0] > y[0]))));
  assign xlty = xltyin | (~xgtyin & ((x[1] < y[1]) | ((x[1]
== y[1]) & (x[0] < y[0]))));
    assign xety = ~(xlty | xgty);
endmodule
```

**Observation / Results:**




**A = B**

# EP WAVE




## Conclusion :

By conducting this experiment we were able to simulate a 2 bit comparator in Verilog HDL using EDA Playground. We also designed and verified the circuit of a 2 bit comparator in TinkerCAD and with this we were able to find out how a 2 bit comparator works and we understood the logic behind it.

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