SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				34 RoS orig 006047			
				6047 GI			

REV / SPEC. NO.

PRELIMINARY

CUSTOMER PROCUREMENT SPECIFICATION

27HC64/27HC641

64K UV ERASABLE RPOM

SHEET													
LAST REV													

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT   **MICROELECTRONICS GROUP**

TITLE
CPS FOR CMOS 64K UV EPROM

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED						SHEET 1	OF 13
BY								SPEC. NO.	REV 7/8/85
DATE		7/8/85							

FORM 1E104 (3/81)

65,536 Bit CMOS ERASABLE PROM

FEATURES

. Organization - 8192 x 8

. Low Power Dissipation:
    80mA Active Mode
    200uA Standby Mode

. Single +5V ± 10% Power Supply

. Access Time:
    50ns max 27HC64-05
    70ns max 27HC64-07
    100ns max 27HC64-10
    150ns max 27HC64-15

. Fast Programming Algorithm

. Auto ID^{TM} Identification Aids Automatic Programming

. Fully Static Operation, No Clocks Required

. All Inputs/Outputs Fully TTL Compatible

. JEDEC Approved Pinout

. Available in Wide Temperature Ranges:
    Commercial (C) = 0° to 70°C
    Industrial (I) = -40° to +85°C
    Militrary (M) = -55°C to +125°C

27HC64

Pin		Pin	
VPP	1	29	VDD
A12	2	27	PGM
A7	3	26	NC
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19	D7
D0	11	18	D6
D1	12	17	D5
D2	13	16	D4
VSS	14	15	D3

27HC641

| Pin		Pin	
A7	1	24	VDD
A6	2	23	A8
A5	3	22	A9
A4	4	21	A10
A3	5	20	CE/Vpp
A2	6	19	A11
A1	7	18	A12
A0	8	17	D7
D0	9	16	D6
D1	10	15	D5
D2	11	14	D4
GND	12	13	D3

DESCRIPTION

The 27HC64 and 27HC641 are high speed CMOS Ultra Violet light erasable electronically programmable Read Only Memories. They are organized as 8192 words by 8 bits per word and operate from a single +5 volt supply with a tolerance of ± 10%.

The 27HC64 and 27HC641 feature a maximum access time of 50ns which is compatible with high speed microprocesors and are designed to utilize a fast programmable algorithm to reduce programming time.

The 27HC64 is packaged in a 29 pin dual-in-line package and the 27HC641 in a 24 pin dual-in-line package with quartz lids. This lid allows the user to erase the bit pattern, whereby a new pattern can then be written into the device.

BLOCK DIAGRAM
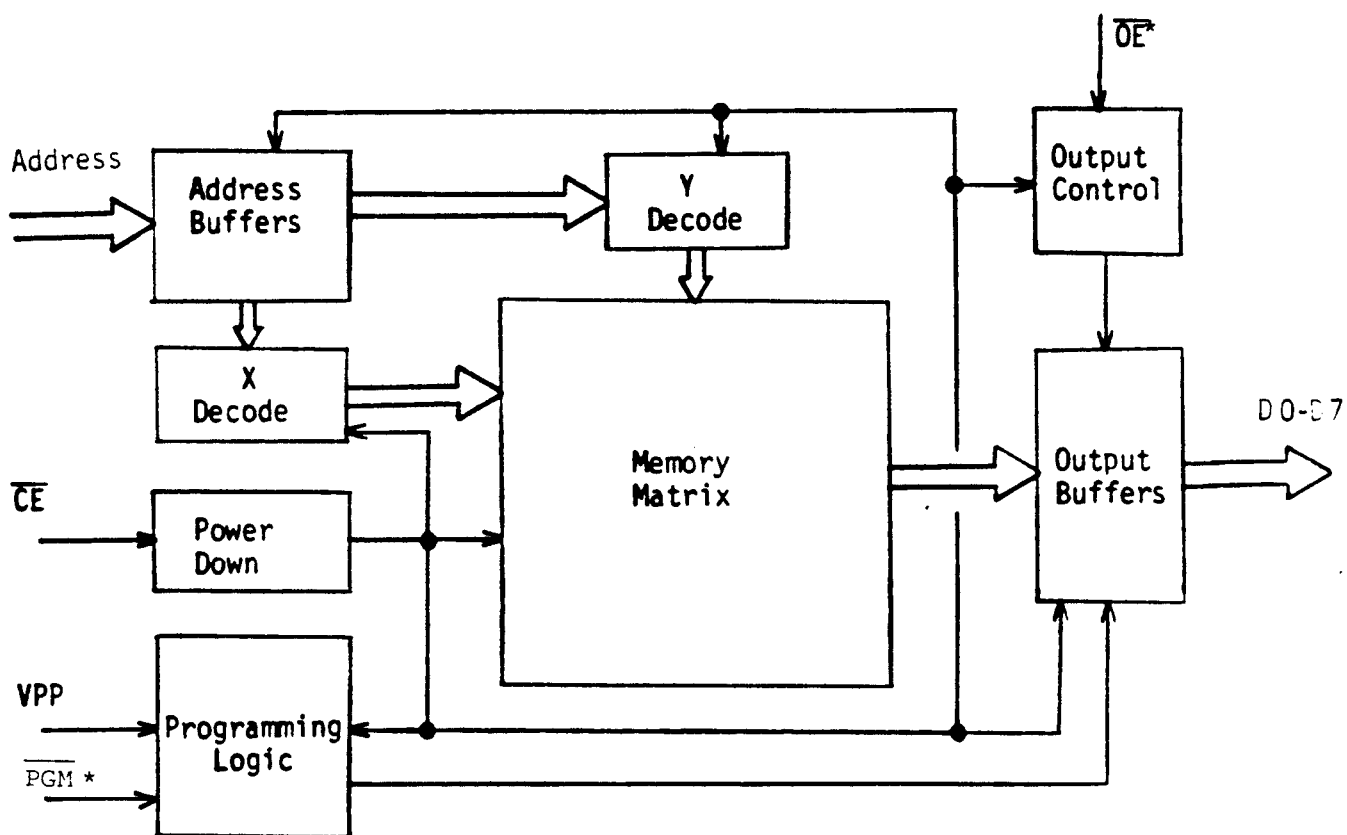
*These inputs on 27HC64 only.

MODES — 27HC64

MODES	$\overline{CE}$	$\overline{OE}$	VPP	A9	DO – D7	$\overline{PGM}$
Read	VIL	VIL	VDD	X	Dout	VOH
Program	VIL	VIH	+12V	X	Din	VIL
Program Verify	VIL	VIL	+12V	X	Dout	VIH
Program Inhibit	VIH	X	+12V	X	High Z	X
Standby	VIH	X	VDD	X	High Z	X
Output Disable	VIL	VIH	VDD	X	High Z	VIH
Identity	VIL	VIL	VDD	+12V	Code	VIH

MODES	CE/Vpp	A9	DO – D7
Read	VIL	X	DOUT
Program	+12V	X	DIN (see note)
Standby	VIH	X	High Z
Identify	VIL	+12V	Code

Note: See programming waveform for 27HC641.

READ MODE   (See Timing Diagrams and AC Characteristics)

Read mode is accessed when:

>   a)   the $\overline{CE}$ pin (20) is low to power up (enable) the chip.
>   b)   the $\overline{OE}$ pin (22) is low to gate the data to the output pins. (27HC64 only)

For read operations, if the addresses are stable, the address access time
(t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is
transferred to the output after a delay (t_{OE}) from the falling edge of OE.
(27HC64 only)

STANDBY MODE

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not
defined.

When these conditions are met, the supply current will drop from 90mA to 200uA.

OUTPUT ENABLE/Vpp   (27HC64 only)

This feature eliminates bus contention in multiple bus microprocessor systems
and the outputs go high impedance when the following conditions are true:

>   The $\overline{OE}$ pin is high and a program mode is not defined. When a +12V input is
>   applied to this pin, it supplies the programming voltage (Vpp) to program
>   the device

ERASE MODE

The memory matrix is erased to the all "1"'s state as a result of being exposed
to Ultra Violet light. To ensure complete erasure a dose of 15 watt-second /
cm^2 is required. This means that the device window must be placed within one
inch and directly underneath an ultraviolet lamp with wavelength of 2537
Angstroms, intensity of 12000 watt-second / cm^2 for 20 minutes.

PROGRAMMING MODE   (27HC64)

Programming takes place when both:

>   a)   Vpp is greater than 12V and
>   b)   The CE pin is low

Since the erased state is "1" in the array, programming of "0" is required.
The address to be programmed is set via A0-A15 and the data to be programmed is
presented to D0-D7. When data and address are stable, a low going pulse on the
CE line programs that location. Fast programming techniques will be accepted by
the chip.

Programming the 27HC641 takes place when the $\overline{CE}$/Vpp pin is taken to 12.5V after
address and data have settled. This programs the required "0"'s in the byte since
the erased status is "1".

PROGRAMMING (continued)

A 1 msec programming pulse will be given and the byte then verified. If the byte
failed to verify, apply another 1 msec programming pulse and check the byte
again. Continue applying 1 msec pulses until either the byte verifies or 25
pulses have been applied. If 25 pulses are applied and the byte still does not
verify, fail the device. After the byte verifies, another 3 times the number of
1 msec pulses previously given will be applied; i.e., minimum each byte will
receive is 4 x 1 msec programming pulses and maximum in the fast programming
mode willbe 100 x 1 ms pulses.

VERIFY (27HC64 only)

After the array has been programmed it must be verified to ensure all the bits
have been correctly programmed. This mode is entered when all the following
conditions are met:

    a) Vpp (pin 1) is greater than 12.0V
    b) the $\overline{PGM}$ line is high
    c) the $\overline{OE}$ line is low
    d) the $\overline{CE}$ line is low

Verifying the 27HC641 is done by taking the $\overline{CE}$/Vpp pin to a low level after the
address has settled and reading the data out.

INHIBIT

When programming multiple devices in parallel with different data, only $\overline{CE}$ need
be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a
particular device (27HC64), that device will be programmed, all other devices
with $\overline{CE}$ held high will not be programmed with the data although address and data
will be available on their iunput pins; i.e., when a high level is present on $\overline{CE}$
(or $\overline{PGM}$, 27HC64 only), the device is inhibited from programming

MANUFACTURERS IDENTITY

In this mode specific data is output identifying manufacturer as General
Instrument, device type, where manufactured, etc. This mode is entered when
pin 24 (A9) is taken up to between 11.5 - 12.5V. the row x-decoders become
disabled internally and the ROM data held in four bytes can be output. The $\overline{CE}$
and $\overline{OE}$ lines on the 27HC64 must be at ^{V}IL ($\overline{OE}$ not required on 27HC641). A0 and
A1 are used to access any of the four non-erasable bytes whose data appears on D0
through D7.

The General Instrument identify code is as follows:

Pin Identity	A0 (10)	D7 (19)	D6 (18)	D5 (17)	D4 (16)	D3 (15)	D2 (13)	D1 (12)	D0 (11)	Hex Code
Manufacturer	VIL	0	0	0	1	1	1	1	1	1F
Device Type	VIH	0	0	0	0	1	0	0	0	08

*

*Code subject to change.

FORM 1E102 (4/82)

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

VDD and input voltages w.r.t. VSS .... -0.6 to +6.25V
Vpp voltage w.r.t. Vss during programming .... -0.6 to +14V
Voltage on pin 24 w.r.t. Vss .... -0.6 to +13.5V
Storage temperature .... -65 deg. C to +150 deg. C
Ambient temperature with power applied .... -65 deg. C to +125 deg. C

DC CHARACTERISTICS (Read Mode)

VDD = +5V ± 10%,
TAMB = -55 to +125 deg. C
Vpp = +12.5 ± 0.5V

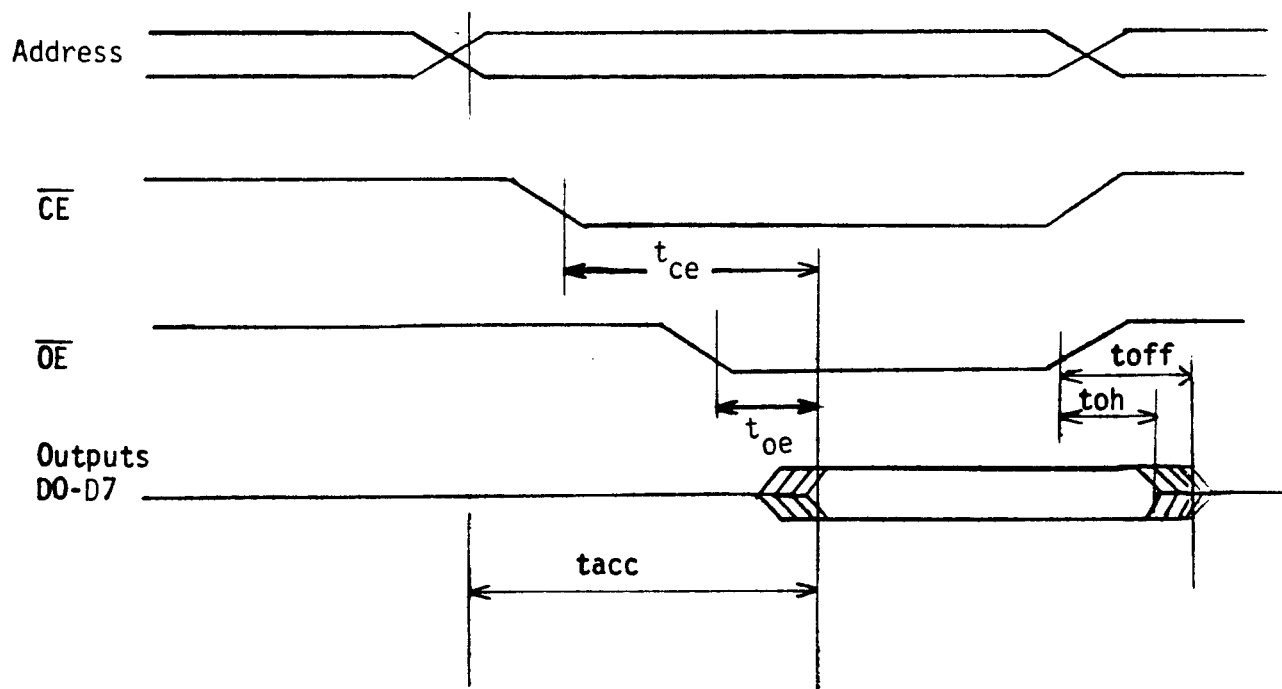| PARAMETER	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Address lines A0-A12					
Data lines(program mode) D0-D7					
PGM, CE & OE					
Logic "1"	VIH	2.0	VDD+1	V	
Logic "0"	VIL	-0.1	0.8	V	
Leakage	IIL	-10	10	uA	VIN = 0 to VDD
Input Capacitance	CIN	0	6	pF	VIN = 0V TAMB=25 deg C f = 1MHz
Programming Voltage	Vpp	12.0	13.0	V	
Outputs					
In read/verify mode D0-D7					
Logic "1"	VOH	2.4	–	V	IOH = -4 mA
Logic "0"	VOL		0.4	V	IOL = 8 mA
Leakage	IOL	-10	10	uA	VIN = 0 to VDD
Power Supply Current					
Active					
VDD	IDD		80	mA	CMOS Levels f=20MHz VDD = 5.5V OE = CE = Vcc + 1 to Vcc -0.3
VPP (When Programming)	IPP		30	mA	Vpp = 12.5 nom
(Read Mode)			100	uA	Vpp = 5.5V
Standby					
Total VDD & Vpp	IDD(S)		200	uA	CE=VIH OE=VIL Vpp=VDD=5.5V
Output Capacitance	COUT		12	pf	VOUT = 0V TAMB = 25 deg C f = 1MHz

AC CHARACTERISTICS

TA: Commercial (C) = 0°C to 70°C
Industrial (I) = -40°C to +85°C
Military (M) = -55°C to +125°C

Output Load = 1 TTL load + 100pF
Note: 27HC64-05 only available at 0° to 70° rating.

Symbol	Parameter	27HC64-05		27HC64-07		27HC64-10		27HC64-15		Units	Test Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
tACC	Address to Output Delay		50		70		100		150	ns	$\overline{CE} = \overline{OE} = VIL$
tCE	$\overline{CE}$ to Output Delay		50		70		100		150	ns	$\overline{OE} = VIL$
tOE	$\overline{OE}$ to Output Delay		25		30		40		70	ns	$\overline{CE} = VIL$
tOFF	$\overline{OE}$ to /OP High Impedance		25		30		40		50	ns	$\overline{CE} = VIL$
tOH	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = VIL$

READ WAVEFORMS FOR 27HC64

DC PROGRAMMING CHARACTERISTICS

TA = 0 to 70°C, Vdd = 6.0 $\pm$ 0.25V, Vpp = 12.5 $\pm$ 0.5V

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS (See Note 1)
ILI	Input Current (All Inputs)		10	uA	VIN = VIL or VIH
VIL	Input Low Level (All Inputs)	-0.1	0.8	V	
VIH	Input High Level	2.0	Vdd+1	V	
VOL	Ouput Low Voltage During Verify		0.45	V	IOL = 2.1 mA
VOH	Output High Voltage During Verify	2.4		V	IOH = -400 uA
Idd2	Vdd Supply Current (Program & Verify)		30	mA	
Ipp2	Vpp Supply Current (Program)		30	mA	$\overline{CE}$ = VIL
VID	A9 Product Identification Voltage	11.5	12.5	V	

Notes: (1) Vdd must be applied simultaneously or before
Vpp and removed simultaneously or after Vpp.

AC CHARACTERISTICS — 27HC64

Conditions: 0 to +70°C, Vdd = 6.0 ± 0.25V, Vpp = 12.5 ± 0.5V

Program, Program Verify, and Program Inhibit Modes

| PARAMETER	SYM	MIN	TYP	MAX	UNITS
Address Set-Up Time	tAS	2			us
Data Set-Up Time	tDS	2			us
Data Hold Time	tDH	2			us
Address Hold Time	tAH	0			us
Float Delay	tDF	0		130	ns
Vdd Set-Up Time	tVCS	2			us
Program Pulse Width	tPW	0.95	1	1.05	ms
CE Set-Up Time	tCES	2			us
OE Set-Up Time	tOES	2			us
Vpp Set-Up Time	tVPS	2			us
Overprogram Pulse Width	tOPW	2.95		78.75	ms
Data Valid from OE	tOE			150	ns

PROGRAM MODE
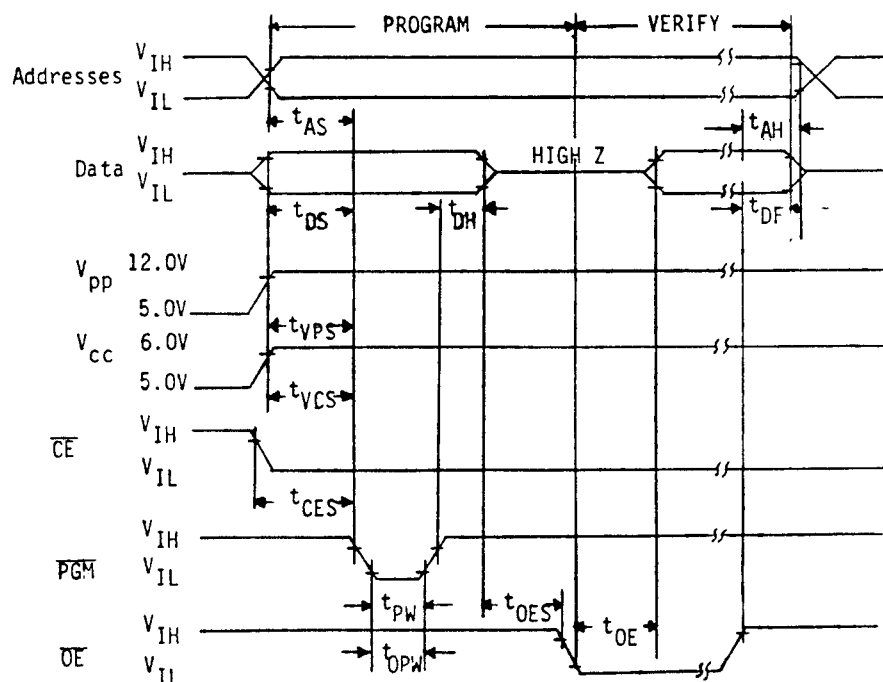
AC CHARACTERISTICS - 27HC641

TA: Commercial (C) = 0°C to 70°C
Industrial (I) = -40°C to +85°C
Military   (M) = -55°C to +125°C

Note: 27HC641-05 is only available in commercial temperature range.

Symbol	Parameter	27HC641-05		27HC641-07		27HC641-10		27HC641-15		Test Condition
		Min	Max	Min	Max	Min	Max	Min	Max	
tACC	Address to Output Delay		50		70		100		150	$\overline{CE}$ = $\overline{OE}$ = VIL
tACE	$\overline{CE}$ to Output Delay		45		60		80		130	$\overline{OE}$ = VIL
tOF	$\overline{OE}$ to Output High Impedance									$\overline{CE}$ = VIL
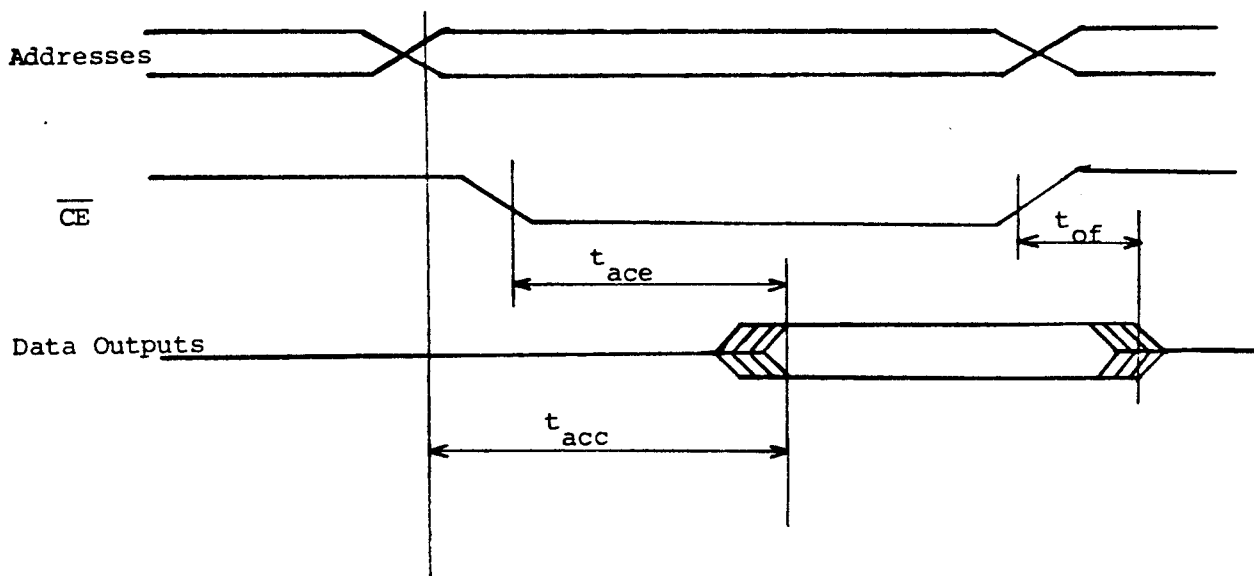
READ WAVEFORMS FOR 27HC641

Program Mode
Conditions: 0 to 70°C, Vdd = 6.0 ± 0.25V, Vpp = 12.5 ± 0.5V

SYMBOL	PARAMETER	MIN	MAX	UNITS
tAS	Address Set-Up Time	2		us
tDS	Data Set-Up Time	2		us
tCES	$\overline{CE}$ Set-Up Time	2		us
tAH	Address Hold Time	0		us
tDH	Data Hold Time	2		ns
tDFP	O/P Float Delay	0	130	ns
tVCS	Vcc Set-Up Time	2		us
tPW	Program Pulse Width	0.95	1.05	ms
tOPW	Over Program Pulse Width	2.85	78.75	ms
tOC	O/P Valid from $\overline{CE}$		150	ns

PROGRAMMING WAVEFORMS FOR 27HC641

START

ADDR=FIRST LOCATION

vdd = 6.0V
vpp =12.5V

X = O

PRG.ONE 1 MSEC PULSE

INCREMENT X

VERIFY BYTE — PASS

FAIL

X=25?? — NO / YES

DEVICE FAILED

PROGRAM 1 PULSE OF 3X MSEC DURATION

LAST ADDR.? — NO → INCREMENT ADDR.

YES

vdd=vpp=5.0V

COMPARE ALL BYTES TO ORIG DATA — PASS → DEVICE PASSED — FAIL → DEVICE FAILED