Quiz 6 (Fall 2022) - Solution

Course Name: Computer Organization Time: 15 mins

Instructor: Dr. Ayaz ul Hassan Khan

Name:	Identification #:			
Date:	Total Marks:	10	Marks Obtained:	
Signature of Instructor: $_$				

In this quiz, you are required to build a simple single-cycle processor that will support one MIPS instruction, add, and four 32-bit registers called \$0, \$1, \$2, \$3.

Q#1: Consider the instruction:

[2 marks]

add \$2, \$1, \$3

What registers will be written and what registers will be read to execute this instruction?

Registers to be written	\$2
Registers to be read	\$1, \$3

Q#2: Since we only support the add instruction, we don't care much for opcodes and funct codes and shamts. Therefore, suppose our programs are given to the processor as three inputs RD, RS, and RT. Each instruction executes within 1 clock period. **[4 marks]**

Translate the following program to the RW, RS, RT inputs (in binary).

clock period	Program	RD	RS	RT		
1	add \$2, \$1, \$3	10	01	11		
2	add \$0, \$0, \$1	00	00	01		
3	add \$1, \$2, \$2	01	10	10		
4	add \$1, \$1, \$1	01	01	01		

Q#3: Design the single-cycle processor datapath (only ID, EX and WB stages) using the following datapath components. Clearly show the number of bits to be transferred in each data line and data bus connections among different components. **[4 marks]**

