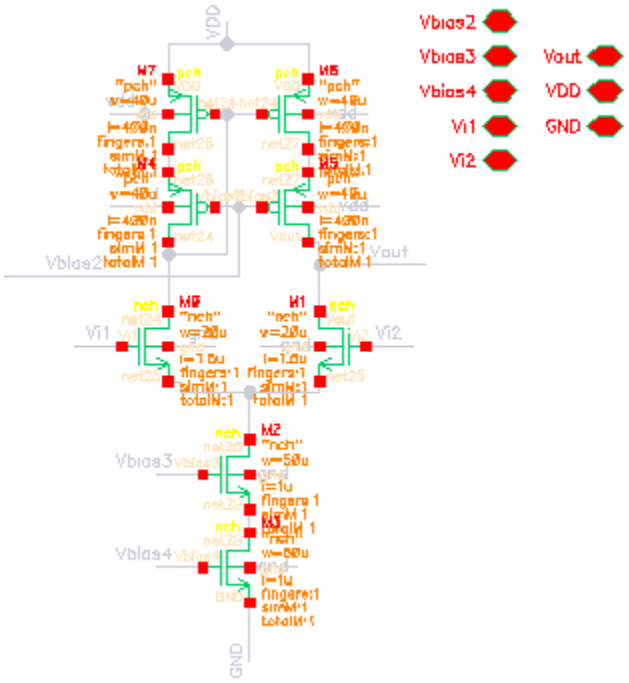
ELEG 587V Homework #2 (50 pts)

For all problems, you are to choose all the transistor properties that are required to meet the desired specification for the circuit as well as draw the circuit. Please box or underline all answers. Design both circuits within the MUSE 65nm technology within Cadence Virtuoso.

1. Design a source-coupled differential amplifier that has a gain of 40 dB.

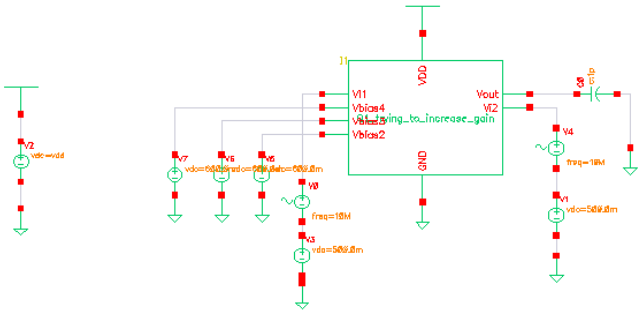
Schematic:



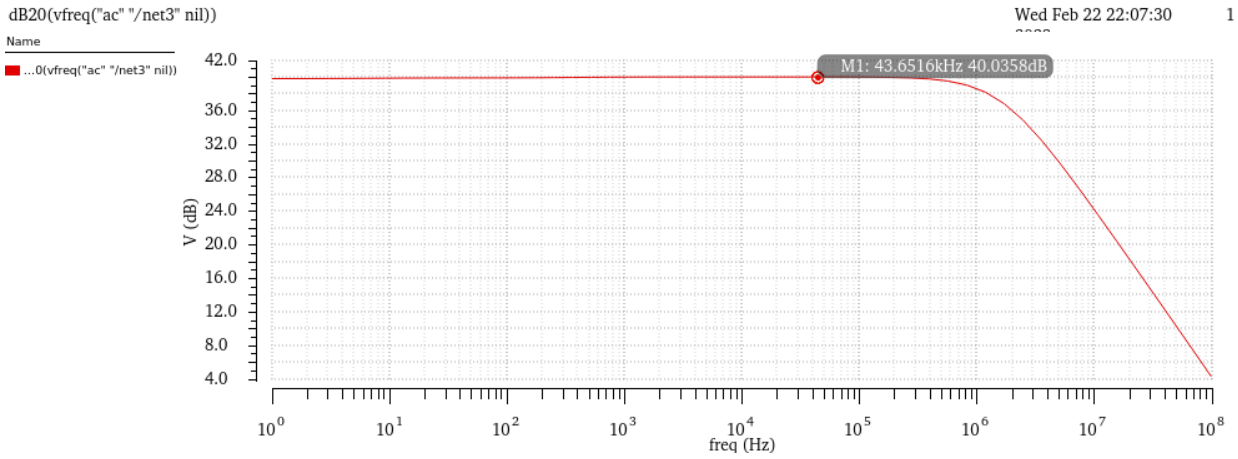
PMOS RATIO W/L	NMOS RATIO W/L
M4 40u/400n	M0 20u/1.5u
M5 40u/400n	M1 20u/1.5u
M6 40u/400n	M2 50u/1u
M7 40u/400n	M3 50u/1u

Testbench:

Vdd=1.2 V

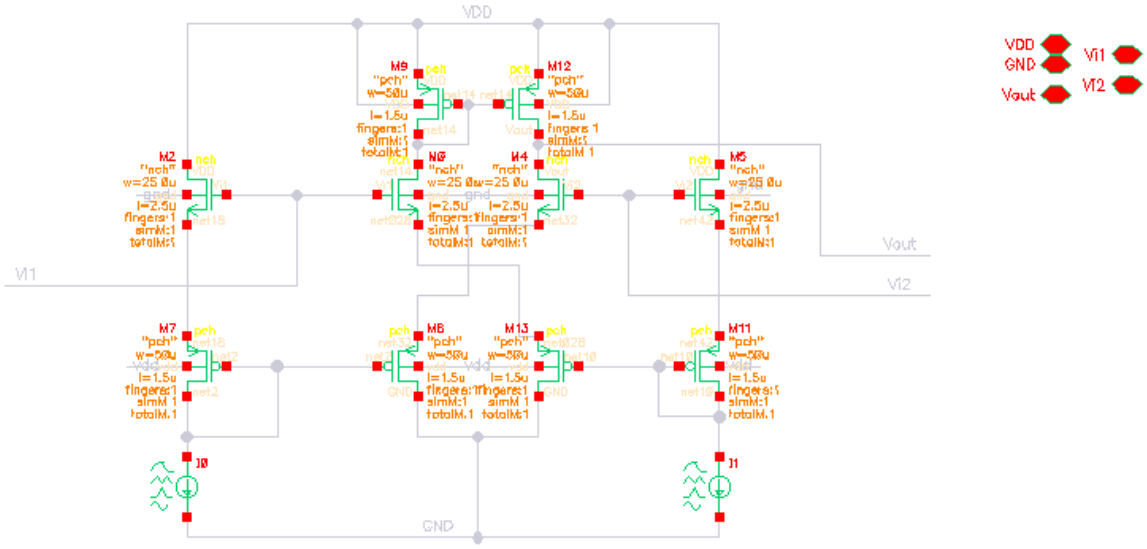


Simulation Results:



2. Design a source cross-coupled differential amplifier that has a gain of 40 dB.

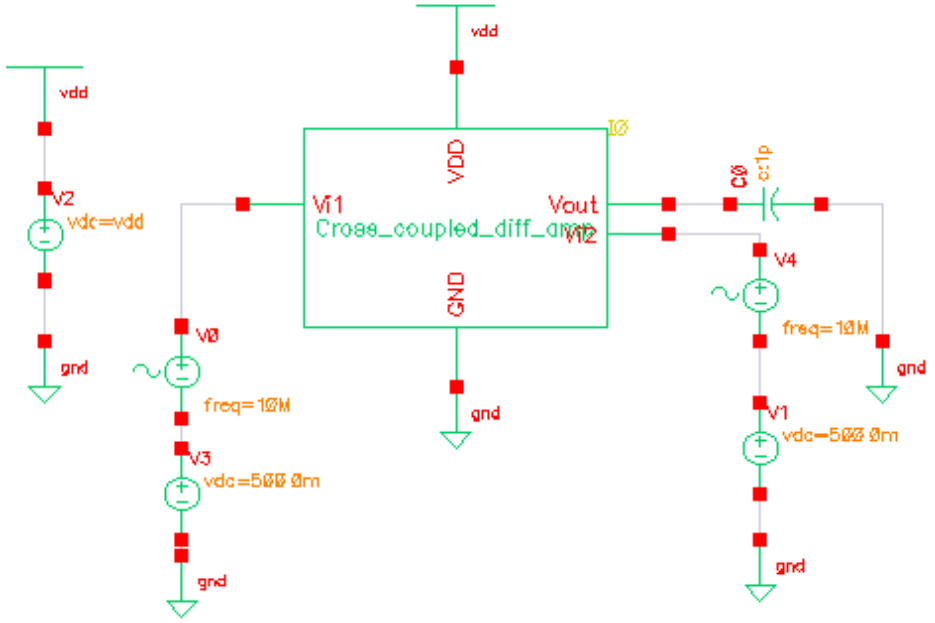
Schematic:



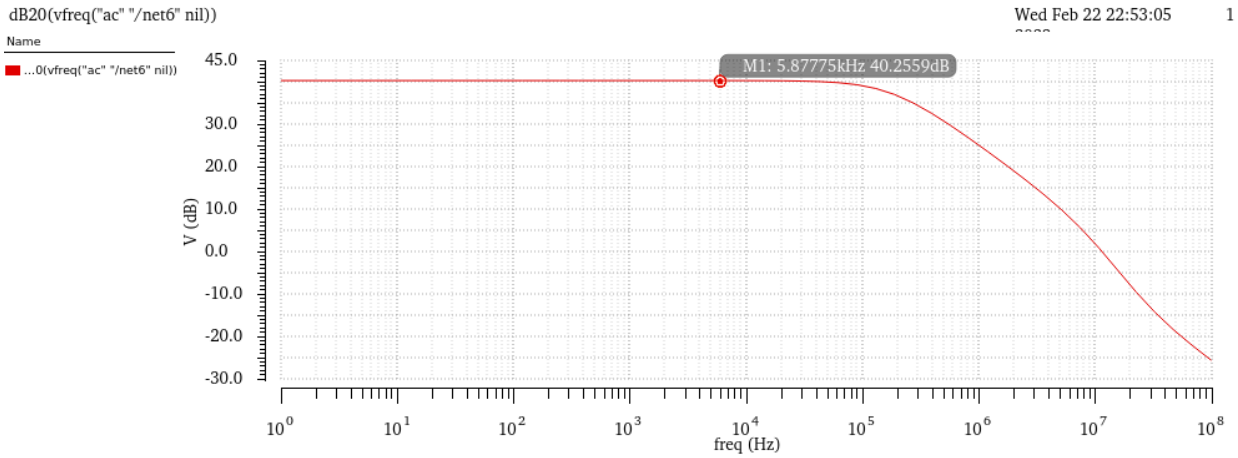
PMOS RATIO W/L	NMOS RATIO W/L
M7 50u/1.5u	M0 25u/2.5u
M8 50u/1.5u	M2 25u/2.5u
M9 50u/1.5u	M4 25u/2.5u
M11 50u/1.5u	M5 25u/2.5u
M12 50u/1.5u	
M13 50u/1.5u	

Testbench:

Vdd=1.2V

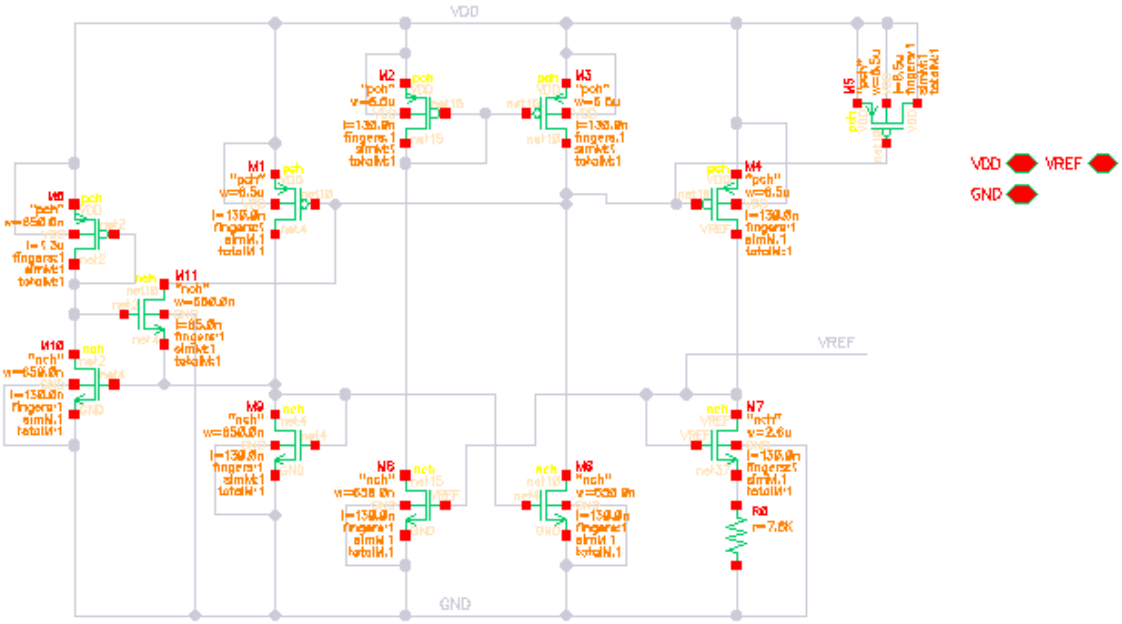


Simulation Results:



3. Design a self-biased voltage reference with the start-up circuit that provides a reference voltage of 400 mV

Schematic:



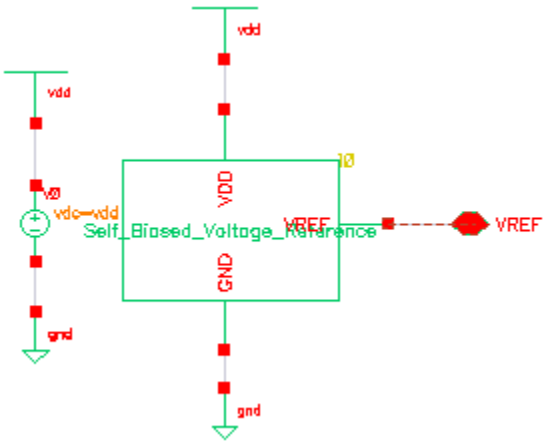
R=7.5K

PMOS W/L ratio	NMOS W/L ratio
M0 650n/130n	M6 650n/130n
M1 6.5u/130n	M7 2.6u/130n
M2 6.5u/130n	M8 650n/130n
M3 6.5u/130n	M9 650n/130n
M4 6.5u/130n	M10 650n/130n
M5 6.5u/6.5u	M11 650n/65n

Testbench:

Vdd=1.2 V

VREF=400 mv



Simulation Results: