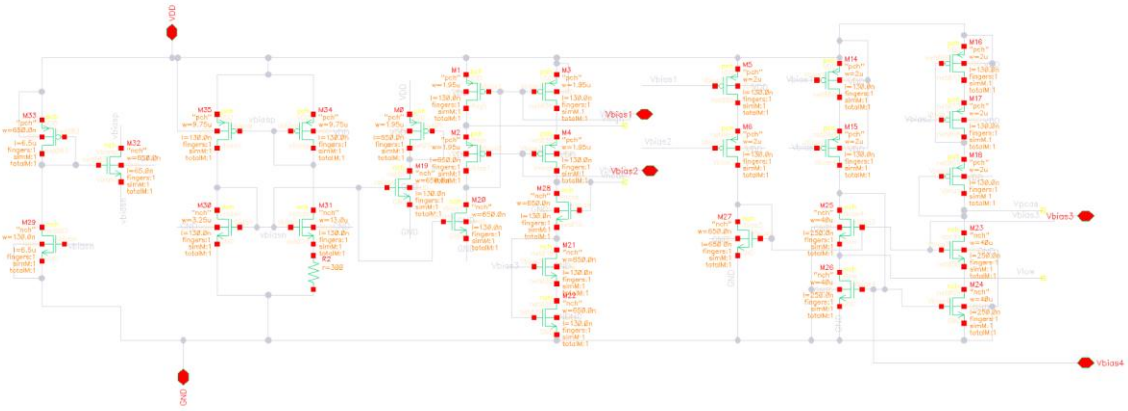
ELEG 587V Project #1 (100 pts)

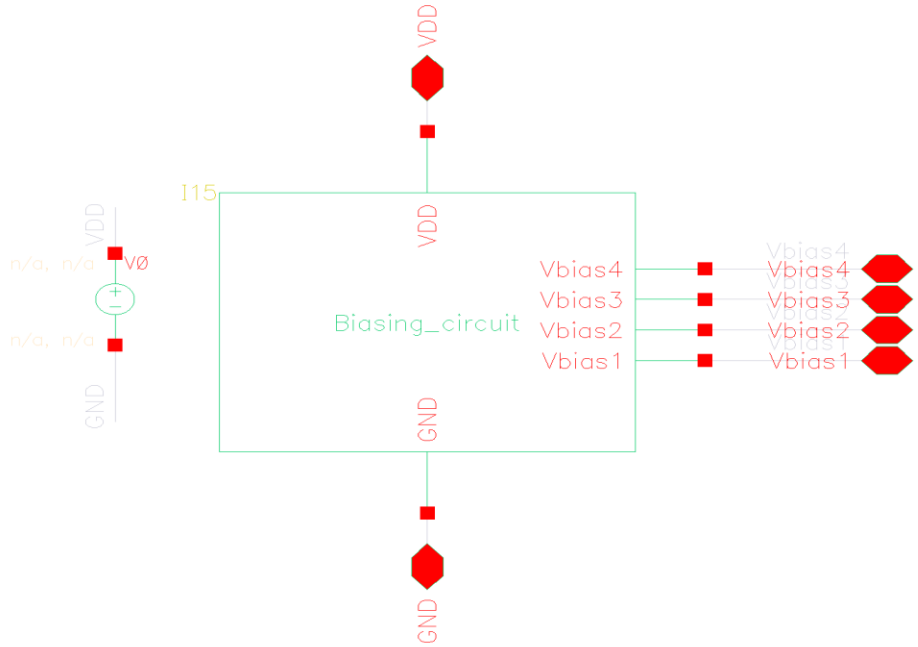
For both parts, you are to utilize Cadence Virtuoso to design the necessary circuits. You supply voltage should be no larger than 1.2 V, and the circuits should be fully contained (i.e., you only provide the input signals and the power). You will write a short report and turn in all necessary schematics, simulations, and waveforms.

1.Design a Beta-Multiplier circuit that provides a reference current of between 100 µA to 500 µA. The Beta-Multiplier should feed into a general biasing circuit that provides four unique biasing levels. Turn in the schematic and DC simulation with the output bias voltages.

**SCHEMATIC:**

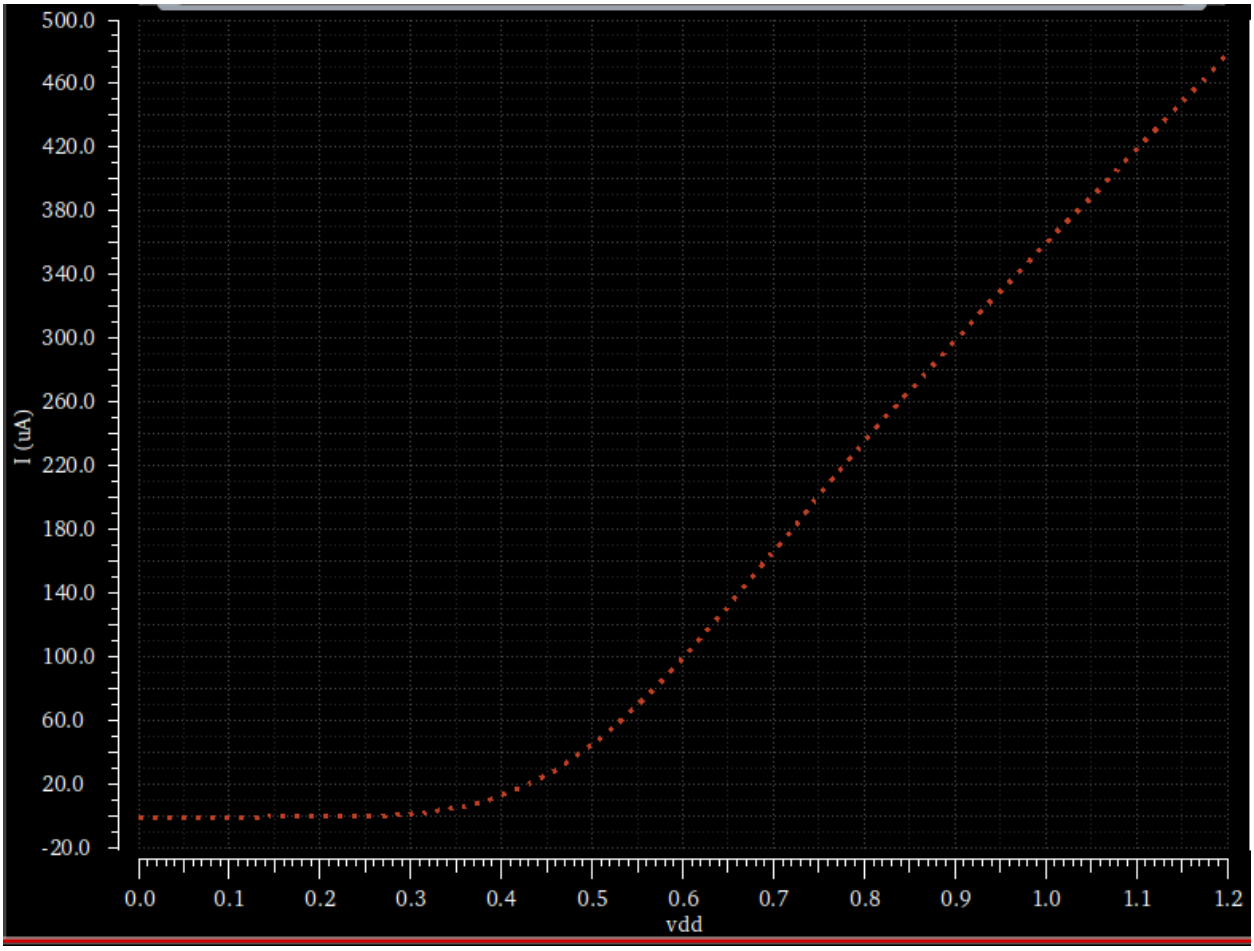


**TESTBENCH:**

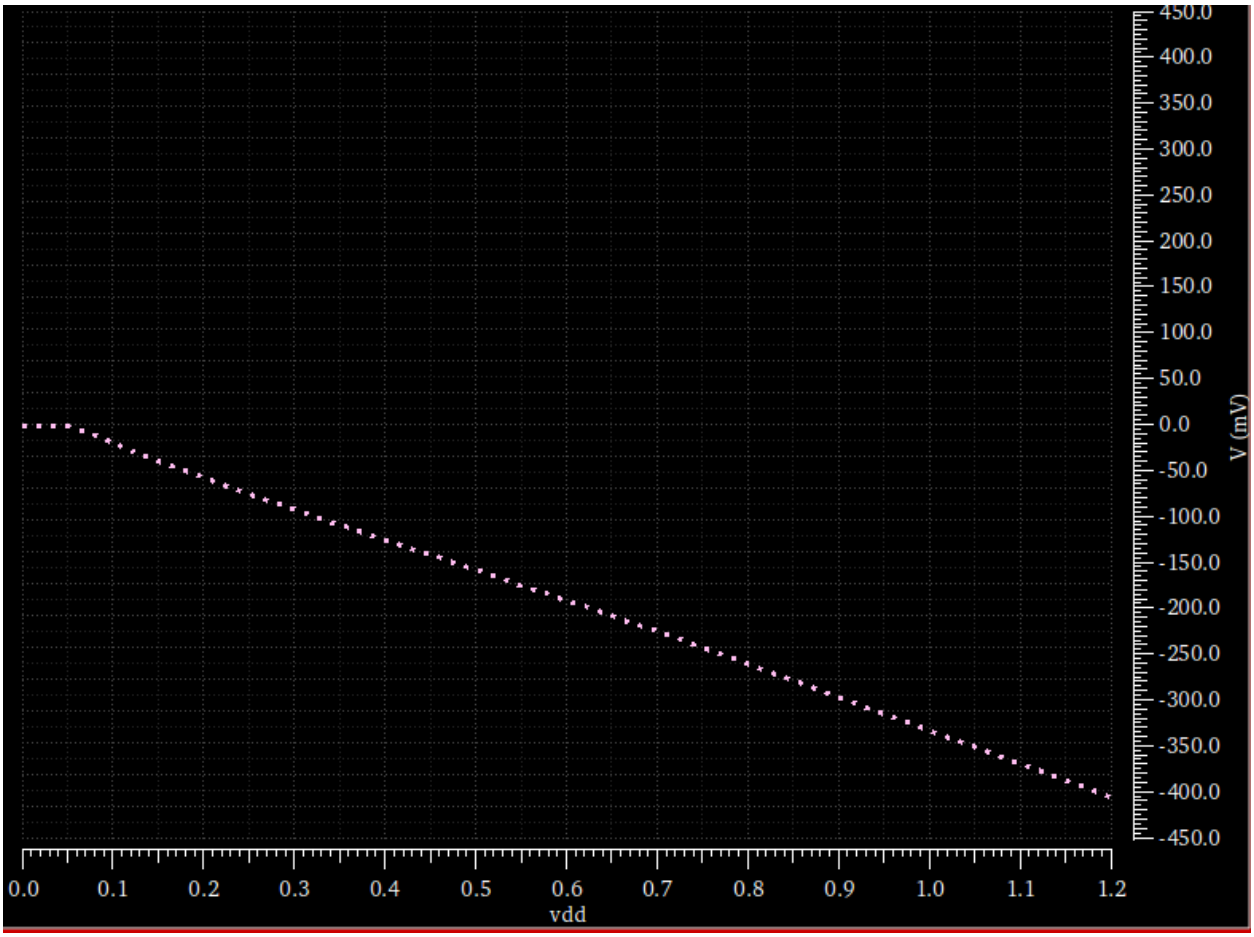


**SIMULATIONS:**

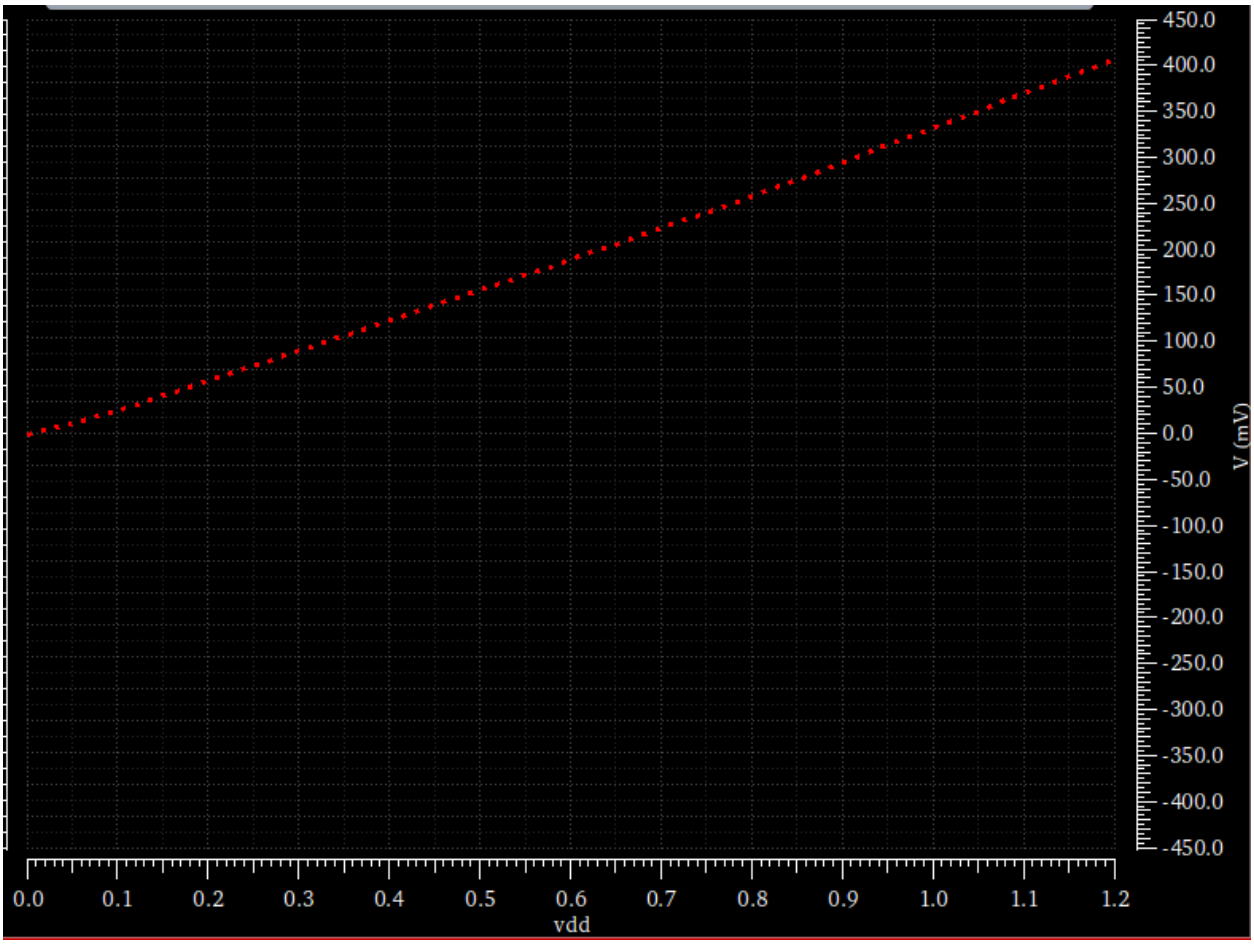
ID vs VDD Curve:



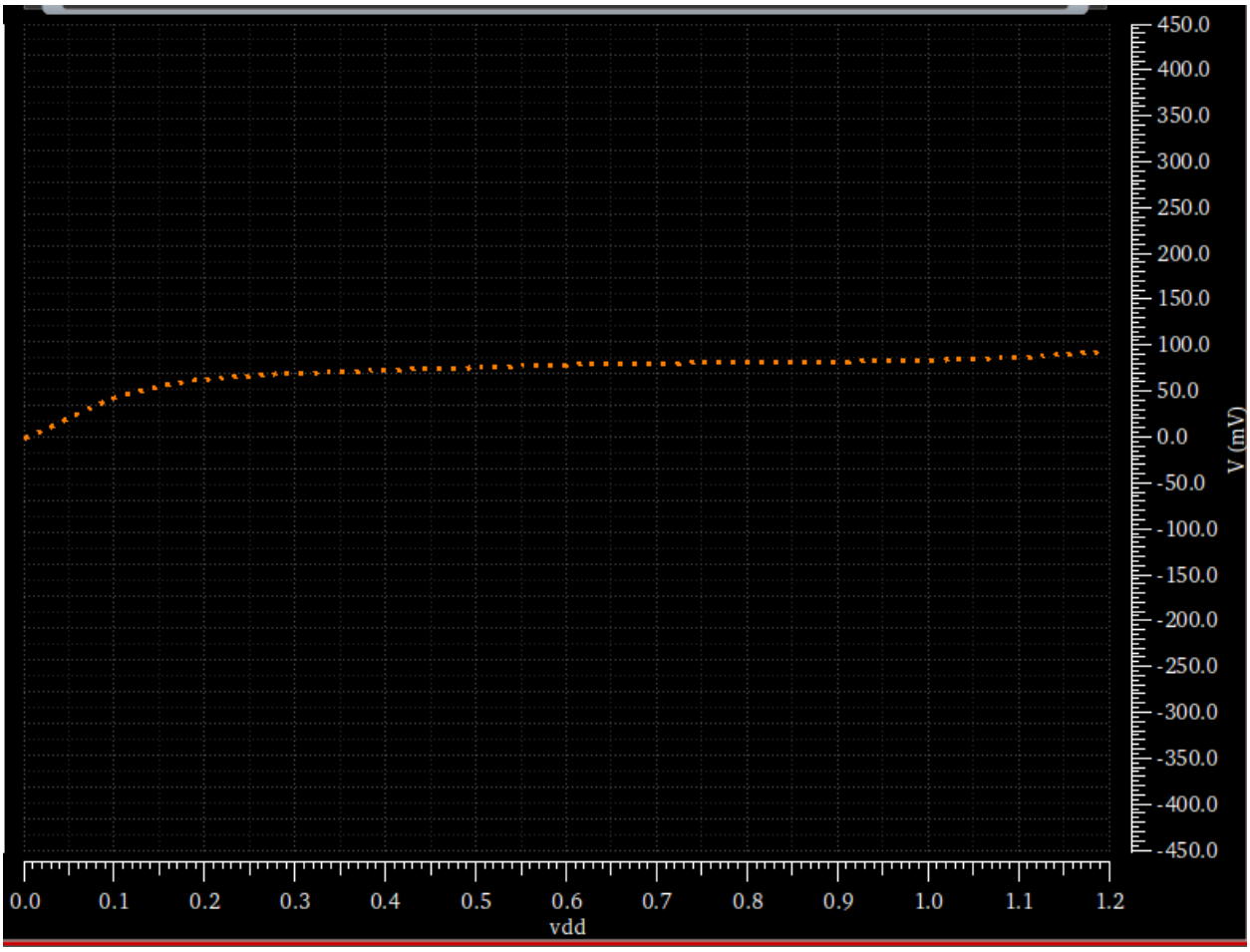

VBIAS1= 404.4mV:


450.0
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0.0
-50.0
-100.0
-150.0
-200.0
-250.0
-300.0
-350.0
-400.0
-450.0
V (mV)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
vdd

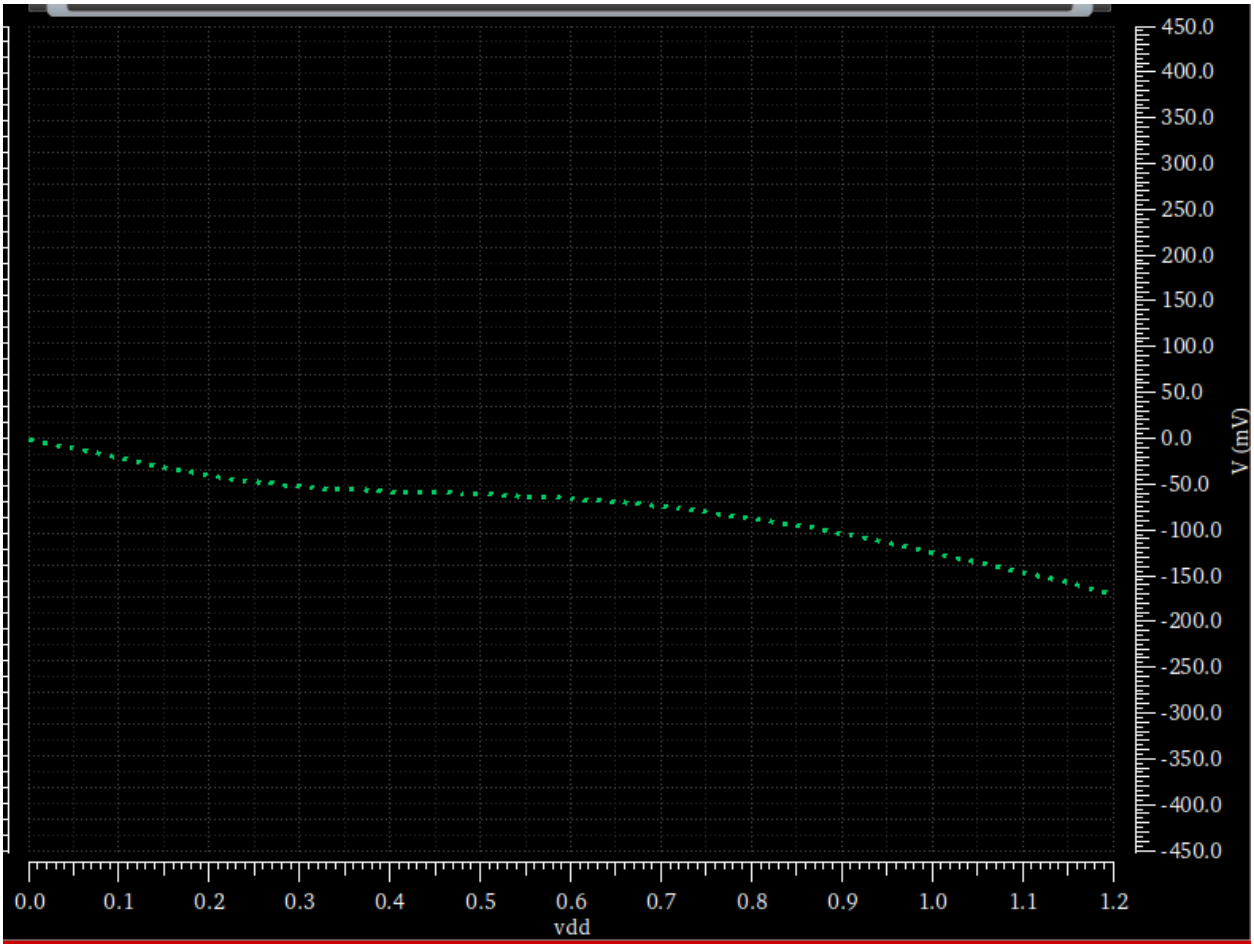
VBIAS2= 408.34 mV:



VBIAS3= 94.55 mV:



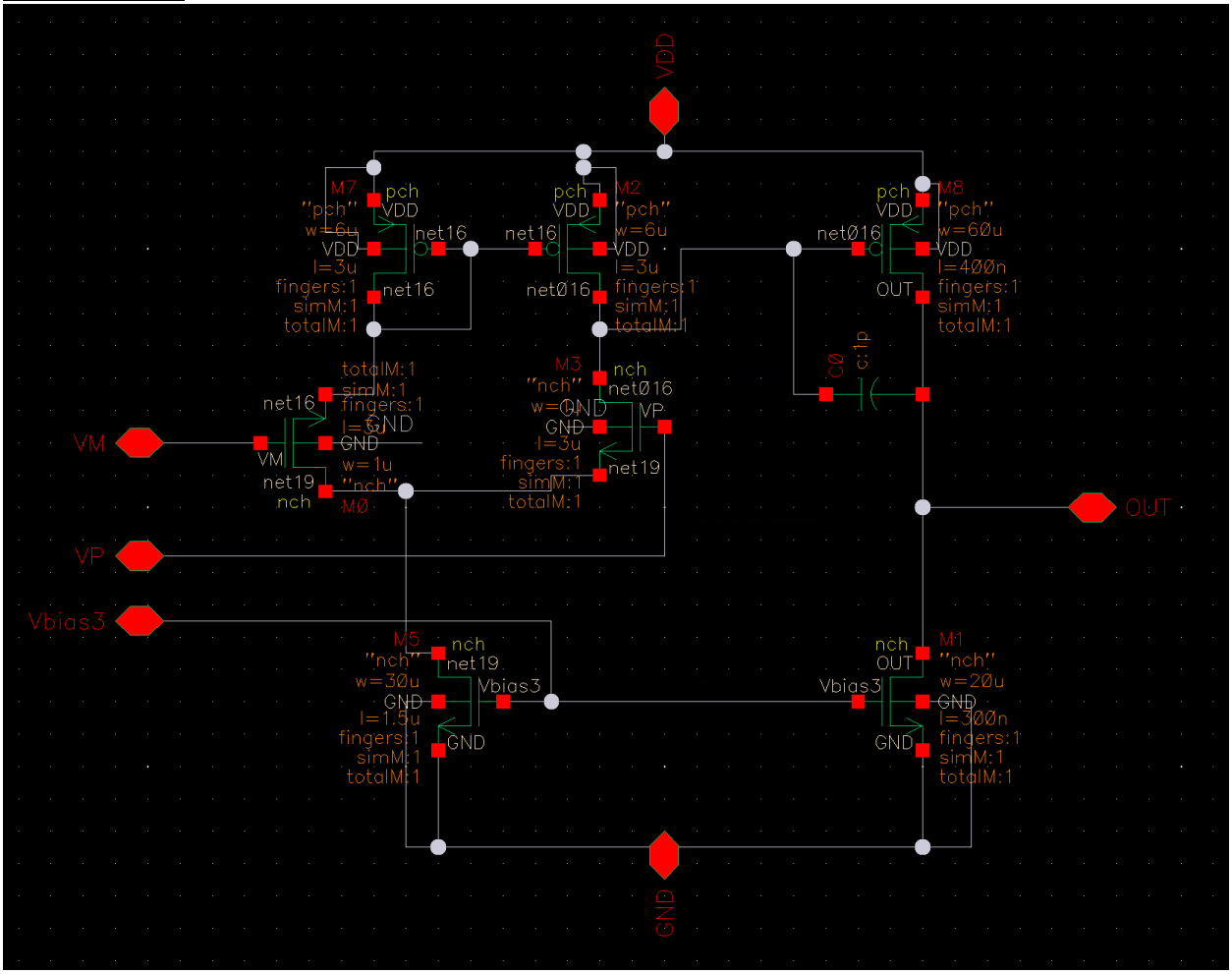

VBIAS4= 168 mV:



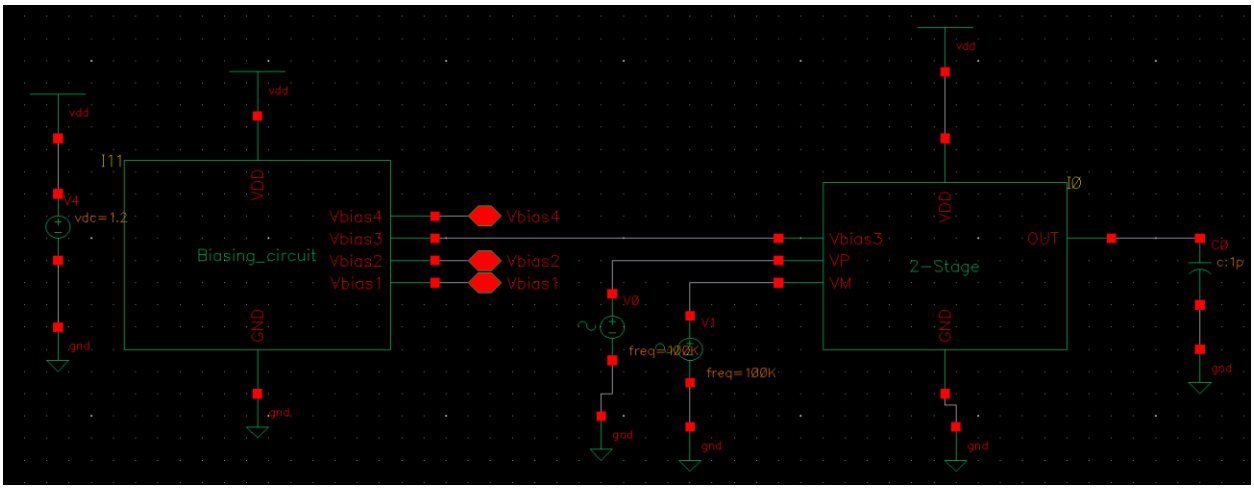

2. Design a differential amplifier (you can choose which topology) that provides a gain between 60-100 dB. Higher gains will receive more points. The differential amplifier should receive all its

biasing from Part #1's circuit. Provide simulations for a 50 mV sine input signal at 100 kHz, 1 MHz, 10 MHz, 100 MHz, 1 GHz, and 10 GHz. Find the input common-mode range in simulation and provide the Bode plot of the gain magnitude and phase of the amplifier.

**SCHEMATIC:**




**TESTBENCH:**

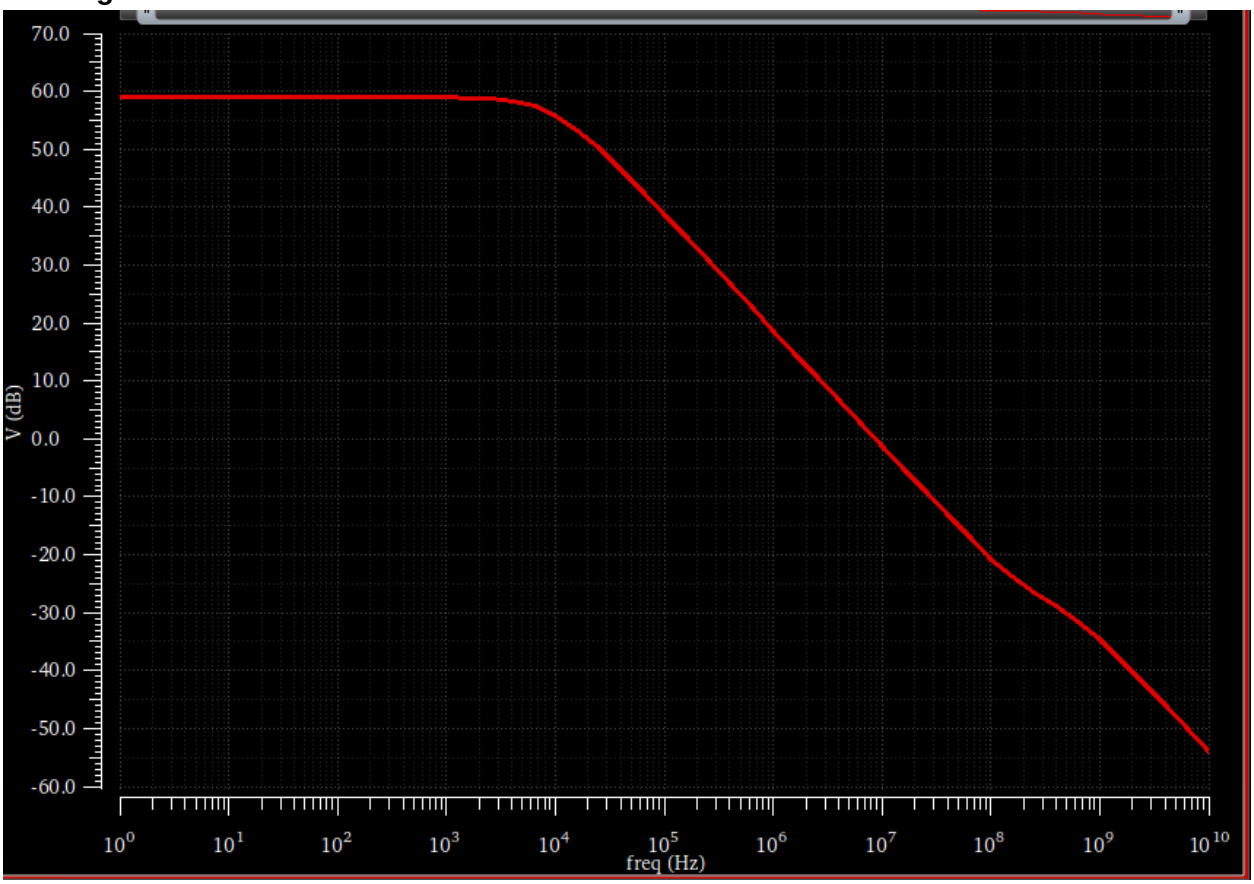



**SIMULATIONS:**

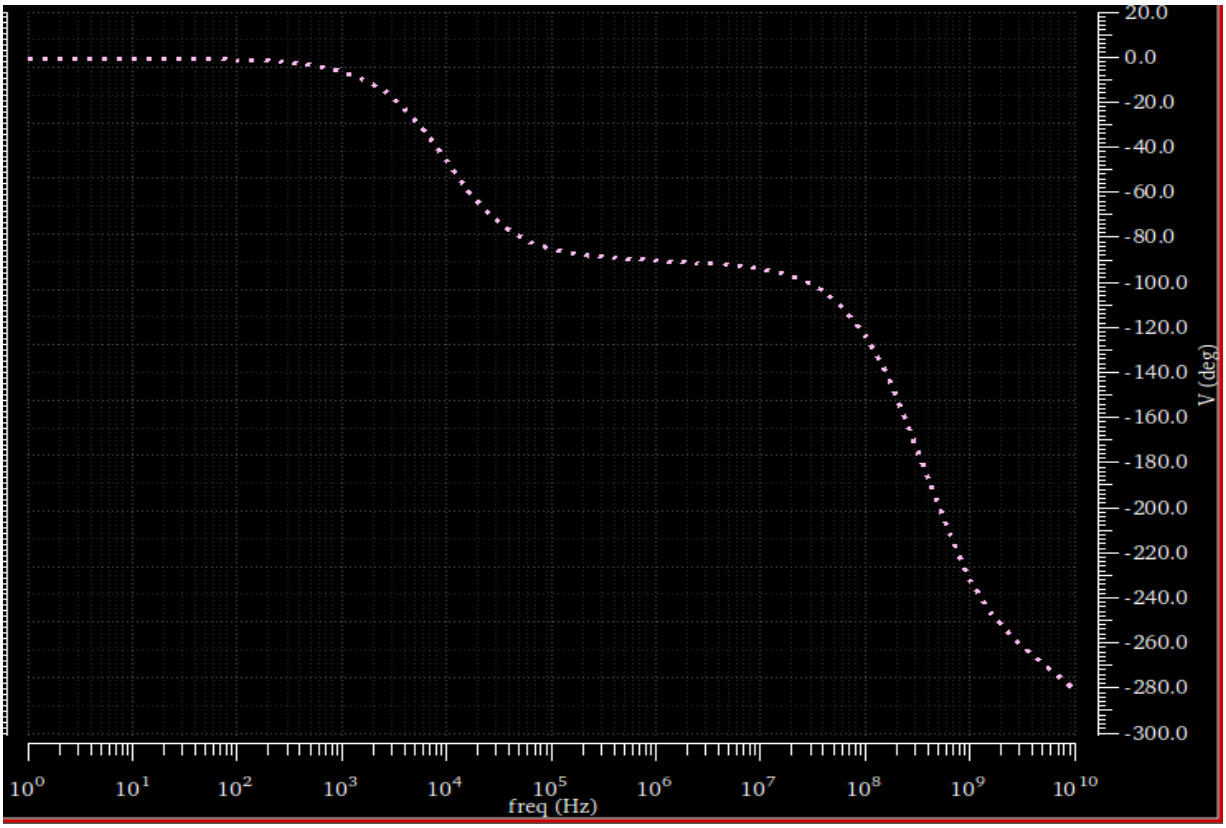
**GAIN (dB):**

**DC Voltage VP=VM=600mv**

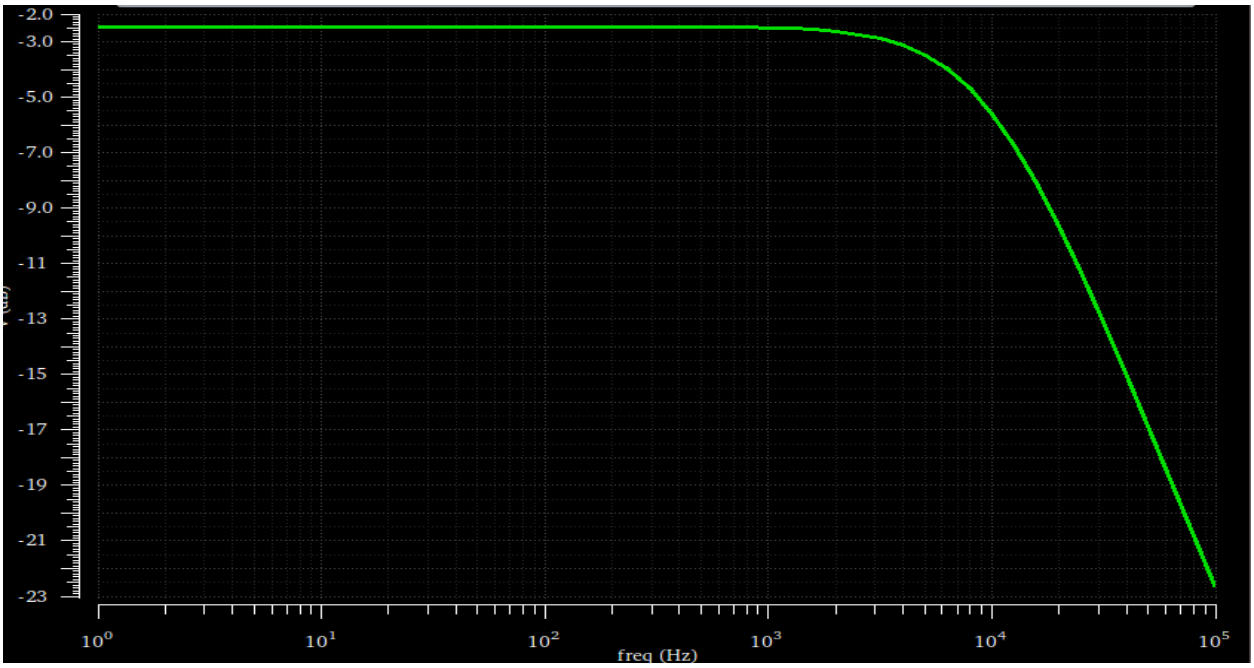
**AC magnitude= 1.5V**



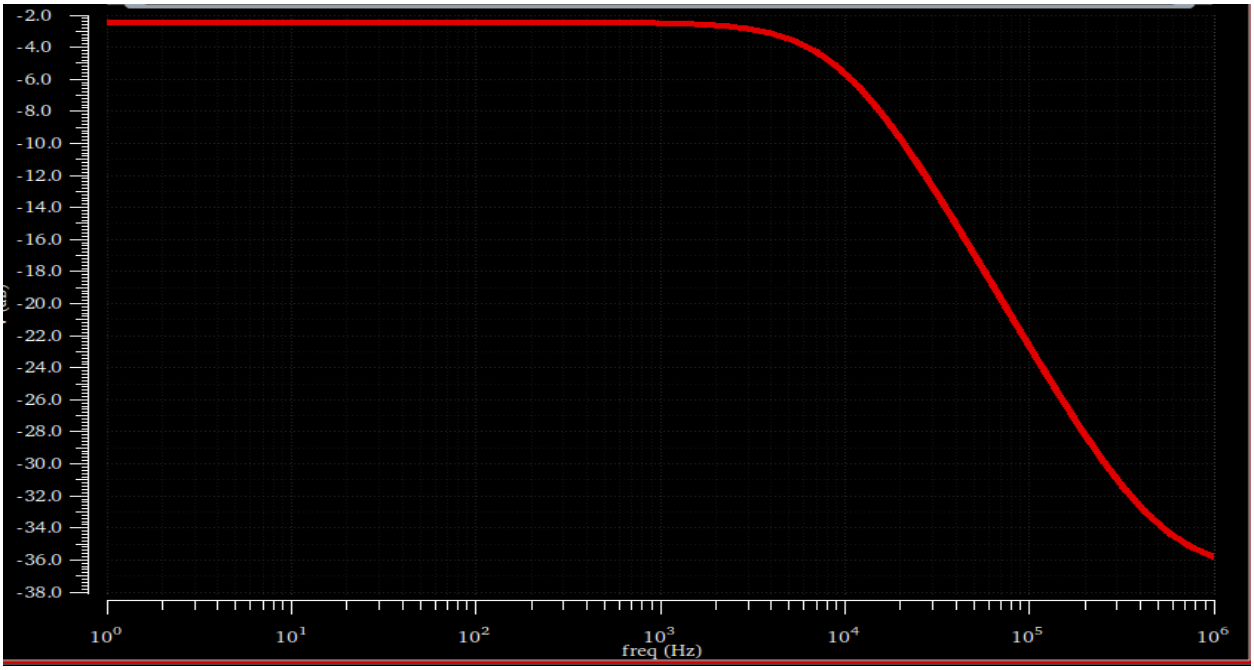

Phase Margin:



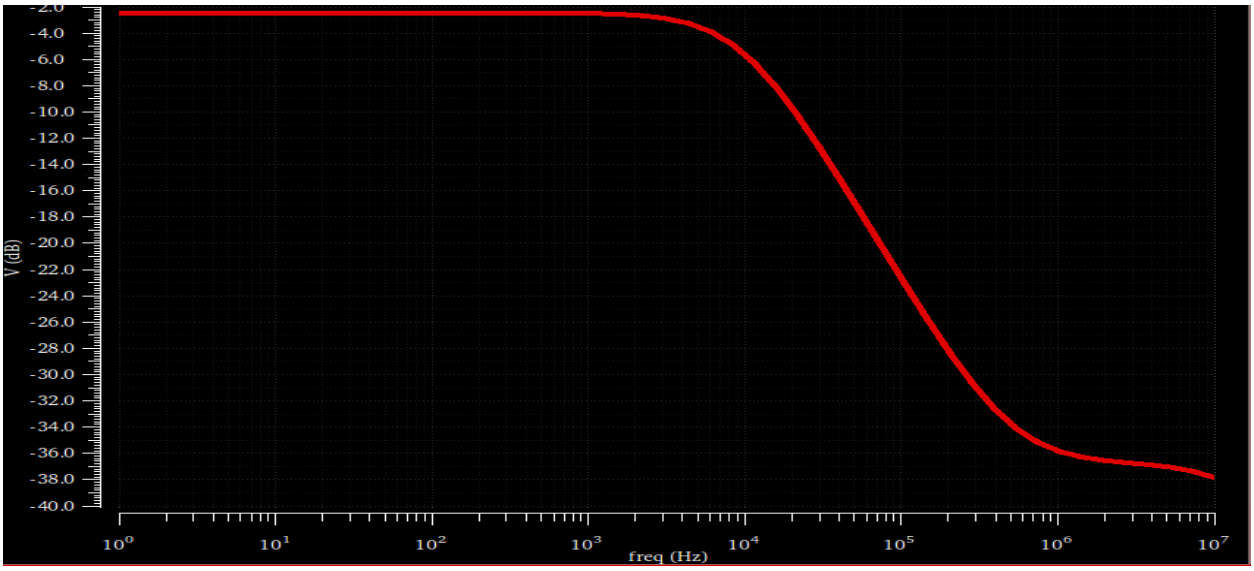

50mv at 100Khz



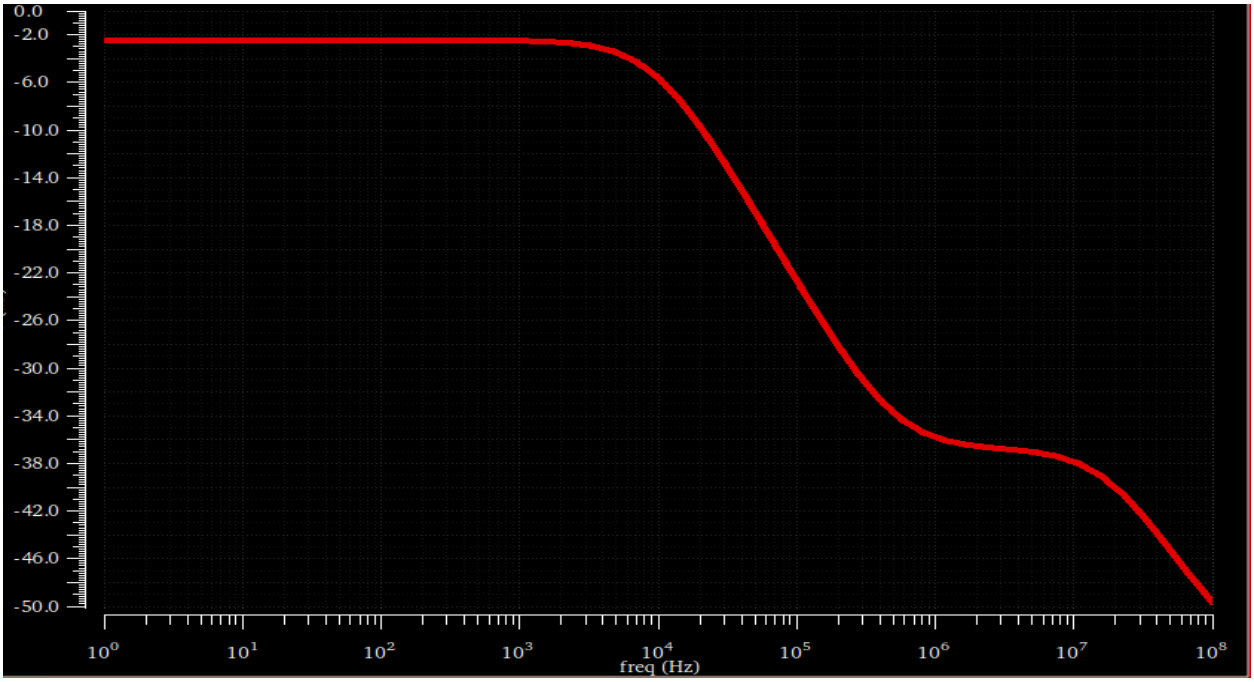

50mv at 1M



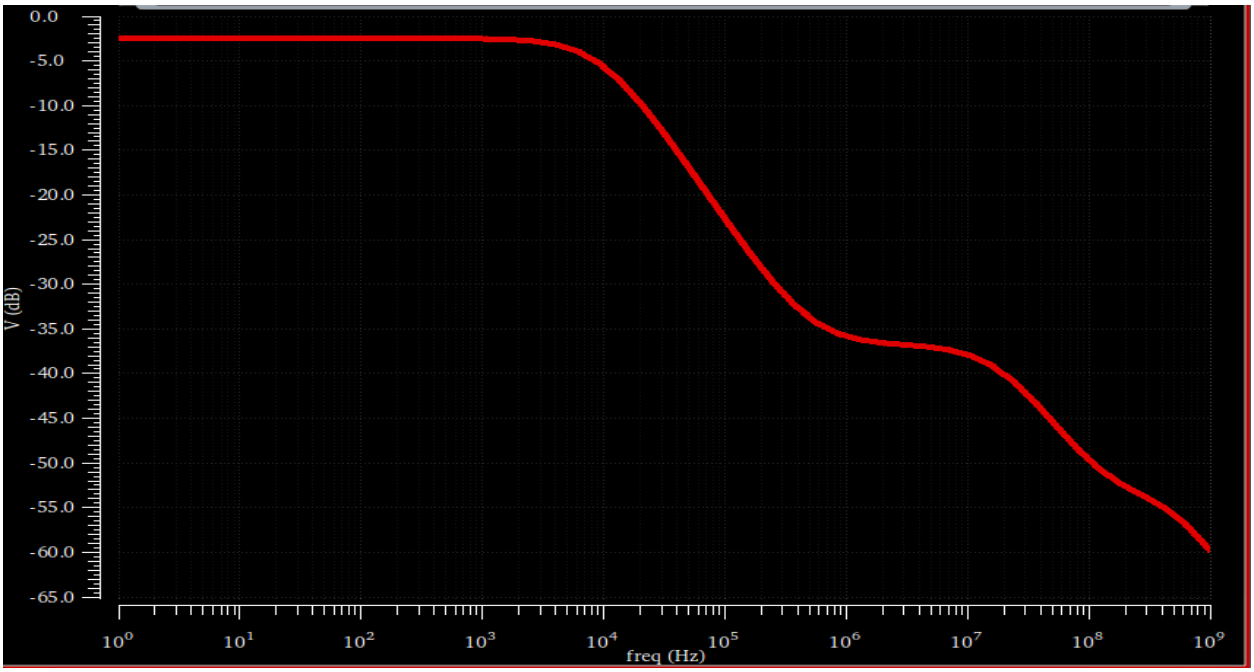

50mv at 10Mhz



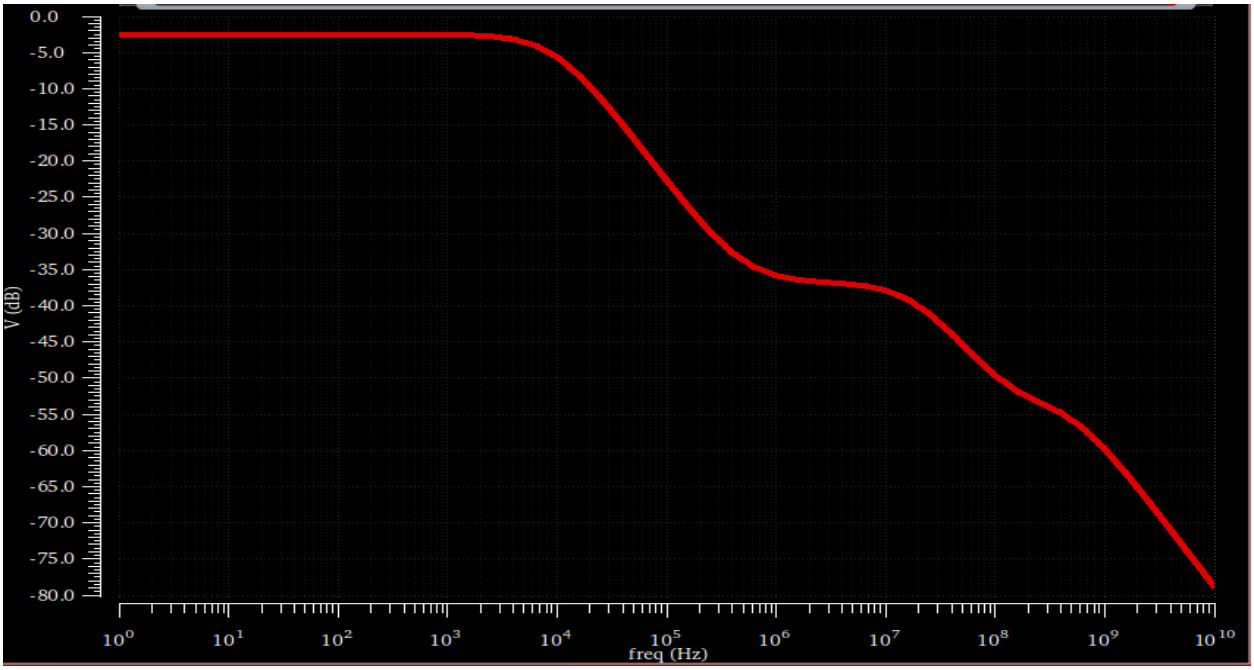

50mv at 100M




50mv at 1G

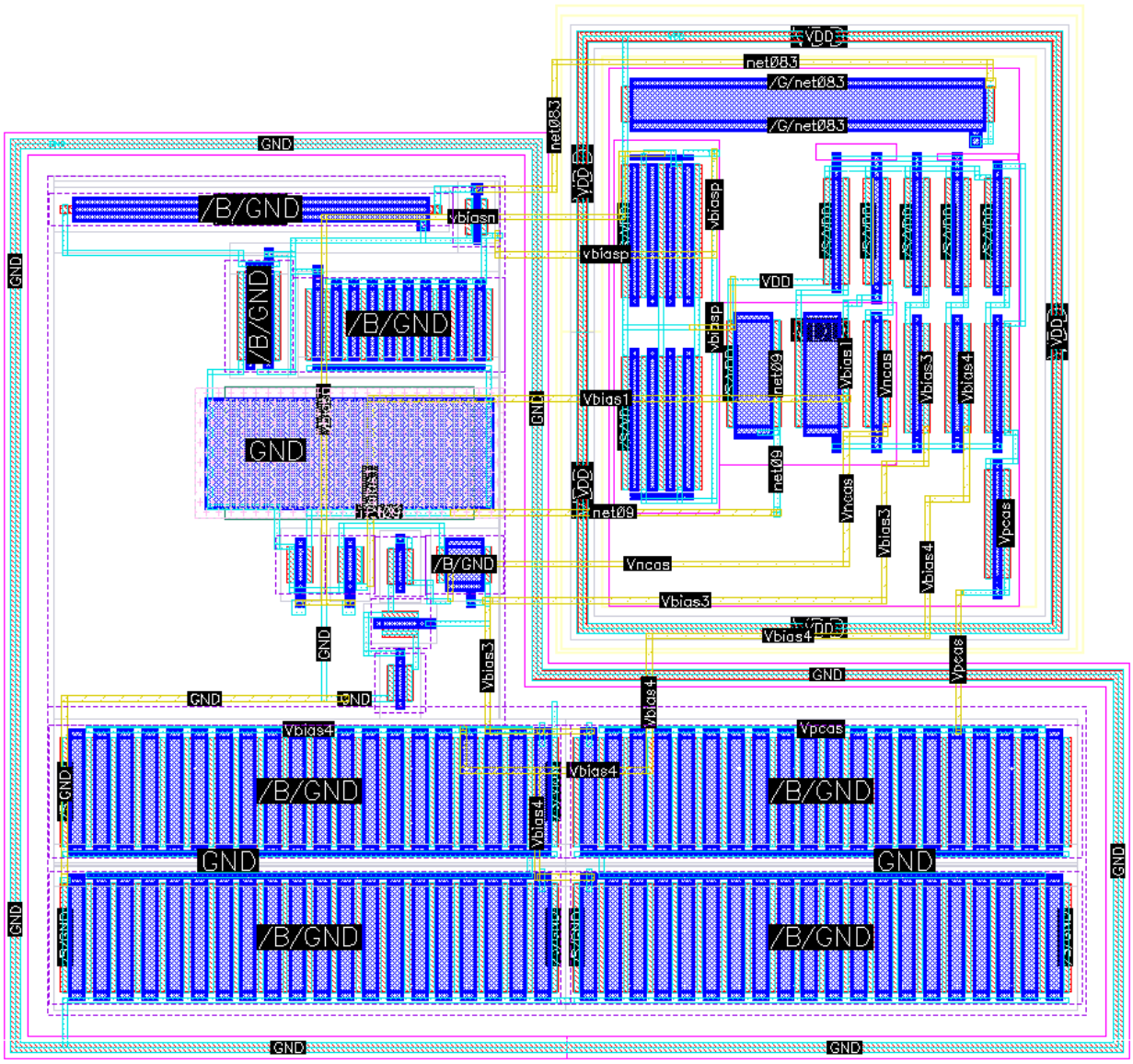



50mv at 10G

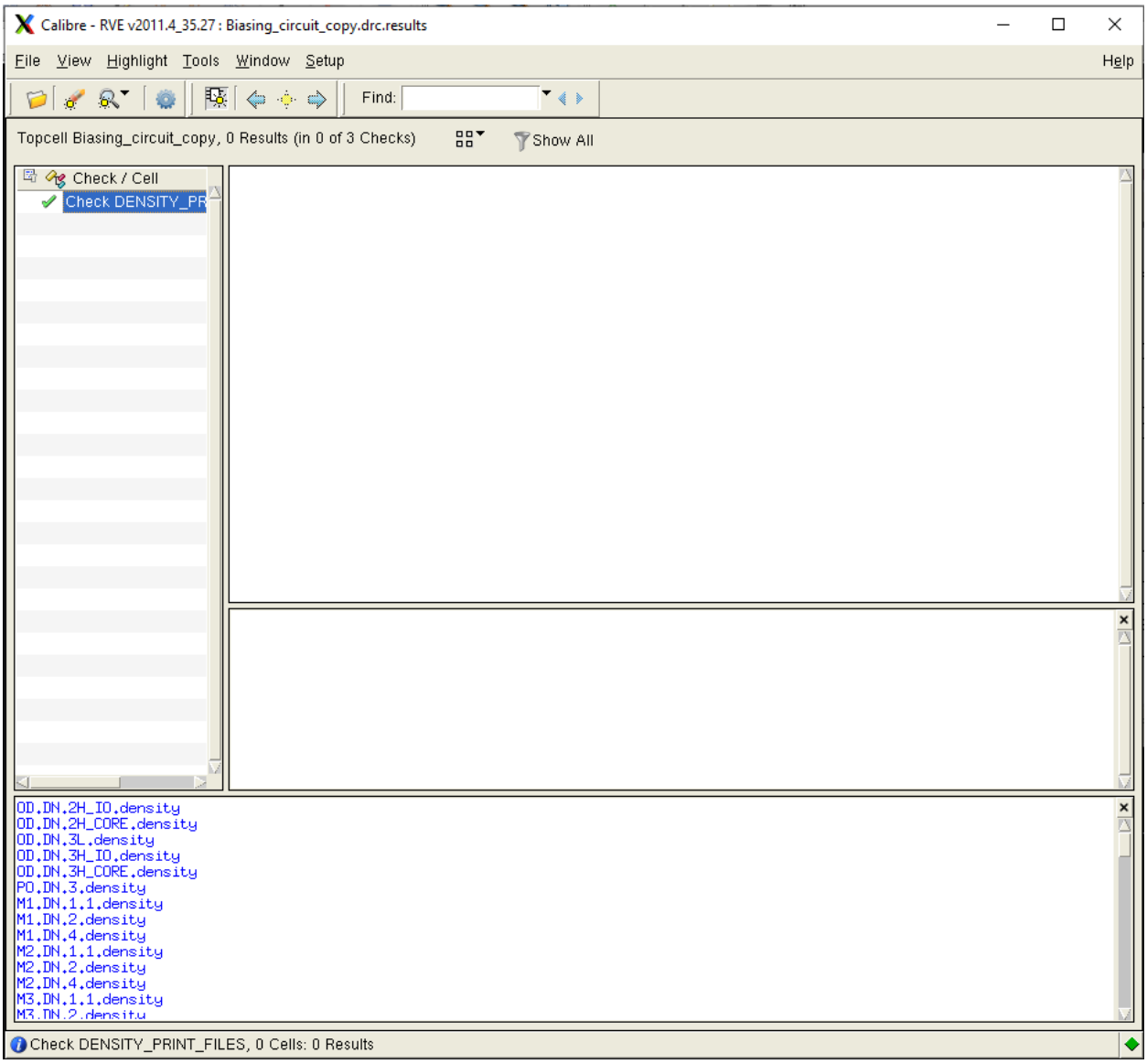



3. Provide a compact analog friendly layout that utilizes guard rings and common-centroid techniques for Parts #1 and #2.

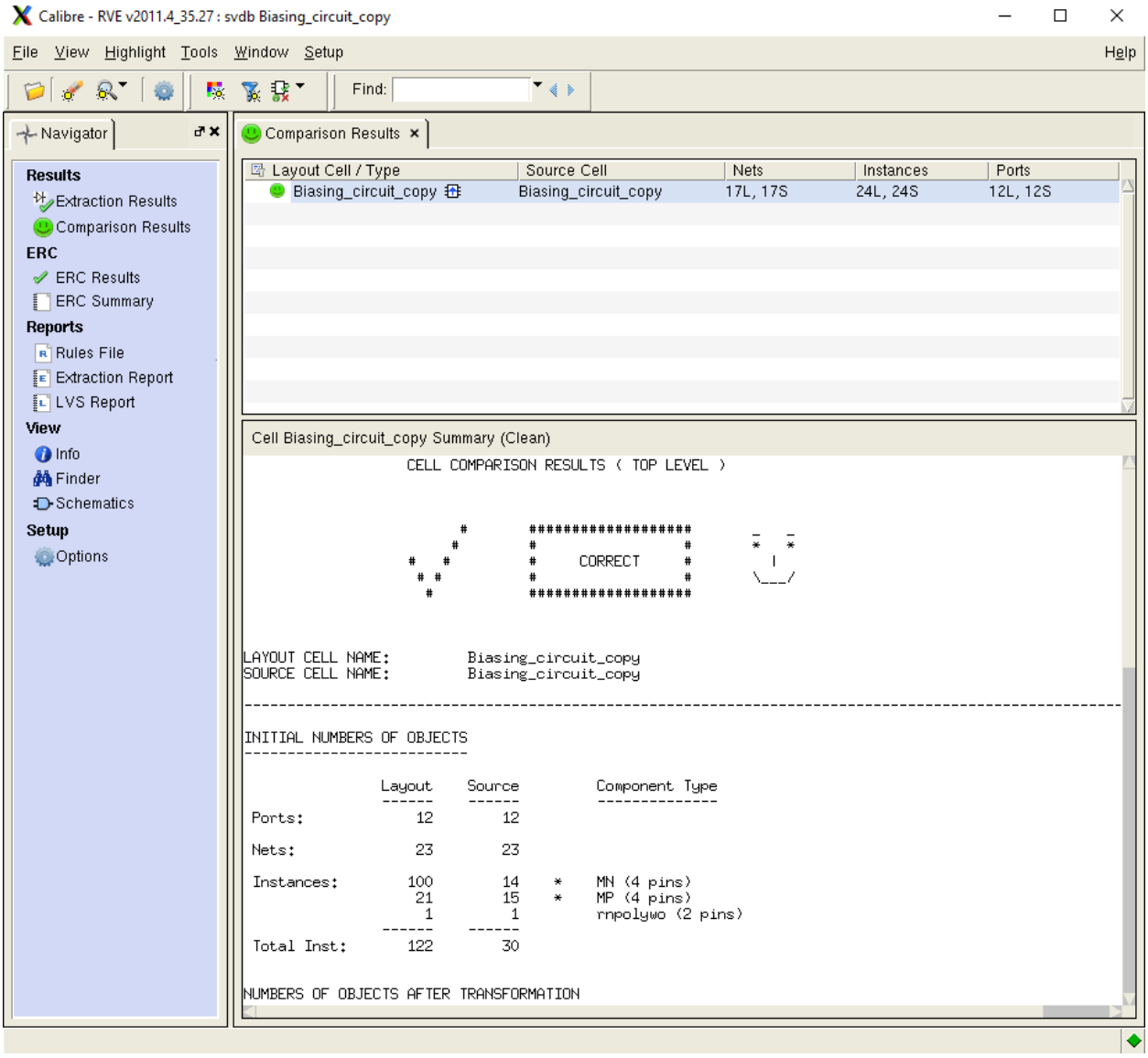
## Part #1 Layout



DRC check


Calibre - RVE v2011.4_35.27 : Biasing_circuit_copy.drc.results
File View Highlight Tools Window Setup Help
Find:
Topcell Biasing_circuit_copy, 0 Results (in 0 of 3 Checks)
Show All
Check / Cell
Check DENSITY_PR
OD.DN.2H_IO.density
OD.DN.2H_CORE.density
OD.DN.3L.density
OD.DN.3H_IO.density
OD.DN.3H_CORE.density
PO.DN.3.density
M1.DN.1.1.density
M1.DN.2.density
M1.DN.4.density
M2.DN.1.1.density
M2.DN.2.density
M2.DN.4.density
M3.DN.1.1.density
Check DENSITY_PRINT_FILES, 0 Cells: 0 Results

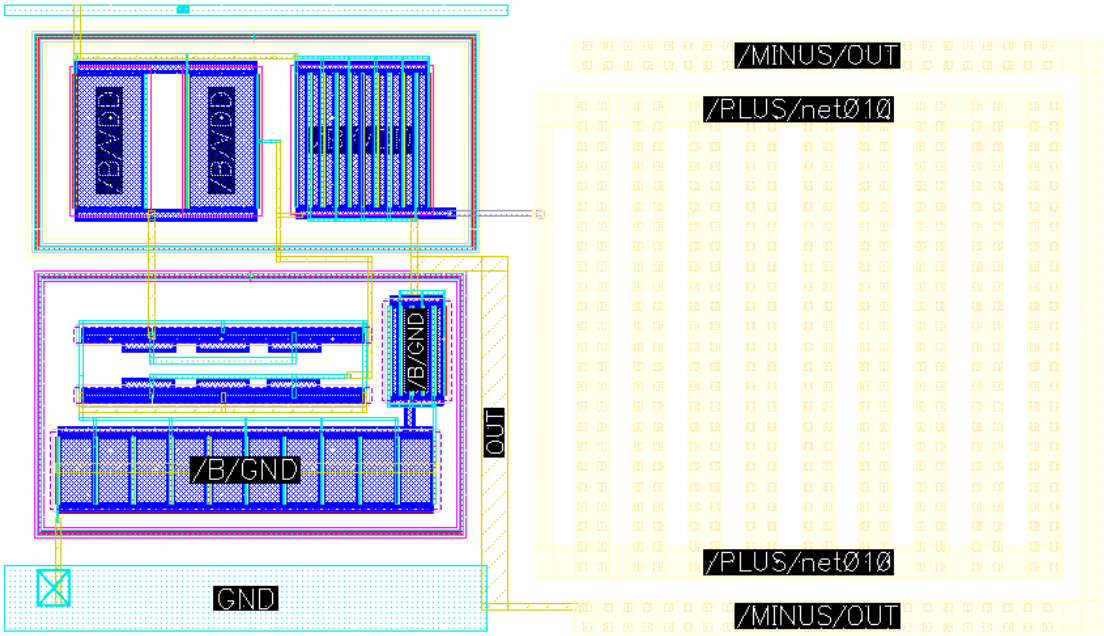
LVS check



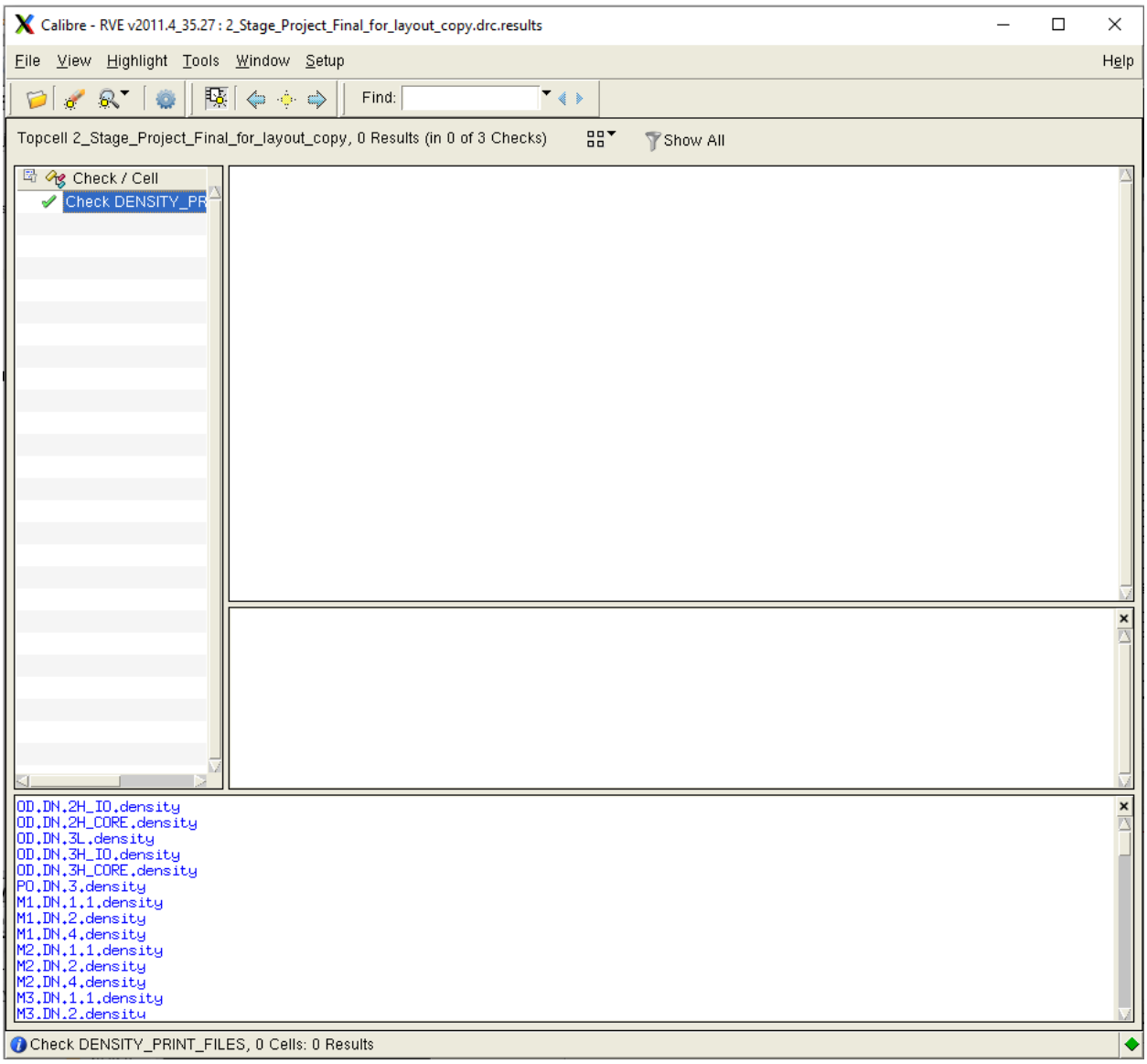

Part#02

The schematic includes a capacitor as well, but for the final layout the capacitor is excluded from the checks as placing it resulted in VMware to hang/stop responding for greater periods of time, delaying our work.

Part #2 layout



DRC check


Calibre - RVE v2011.4_35.27 : 2_Stage_Project_Final_for_layout_copy.drc.results
File View Highlight Tools Window Setup Help
Find:
Topcell 2_Stage_Project_Final_for_layout_copy, 0 Results (in 0 of 3 Checks)
Show All
Check / Cell
Check DENSITY_PR
OD.DN.2H_IO.density
OD.DN.2H_CORE.density
OD.DN.3L.density
OD.DN.3H_IO.density
OD.DN.3H_CORE.density
PO.DN.3.density
M1.DN.1.1.density
M1.DN.2.density
M1.DN.4.density
M2.DN.1.1.density
M2.DN.2.density
M2.DN.4.density
M3.DN.1.1.density
M3.DN.2.density
Check DENSITY_PRINT_FILES, 0 Cells: 0 Results

Final Layout