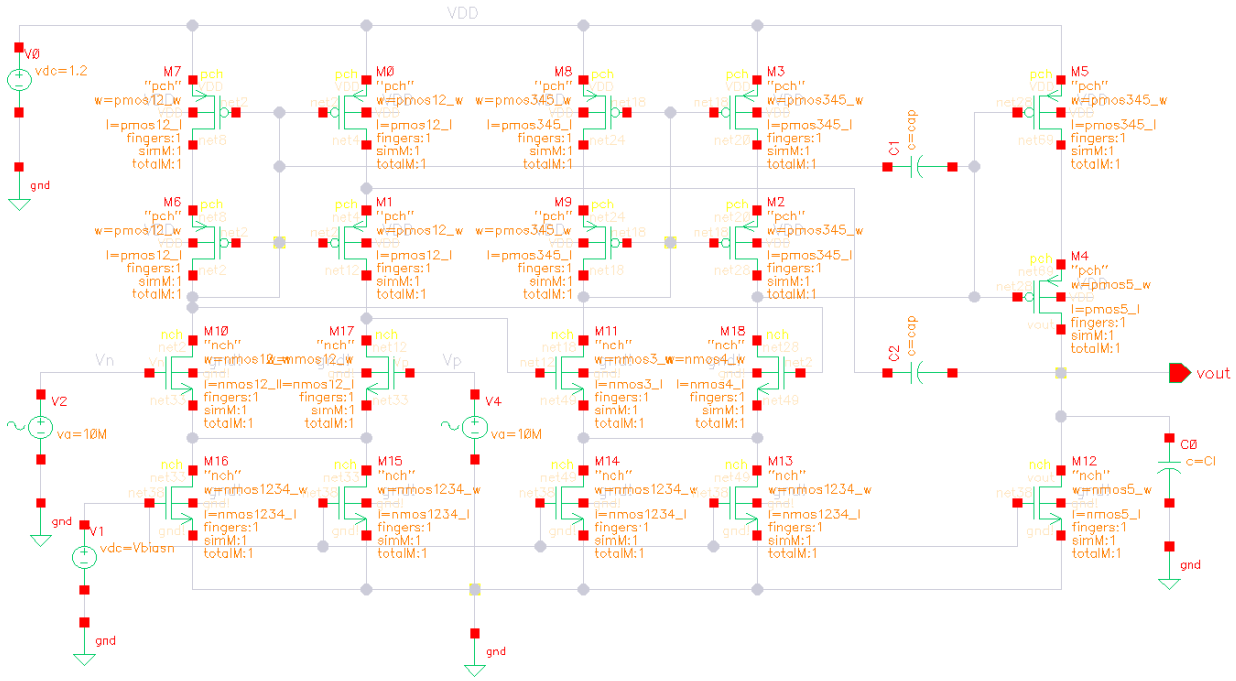
ELEG 587V Project #2 (100 pts)

For both parts, you are to utilize Cadence Virtuoso to design the necessary circuits. You supply voltage should be no larger than 1.2 V, and the circuits should be fully contained (i.e., you only provide the input signals and the power). You will write a short report and turn in all necessary schematics, simulations, and waveforms.

1. Design a three-stage op-amp that has a unity frequency of at least 100 MHz and provides 120 dB of gain. You have the choice of topologies. Plot the bode plot with phase and gain.

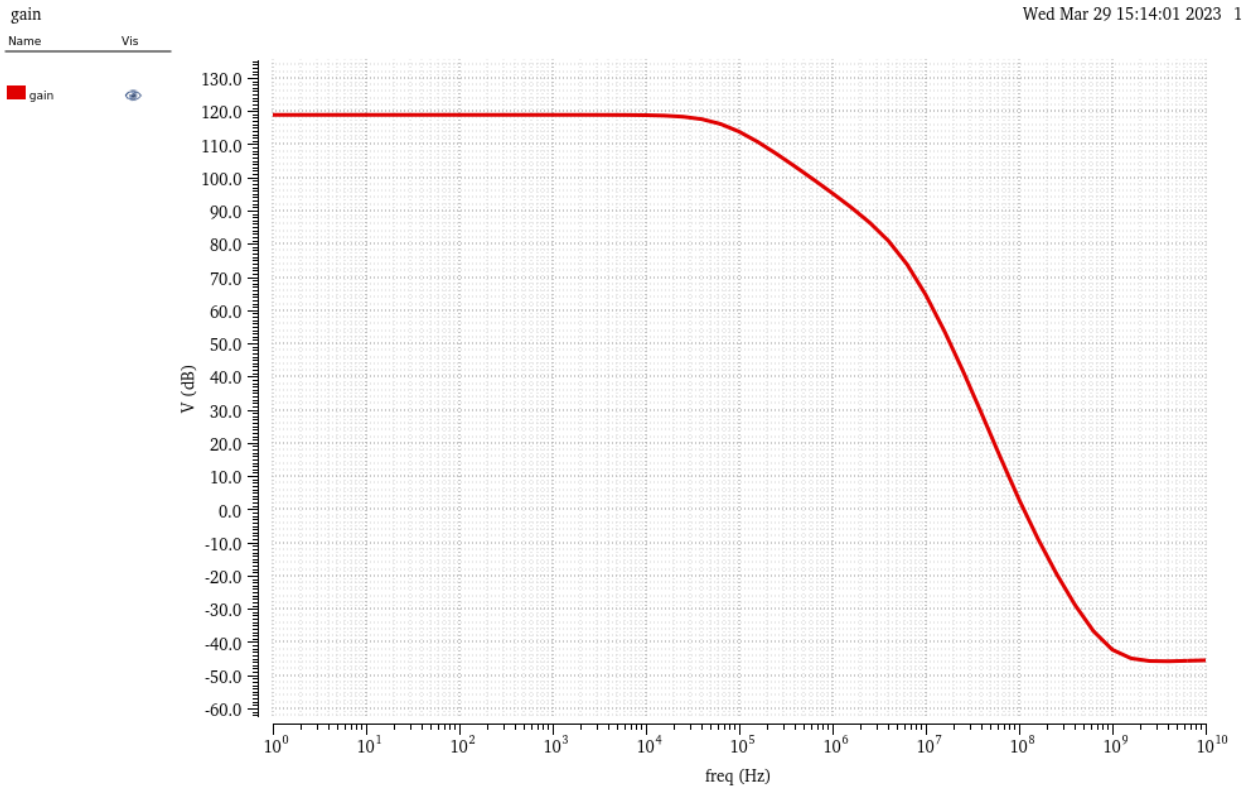
Schematic



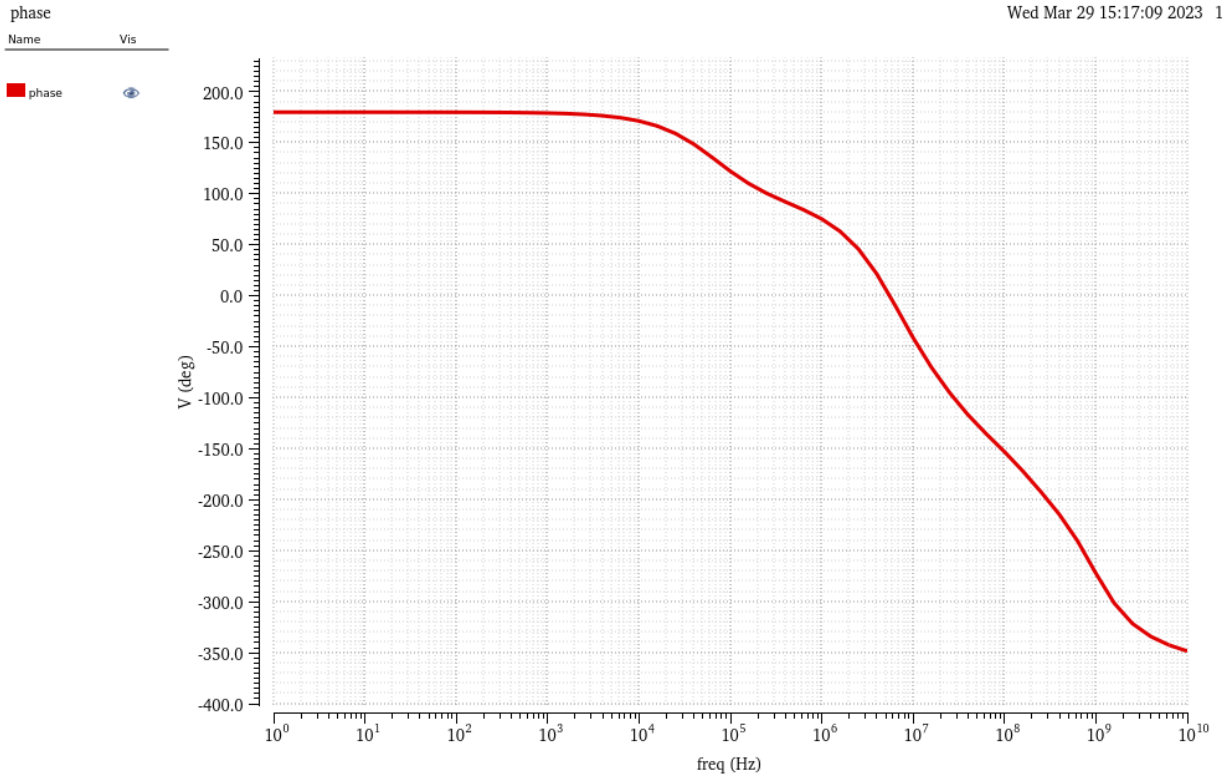
The schematic above shows a three-stage op-amp, built from a cascade of two diff-amps and a common-source amplifier. The cascaded gain of the diff-amps helps keep the overall gain high. The following page shows the gain and phase of this three-stage op-amp topology. The following list shows the design variables:

Design Variables	
cap	1f
Cl	1f
Vbiasn	295.3m
pmos12_l	222.6n
pmos345_l	847.5n
pmos12_w	190.2n
pmos345_w	7.92u
nmos1_l	1u
nmos2_l	1u
nmos12_l	4.044u
nmos3_l	1u
nmos4_l	1u
nmos5_l	2.703u
nmos1234_l	1.5u
nmos1_w	18u
nmos2_w	18u
nmos12_w	468.8u
nmos3_w	10u
nmos4_w	9.9u
nmos5_w	25u
nmos1234_w	13u
v_ac	1.2
pmos5_l	1.543u
pmos5_w	14.67u
pmos34_w	6u
pmos34_l	750n
v_dc	437m

Gain

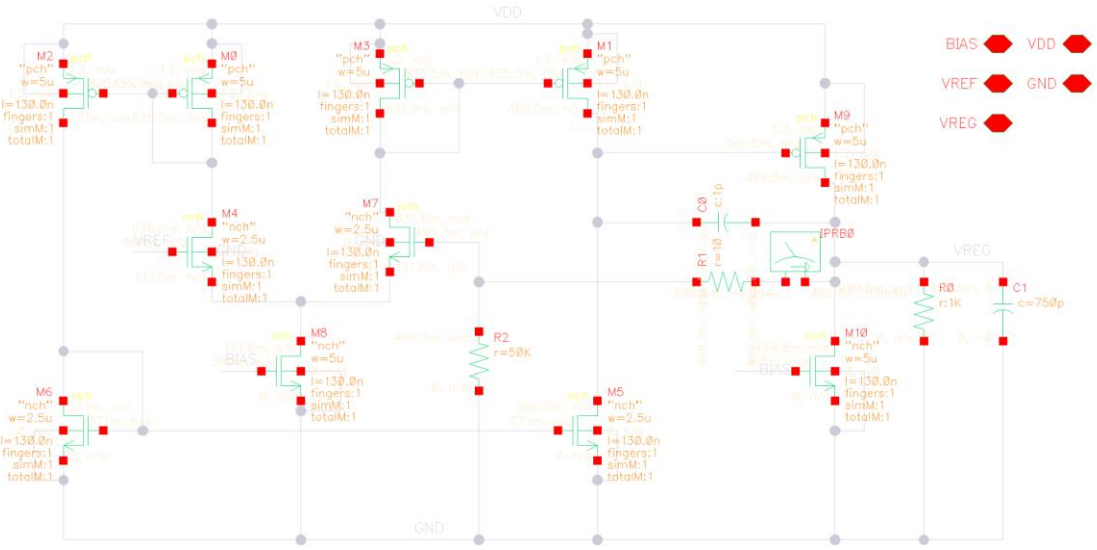

gain
Name
Vis
gain
Wed Mar 29 15:14:01 2023 1
V (dB)
130.0
120.0
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
freq (Hz)

Phase

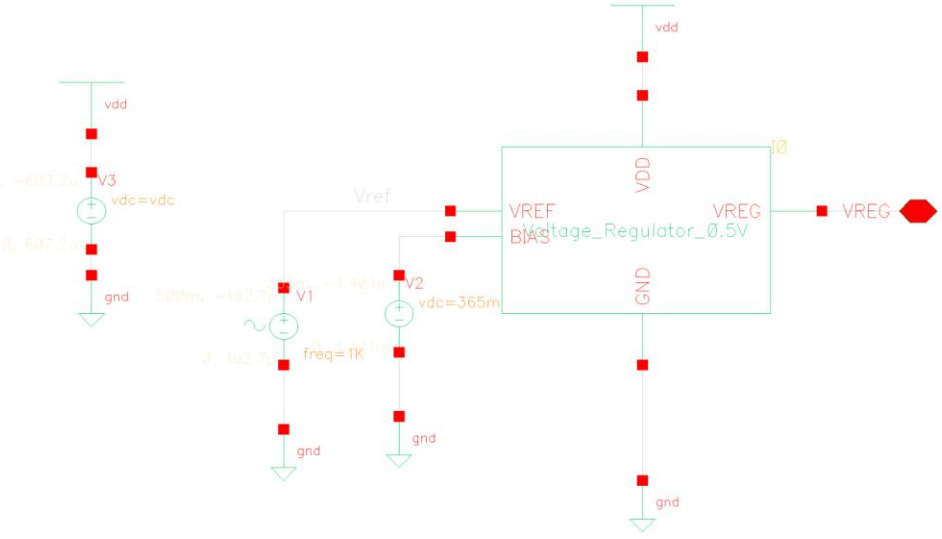

phase
Name
Vis
phase
Wed Mar 29 15:17:09 2023 1
V (deg)
200.0
150.0
100.0
50.0
0.0
-50.0
-100.0
-150.0
-200.0
-250.0
-300.0
-350.0
-400.0
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
freq (Hz)

2. Design a voltage regulator that has a stable output voltage of 0.5 V. Show the minimum load capacitance and maximum load resistance that the regulator can safely operate via simulations. Provide the bode plot that shows the stability of the regulator over frequency.

Schematic:

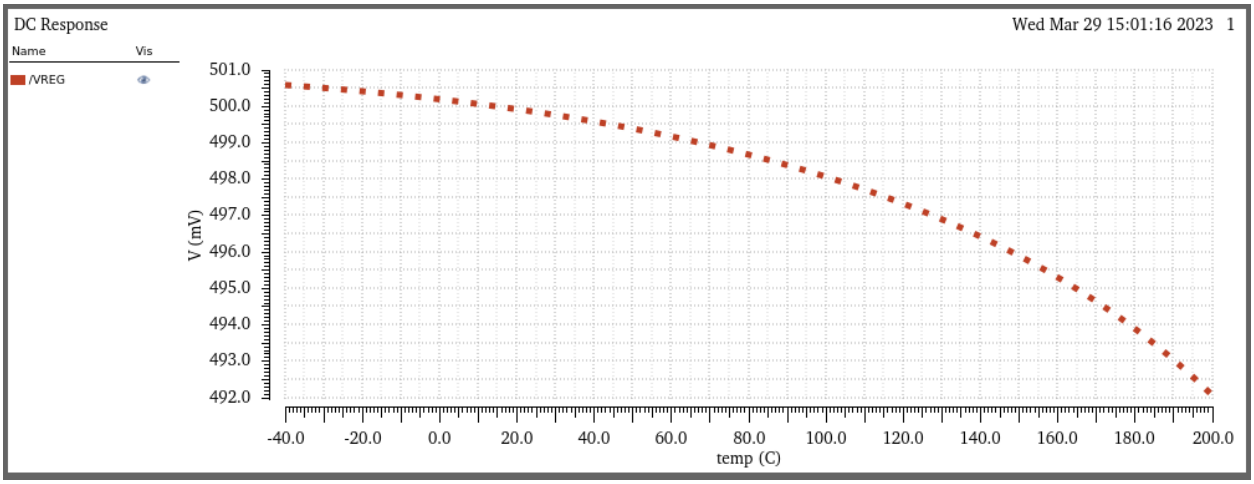


Test Bench:



Simulation:

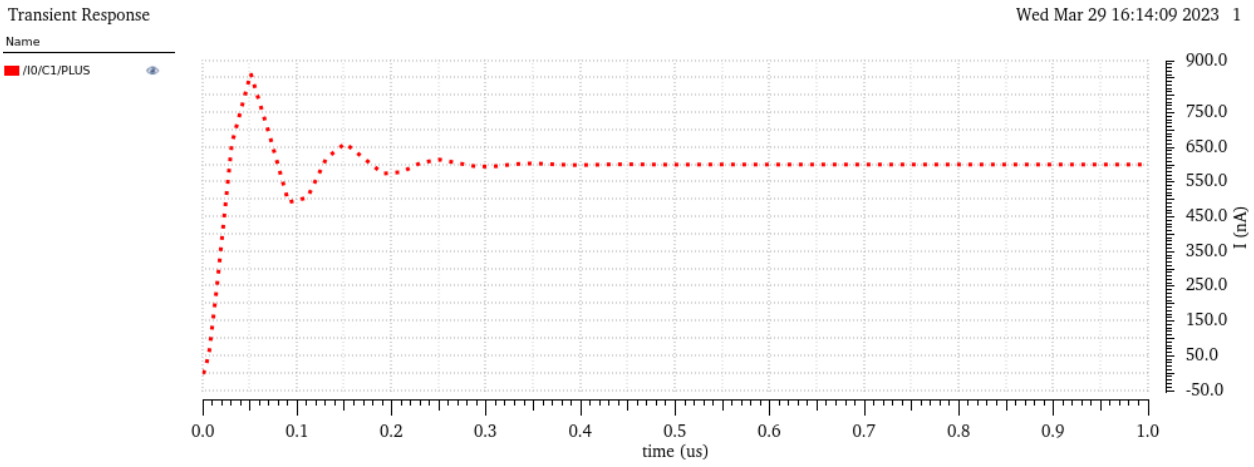
For the voltage regulator to have a stable output of 0.5V, the above circuit is simulated at varying temperatures (-40C to 200C) and the output voltage denoted by VREG is observed.



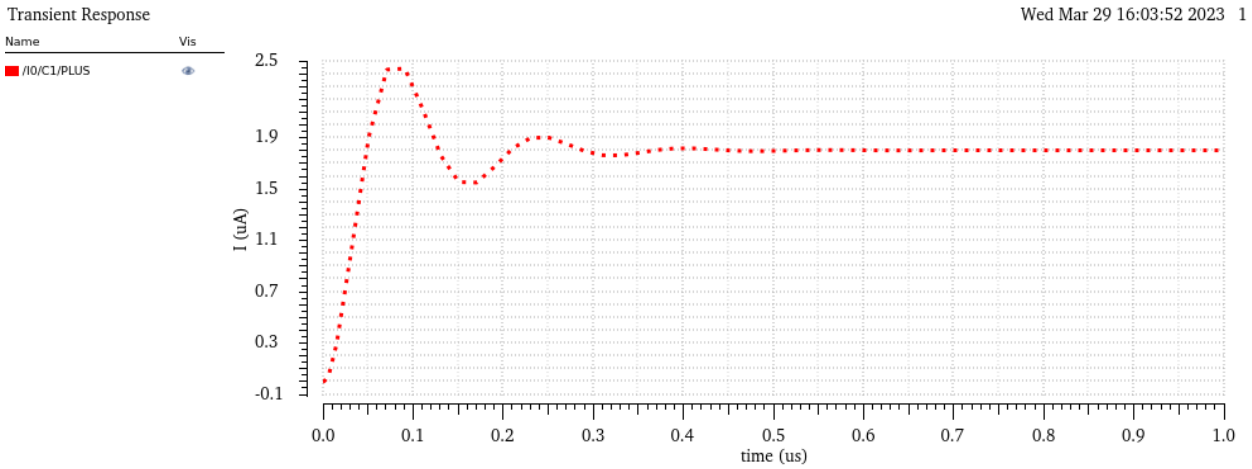
The above plot shows little variations for the change in temperature on the regulated output voltage.

Inorder to identify the minimum load capacitance, the transient response of the output current is observed. The plots below shows the response of output current with time for varying capacitive values.

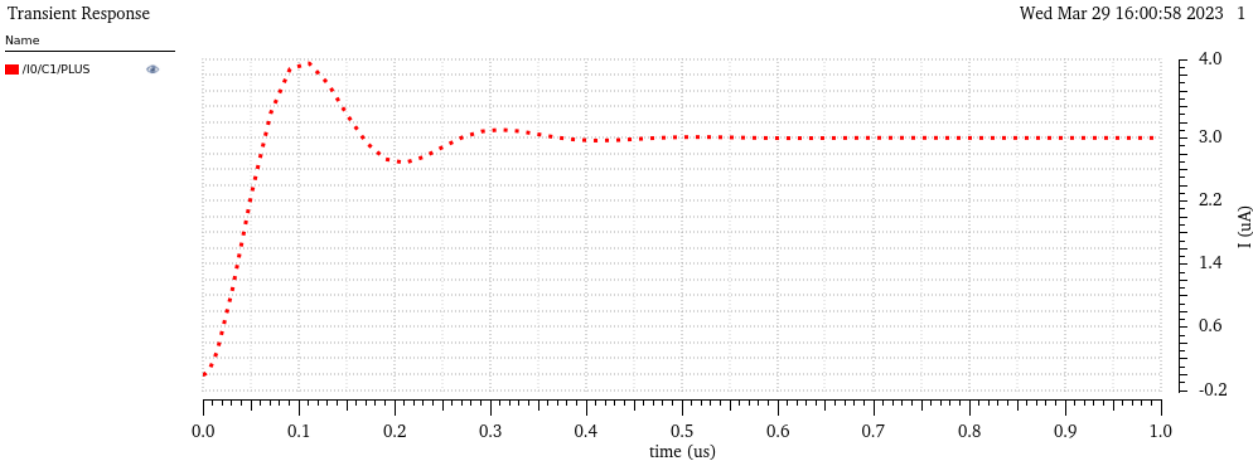
C_{load}=100p F VREF=499.8 mV Phase=34.22



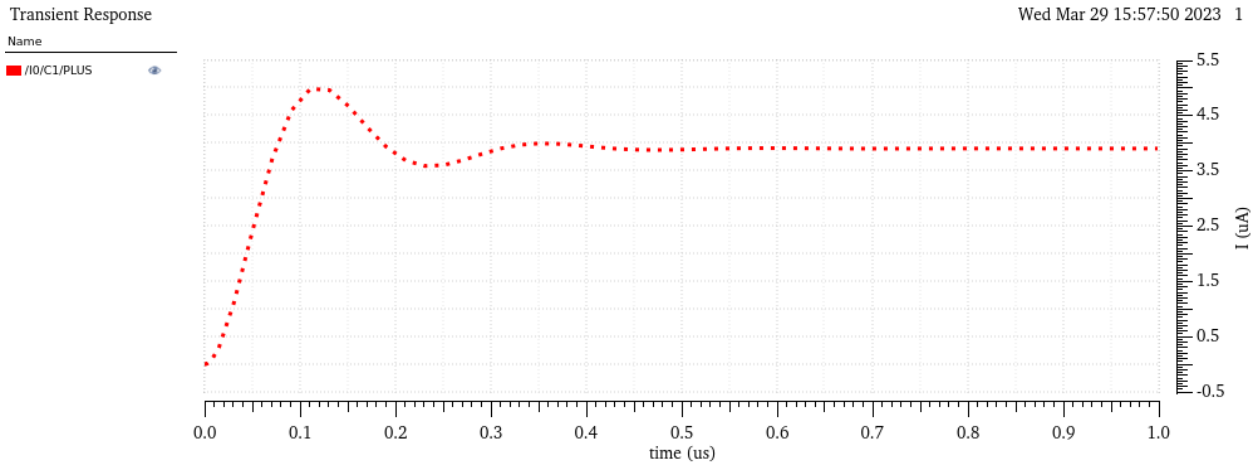
C_{load}=300p F VREF=499.8 mV Phase=36.33



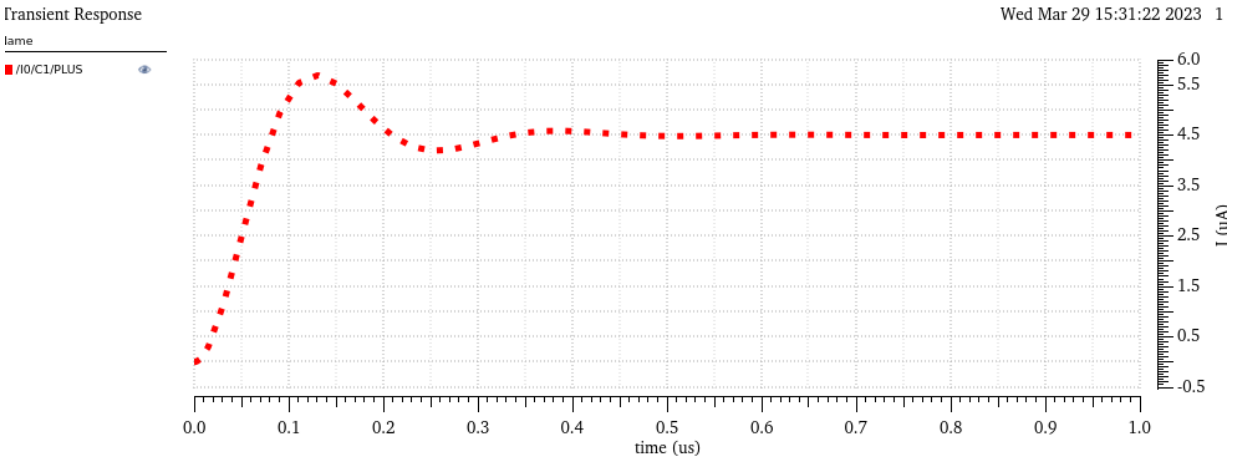
C_{load}=500p F VREF=499.8 mV Phase=40.57



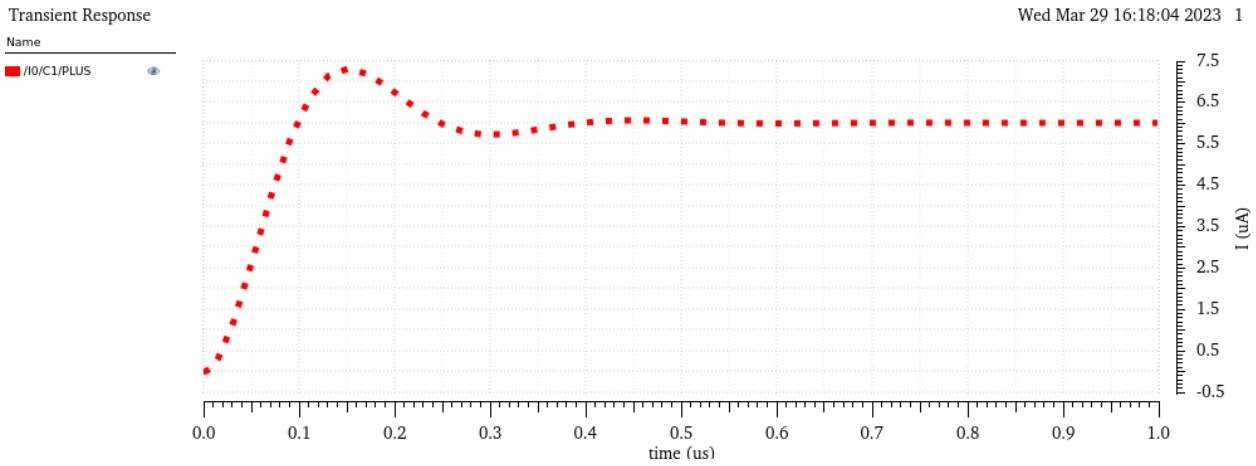
C_{load}=700p F VREF=499.8 mV Phase=43.54



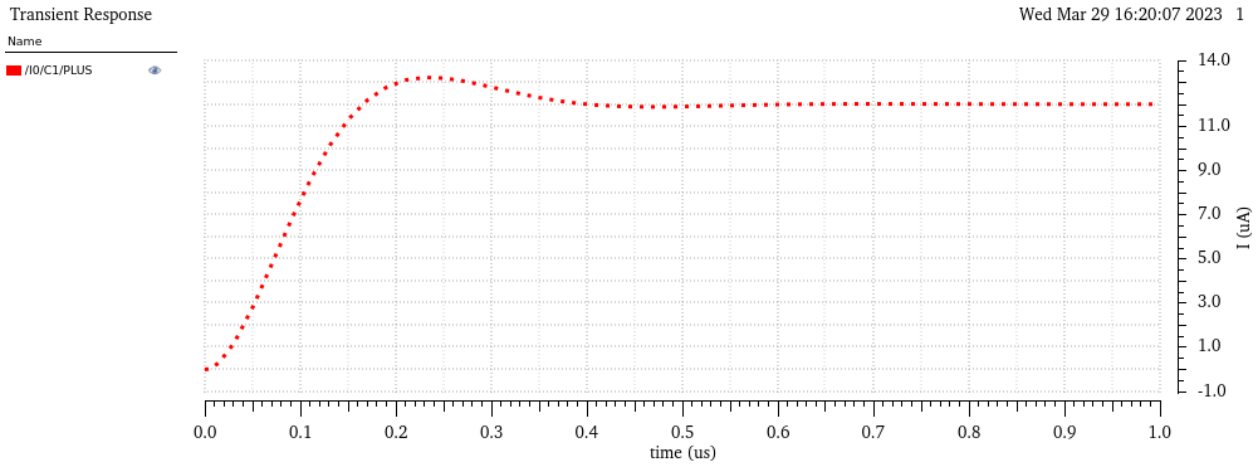
C_{load}=750p F VREF=499.8 mV Phase=45.4



C_{load}=1000p F VREF=499.8 mV Phase=49.57

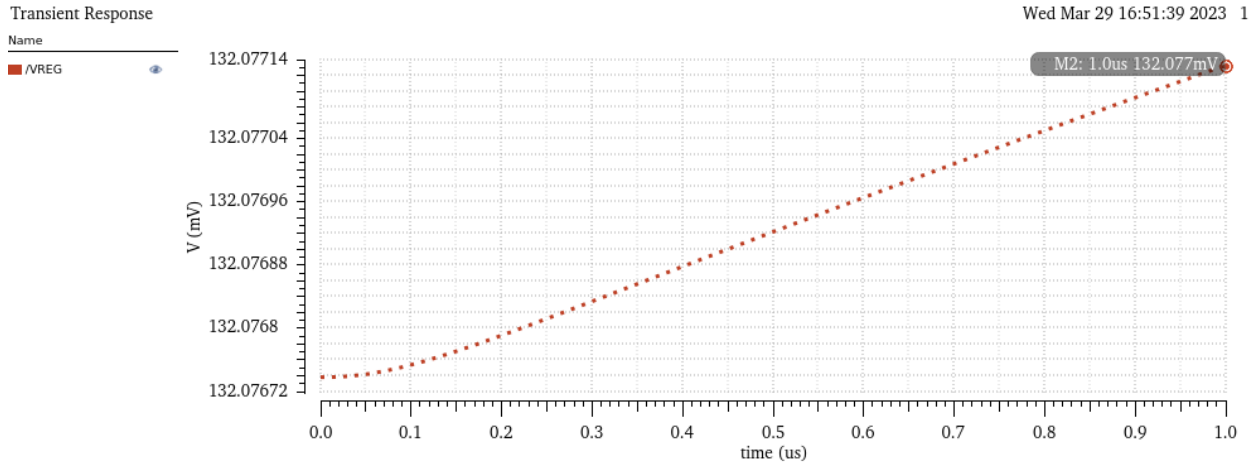


C_{load}=2n F VREF=499.8 mV Phase=61.38

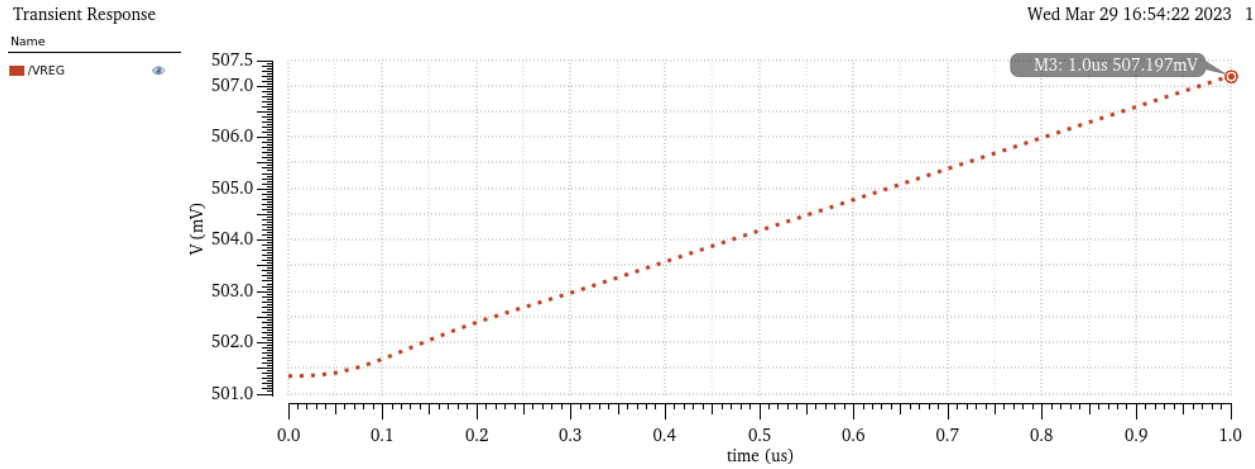


From the above analysis, it can be observed that the minimum load capacitance is **750p F**. The transient response can be seen to improve if we keep on increasing the value of C_{load}.

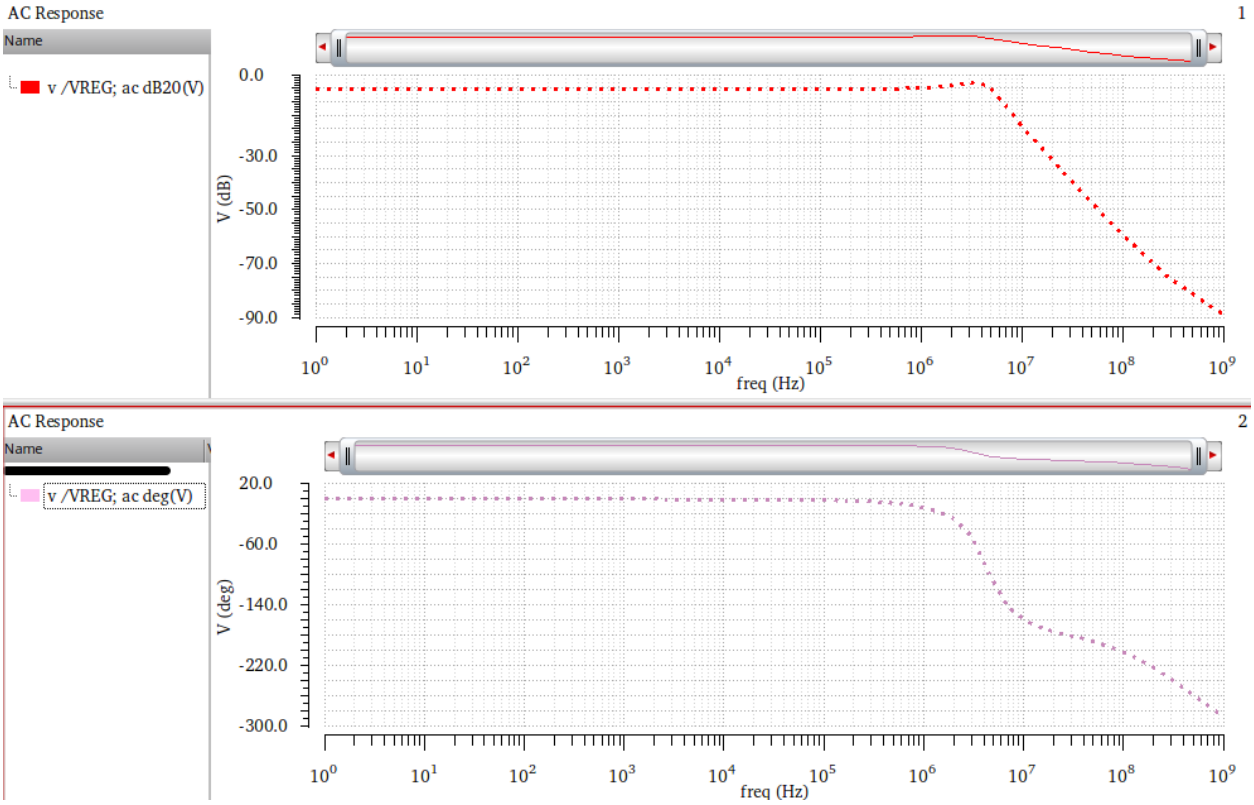
The maximum value of load resistance comes out to be **1K ohms**, decreasing, results in a decreased VREF. Below is a plot for Rload= 100 Ohms



Increasing above 1K ohms, the value of VREF starts to increase. A plot for Rload= 1.1K ohms is shown below.



Bode Plot:


AC Response
1
Name
v /VREG; ac dB20(V)
0.0
-30.0
-50.0
-70.0
-90.0
V (dB)
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9
freq (Hz)
AC Response
2
Name
v /VREG; ac deg(V)
20.0
-60.0
-140.0
-220.0
-300.0
V (deg)
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9
freq (Hz)