Aireen Amir Jalal
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Integrated Design Lab I

Homework #3 (due April 18th)

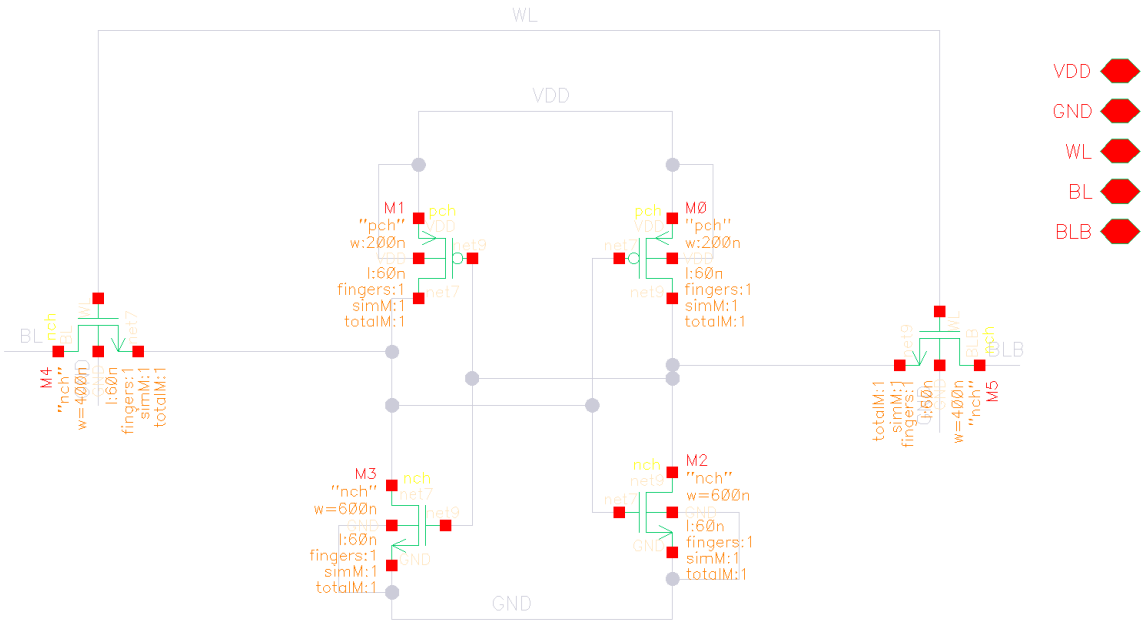
1. Implement a SRAM cell in schematic and layout (26 by 45 λ) with DRC and LVS checks. You must give me the pitch distances and total x and y dimensions on this or lose points.

2. Create a separate schematic and generate a SRAM array of 32 4-bit words. You have creative control over the shape of the array but remember to account for capacitance delays you will experience on long lines. The devices should be connected in schematic.

3. In layout and using SKILL code (optional but useful), generate your SRAM array. The devices should already be interconnected via smart layout in item #1. This should be the shortest task in the homework as it is copy and paste operation. Provide DRC and LVS checks.

Turn in all schematics, layouts, checks, and SKILL code used for this homework as well as the pitch distances.

SRAM BITCELL:



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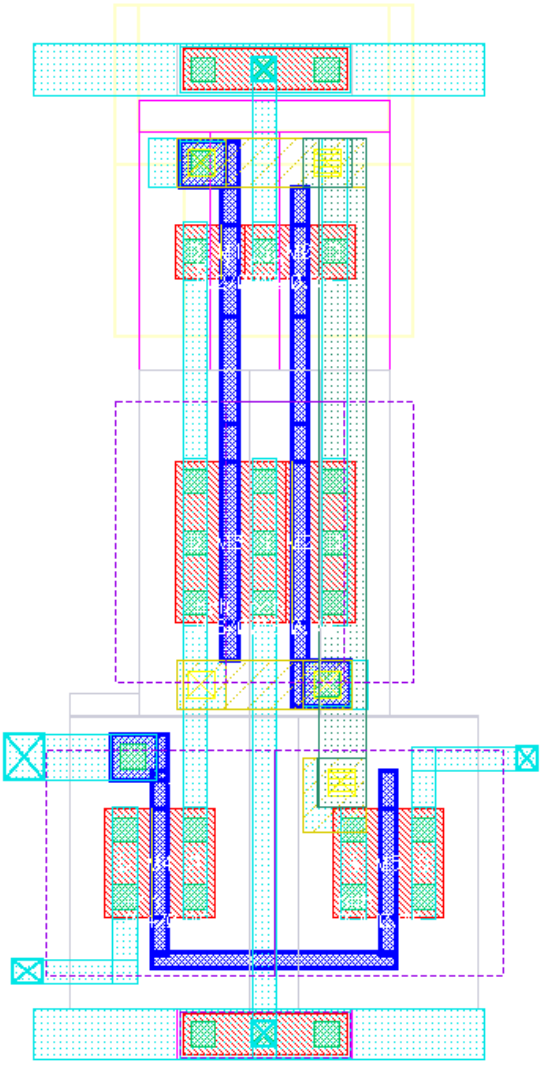
BITCELL LAYOUT:



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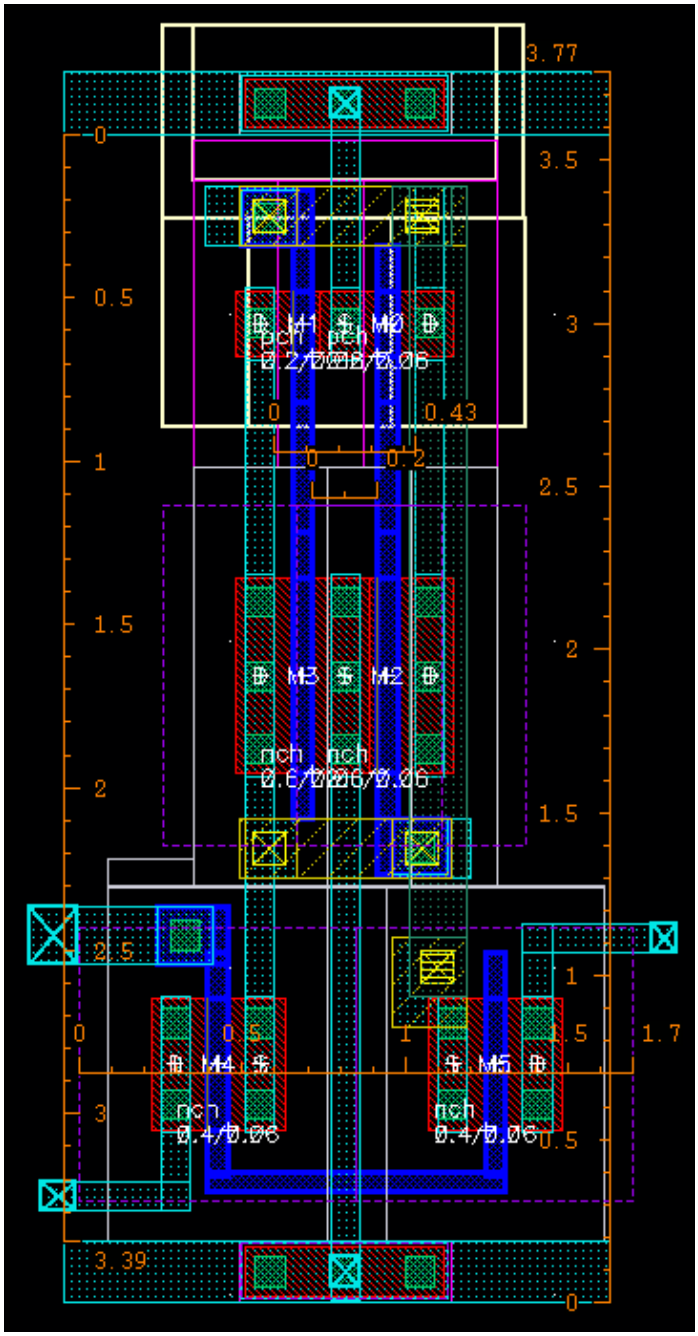
PITCH DISTANCES (shown in the image below):

Lambda=65nm

X AND Y DIMENSIONS:

X=1.7 microns

Y=3.77 microns



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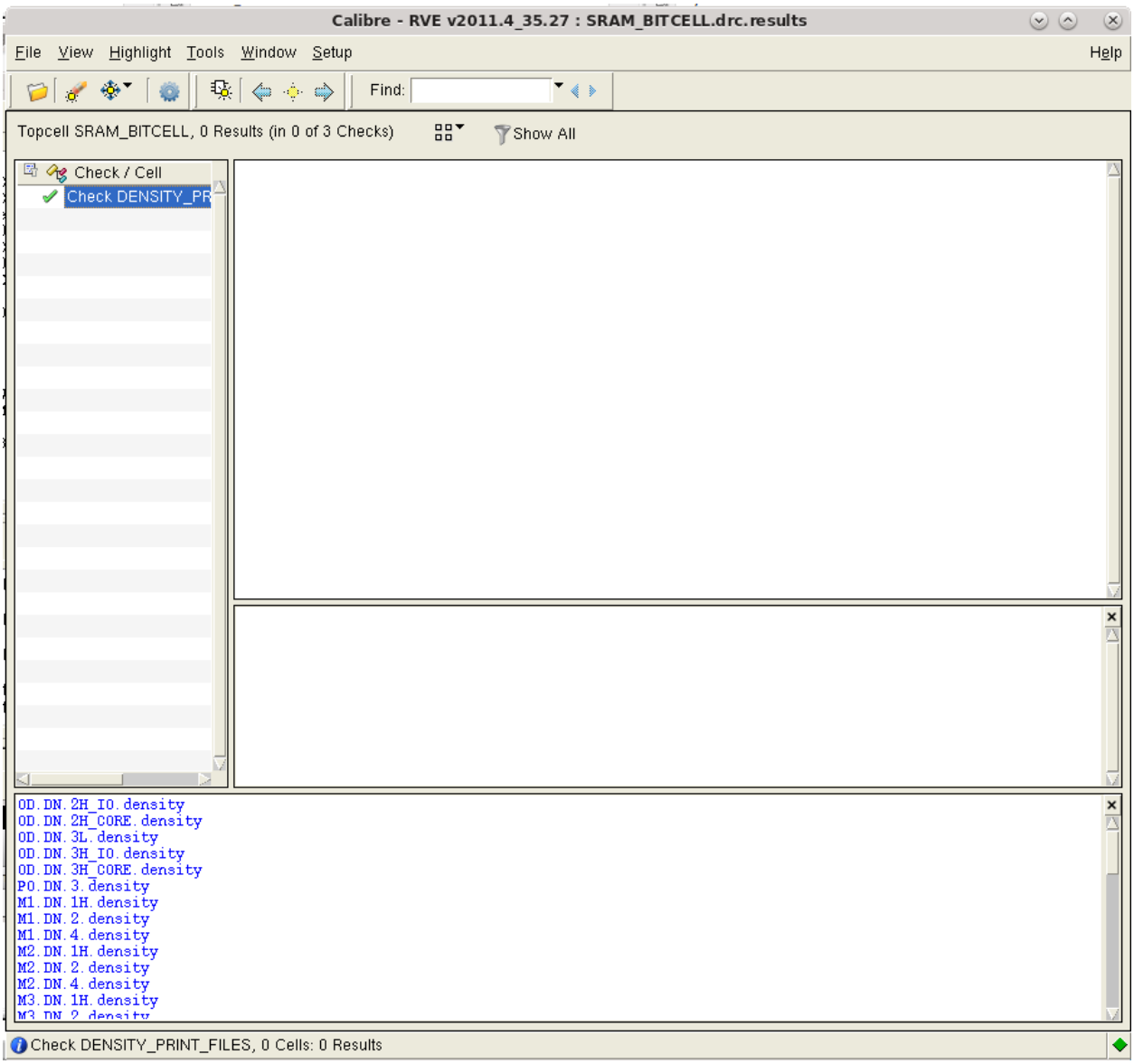
DRC:



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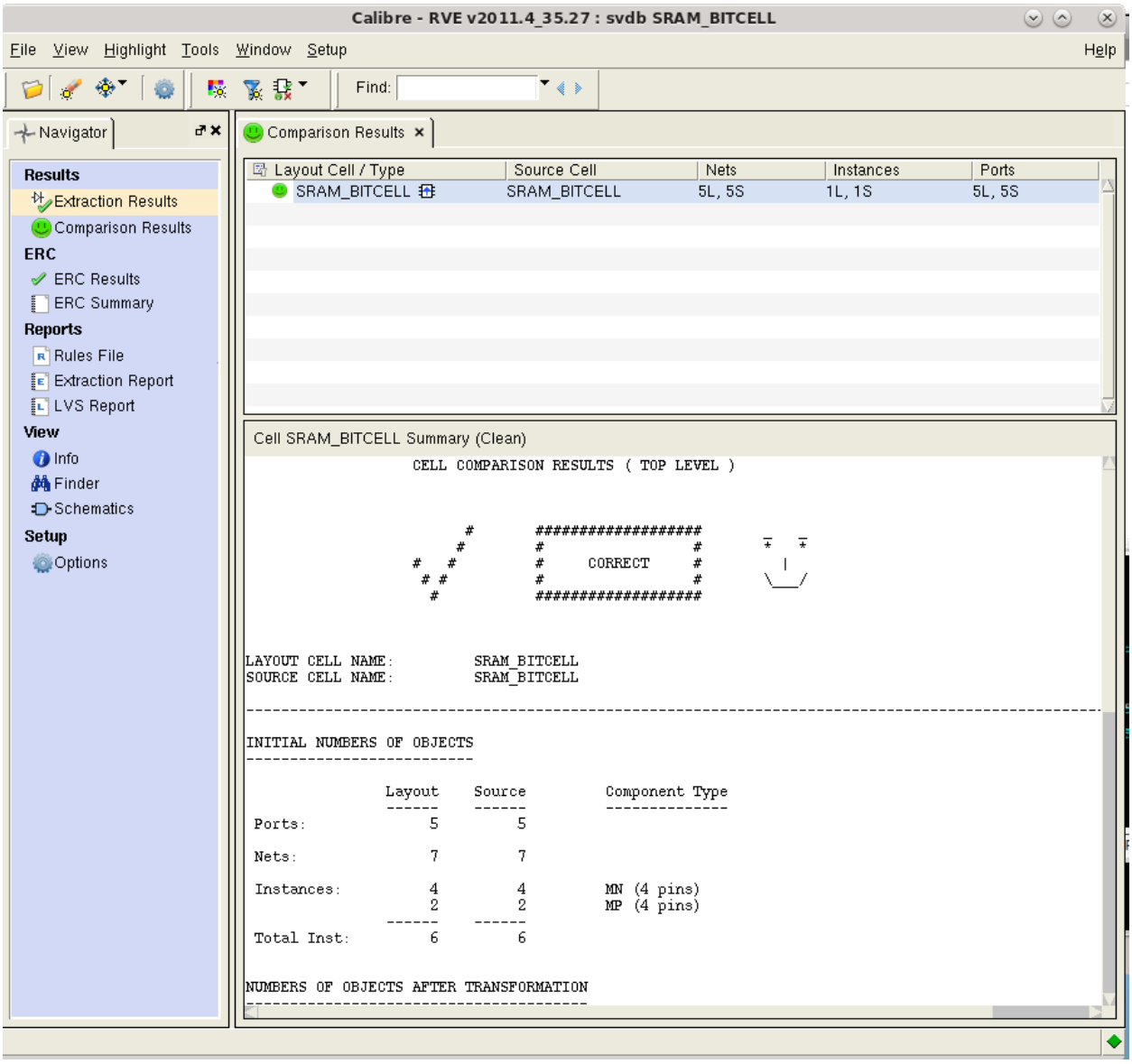
LVS:



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32X4 SRAM ARRAY:

SCHEMATIC:

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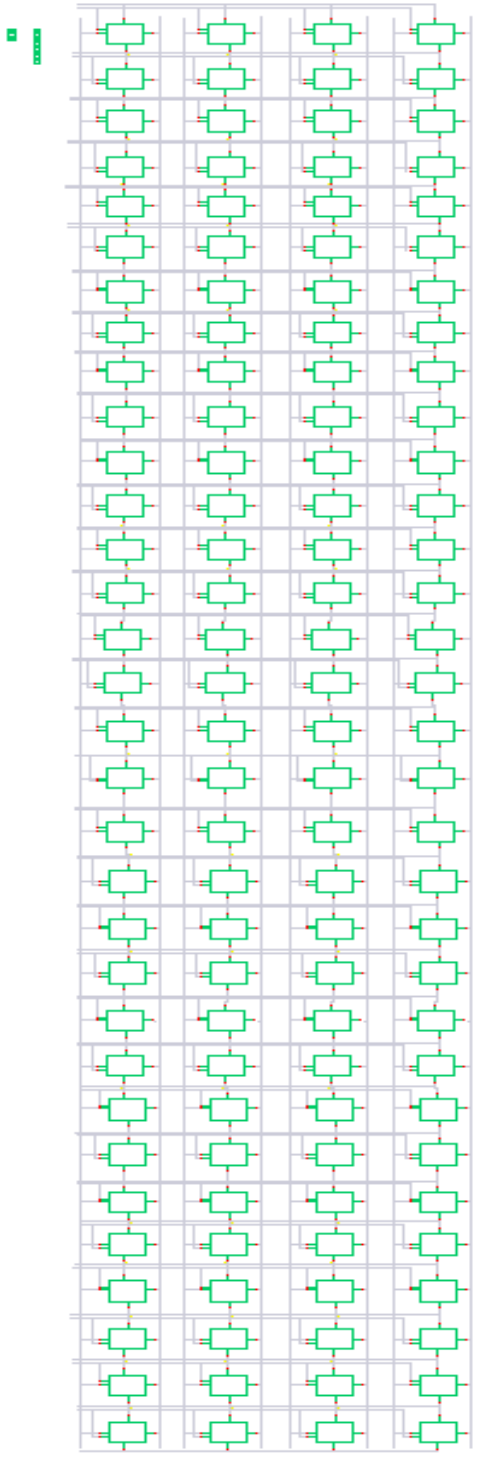

LAYOUT:

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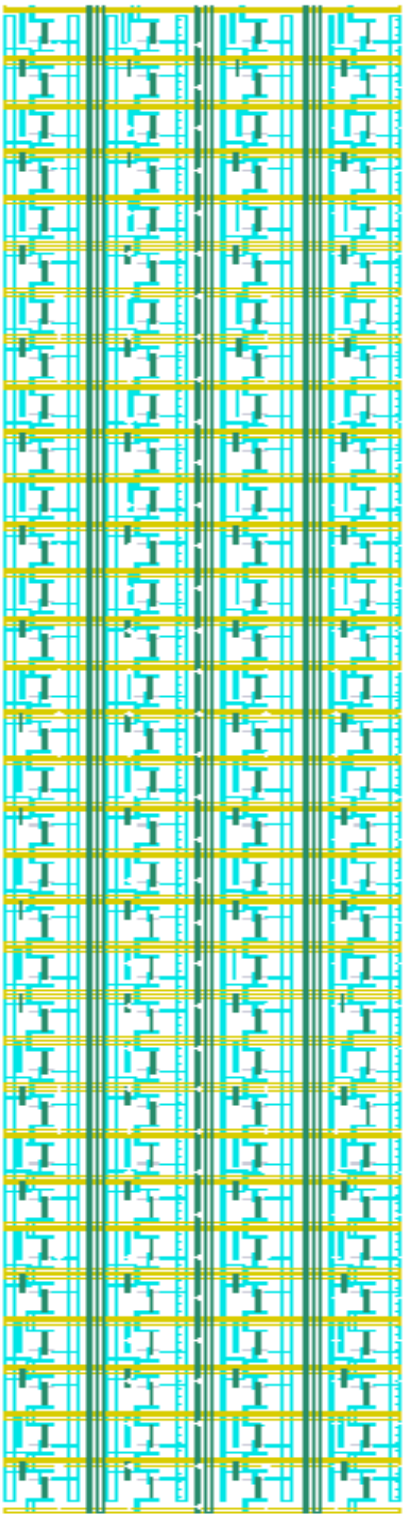

DRC:

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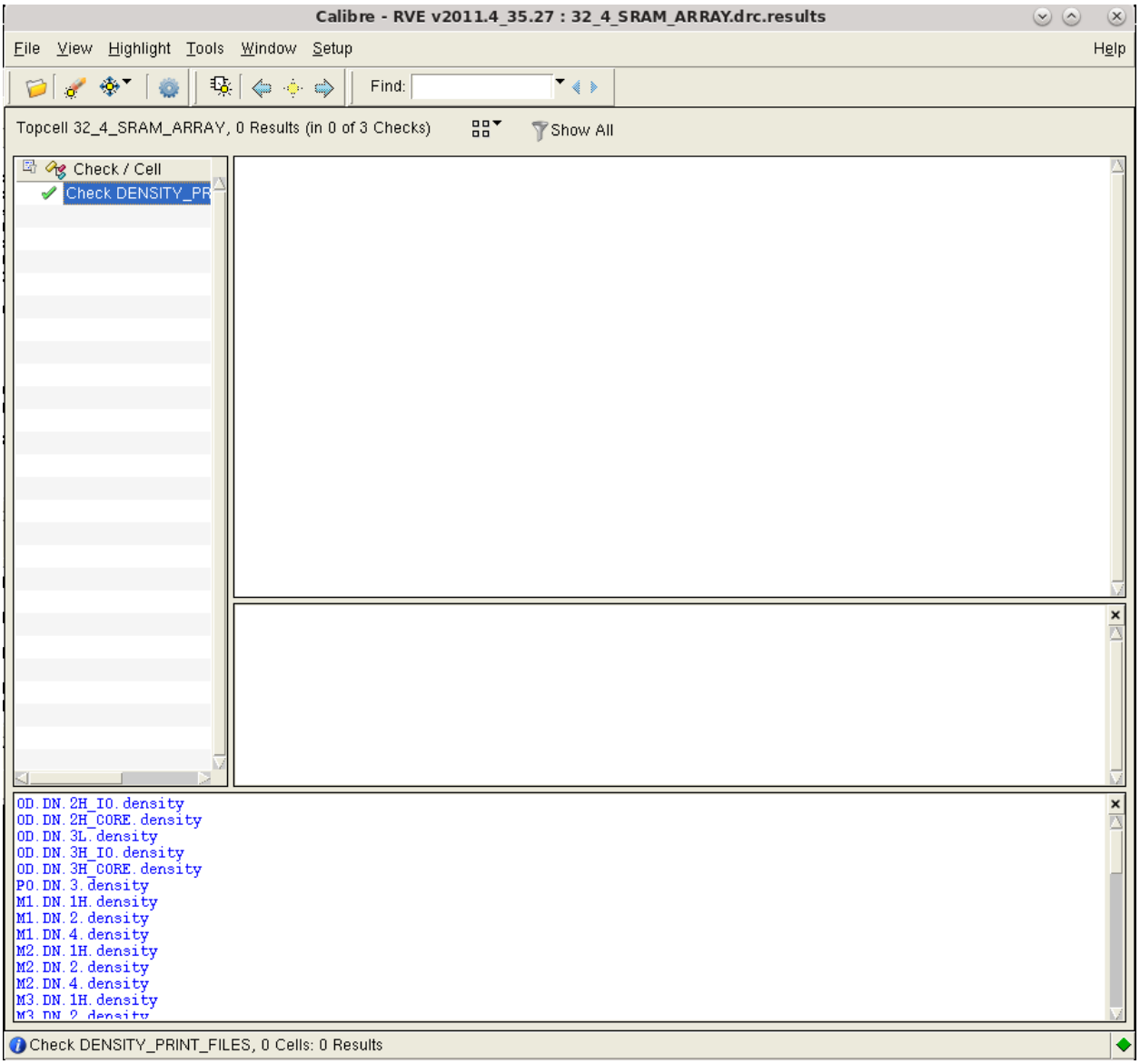

LVS:

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