

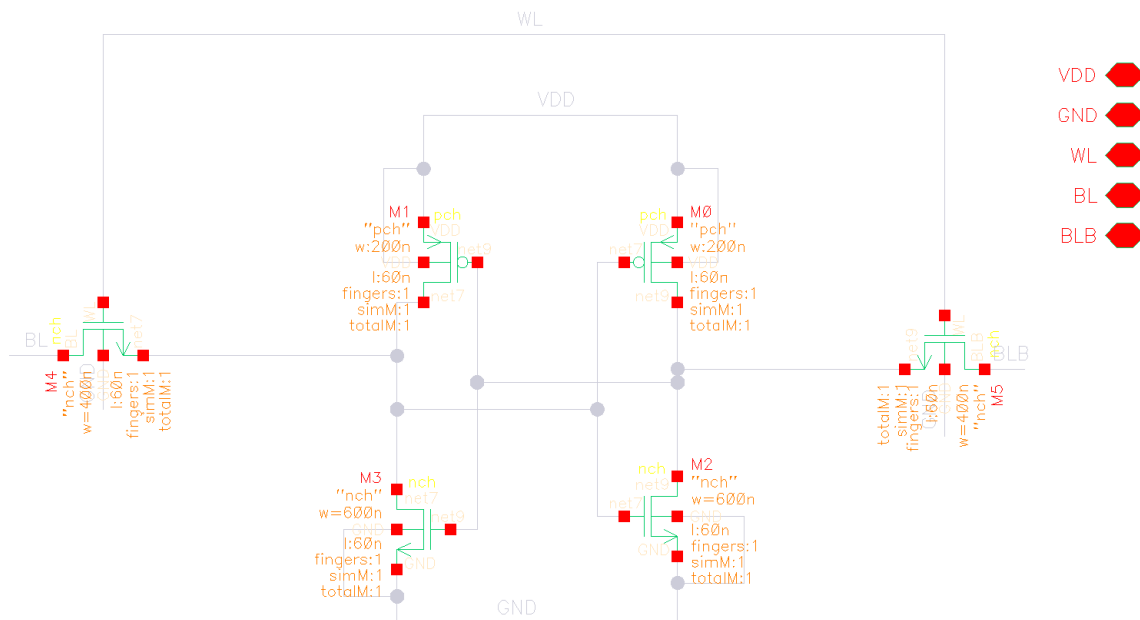
Integrated Design Lab I

Homework #3 (due April 18th)

1. Implement a SRAM cell in schematic and layout (26 by 45 λ) with DRC and LVS checks. You must give me the pitch distances and total x and y dimensions on this or lose points.
2. Create a separate schematic and generate a SRAM array of 32 4-bit words. You have creative control over the shape of the array but remember to account for capacitance delays you will experience on long lines. The devices should be connected in schematic.
3. In layout and using SKILL code (optional but useful), generate your SRAM array. The devices should already be interconnected via smart layout in item #1. This should be the shortest task in the homework as it is copy and paste operation. Provide DRC and LVS checks.

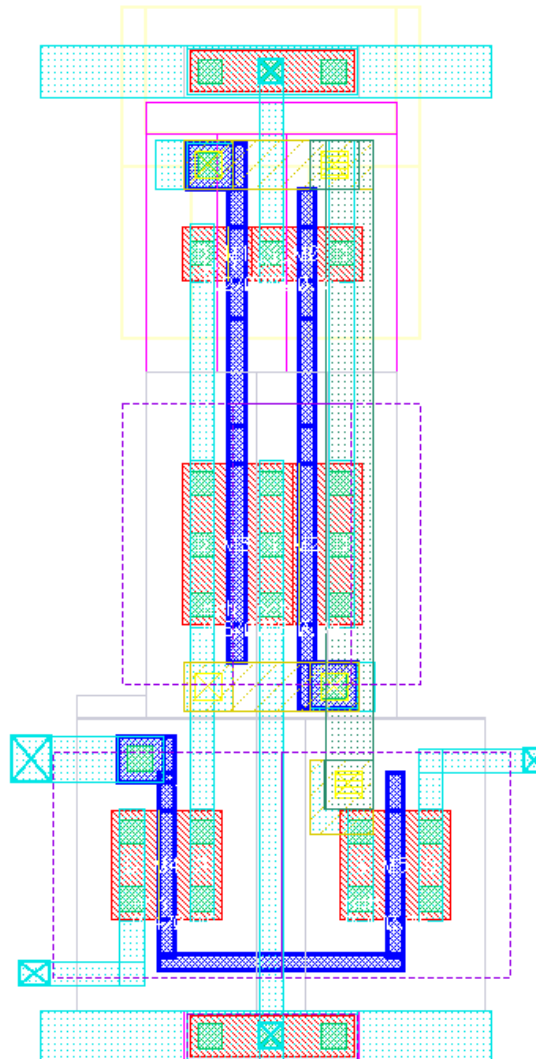
Turn in all schematics, layouts, checks, and SKILL code used for this homework as well as the pitch distances.

SRAM BITCELL:



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BITCELL LAYOUT:



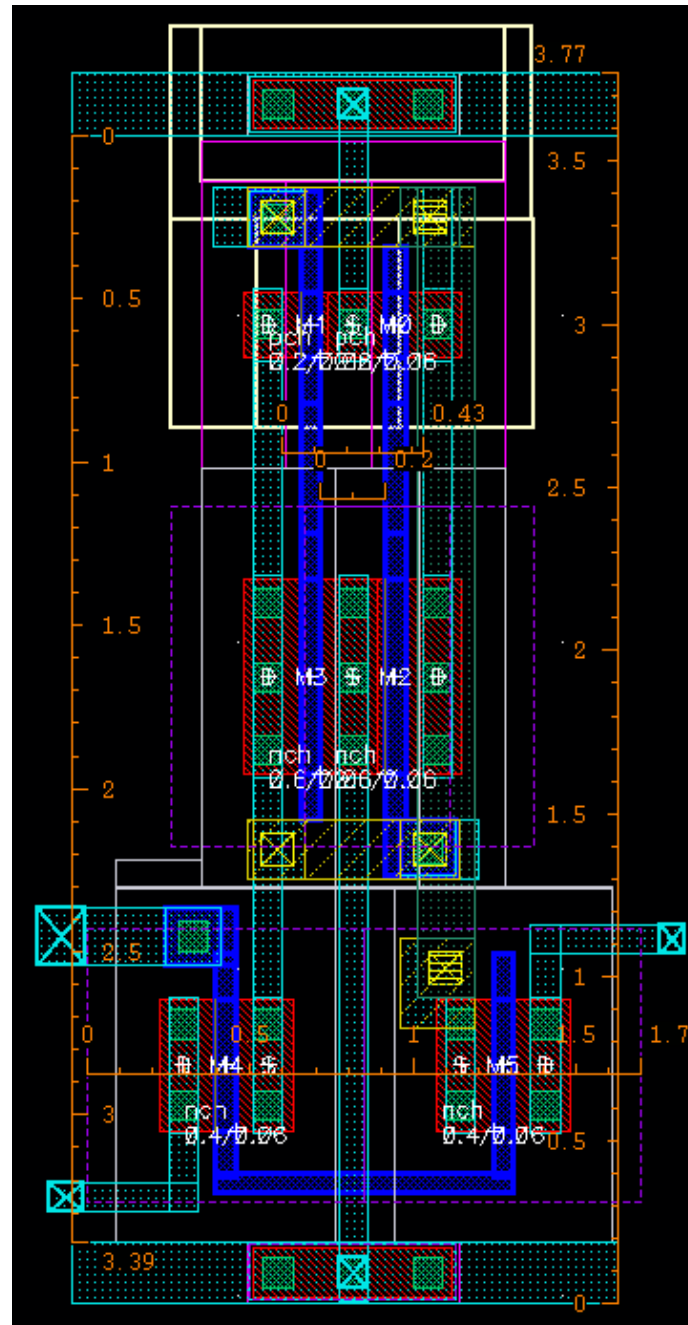
PITCH DISTANCES (shown in the image below):

Lambda=65nm

X AND Y DIMENSIONS:

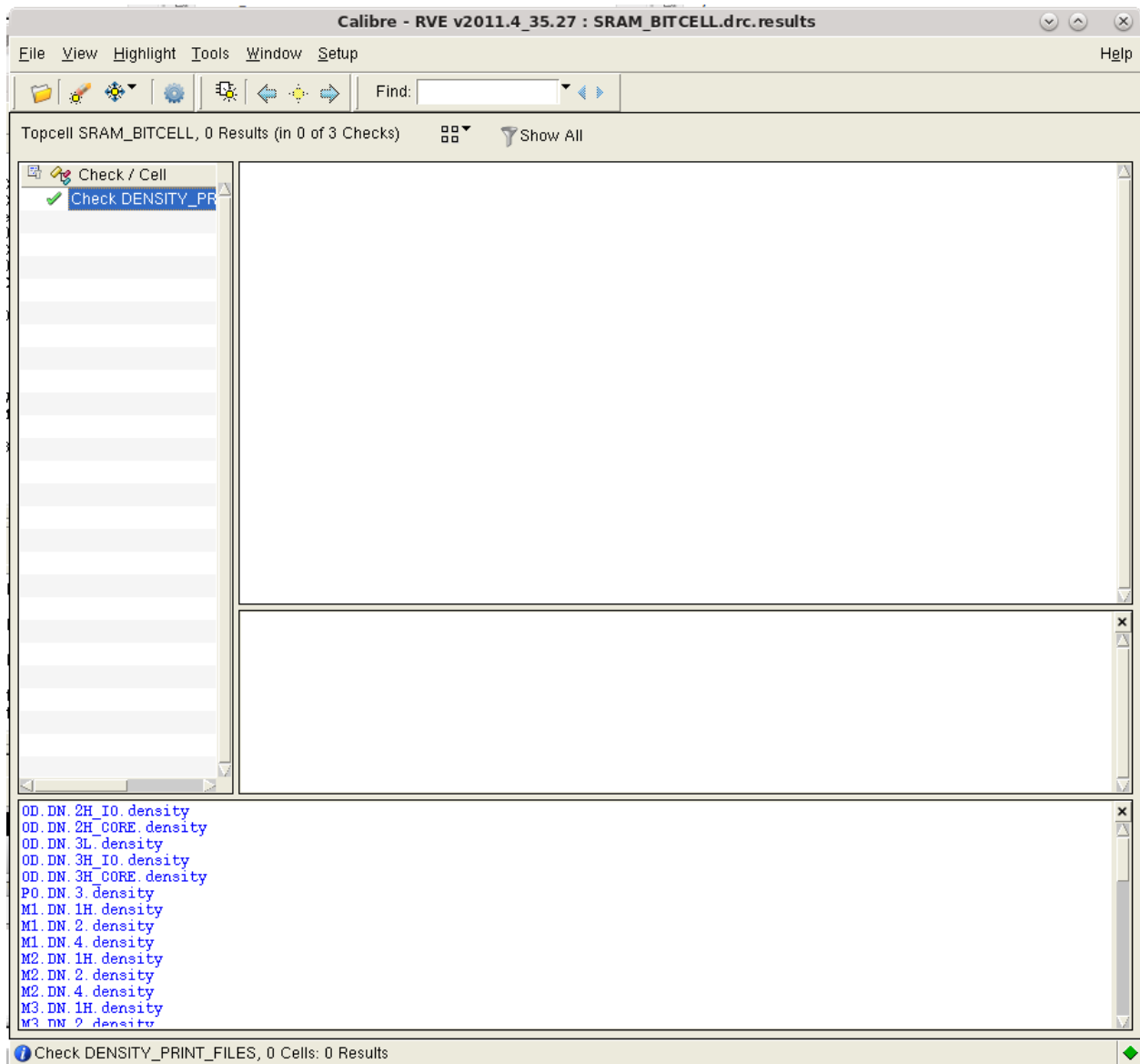
X=1.7 microns

Y=3.77 microns



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DRC:



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LVS:

Calibre - RVE v2011.4_35.27 : svdb SRAM_BITCELL

File View Highlight Tools Window Setup Help

Find:

Navigator

Results

- Extraction Results
- Comparison Results

ERC

- ERC Results
- ERC Summary

Reports

- Rules File
- Extraction Report
- LVS Report

View

- Info
- Finder
- Schematics

Setup

- Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
SRAM_BITCELL	SRAM_BITCELL	5L, 5S	1L, 1S	5L, 5S

Cell SRAM_BITCELL Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```
#####  
#          #          #          #  
# CORRECT  #          #          #  
#          #          #          #  
#####
```

LAYOUT CELL NAME: SRAM_BITCELL
SOURCE CELL NAME: SRAM_BITCELL

INITIAL NUMBERS OF OBJECTS

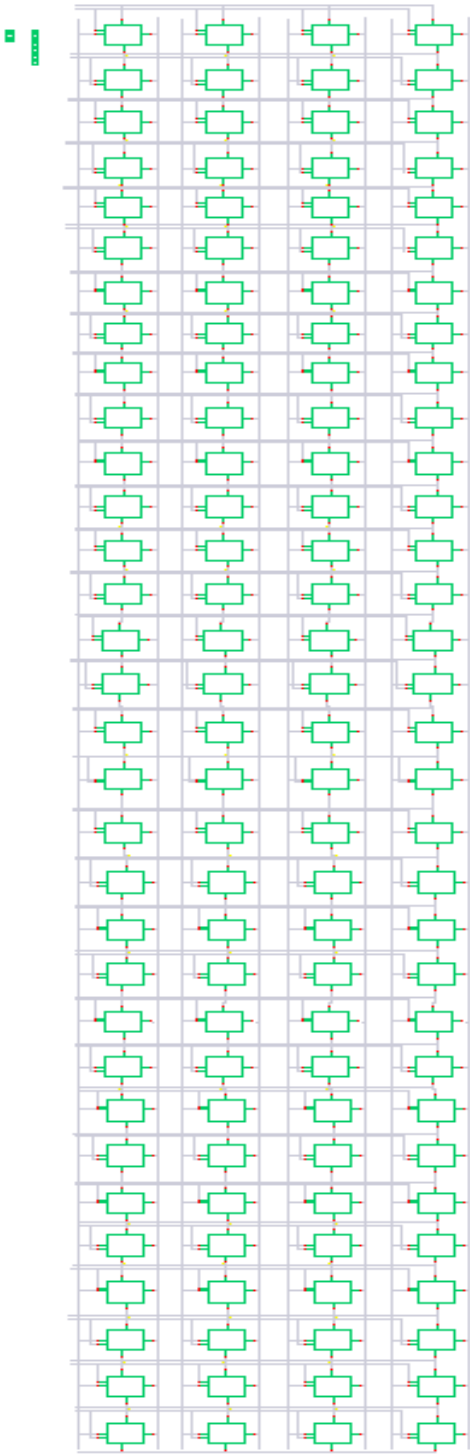
	Layout	Source	Component Type
Ports:	5	5	
Nets:	7	7	
Instances:	4	4	MN (4 pins)
	2	2	MP (4 pins)
Total Inst:	6	6	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

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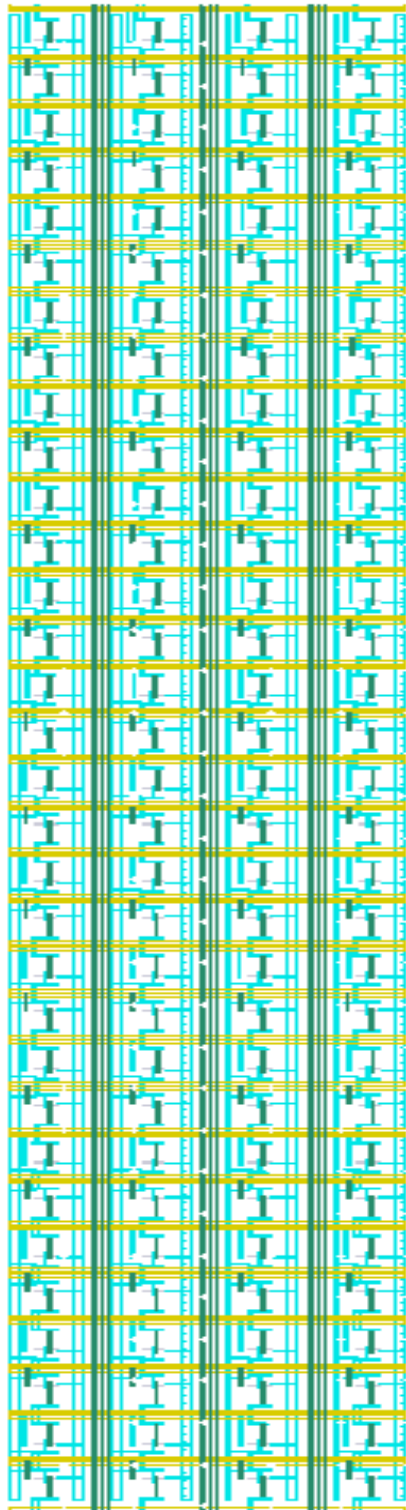
32X4 SRAM ARRAY:

SCHEMATIC:



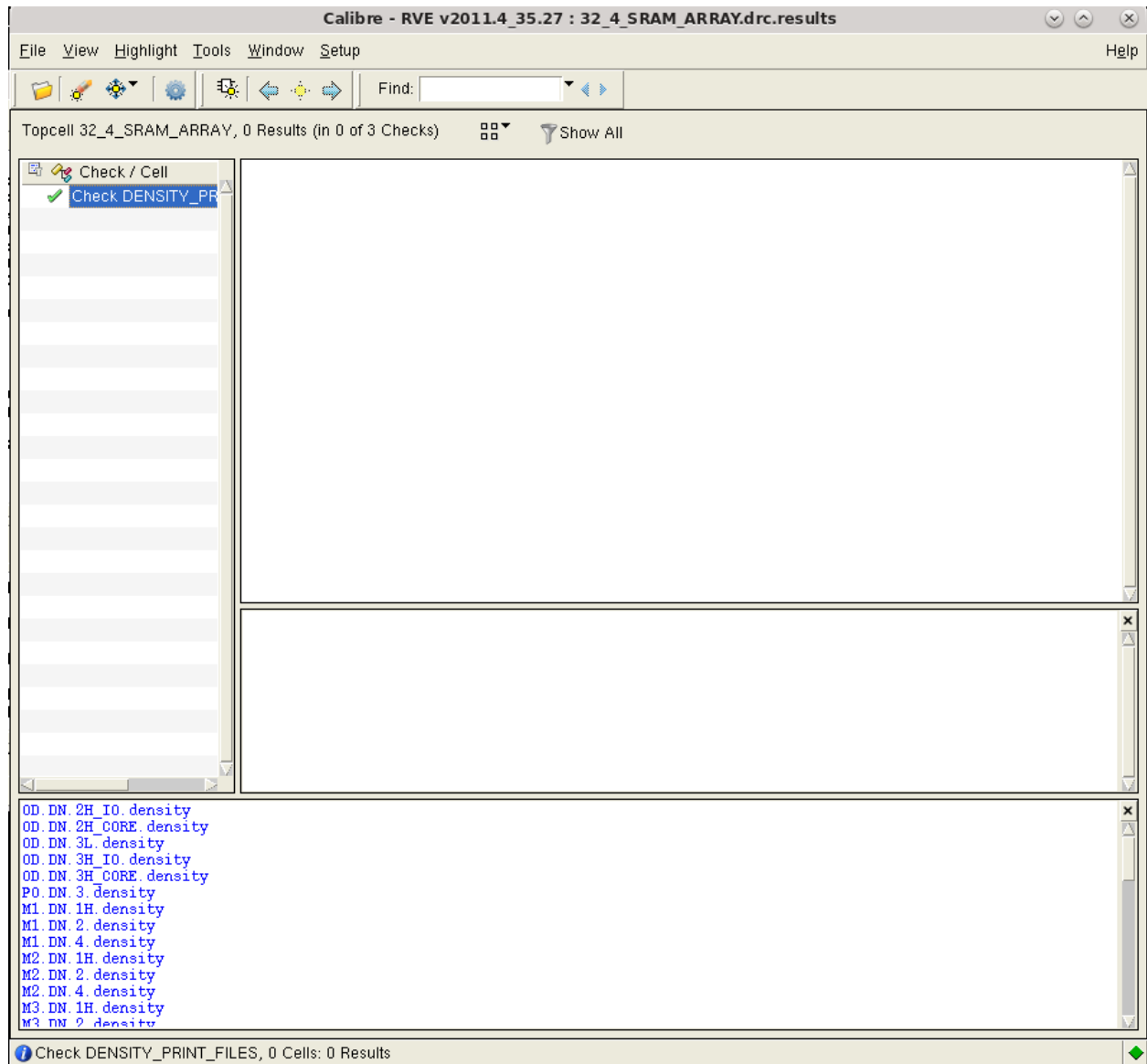
LAYOUT:

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DRC:

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LVS:

Calibre - RVE v2011.4_35.27 : svdb 32_4_SRAM_ARRAY

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Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
32_4_SRAM_ARRAY	32_4_SRAM_ARRAY	42L, 42S	4L, 4S	42L, 42S

Cell 32_4_SRAM_ARRAY Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```
#####  
#          #  
#  CORRECT  #  
#          #  
#####
```

LAYOUT CELL NAME: 32_4_SRAM_ARRAY
SOURCE CELL NAME: 32_4_SRAM_ARRAY

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	42	42	
Nets:	298	298	
Instances:	512	512	MN (4 pins)
	256	256	MP (4 pins)
Total Inst:	768	768	

NUMBERS OF OBJECTS AFTER TRANSFORMATION