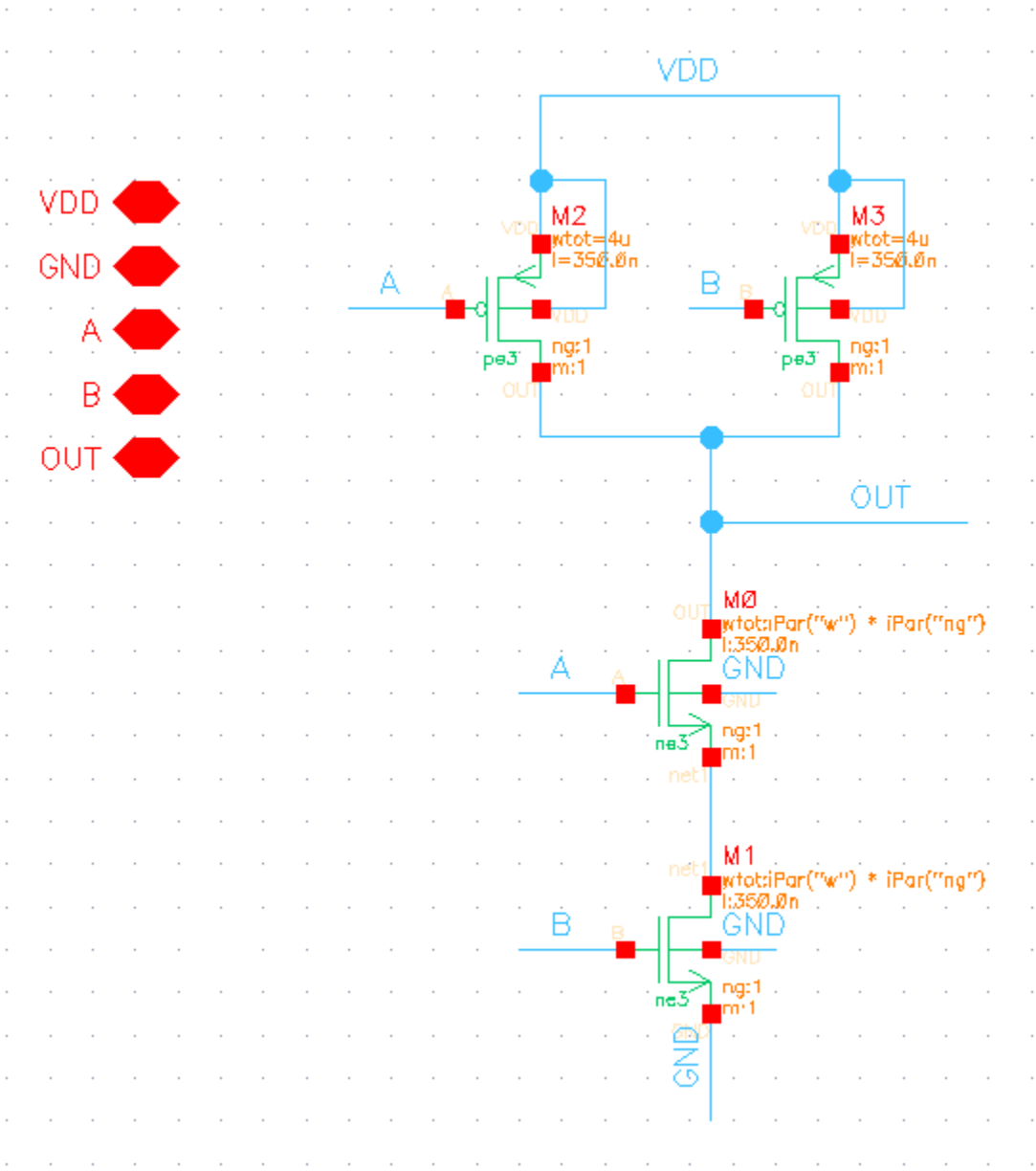
Aireen Amir Jalal - 010989584
HW 01

Q1. Implement NAND2 gate in schematic and layout. Give me screenshots of schematic, layout, DRC, and LVS.

Schematic:



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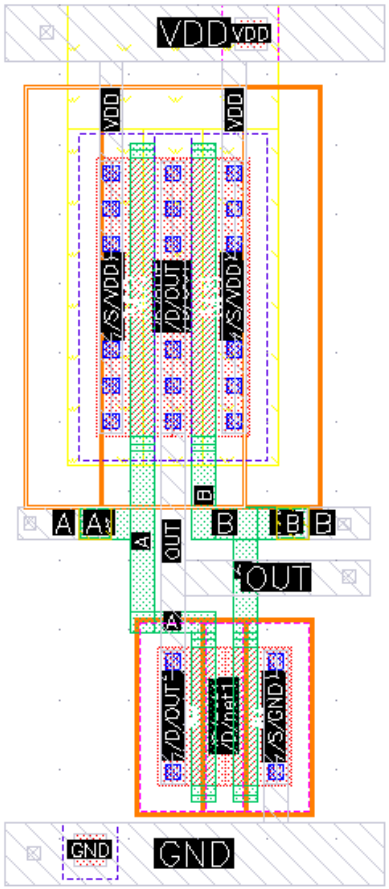
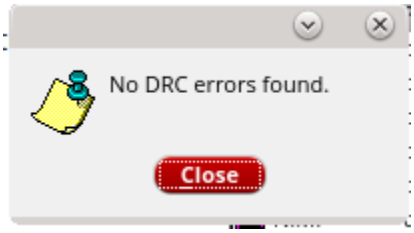
Layout:



DRC:



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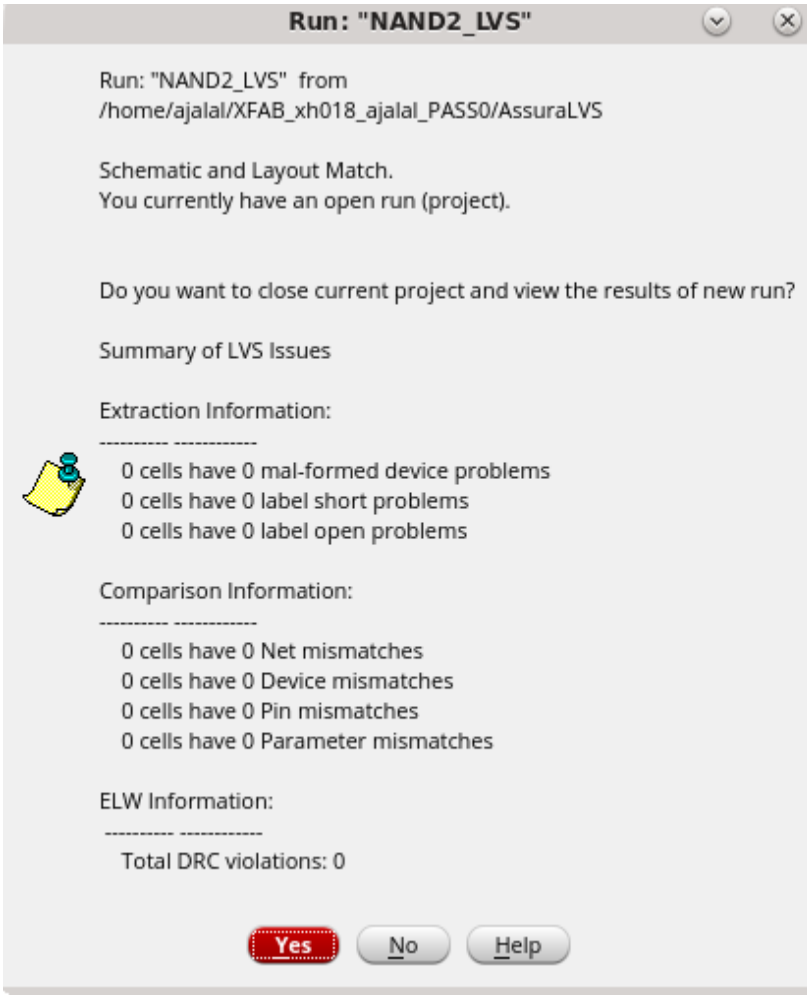
LVS:



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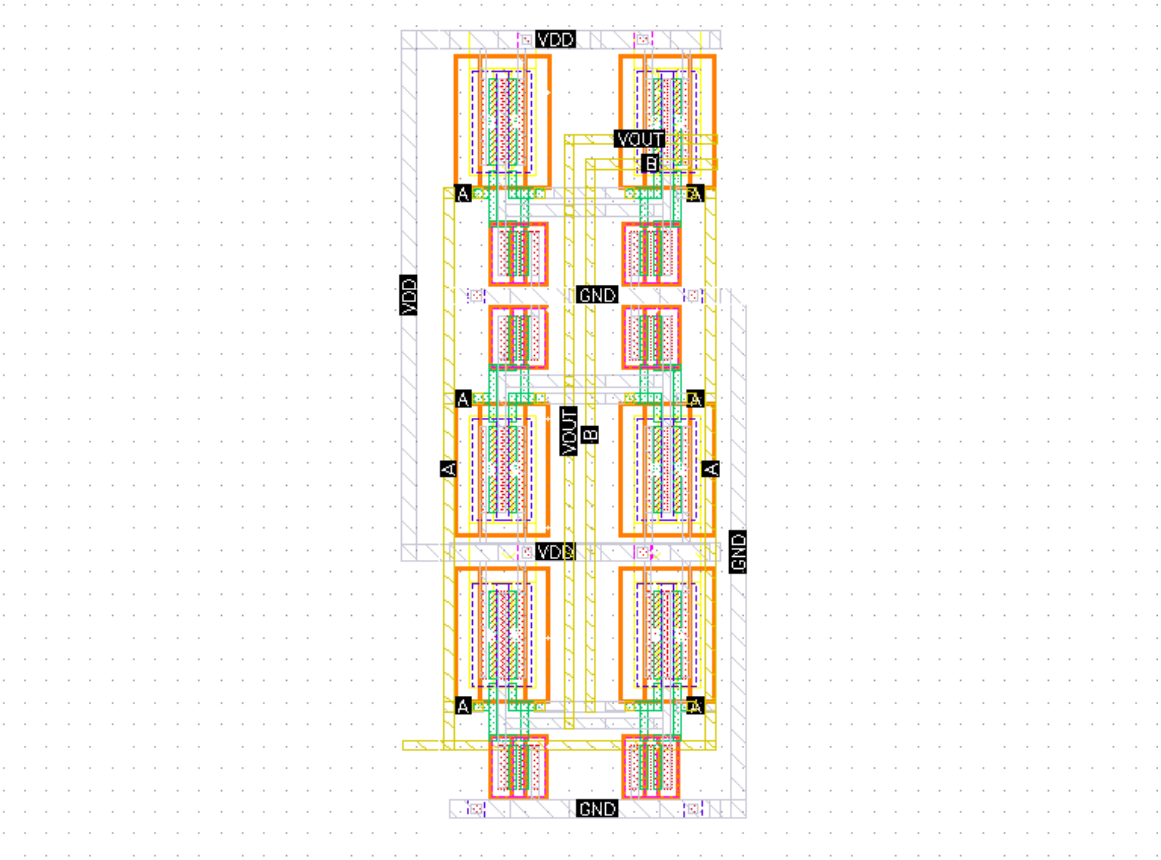
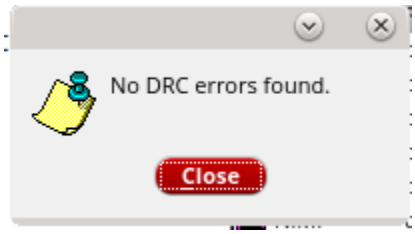
Q2. Implement 3x2 array of NAND2 gates in layout with horizontal and vertical buses at the minimum pitch for both. Give me screenshots of layout and DRC.Implement 3x2 array of NAND2 gates in layout with horizontal and vertical buses at the minimum pitch for both. Give me screenshots of layout and DRC.

Layout:



DRC:



LVS: I was not able to complete LVS as mantooth's server kept on crashing.

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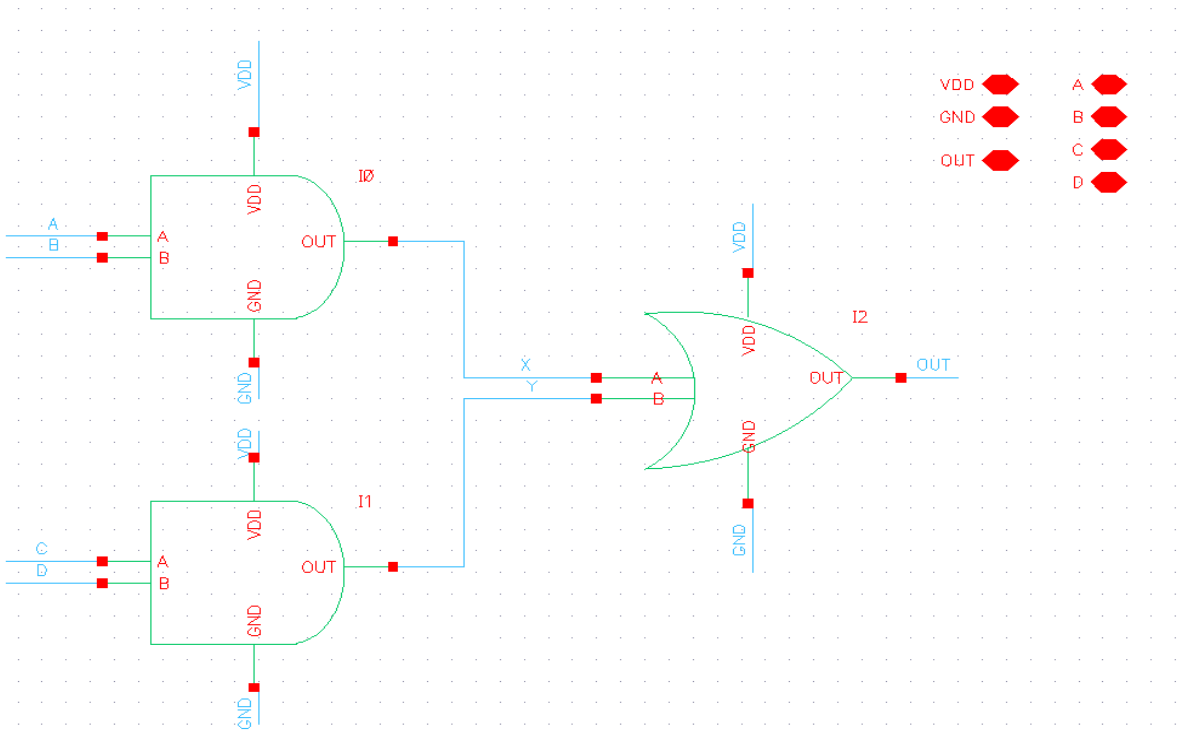
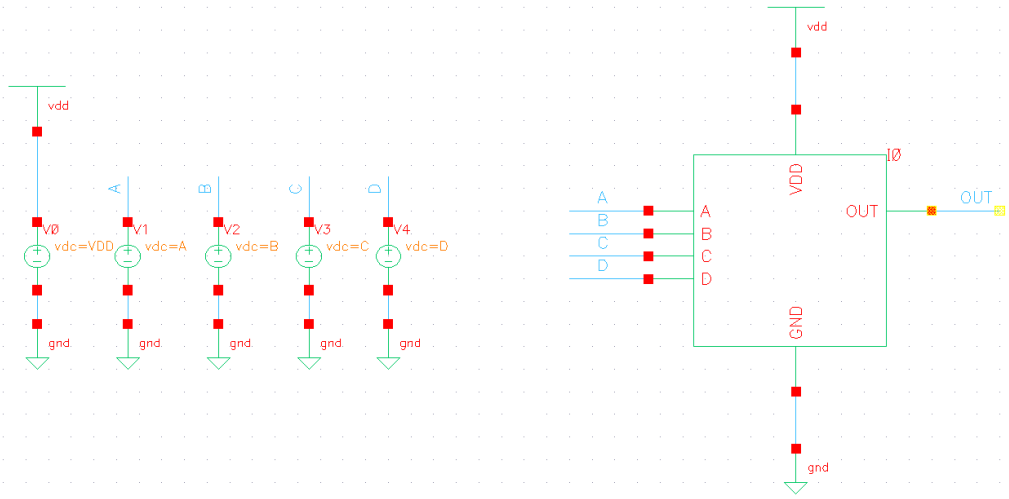
Q3. Implement the function: AB + CD. Give me screenshots of the schematic, layout, DRC, LVS, testbench, and simulation (test all possible scenarios).

Schematic:



Testbench:



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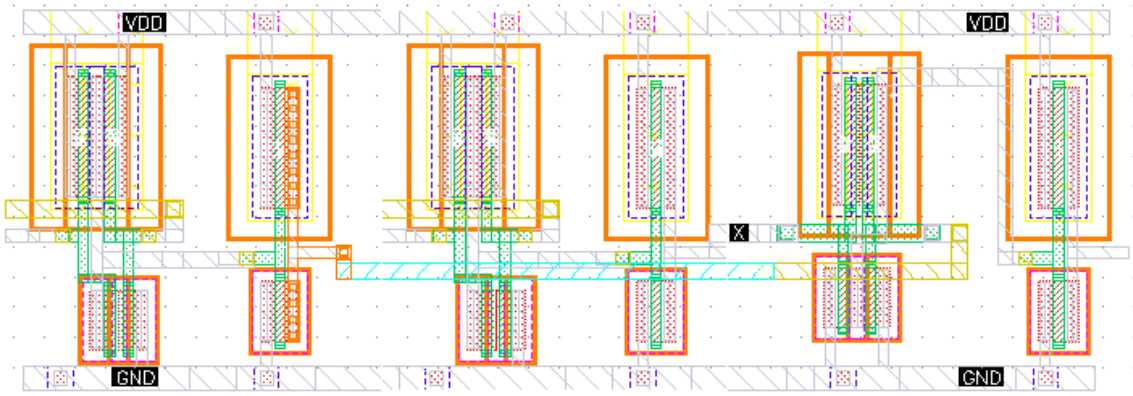
Layout:



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Simulation Results:

	A	B	C	D	Z
CASE 1	0	0	0	0	0
CASE 2	0	0	0	1	0
CASE 3	0	0	1	0	0
CASE 4	0	0	1	1	1
CASE 5	0	1	0	0	0
CASE 6	0	1	0	1	0
CASE 7	0	1	1	0	0
CASE 8	0	1	1	1	1
CASE 9	1	0	0	0	0
CASE 10	1	0	0	1	0
CASE 11	1	0	1	0	0
CASE 12	1	0	1	1	1
CASE 13	1	1	0	0	1
CASE 14	1	1	0	1	1
CASE 15	1	1	1	0	1
CASE 16	1	1	1	1	1

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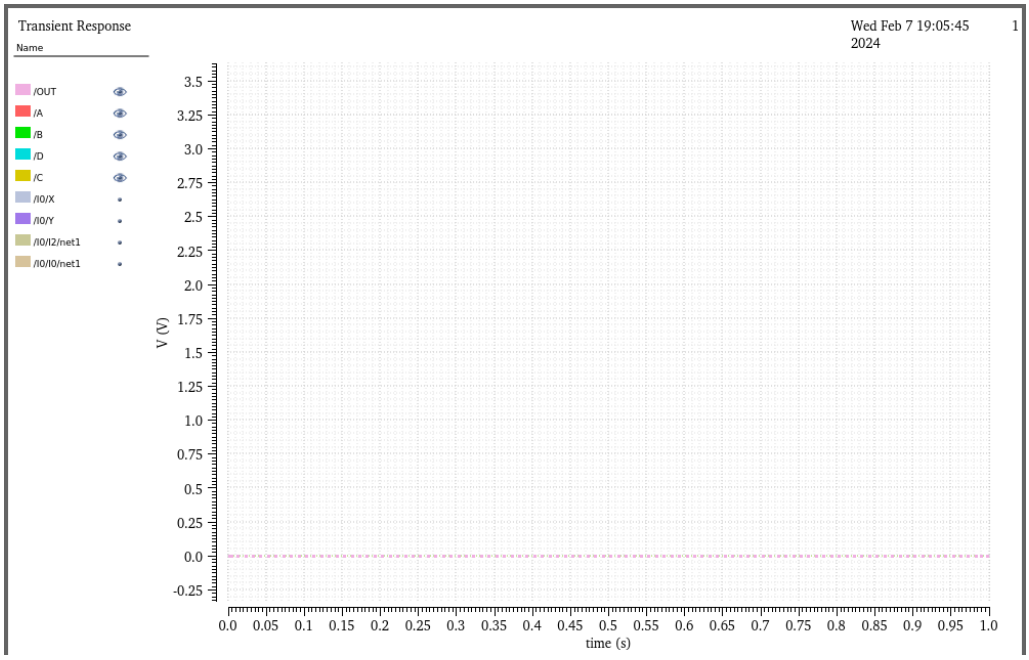
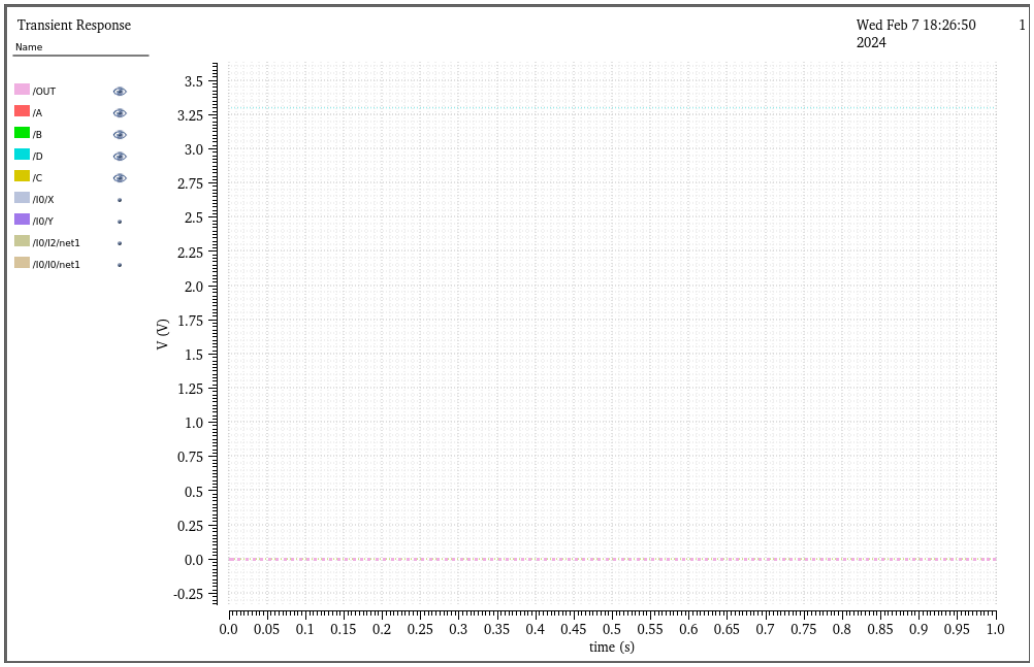
CASE 1:



CASE 2:



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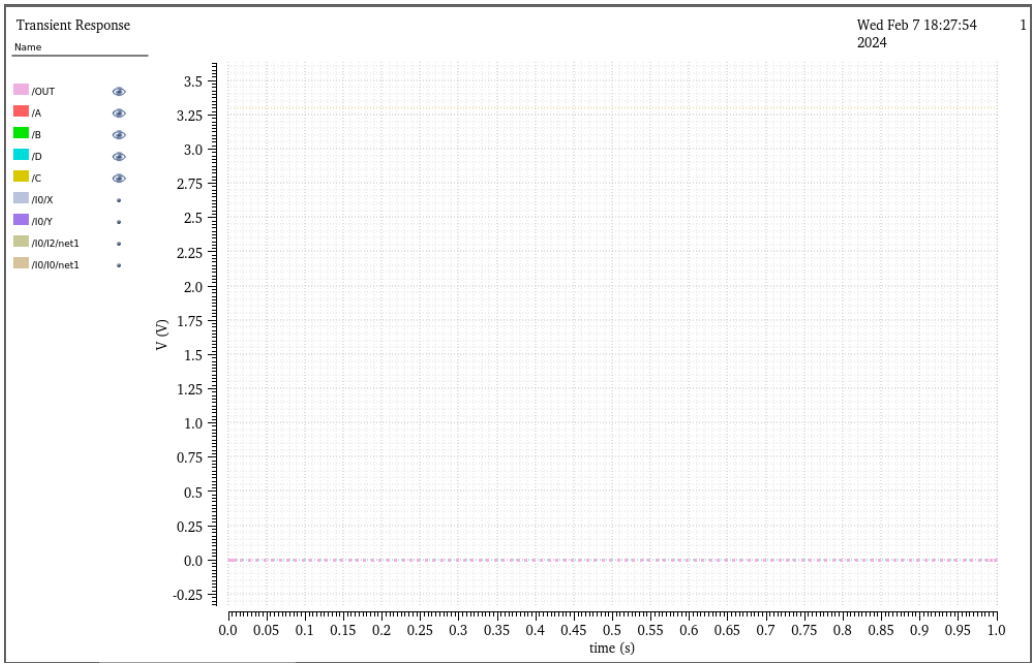
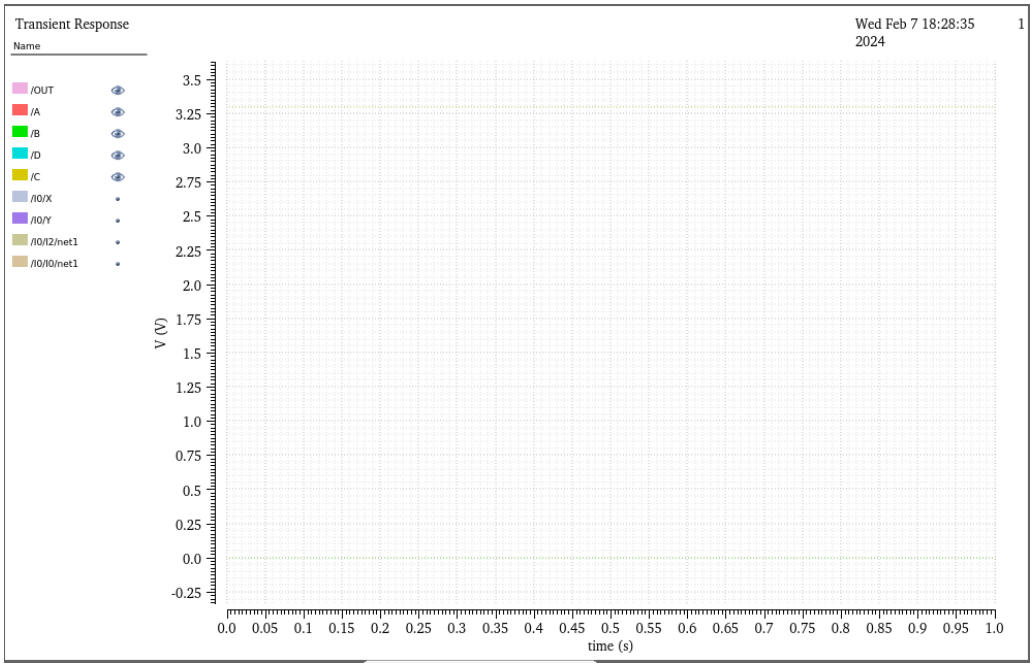
CASE 3:



CASE 4:



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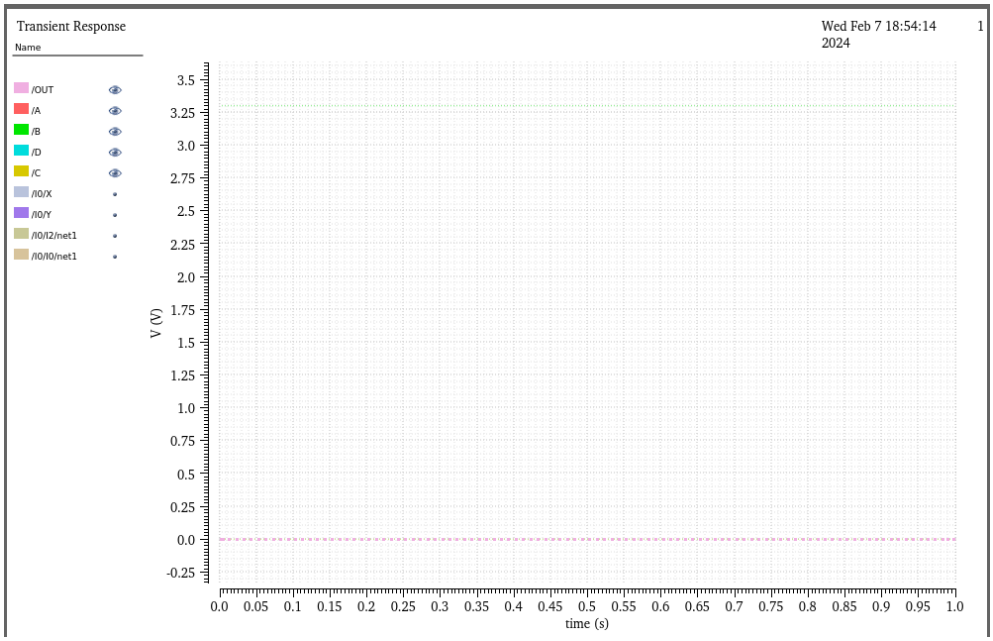
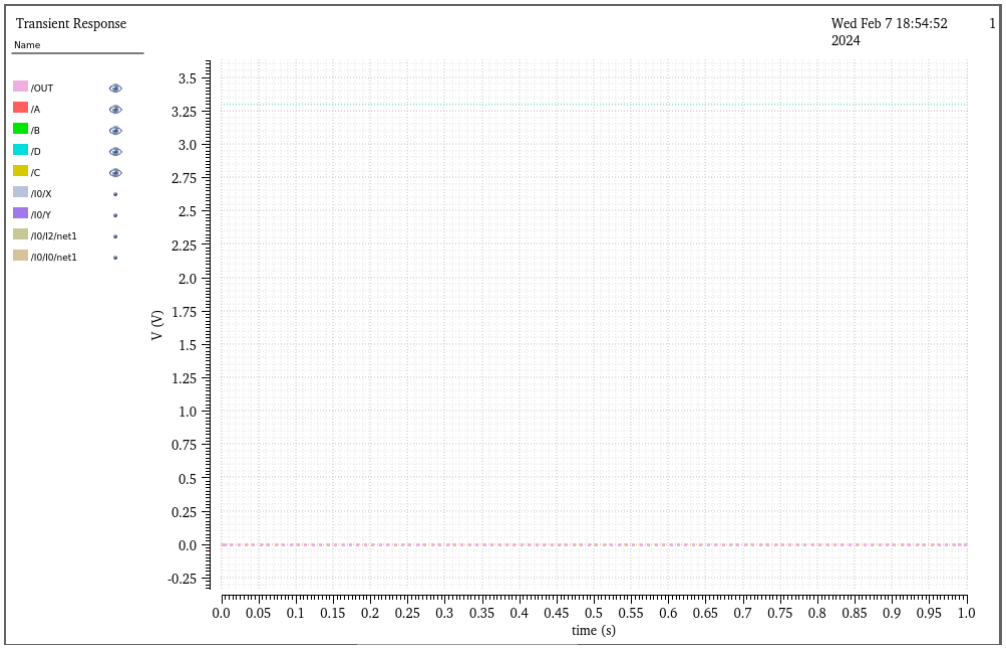
CASE 5:



CASE 6:



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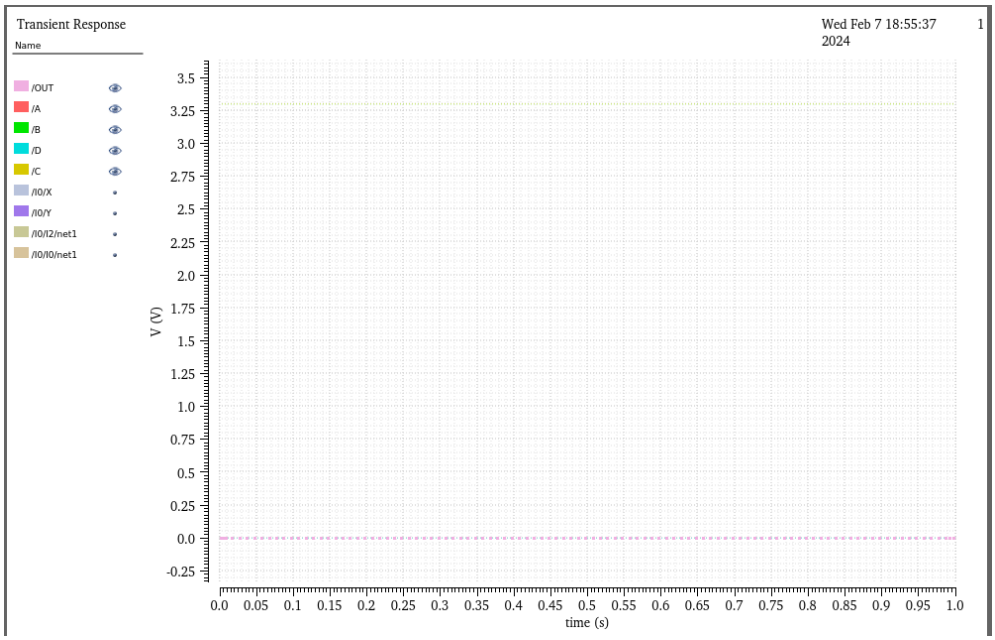
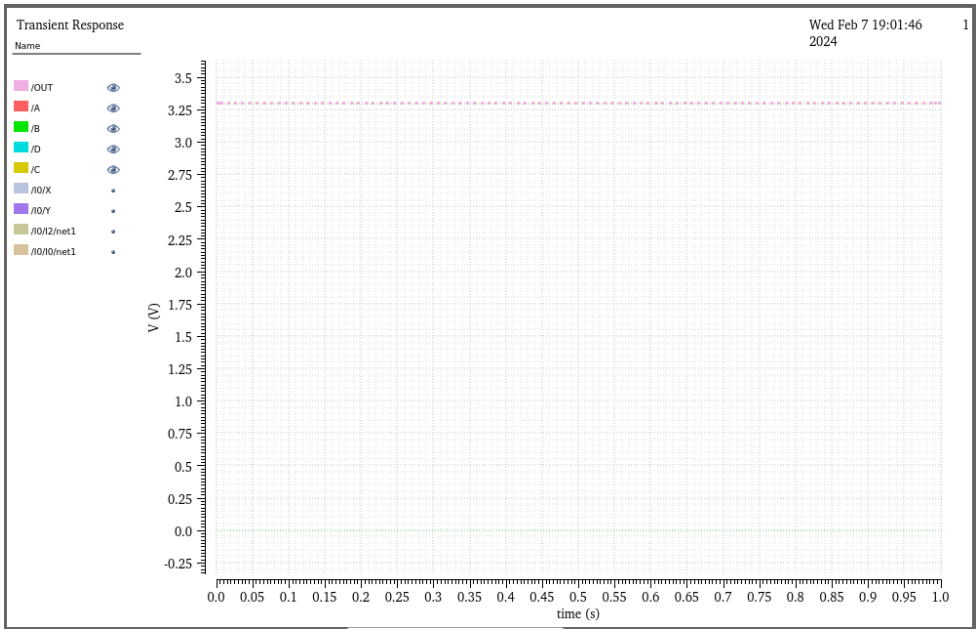
CASE 7:



CASE 8:



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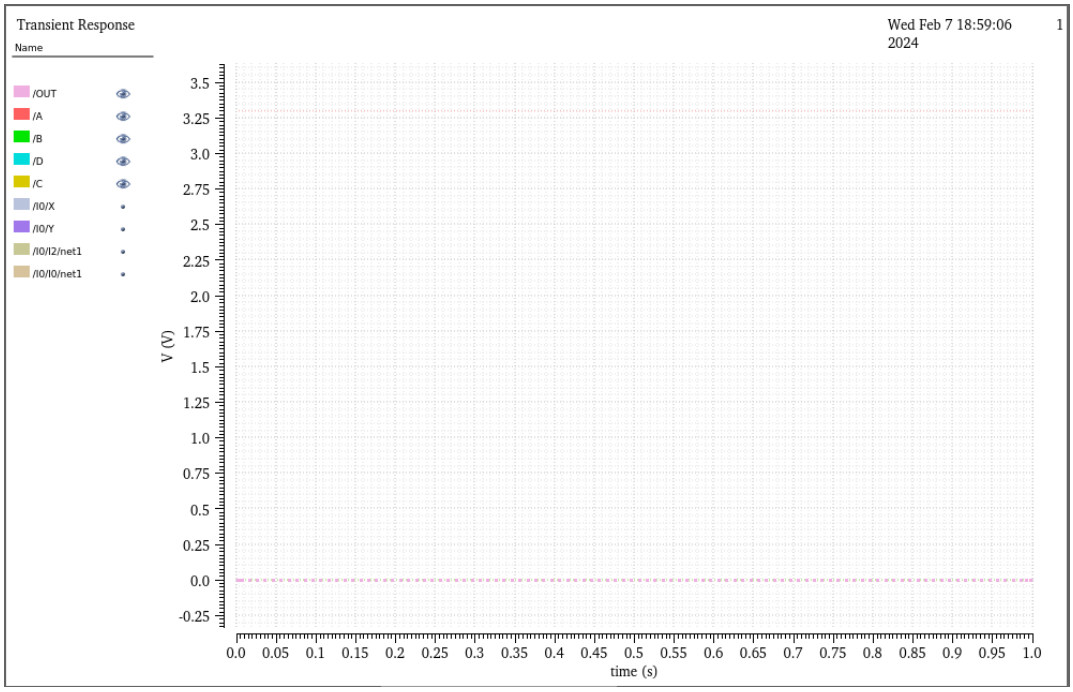
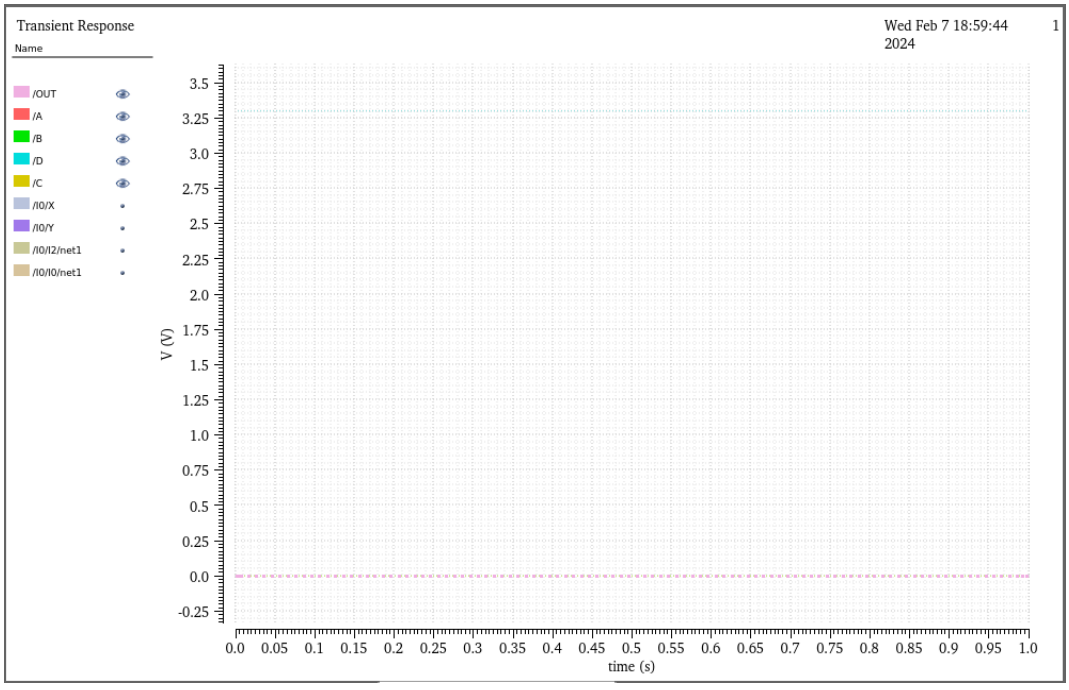
CASE 9:



CASE 10:



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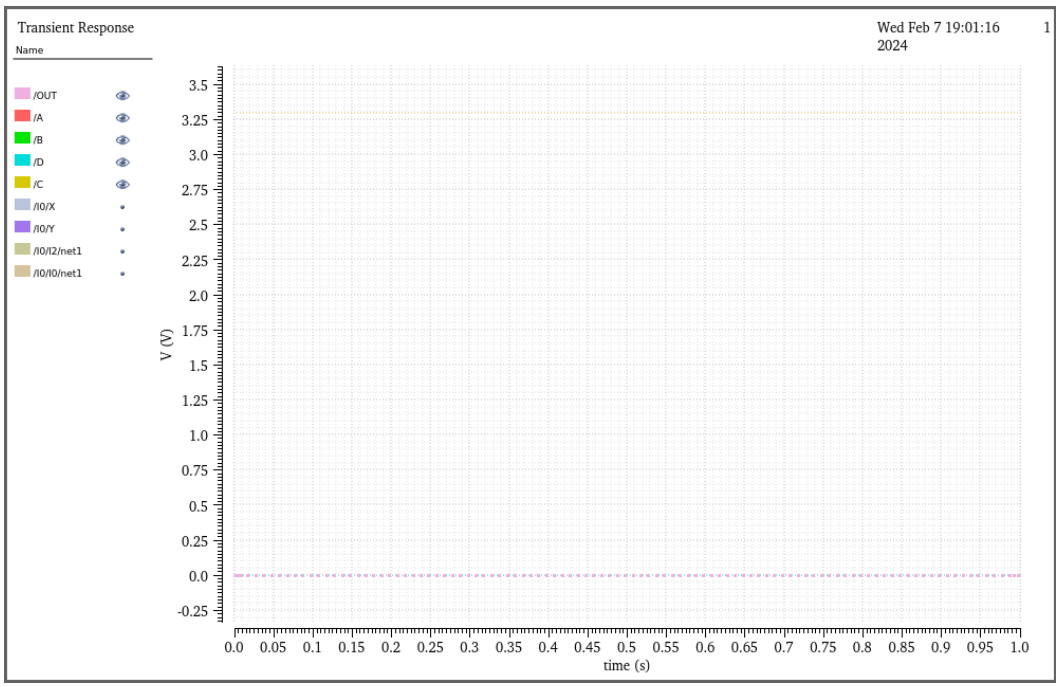
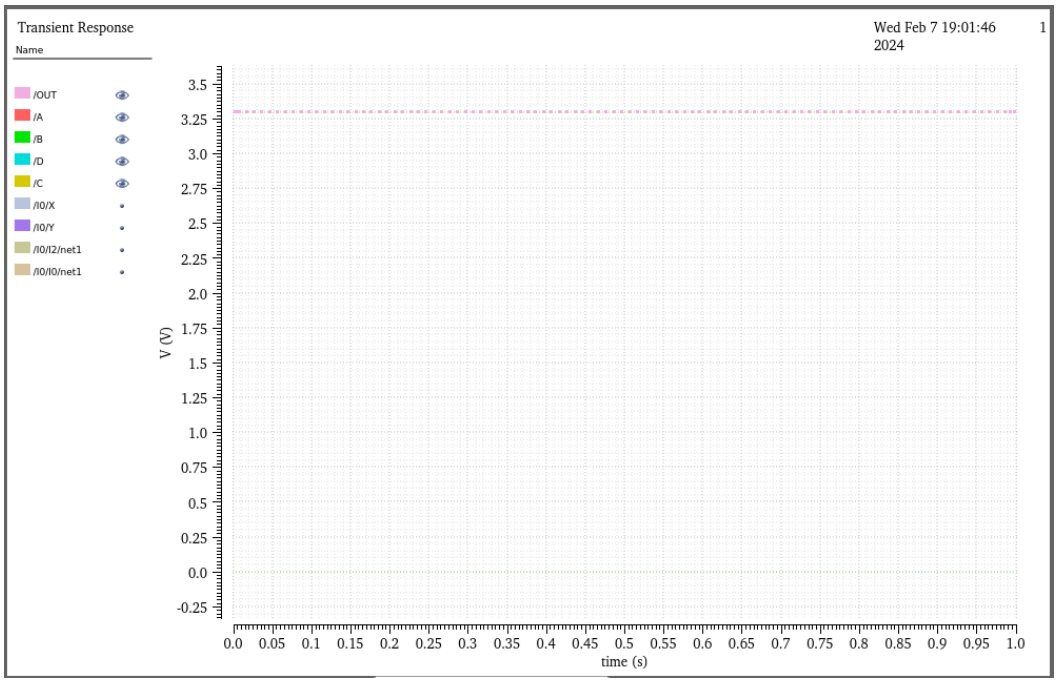
CASE 11:



CASE 12:



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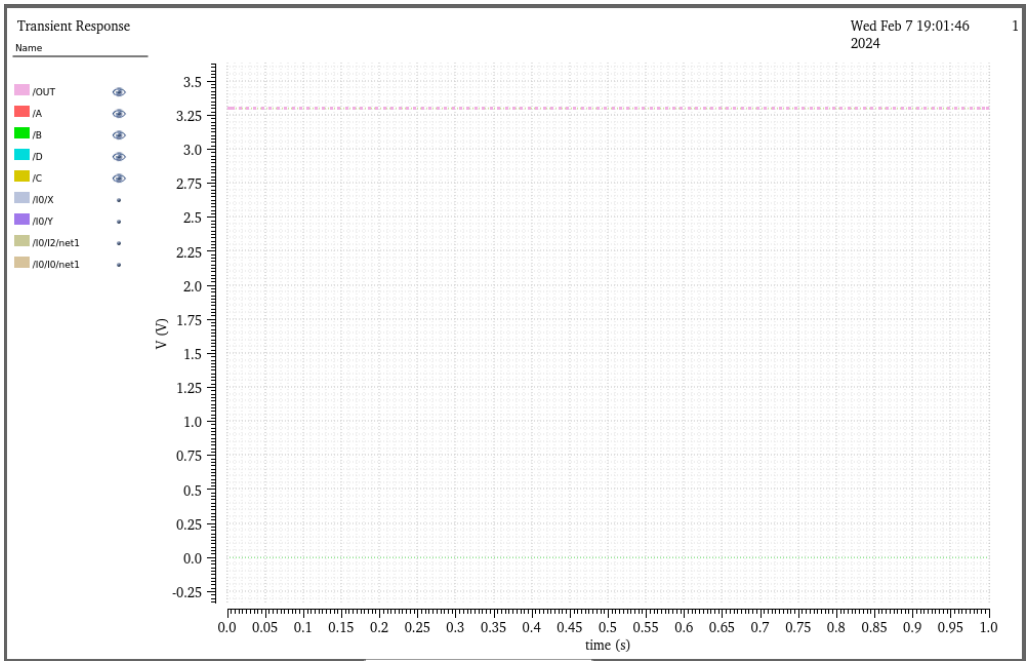
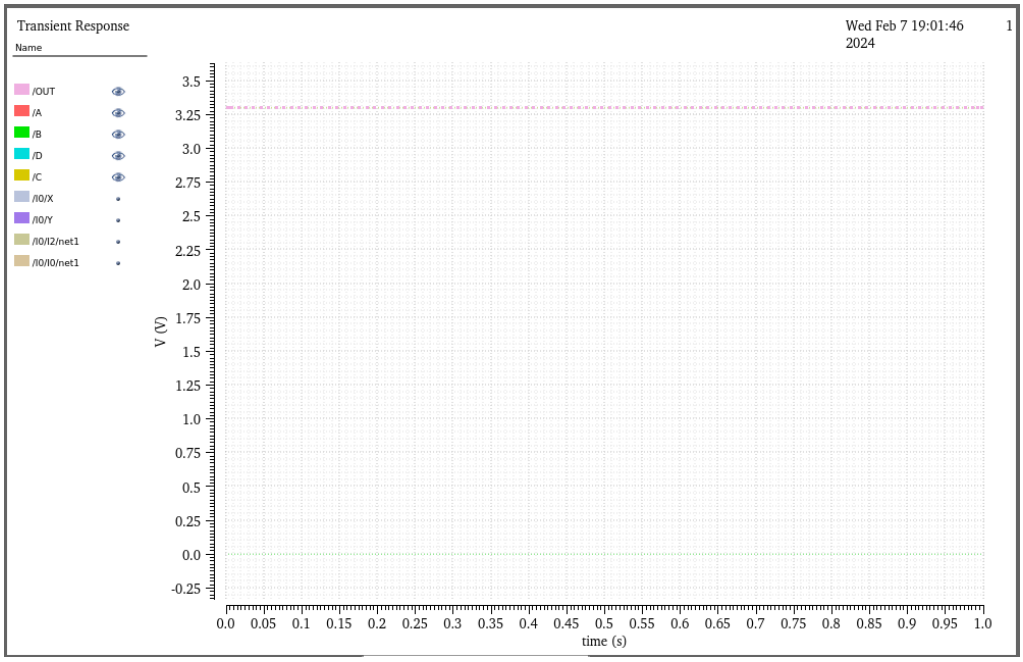
CASE 13:



CASE 14:



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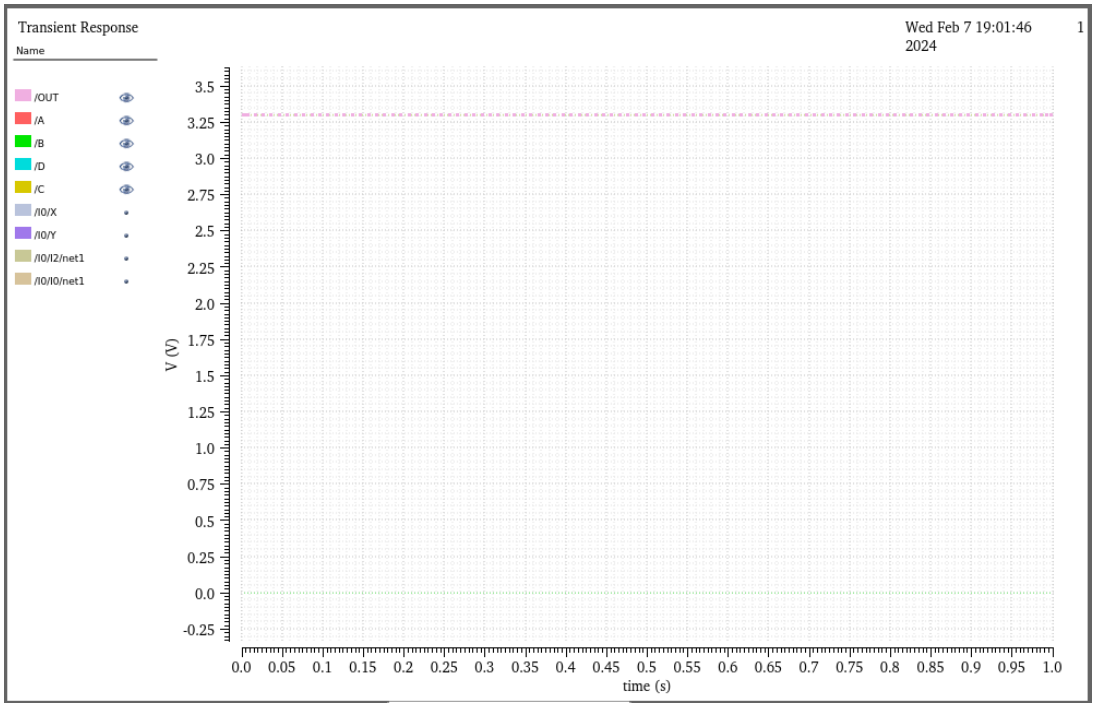
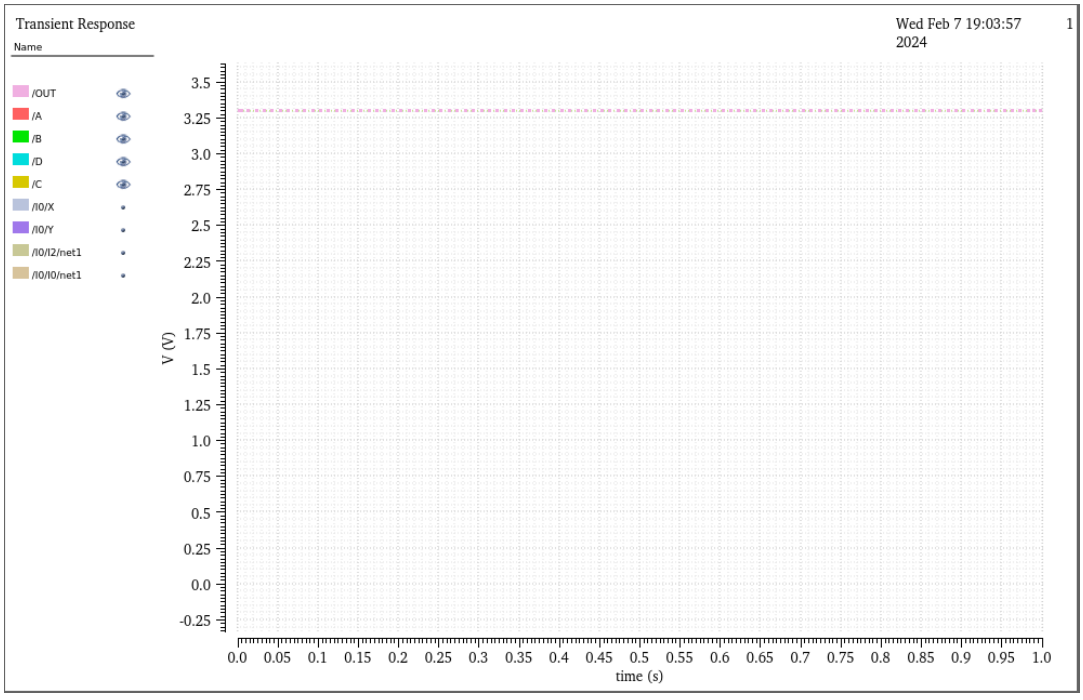
CASE 15:



CASE 16:



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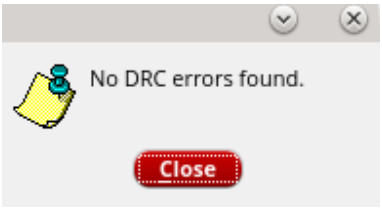
DRC:



LVS: