CIII51016-2.2

This chapter describes the configuration, design security, and remote system upgrades in Cyclone® III devices. The Cyclone III device family (Cyclone III and Cyclone III LS devices) uses SRAM cells to store configuration data. Configuration data must be downloaded to Cyclone III device family each time the device powers up because SRAM memory is volatile.

The Cyclone III device family is configured using one of the following configuration schemes:

- Fast Active serial (AS)

- Active parallel (AP) for Cyclone III devices only

- Passive serial (PS)

- Fast passive parallel (FPP)

- Joint Test Action Group (JTAG)

All configuration schemes use an external configuration controller (for example, MAX® II devices or a microprocessor), a configuration device, or a download cable.

The Cyclone III device family offers the following configuration features:

- Configuration data decompression

- Design security (for Cyclone III LS devices only)

- Remote system upgrade

As Cyclone III LS devices play a role in larger and more critical designs in competitive commercial and military environments, it is increasingly important to protect your designs from copying, reverse engineering, and tampering. Cyclone III LS devices address these concerns with 256-bit advanced encryption standard (AES) programming file encryption and anti-tamper feature support to prevent tampering. For more information about the design security feature in Cyclone III LS devices, refer to "Design Security" on page 9–70.

System designers face difficult challenges such as shortened design cycles, evolving standards, and system deployments in remote locations. The Cyclone III device family helps overcome these challenges with inherent re-programmability and dedicated circuitry to perform remote system upgrades. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life. Remote system upgrades can also be implemented with the advanced Cyclone III device family features such as real-time decompression of configuration data. For more information about the remote system upgrade feature in Cyclone III device family, refer to "Remote System Upgrade" on page 9–74.

Subscribe

This chapter describes the Cyclone III device family configuration features and describes how to configure Cyclone III device family using the supported configuration schemes. This chapter also includes configuration pin descriptions and the Cyclone III device family configuration file formats. In this chapter, the generic term "device" includes all Cyclone III device family.

This chapter contains the following sections:

■ "Configuration Features" on page 9–2

■ "Design Security" on page 9–70

■ "Remote System Upgrade" on page 9–74

Configuration Features

Cyclone III device family offers configuration data decompression to reduce configuration file storage, provides design security feature to protect your configuration data (for Cyclone III LS devices only), and provides remote system upgrade to allow you to remotely update your Cyclone III device family designs.

Table 9–1 lists which configuration methods you can use in each configuration scheme.

Table 9–1. Cyclone III Device Family Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade *(1)*	Design Security (Cyclone III LS Devices Only)
Fast Active Serial Standard (AS Standard POR)	Serial Configuration Device	✓	✓	✓
Fast Active Serial Fast (AS Fast POR)	Serial Configuration Device	✓	✓	✓
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	Supported Flash Memory *(2)*	—	✓	—
Active Parallel ×16 Fast (AP Fast POR, for Cyclone III devices only)	Supported Flash Memory *(2)*	—	✓	—
Passive Serial Standard (PS Standard POR)	External Host with Flash Memory	✓	—	✓
Passive Serial Standard (PS Standard POR)	Download Cable	✓	—	✓ *(3)*
Passive Serial Fast (PS Fast POR)	External Host with Flash Memory	✓	—	✓
Passive Serial Fast (PS Fast POR)	Download Cable	✓	—	✓ *(3)*
Fast Passive Parallel Fast (FPP Fast POR)	External Host with Flash Memory	—	—	✓

Table 9–1. Cyclone III Device Family Configuration Features (Part 2 of 2)

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade *(1)*	Design Security (Cyclone III LS Devices Only)
JTAG based configuration	External Host with Flash Memory	—	—	—
	Download Cable	—	—	—

Notes to Table 9–1:

(1) Remote update mode is supported when using the remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus® II software. For more information about the remote system upgrade feature, refer to "Remote System Upgrade" on page 9–74.

(2) For more information about the supported families for the Micron commodity parallel flash, refer to Table 9–11 on page 9–24.

(3) The design security feature is not supported using a SRAM Object File (**.sof**).

☞ The design security feature is for Cyclone III LS devices only and is available in all configuration schemes except the JTAG-based configuration. The decompression feature is not supported when you have enabled the design security feature.

☞ When using a serial configuration scheme such as PS or fast AS, the configuration time is the same whether or not you have enabled the design security feature. A ×4 DCLK is required if you use the FPP scheme with the design security feature.

☞ Cyclone III devices support remote system upgrade in AS and AP configuration schemes. Cyclone III LS devices only support remote system upgrade in the AS configuration scheme.

This section only describes the decompression feature. For more information about the design security and remote system upgrade, refer to "Design Security" on page 9–70 and "Remote System Upgrade" on page 9–74.

Configuration Data Decompression

Cyclone III device family supports configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to Cyclone III device family. During configuration, Cyclone III device family decompress the bitstream in real time and program SRAM cells. The decompression feature is not supported when you have enabled the design security feature.

☞ Compression may reduce the configuration bitstream size by 35 to 55%.

Cyclone III device family supports decompression in the AS and PS configuration schemes. Decompression is not supported in the AP, FPP, or JTAG-based configuration schemes. In PS mode, use the Cyclone III device family decompression feature to reduce configuration time.

☞ Altera recommends using the Cyclone III device family decompression feature during AS configuration if you must save configuration memory space in the serial configuration device.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time needed to send the bitstream to the Cyclone III device family. The time needed by a Cyclone III device family to decompress a configuration file is less than the time needed to send the configuration data to the device. There are two methods for enabling compression for Cyclone III device family bitstreams in the Quartus II software:

■ Before design compilation (using the Compiler Settings menu).

■ After design compilation (use the **Convert Programming Files** dialog box).

To enable compression in the compiler settings of the project in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.

2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.

3. Click the **Configuration** tab.

4. Turn on **Generate compressed bitstreams** (Figure 9–1).

5. Click **OK**.

6. In the **Settings** dialog box, click **OK**.

Figure 9–1. Enabling Compression for Cyclone III Device Family Bitstreams in Compiler Settings
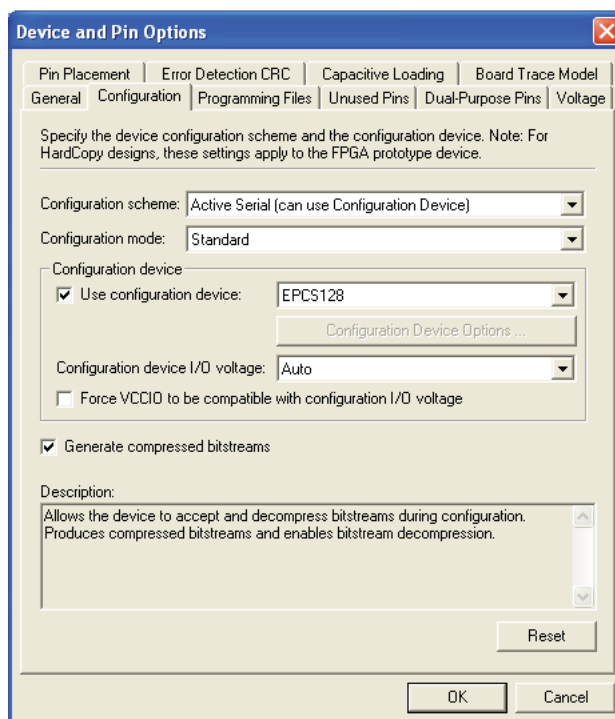

To enable compression when creating programming files from the **Convert Programming Files** window, follow these steps:

1. On the File menu, click **Convert Programming Files**.

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Configuration Features

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2. Under **Output programming file**, from the pull-down menu, select your desired file type.

3. If you select the Programmer Object File (**.pof**), you must specify a configuration device, directly under the file type.

4. In the **Input files to convert** box, select **SOF Data**.

5. Click **Add File** to browse to the Cyclone III device family **.sof**s.

6. In the **Convert Programming Files** dialog box, select the **.pof** you added to **SOF Data** and click **Properties**.

7. In the **SOF File Properties** dialog box, turn on the **Compression** option.

When multiple devices in Cyclone III device family are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 9–2 shows a chain of two devices in Cyclone III device family. The first device has compression enabled and receives compressed bitstream from the configuration device. The second device has the compression feature disabled and receives uncompressed data. You can generate programming files for this setup from the **Convert Programming Files** dialog box from the File menu in the Quartus II software.

Figure 9–2. Compressed and Uncompressed Configuration Data in the Same Configuration File
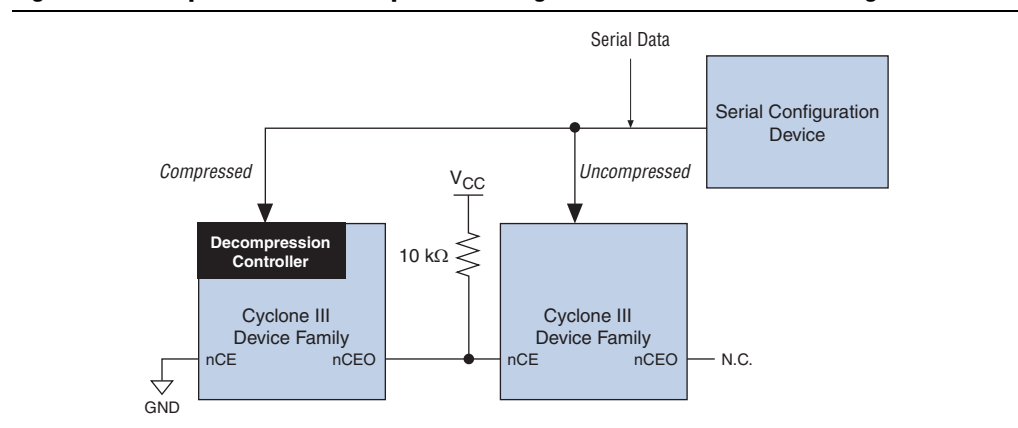
Configuration Requirement

The following section describes power-on-reset (POR) for Cyclone III device family.

POR Circuit

The POR circuit keeps the device in the reset state until the power supply voltage levels have stabilized after device power-up. After device power-up, the device does not release nSTATUS until the required voltages listed in table Table 9–4 on page 9–8 are above the POR trip point of the device. V_{CCINT} and V_{CCA} are monitored for brown-out conditions after device power-up.

☞ V_{CCA} is the analog power to the phase-locked loop (PLL).

In Cyclone III device family, you can select either a fast POR time or standard POR time depending on the MSEL pin settings. The fast POR time is 3 ms < TPOR < 9 ms for the fast configuration time. The standard POR time is 50 ms < TPOR < 200 ms, which has a lower power-ramp rate.

Table 9–2 lists the supported POR times for each configuration scheme.

Table 9–2. Cyclone III Device Family Supported POR Times Across Configuration Schemes [1]

Configuration Scheme	Fast POR Time (3 ms< TPOR < 9 ms)	Standard POR Time (50 ms< TPOR < 200 ms)	Configuration Voltage Standard (V) [2]
Fast Active Serial Standard (AS Standard POR)	—	✓	3.3
Fast Active Serial Standard (AS Standard POR)	—	✓	3.0/2.5
Fast Active Serial Fast (AS Fast POR)	✓	—	3.3
Fast Active Serial Fast (AS Fast POR)	✓	—	3.0/2.5
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	—	✓	3.3
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	—	✓	3.0/2.5
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	—	✓	1.8
Active Parallel ×16 Fast (AP Fast POR, for Cyclone III devices only)	✓	—	3.3
Active Parallel ×16 Fast (AP Fast POR, for Cyclone III devices only)	✓	—	1.8
Passive Serial Standard (PS Standard POR)	—	✓	3.3/3.0/2.5
Passive Serial Fast (PS Fast POR)	✓	—	3.3/3.0/2.5
Fast Passive Parallel Fast (FPP Fast POR)	✓	—	3.3/3.0/2.5
Fast Passive Parallel Fast (FPP Fast POR)	✓	—	1.8/1.5
JTAG-based configuration	[3]	[3]	—

Notes to Table 9–2:

(1) Altera recommends connecting the MSEL pins to V_{CCA} or GND depending on the MSEL pin settings.

(2) The configuration voltage standard is applied to the V_{CCIO} supply of the bank in which the configuration pins reside.

(3) JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored. However, the POR time is dependent on the MSEL pin settings.

In some applications, it is necessary for a device to wake up very quickly to begin operation. The Cyclone III device family offers the fast **POR time** option to support fast wake-up time applications. The **fast POR time** option has stricter power-up requirements when compared with the **standard POR time** option. You can select either the fast POR or standard POR options with the MSEL pin settings.

☞   The automotive application is for Cyclone III devices only. The Cyclone III devices fast wake-up time meets the requirement of common bus standards in automotive applications, such as Media Orientated Systems Transport (MOST) and Controller Area Network (CAN).

👉   For more information about wake-up time and the POR circuit, refer to the *Hot-Socketing and Power-On Reset in Cyclone III Devices* chapter.

Configuration File Size

Table 9–3 lists the uncompressed configuration file sizes for the Cyclone III device family. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 9–3. Cyclone III Device Family Uncompressed Raw Binary File (.rbf) Sizes

Device		Data Size (bits)
Cyclone III	EP3C5	3,000,000
	EP3C10	3,000,000
	EP3C16	4,100,000
	EP3C25	5,800,000
	EP3C40	9,600,000
	EP3C55	14,900,000
	EP3C80	20,000,000
	EP3C120	28,600,000
Cyclone III LS	EP3CLS70	26,766,760
	EP3CLS100	26,766,760
	EP3CLS150	50,610,728
	EP3CLS200	50,610,728

Use the data in Table 9–3 only to estimate the file size before design compilation. Different configuration file formats, such as Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) formats, have different file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size varies after each compilation because the compression ratio is design dependent.

For more information about setting device configuration options or creating configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

Configuration and JTAG Pin I/O Requirements

Cyclone III devices are manufactured using the TSMC 65-nm low-k dielectric process; Cyclone III LS devices are manufactured using the TSMC 60-nm low-k dielectric process. Although Cyclone III device family uses TSMC 2.5-V transistor technology in the I/O buffers, the devices are compatible and able to interface with 2.5-, 3.0-, 3.3-V configuration voltage standards. However, you must follow specific requirements when interfacing Cyclone III device family with 2.5-, 3.0-, 3.3-V configuration voltage standards.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. When using a JTAG configuration scheme or a serial configuration device in an AS configuration scheme, you must connect a 25-Ω series resistor at the near end of the TDO and TDI pin or the serial configuration device for the DATA[0] pin. When cascading Cyclone III device family in a multi-device configuration, you must connect the repeater buffers between the master and slave devices for DATA and DCLK.

The output resistance of the repeater buffers must fit the maximum overshoot equation shown in Equation 9–1:

Equation 9–1. [1]

$$0.8Z_O \le R_E \le 1.8Z_O$$

Note to Equation 9–1:

(1) Z_0 is the transmission line impedance and R_E is the equivalent resistance of the output buffer.

Configuration Process

This section describes the configuration process.

For more information about the configuration cycle state machine of Altera® FPGAs, refer to the *Configuring Altera FPGAs* chapter in volume 1 of the *Configuration Handbook.*

Power Up

If the device is powered up from the power-down state, the V_{CCIO} for all the I/O banks must be powered up to the appropriate level for the device to exit POR.

To begin configuration, the required voltages listed in Table 9–4 must be powered up to the appropriate voltage levels.

Table 9–4. **Power-Up Voltage for Cyclone III Device Family Configuration**

Device	Voltage that must be Powered-Up [1]
Cyclone III	V_{CCINT}, V_{CCA}, V_{CCIO} [2]
Cyclone III LS	V_{CCBAT}, V_{CCINT}, V_{CCA}, V_{CCIO} [2]

Notes to Table 9–4:

(1) Voltages must be powered up to the appropriate voltage levels to begin configuration.

(2) V_{CCIO} is for banks in which the configuration and JTAG pins reside.

Reset

When nCONFIG or nSTATUS is low, the device is in reset. After power-up, the Cyclone III device family goes through POR. POR delay depends on the MSEL pin settings, which correspond to your configuration scheme.

Depending on the configuration scheme, a fast or standard POR time is available. POR time for fast POR ranges between 3–9 ms. POR time for standard POR, which has a lower power-ramp rate, ranges between 50–200 ms.

During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins.

☞   The configuration bus is not tri-stated in POR stage if the MSEL pins are set to AS or AP mode. To tri-state the configuration bus for AS and AP configuration schemes, you must tie nCE high and nCONFIG low. For more information about the hardware implementation, refer to "Configuring With Multiple Bus Masters" on page 9–30.

When the device exits POR, all user I/O pins continue to tri-state. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors that are always enabled (after POR) before and during configuration. After POR, the Cyclone III device family releases nSTATUS, which is pulled high by an external 10-kΩ pull-up resistor and enters configuration mode.

When nCONFIG goes high, the device exits reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. After nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins.

Cyclone III LS devices are accessible by limited JTAG instructions after POR. For more information about enabling full JTAG instructions access, refer to "JTAG Instructions" on page 9–60.

For more information about the value of weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

Configuration

Configuration data is latched into the Cyclone III device family at each DCLK cycle. However, the width of the data bus and the configuration time taken for each scheme are different. After the device receives all the configuration data, the device releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ pull-up resistor. A low-to-high transition on the CONF_DONE pin indicates that configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-kΩ pull-up resistor for the device to initialize.

You can begin reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin must be low for at least 500 ns. When nCONFIG is pulled low, the Cyclone III device family is reset. The Cyclone III device family also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic-high level and nSTATUS is released by the Cyclone III device family, reconfiguration begins.

Configuration Error

If an error occurs during configuration, the Cyclone III device family asserts the nSTATUS signal low, indicating a data frame error, and the CONF_DONE signal stays low. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box) is turned on, the Cyclone III device family releases nSTATUS after a reset time-out period (a maximum of 230 µs), and retries configuration. If this option is turned off, the system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 500 ns to restart configuration.

Initialization

In Cyclone III device family, the clock source for initialization is either a 10-MHz (typical) internal oscillator (separate from the AS internal oscillator) or an optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the device provides itself with enough clock cycles for a proper initialization. When using the internal oscillator, you do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. Additionally, you can use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the **CLKUSR** option. The CLKUSR pin allows you to control when your device enters user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. When you turn on the **Enable user supplied start-up clock option (CLKUSR)** option, the CLKUSR pin is the initialization clock source. Supplying a clock on the CLKUSR pin does not affect the configuration process. After the configuration data is accepted and CONF_DONE goes high, the Cyclone III device family requires a certain amount of clock cycles to initialize and to enter user mode.

Table 9–5 lists the required clock cycles for proper initialization in Cyclone III device family.

Table 9–5. Initialization Clock Cycles Required in Cyclone III Device Family

Device	Initialization Clock Cycles
Cyclone III	3,185
Cyclone III LS	3,192

Table 9–6 lists the maximum CLKUSR frequency (f_{MAX}) for Cyclone III device family.

Table 9–6. Maximum CLKUSR Frequency for Cyclone III Device Family

Device	f_{MAX} (MHz)
Cyclone III	133
Cyclone III LS	100

☞ If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure that the CLKUSR pin continues to toggle when nSTATUS is low (a maximum of 230 μs).

User Mode

An optional INIT_DONE pin is available that signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it is high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. After the option bit to enable INIT_DONE is programmed into the device

(during the first frame of configuration data), the `INIT_DONE` pin goes low. When initialization is complete, the `INIT_DONE` pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. In user mode, the user I/O pins function as assigned in your design and no longer have weak pull-up resistors.

Configuration Scheme

A configuration scheme with different configuration voltage standards is selected by driving the MSEL pins either high or low, as listed in Table 9–7.

The MSEL pins are powered by V_{CCINT}. The `MSEL[3..0]` pins have 9-kΩ internal pull-down resistors that are always active.

☞ Smaller Cyclone III devices or package options (E144, M164, Q240, F256, and U256 packages) do not have the `MSEL[3]` pin. The AS Fast POR configuration scheme at 3.0- or 2.5-V configuration voltage standard and the AP configuration scheme are not supported in Cyclone III devices without the `MSEL[3]` pin. To configure these devices with other supported configuration schemes, select the `MSEL[2..0]` pins according to the MSEL settings in Table 9–7.

☞ Hardwire the MSEL pins to V_{CCA} or GND without any pull-up or pull-down resistors to avoid any problems detecting an incorrect configuration scheme. Do not drive the MSEL pins with a microprocessor or another device.

☞ The Quartus II software prohibits you from using the LVDS I/O standard in I/O Bank 1 when the configuration device I/O voltage is not 2.5 V. If you need to assign LVDS I/O standard in I/O Bank 1, navigate to Assignments>Device>Settings>Device and Pin Option>Configuration to change the Configuration Device I/O voltage to **2.5 V** or **Auto**.

Table 9–7. Cyclone III Device Family Configuration Schemes [1] (Part 1 of 2)

Configuration Scheme	MSEL				Configuration Voltage Standard (V) [2], [3]
	3	2	1	0	
Fast Active Serial Standard (AS Standard POR)	0	0	1	0	3.3
Fast Active Serial Standard (AS Standard POR)	0	0	1	1	3.0/2.5
Fast Active Serial Fast (AS Fast POR)	1	1	0	1	3.3
Fast Active Serial Fast (AS Fast POR)	0	1	0	0	3.0/2.5
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	0	1	1	1	3.3
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	1	0	1	1	3.0/2.5
Active Parallel ×16 Standard (AP Standard POR, for Cyclone III devices only)	1	0	0	0	1.8
Active Parallel ×16 Fast (AP Fast POR, for Cyclone III devices only)	0	1	0	1	3.3

Table 9–7. Cyclone III Device Family Configuration Schemes [1] **(Part 2 of 2)**

Configuration Scheme	MSEL				Configuration Voltage Standard (V) [2], [3]
	3	**2**	**1**	**0**	
Active Parallel ×16 Fast (AP Fast POR, for Cyclone III devices only)	0	1	1	0	1.8
Passive Serial Standard (PS Standard POR)	0	0	0	0	3.3/3.0/2.5
Passive Serial Fast (PS Fast POR)	1	1	0	0	3.3/3.0/2.5
Fast Passive Parallel Fast (FPP Fast POR) [4]	1	1	1	0	3.3/3.0/2.5
Fast Passive Parallel Fast (FPP Fast POR) (for Cyclone III devices only) [4]	1	1	1	1	1.8/1.5
Fast Passive Parallel Fast (FPP Fast POR) (for Cyclone III LS devices only)	0	0	0	1	1.8/1.5
Fast Passive Parallel Fast (FPP Fast POR) with Encryption (for Cyclone III LS devices only)	0	1	0	1	3.3/3.0/2.5
Fast Passive Parallel Fast (FPP Fast POR) with Encryption (for Cyclone III LS devices only)	0	1	1	0	1.8/1.5
JTAG-based configuration [5]	[6]	[6]	[6]	[6]	—

Notes to Table 9–7:

(1) Altera recommends connecting the MSEL pins to V_{CCA} or GND depending on the MSEL pin settings.

(2) The configuration voltage standard is applied to the V_{CCIO} supply of the bank in which the configuration pins reside.

(3) You must follow specific requirements when interfacing Cyclone III device family with 2.5-, 3.0-, and 3.3-V configuration voltage standards. For more information about these requirements, refer to "Configuration and JTAG Pin I/O Requirements" on page 9–7.

(4) FPP configuration is not supported in the Cyclone III E144 device package of Cyclone III devices.

(5) The JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored.

(6) Do not leave the MSEL pins floating. Connect them to V_{CCA} or GND. These pins support the non-JTAG configuration scheme used in production. Altera recommends connecting the MSEL pins to GND if your device is only using the JTAG configuration.

AS Configuration (Serial Configuration Devices)

In the AS configuration scheme, Cyclone III device family is configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memories that feature a simple four-pin interface and a small form factor. These features make serial configuration devices the ideal low-cost configuration solution.

For more information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

In Cyclone III device family, the active master clock frequency runs at a maximum of 40 MHz, and typically at 30 MHz. Cyclone III device family only work with serial configuration devices that support up to 40 MHz.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone III device family reads configuration data using the serial interface, decompress data if necessary, and configure their SRAM cells. This scheme is referred to as the AS configuration scheme because the device controls the configuration interface.

☞ If you want to gain control of the EPCS pins, hold the nCONFIG pin low and pull the nCE pin high to cause the device to reset and tri-state the AS configuration pins.
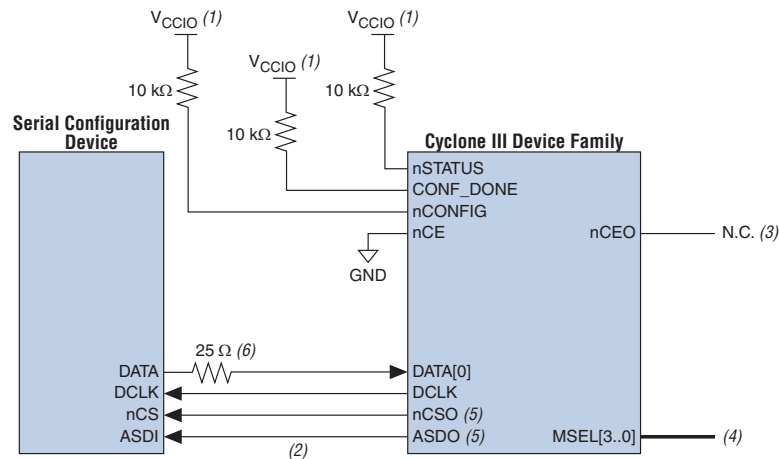
Single-Device AS Configuration

The four-pin interface of serial configuration devices consists of the following pins:

■ Serial clock input (DCLK)

■ Serial data output (DATA)

■ AS data input (ASDI)

■ Active-low chip select (nCS)

This four-pin interface connects to Cyclone III device family pins, as shown in Figure 9–3.

Figure 9–3. Single-Device AS Configuration

Notes to Figure 9–3:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Cyclone III device family uses the ASDO-to-ASDI path to control the configuration device.

(3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. The nCSO pin functions as the FLASH_NCE pin in AP mode. The ASDO pin functions as the DATA[1] pin in other AP and FPP modes.

(6) Connect the series resistor at the near end of the serial configuration device.

☞ To tri-state the configuration bus for AS configuration schemes, you must tie nCE high and nCONFIG low.

☞ When connecting a serial configuration device to a Cyclone III device family in the single-device AS configuration, you must connect a 25-Ω series resistor at the near end of the serial configuration device for DATA[0]. The 25-Ω resistor in the series works to minimize the driver impedance mismatch with the board trace and reduce overshoot seen at the Cyclone III device family DATA[0] input pin.

In a single-device AS configuration, the maximum board loading and board trace length between the supported serial configuration device and the Cyclone III device family must follow the recommendations in Table 9–9 on page 9–20.

The DCLK generated by the Cyclone III device family controls the entire configuration cycle and provides timing for the serial interface. Cyclone III device family uses a 40-MHz internal oscillator to generate DCLK. There are some variations in the internal oscillator frequency because of the process, voltage, and temperature conditions in Cyclone III device family. The internal oscillator is designed to ensure that its maximum frequency is guaranteed to meet the EPCS device specifications.

☞ EPCS1 does not support Cyclone III device family because of its insufficient memory capacity.

Table 9–8 lists the AS DCLK output frequency for Cyclone III device family.

Table 9–8. AS DCLK Output Frequency

Oscillator	Minimum	Typical	Maximum	Unit
40 MHz	20	30	40	MHz

In the AS configuration scheme, the serial configuration device latches input and control signals on the rising edge of DCLK and drives out configuration data on the falling edge. Cyclone III device family drives out control signals on the falling edge of DCLK and latch configuration data on the falling edge of DCLK.

In configuration mode, the Cyclone III device family enables the serial configuration device by driving the nCSO output pin low, which connects to the nCS pin of the configuration device. The Cyclone III device family uses the DCLK and DATA[1] pins to send operation commands and read address signals to the serial configuration device. The configuration device provides data on its DATA pin, which connects to the DATA[0] input of the Cyclone III device family.

After all the configuration bits are received by the Cyclone III device family, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ resistor. Initialization begins only after the CONF_DONE signal reaches a logic-high level. All AS configuration pins (DATA[0], DCLK, nCSO, and DATA[1]) have weak internal pull-up resistors that are always active. After configuration, these pins are set as input tri-stated and are driven high by weak internal pull-up resistors. The CONF_DONE pin must have an external 10-kΩ pull-up resistor for the device to initialize.

The timing parameters for AS mode are not listed here because the t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, t_{CF2ST1}, and t_{CD2UM} timing parameters are identical to the timing parameters for PS mode listed in Table 9–13 on page 9–39.

Multi-Device AS Configuration

You can configure multiple Cyclone III device family using a single serial configuration device. You can cascade multiple Cyclone III device family using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its V_CCIO level to help the internal weak pull-up resistor. When the first device captures all its configuration data from the bitstream, it drives the nCEO pin low,

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Configuration Features

9–15

enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone III device family. The nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA[0] pins of each device in the chain are connected (Figure 9–4).

Figure 9–4. Multi-device AS Configuration
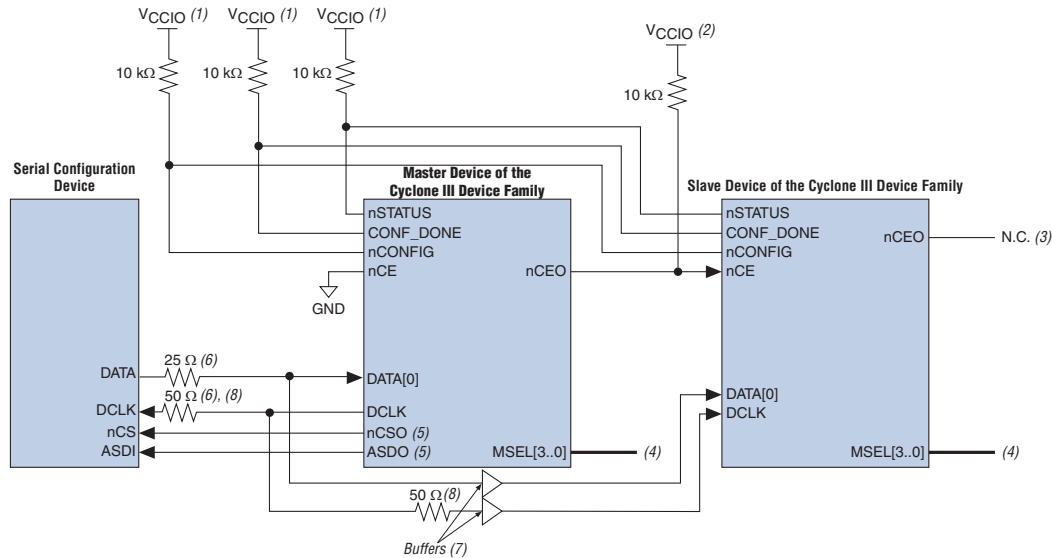
Notes to Figure 9–4:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.

(3) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed the nCE pin of another device.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device of the Cyclone III device family in AS mode and the slave devices in PS mode. To connect MSEL[3..0] for the master device in AS mode and slave devices in PS mode, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. The nCSO pin functions as the FLASH_NCE pin in AP mode. The ASDO pin functions as the DATA[1] pin in other AP and FPP modes.

(6) Connect the series resistor at the near end of the serial configuration device.

(7) Connect the repeater buffers between the master and slave devices of the Cyclone III device family for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

(8) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

The first Cyclone III device family in the chain is the configuration master and controls the configuration of the entire chain. You must connect its MSEL pins to select the AS configuration scheme. The remaining Cyclone III device family is configuration slaves and you must connect their MSEL pins to select the PS configuration scheme. Any other Altera device that supports PS configuration can also be part of the chain as a configuration slave.

☞ When connecting a serial configuration device to the Cyclone III device family in the multi-device AS configuration, you must connect a 25-Ω series resistor at the near end of the serial configuration device for DATA[0].

☞ In the multi-device AS configuration, the board trace length between the serial configuration device to the master device of the Cyclone III device family must follow the recommendations in Table 9–9 on page 9–20. You must also connect the repeater buffers between the master and slave devices of the Cyclone III device family for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

As shown in Figure 9–4 on page 9–15, the `nSTATUS` and `CONF_DONE` pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts `nCEO` (after receiving all its configuration data), it releases its `CONF_DONE` pin. However, the subsequent devices in the chain keep this shared `CONF_DONE` line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release `CONF_DONE`, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

☞ Although you can cascade Cyclone III device family, serial configuration devices cannot be cascaded or chained together.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device, enable the compression feature, or both. When configuring multiple devices, the size of the bitstream is the sum of the individual devices configuration bitstreams.

Configuring Multiple Cyclone III Device Family with the Same Design

Certain designs require you to configure multiple Cyclone III device family with the same design through a configuration bitstream or a **.sof**. You can do this using the following methods:

■ Multiple SRAM Object Files

■ Single SRAM Object File

   ☞ For both methods, the serial configuration devices cannot be cascaded or chained together.

Multiple SRAM Object Files

Two copies of the **.sof** are stored in the serial configuration device. Use the first copy to configure the master device of the Cyclone III device family and the second copy to configure all the remaining slave devices concurrently. All slave devices must be of the same density and package. The setup is similar to Figure 9–4 on page 9–15, in which the master device is set up in AS mode and the slave devices are set up in PS mode.

To configure four identical Cyclone III device family with the same **.sof**, you must set up the chain similar to Figure 9–5. The first device is the master device and its MSEL pins must be set to select the AS configuration. The other three slave devices are set up for concurrent configuration and their MSEL pins must be set to select the PS configuration. The `nCEO` pin from the master device drives the `nCE` input pins on all three slave devices, as well as the `DATA` and `DCLK` pins that connect in parallel to all

four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master device drives nCE low and sends the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of using the setup in Figure 9–5 is that you can have a different **.sof** for the master device. However, all the slave devices must be configured with the same **.sof**. In this configuration method, you can either compress or uncompress the **.sof**s.

☞ You can still use this method if the master and slave devices use the same **.sof**.

Figure 9–5. Multi-Device AS Configuration where the Devices Receive the Same Data with Multiple SRAM Object Files
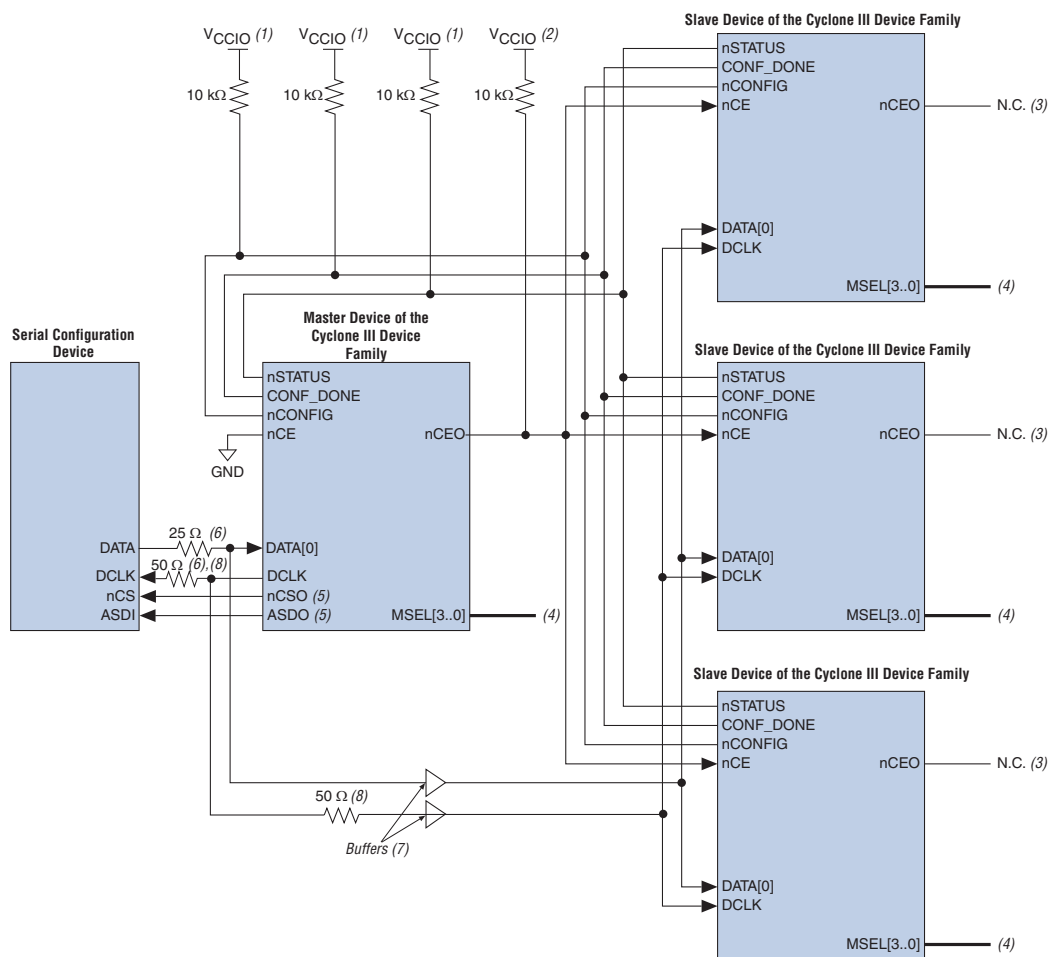
Notes to Figure 9–5:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device in AS mode and the slave devices in PS mode. To connect MSEL[3..0] for the master device in AS mode and the slave devices in PS mode, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. The nCSO pin functions as the FLASH_nCE pin in AP mode. The ASDO pin functions as the DATA[1] pin in other AP and FPP modes.

(6) Connect the series resistor at the near end of the serial configuration device.

(7) Connect the repeater buffers between the master and slave devices for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

(8) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

Single SRAM Object File

The second method configures both the master device and slave devices with the same **.sof**. The serial configuration device stores one copy of the **.sof**. This setup is shown in Figure 9–6 where the master is set up in AS mode and the slave devices are set up in PS mode. You must set up one or more slave devices in the chain. All the slave devices must be set up as shown in Figure 9–6.

Figure 9–6. Multi-Device AS Configuration where the Devices Receive the Same Data with a Single .sof

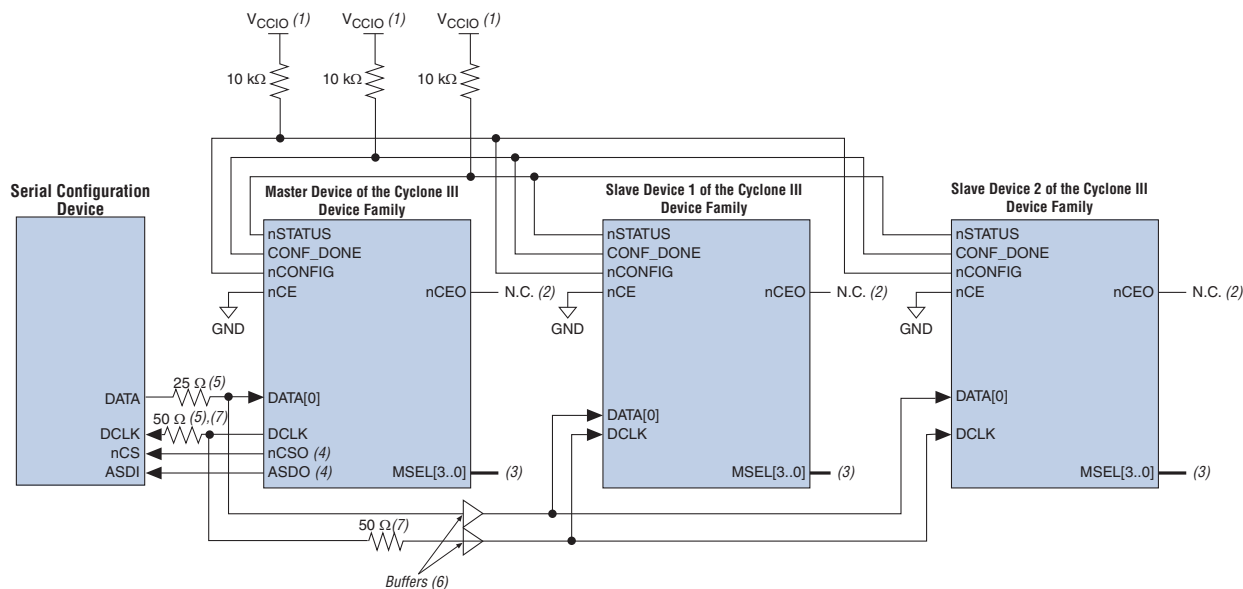**Notes to Figure 9–6:**

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin is left unconnected or used as a user I/O pin when it does not feed the `nCE` pin of another device.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device of the Cyclone III device family in AS mode and the slave devices in PS mode. To connect `MSEL[3..0]` for the master device in AS mode and slave devices in PS mode, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(4) These are dual-purpose I/O pins. The `nCSO` pin functions as the `FLASH_nCE` pin in AP mode. The `ASDO` pin functions as the `DATA[1]` pin in other AP and FPP modes.

(5) Connect the series resistor at the near end of the serial configuration device.

(6) Connect the repeater buffers between the master and slave devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

(7) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

In this setup, all the Cyclone III device family in the chain are connected for concurrent configuration. This can reduce the AS configuration time because all the Cyclone III device family is configured in one configuration cycle. Connect the `nCE` input pins of all the Cyclone III device family to ground. You can either leave the `nCEO` output pins on all the Cyclone III device family unconnected or use the `nCEO` output pins as normal user I/O pins. The `DATA` and `DCLK` pins are connected in parallel to all the Cyclone III device family.

Altera recommends putting a buffer before the DATA and DCLK output from the master device to avoid signal strength and integrity issues. The buffer must not significantly change the DATA-to-DCLK relationships or delay them with respect to other AS signals (ASDI and nCS). Also, the buffer must only drive the slave devices to ensure that the timing between the master device and the serial configuration device is unaffected.

This configuration method supports both compressed and uncompressed **.sof**s. Therefore, if the configuration bitstream size exceeds the capacity of a serial configuration device, you can enable the compression feature in the **.sof** or you can select a larger serial configuration device.

Guidelines for Connecting Serial Configuration Device to Cyclone III Device Family on AS Interface

For single- and multi-device AS configurations, the board trace length and loading between the supported serial configuration device and Cyclone III device family must follow the recommendations listed in Table 9–9.

Table 9–9. Maximum Trace Length and Loading for the AS Configuration

Cyclone III Device Family AS Pins	Maximum Board Trace Length from the Cyclone III Device Family to the Serial Configuration Device (Inches)	Maximum Board Load (pF)
DCLK	10	15
DATA[0]	10	30
nCSO	10	30
ASDO	10	30

Estimating AS Configuration Time

AS configuration time is dominated by the time it takes to transfer data from the serial configuration device to the Cyclone III device family. This serial interface is clocked by the Cyclone III device family DCLK output (generated from an internal oscillator). Equation 9–2 and Equation 9–3 show the configuration time estimation for the Cyclone III device family.

Equation 9–2.

$$\text{Size} \times \left(\frac{\text{maximum DCLK period}}{1 \text{ bit}} \right) = \text{estimated maximum configuration ti}$$

Equation 9–3.

$$3{,}500{,}000 \text{ bits} \times \left(\frac{50 \text{ ns}}{1 \text{ bit}} \right) = 175 \text{ ms}$$

To estimate the typical configuration time, use the typical DCLK period shown in Figure 9–7 on page 9–22. With a typical DCLK period of 33.33 ns, the typical configuration time is 116.7 ms. Enabling compression reduces the amount of configuration data that is sent to the Cyclone III device family, which also reduces configuration time. On average, compression reduces configuration time by 50%.

Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash memory-based devices. You can program these devices in-system using the USB-Blaster™ or ByteBlaster™ II download cable. Alternatively, you can program them using the Altera Programming Unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can perform in-system programming of serial configuration devices using the AS programming interface. During in-system programming, the download cable disables device access to the AS interface by driving the nCE pin high. Cyclone III device family is also held in reset by a low level on nCONFIG. After programming is complete, the download cable releases nCE and nCONFIG, allowing the pull-down and pull-up resistors to drive GND and V$_{CC}$, respectively.

To perform in-system programming of a serial configuration device using the AS programming interface, the diodes and capacitors must be placed as close as possible to the Cyclone III device family. Ensure that the diodes and capacitors maintain a maximum AC voltage of 4.1 V (Figure 9–7).

☞ If you wish to use the same setup shown in Figure 9–7 to perform in-system programming of a serial configuration device and single- or multi-device AS configuration, you do not need a series resistor on the DATA line at the near end of the serial configuration device. The existing diodes and capacitors are sufficient.

Altera has developed the Serial FlashLoader (SFL), a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the Cyclone III device family that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the SFL design.

👣 For more information about implementing the SFL with Cyclone III device family, refer to *AN 370: Using the Serial FlashLoader with the Quartus II Software*.

👣 For more information about the USB-Blaster download cable, refer to the *USB-Blaster Download Cable User Guide*. For more information about the ByteBlaster II download cable, refer to the *ByteBlaster II Download Cable User Guide*.

Figure 9–7 shows the download cable connections to the serial configuration device.

Figure 9–7. In-System Programming of Serial Configuration Devices
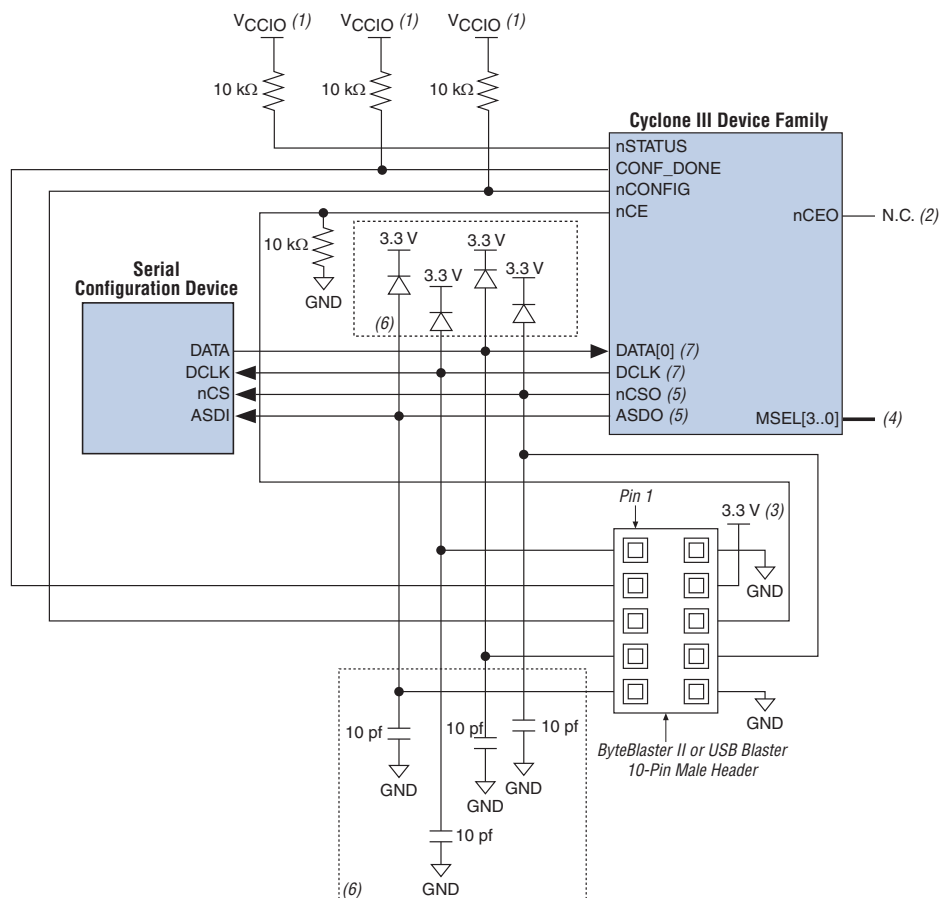
Notes to Figure 9–7:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin is left unconnected or used as a user I/O pin when it does not feed the `nCE` pin of another device.

(3) Power up the V_{CC} of the ByteBlaster II or USB-Blaster download cable with the 3.3-V supply.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or ground.

(5) These are dual-purpose I/O pins. This `nCSO` pin functions as the `FLASH_NCE` pin in AP mode. The `ASDO` pin functions as the `DATA[1]` pin in other AP and FPP modes.

(6) The diodes and capacitors must be placed as close as possible to the Cyclone III device family. Ensure that the diodes and capacitors maintain a maximum AC voltage of 4.1 V. The external diodes and capacitors are required to prevent damage to the Cyclone III device family AS configuration input pins due to possible overshoot when programming the serial configuration device using a download cable. For effective voltage clamping, Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes. For more information about the interface guidelines using Schottky diodes, refer to *AN 523: Cyclone III Configuration Interface Guidelines with EPCS Devices.*

(7) When cascading Cyclone III device family in a multi-device AS configuration, connect the repeater buffers between the master and slave devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

You can use the Quartus II software with the APU and the appropriate configuration device programming adapter to program serial configuration devices. All serial configuration devices are offered in an 8- or 16-pin small outline integrated circuit (SOIC) package.

In production environments, serial configuration devices are programmed using multiple methods. Altera programming hardware or other third-party programming hardware is used to program blank serial configuration devices before they are mounted onto PCBs. Alternatively, you can use an on-board microprocessor to program the serial configuration device in-system by porting the reference C-based SRunner software driver provided by Altera.

A serial configuration device is programmed in-system by an external microprocessor using the SRunner software driver. The SRunner software driver is a software driver developed for embedded serial configuration device programming, which is easily customized to fit in different embedded systems. The SRunner software driver is able to read a Raw Programming Data (**.rpd**) file and write to the serial configuration devices. The serial configuration device programming time using the SRunner software driver is comparable to the programming time with the Quartus II software.

For more information about the SRunner software driver, refer to *AN 418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code at the Altera website (www.altera.com).

AP Configuration (Supported Flash Memories)

The AP configuration scheme is for Cyclone III devices only. In the AP configuration scheme, Cyclone III devices are configured using commodity 16-bit parallel flash memory. These external non-volatile configuration devices are industry standard microprocessor flash memories. The flash memories provide a fast interface to access the configuration data. The speed-up in configuration time is mainly due to the 16-bit wide parallel data bus, which is used to retrieve data from the flash memory.

Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin. Table 9–10 lists the supported AP configuration scheme for each Cyclone III device.

Table 9–10. Supported AP Configuration Scheme for Cyclone III Devices

Device	Package Options								
	E144	M164	Q240	F256	F324	F484	F780	U256	U484
EP3C5	—	—	—	—	—	—	—	—	—
EP3C10	—	—	—	—	—	—	—	—	—
EP3C16	—	—	—	—	—	✓	—	—	✓
EP3C25	—	—	—	—	✓	—	—	—	—
EP3C40	—	—	—	—	✓	✓	✓	—	✓
EP3C55	—	—	—	—	—	✓	✓	—	✓
EP3C80	—	—	—	—	—	✓	✓	—	✓
EP3C120	—	—	—	—	—	✓	✓	—	—

During device configuration, Cyclone III devices read configuration data using the parallel interface and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where an external host controls the interface.

AP Configuration Supported Flash Memory

The AP configuration controller in Cyclone III devices is designed to interface with the Micron P30 Parallel NOR flash family and the Micron P33 Parallel NOR flash family, which are two industry standard flash families. Unlike serial configuration devices, both of the flash families supported in the AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash after entering user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Micron P30 and P33 flash families support a continuous synchronous burst read mode at 40 MHz DCLK frequency for reading data from the flash. Additionally, the Micron P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.

☞ Cyclone III devices use a 40-MHz oscillator for the AP configuration scheme.

Table 9–11 lists the supported families of the commodity parallel flash for the AP configuration scheme.

Table 9–11. Supported Commodity Flash for the AP Configuration Scheme for Cyclone III Devices [1]

Flash Memory Density	Micron P30 Flash Family [2]	Micron P33 Flash Family [3]
64 Mbit	✔	✔
128 Mbit	✔	✔
256 Mbit	✔	✔

Notes to Table 9–11:

(1) The AP configuration scheme only supports flash memory speed grades of 40 MHz and above.
(2) 3.3- , 3.0-, 2.5-, and 1.8-V I/O options are supported for the Micron P30 flash family.
(3) 3.3-, 3.0- and 2.5-V I/O options are supported for the Micron P33 flash family.

The AP configuration scheme of Cyclone III devices supports the Micron P30 and P33 family 64-, 128-, and 256-Mbit flash memories. Configuring Cyclone III devices from the Micron P30 and P33 family 512-Mbit flash memory is possible, but you must properly drive the extra address and FLASH_nCE pins as required by these flash memories.

☞ You must refer to the respective flash data sheets to check for supported speed grades and package options.

The AP configuration scheme in Cyclone III devices supports flash speed grades of 40 MHz and above. However, the AP configuration for all these speed grades must be capped at 40 MHz. The advantage of faster speed grades is realized when your design in the Cyclone III device accesses flash memory in user mode.

📌 For more information about the operation of the Micron P30 Parallel NOR and P33 flash memories, search for the keyword "P30" or "P33" on the Micron website (www.micron.com) to obtain the P30 or P33 family data sheet.

Single-Device AP Configuration

The following groups of interface pins are supported in Micron P30 and P33 flash memories:

■ Control pins

■ Address pins

■ Data pins

Following are the control signals from the supported parallel flash memories:

■ CLK

■ active-low reset (RST#)

■ active-low chip enable (CE#)

■ active-low output enable (OE#)

■ active-low address valid (ADV#)

■ active-low write enable (WE#)

The supported parallel flash memories output a control signal (WAIT) to Cyclone III devices to indicate when synchronous data is ready on the data bus. Cyclone III devices have a 24-bit address bus connecting to the address bus (A[24:1]) of the flash memory. A 16-bit bidirectional data bus (DATA[15..0]) provides data transfer between the Cyclone III device and the flash memory.

The following are the control signals from the Cyclone III device to flash memory:

■ DCLK

■ nRESET

■ FLASH_nCE

■ nOE

■ nAVD

■ nWE

The interface for the Micron P30 flash memory and P33 flash memory connects to Cyclone III device pins, as shown in Figure 9–8.

Figure 9–8. Single-Device AP Configuration Using Micron P30 and P33 Flash Memory
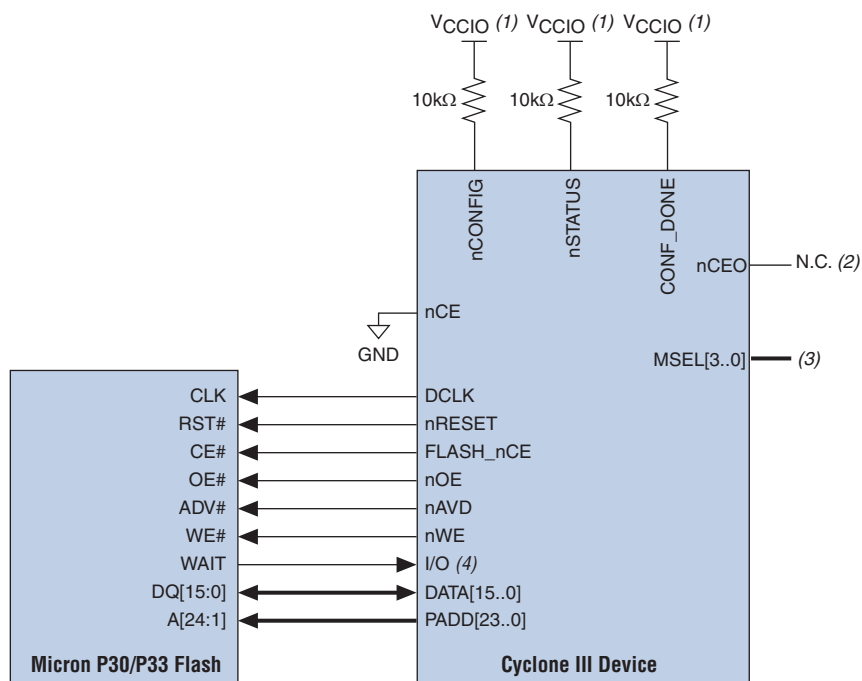
Notes to Figure 9–8:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use a normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

☞ To tri-state the configuration bus for AP configuration schemes, you must tie nCE high and nCONFIG low.

☞ In a single-device AP configuration, the maximum board loading and board trace length between the supported parallel flash and Cyclone III devices must follow the recommendations listed in Table 9–12 on page 9–30.

☞ If you use the AP configuration scheme for Cyclone III devices, the V_{CCIO} of I/O banks 1, 6, 7, and 8 must be 3.3, 3.0, 2.5, or 1.8 V. Altera does not recommend using the level shifter between the Micron P30/P33 flash and the Cyclone III device in the AP configuration scheme.

☞ There are no series resistors required in the AP configuration mode for Cyclone III devices when using the Micron flash at 2.5-, 3.0-, and 3.3-V I/O standard. The output buffer of the Micron P30 IBIS model does not overshoot above 4.1 V. Thus, series resistors are not required for the 2.5-, 3.0-, and 3.3-V AP configuration option. However, if there are any other devices sharing the same flash I/Os with Cyclone III devices, all shared pins are still subject to the 4.1-V limit and may require series resistors.

The default read mode of the supported parallel flash memory and all writes to the parallel flash memory are asynchronous. Both the parallel flash families support a synchronous read mode, with data supplied on the positive edge of DCLK.

■ nRESET is an active-low hard reset

■ FLASH_nCE is an active-low chip enable

■ nOE is an active-low output enable for the DATA[15..0] bus and WAIT pin

■ nAVD is an active-low address valid signal and is used to write addresses into the flash

■ nWE is an active-low write enable and is used to write data into the flash

■ PADD[23..0] bus is the address bus supplied to the flash

■ DATA[15..0] bus is a bidirectional bus used to supply and read data to and from the flash, with the flash output controlled by nOE

The serial clock (DCLK) generated by Cyclone III devices controls the entire configuration cycle and provides timing for the parallel interface. Cyclone III devices use a 40-Mhz internal oscillator to generate DCLK. The oscillator is the same oscillator used in the AS configuration scheme. The active DCLK output frequency is listed in Table 9–8 on page 9–14.

Multi-Device AP Configuration

You can cascade multiple Cyclone III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. Connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone III device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, DATA[15..8], and DATA[7..0] pins of each device in the chain are connected (Figure 9–9 on page 9–28 and Figure 9–10 on page 9–29).

The first Cyclone III device in the chain, as shown in Figure 9–9 on page 9–28 and Figure 9–10 on page 9–29, is the configuration master device and controls the configuration of the entire chain. Connect its MSEL pins to select the AP configuration scheme. The remaining Cyclone III devices are used as configuration slaves. Connect their MSEL pins to select the FPP configuration scheme. Any other Altera device that supports FPP configuration can also be part of the chain as a configuration slave.

The following are the configurations for the DATA[15..0] bus in a multi-device AP configuration:

- Byte-wide multi-device AP configuration
- Word-wide multi-device AP configuration

Byte-Wide Multi-Device AP Configuration

The simpler method for multi-device AP configuration is the byte-wide multi-device AP configuration. In the byte-wide multi-device AP configuration, the LSB of the DATA[7..0] pin from the flash and master device (set to the AP configuration scheme) is connected to the slave devices set to the FPP configuration scheme, as shown in Figure 9–9.

Figure 9–9. Byte-Wide Multi-Device AP Configuration
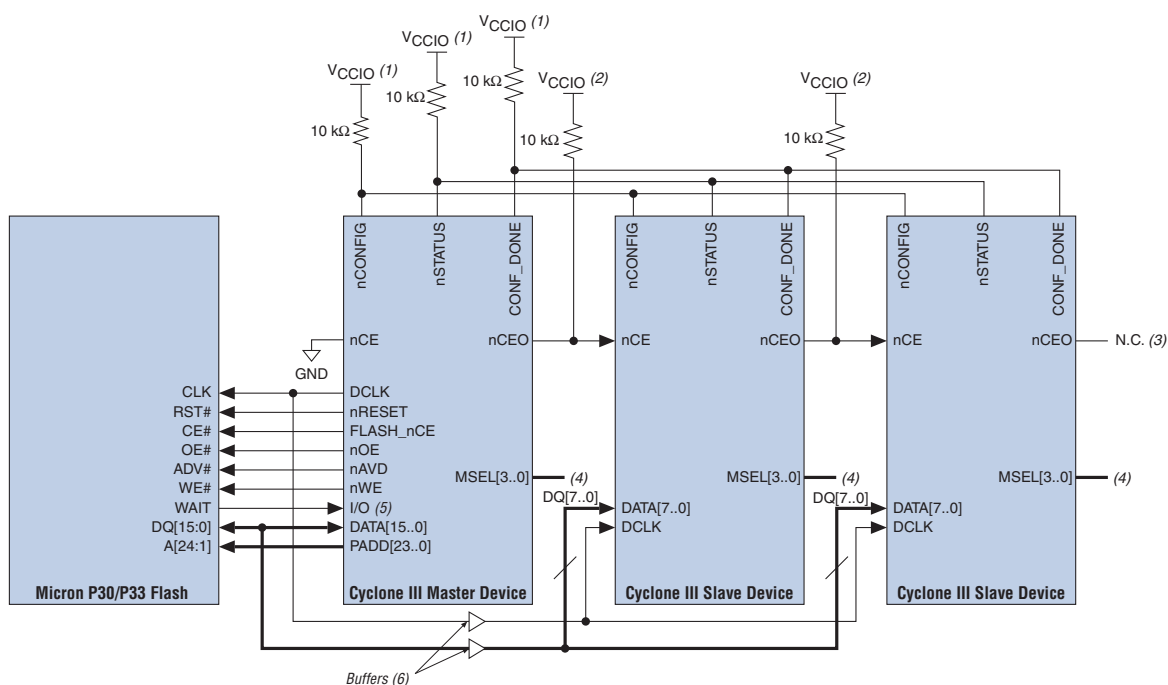
Notes to Figure 9–9:

(1) Connect the pull-up resistors to the V$_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V$_{CCIO}$ supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device in AP mode and the slave devices in FPP mode. To connect MSEL[3..0] for the master device in AP mode and the slave devices in FPP mode, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V$_{CCA}$ or GND.

(5) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

(6) Connect the repeater buffers between the master device and slave devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

Word-Wide Multi-Device AP Configuration

The more efficient setup is one in which some of the slave devices are connected to the LSB of DATA[7..0] and the remaining slave devices are connected to the MSB of DATA[15..8]. In the word-wide multi-device AP configuration, the nCEO pin of the master device enables two separate daisy-chains of slave devices, allowing both chains to be programmed concurrently, as shown in Figure 9–10.

Figure 9–10. Word-Wide Multi-Device AP Configuration

Notes to Figure 9–10:

(1) Connect the pull-up resistors to the V$_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V$_{CCIO}$ supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
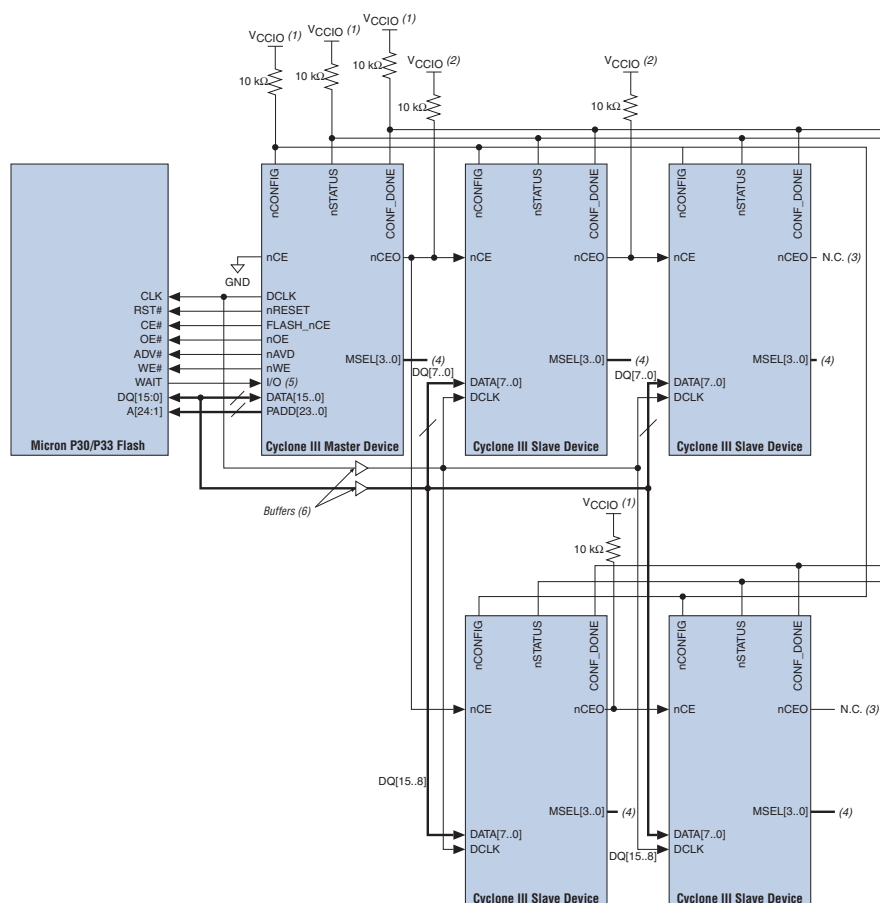
(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device in AP mode and the slave devices in FPP mode. To connect MSEL[3..0] for the master device in AP mode and the slave devices in FPP mode, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V$_{CCA}$ or GND.

(5) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O pin to monitor the WAIT signal from the Micron P30 or P33 flash.

(6) Connect the repeater buffers between the Cyclone III master device and slave devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

☞ In a multi-device AP configuration, the board trace length between the parallel flash and the master device must follow the recommendations listed in Table 9–12.

As shown in Figure 9–9 and Figure 9–10, the nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

Guidelines for Connecting Parallel Flash to Cyclone III Devices for the AP Interface

For the single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and Cyclone III devices must follow the recommendations listed in Table 9–12. These recommendations also apply to an AP configuration with multiple bus masters.

Table 9–12. Maximum Trace Length and Loading for the AP Configuration

Cyclone III AP Pins	Maximum Board Trace Length from the Cyclone III Device to the Flash Device (Inches)	Maximum Board Load (pF)
DCLK	6	15
DATA[15..0]	6	30
PADD[23..0]	6	30
nRESET	6	30
Flash_nCE	6	30
nOE	6	30
nAVD	6	30
nWE	6	30
I/O [1]	6	30

Note to Table 9–12:

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, the master must assert nCONFIG low for at least 500 ns to reset the master Cyclone III device and override the weak 10 kΩ pull-down resistor on the nCE pin. This resets the master Cyclone III device and causes it to tri-state its AP configuration bus. The other master then takes control of the AP configuration bus. After the other master is done, it releases the AP configuration bus, then releases the nCE pin, and finally pulses nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

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Figure 9–11 shows the AP configuration with multiple bus masters.

Figure 9–11. AP Configuration with Multiple Bus Masters
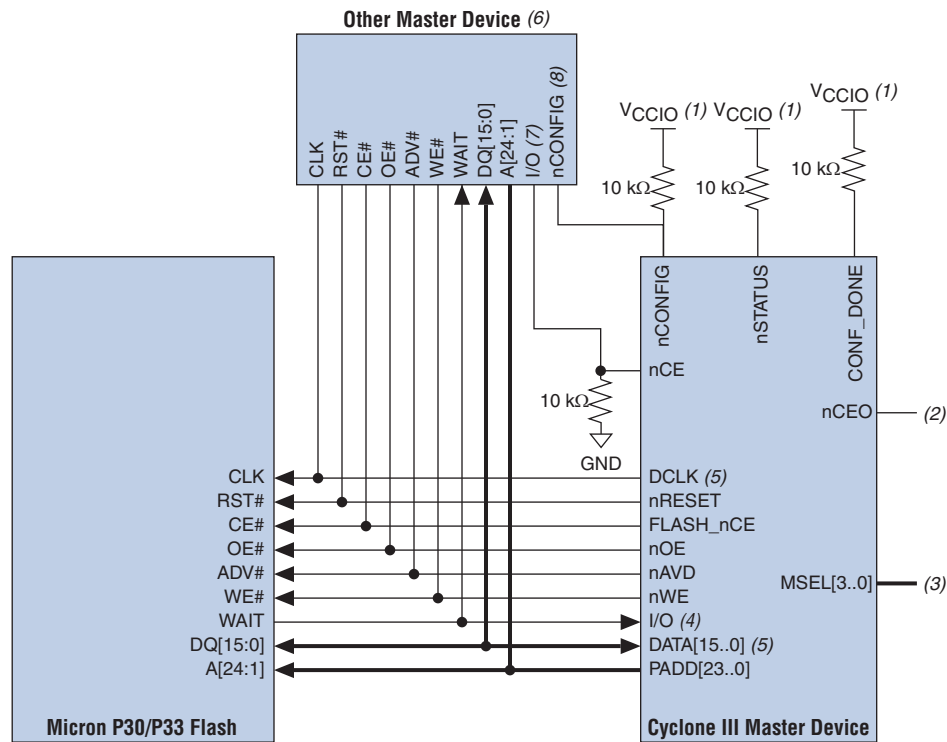
Notes to Figure 9–11:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

(5) When cascading Cyclone III devices in a multi-device AP configuration, connect the repeater buffers between the master device and slave devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

(6) The other master device must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

(7) The other master device can control the AP configuration bus by driving the nCE pin to high with an output high on the I/O pin.

(8) The other master device can pulse nCONFIG if it is under system control rather than tied to V_{CCIO}.

Figure 9–12 shows the recommended balanced star routing for multiple bus master interfaces to minimize signal integrity issue.

Figure 9–12. Balanced Star Routing
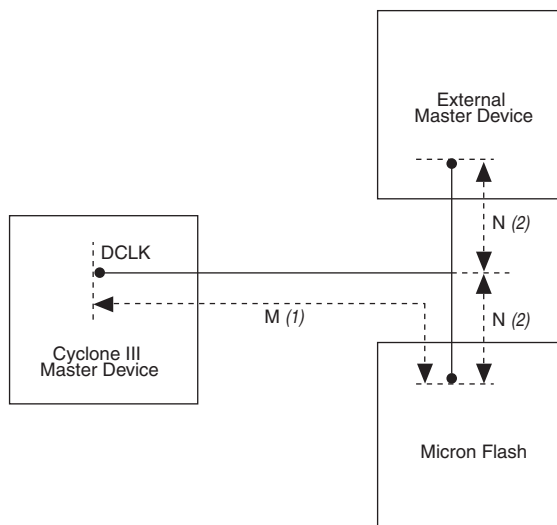
Notes to Figure 9–12:

(1) Altera does not recommend *M* to exceed six inches as listed in Table 9–12 on page 9–30.

(2) Altera recommends using a balanced star routing. Try to keep the *N* length equal and as short as possible to minimize reflection noise from the transmission line. The *M* length is applicable for this setup.

Estimating the AP Configuration Time

AP configuration time is dominated by the time it takes to transfer data from the parallel flash to the Cyclone III devices. This parallel interface is clocked by the Cyclone III DCLK output (generated from an internal oscillator). As listed in Table 9–8 on page 9–14, the DCLK minimum frequency when using the 40-MHz oscillator is 20 MHz (50 ns). In word-wide cascade programming, the DATA[15..0] bus transfers a 16-bit word and essentially cuts configuration time to approximately 1/16 of the AS configuration time. Therefore, the maximum configuration time estimation for an EP3C40 device (9,600,000 bits of uncompressed data) is defined in Equation 9–4 and Equation 9–5.

Equation 9–4.

$$\text{Size} \times \left(\frac{\text{maximum DCLK period}}{\text{16 bits per DCLK cycle}} \right) = \text{estimated maximum configuration ti}$$

Equation 9–5.

$$9{,}600{,}000 \text{ bits} \times \left(\frac{50 \text{ ns}}{16 \text{ bits}} \right) = 30 \text{ ms}$$

To estimate a typical configuration time, use the typical DCLK period listed in Table 9–8 on page 9–14. With a typical DCLK period of 33.33 ns, the typical configuration time is 20 ms.

Programming Parallel Flash Memories

Supported parallel flash memories are external non-volatile configuration devices. They are industry standard microprocessor flash memories. For more information about the supported families for the commodity parallel flash, refer to Table 9–11 on page 9–24.

Cyclone III devices in a single- or multiple-device chains support in-system parallel flash programming with the JTAG interface using the flash loader megafunction. For Cyclone III devices, the board-intelligent host or download cable uses four JTAG pins to program the parallel flash in system, even if the host or download cable cannot access the configuration pins of the parallel flash.

For more information about using the JTAG pins on Cyclone III devices to program the parallel flash in-system, refer to *AN 478: Using FPGA-Based Parallel Flash Loader (PFL) with the Quartus II Software*.

In the AP configuration scheme, the default configuration boot address is **0×010000** when represented in 16-bit word addressing in the supported parallel flash memory (Figure 9–13). In the Quartus II software, the default configuration boot address is 0x020000 because it is represented in 8-bit byte addressing. Cyclone III devices configure from word address 0x010000, which is equivalent to byte address 0x020000.

The Quartus II software uses byte addressing for the default configuration boot address. You must set the start address field to **0x020000**.

The default configuration boot addressing allows the system to use special parameter blocks in the flash memory map. Parameter blocks are at the top or bottom of the memory map. The configuration boot address in the AP configuration scheme is shown in Figure 9–13. You can change the default configuration default boot address **0x010000** to any desired address using the `APFC_BOOT_ADDR` JTAG instruction. For more information about the `APFC_BOOT_ADDR` JTAG instruction, refer to "JTAG Instructions" on page 9–60.

Figure 9–13. Configuration Boot Address in AP Flash Memory Map
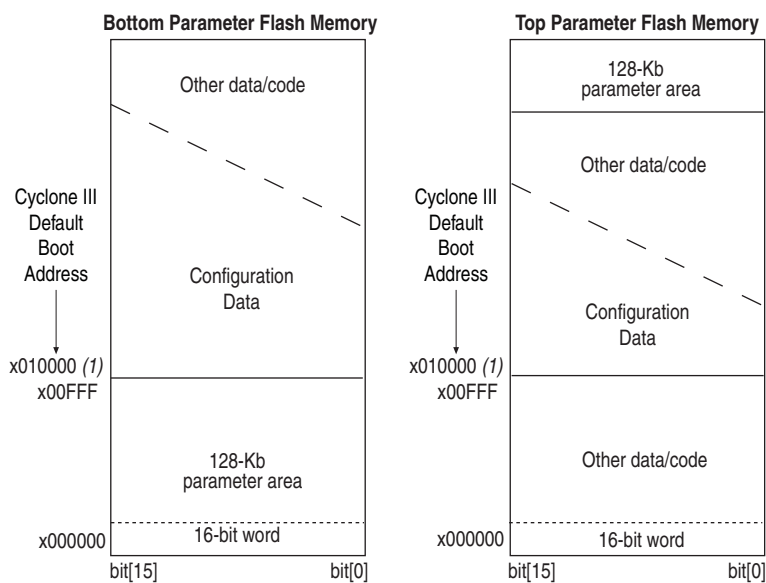
Note to Figure 9–13:

(1) The default configuration boot address is x010000 when represented in 16-bit word addressing.

PS Configuration

You can perform PS configuration on Cyclone III device family with an external intelligent host, such as a MAX II device, microprocessor with flash memory, or a download cable. In the PS scheme, an external host controls the configuration. Configuration data is clocked into the target Cyclone III device family using the `DATA[0]` pin at each rising edge of `DCLK`.

If your system already contains a common flash interface (CFI) flash memory, you can use it for the Cyclone III device family configuration storage as well. The MAX II PFL feature provides an efficient method to program CFI flash memory devices through the JTAG interface and provides the logic to control the configuration from the flash memory device to the Cyclone III device family. Both PS and FPP configuration schemes are supported using the PFL feature.

For more information about the PFL, refer to *Parallel Flash Loader Megafunction User Guide*.

☞ Cyclone III device family does not support enhanced configuration devices for PS or FPP configurations.

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PS Configuration Using an External Host

In the PS configuration scheme, you can use an intelligent host such as MAX II or microprocessor that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device family. You can store the configuration data in **.rbf**, **.hex**, or **.ttf** format.

Figure 9–14 shows the configuration interface connections between a Cyclone III device family and an external host device for a single-device configuration.

Figure 9–14. Single-Device PS Configuration Using an External Host
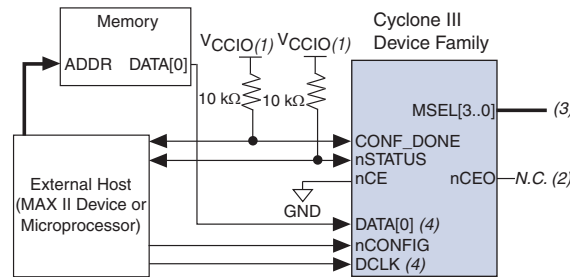
Notes to Figure 9–14:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or ground.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

To begin configuration, the external host device must generate a low-to-high transition on the nCONFIG pin. When nSTATUS is pulled high, the external host device must place the configuration data one bit at a time on the DATA[0] pin. If you are using configuration data in a **.rbf**, **.ttf**, or **.hex** file, you must first send the LSB of each data byte. For example, if the **.rbf** contains the byte sequence 02 1B EE 01 FA, the serial bitstream you must send to the device is:

> 0100-0000 1101-1000 0111-0111 1000-0000 0101-1111

Cyclone III device family receives configuration data on the DATA[0] pin and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high and the device enters the initialization state.

☞ Two DCLK falling edges are required after CONF_DONE goes high to begin device initialization.

The INIT_DONE pin is released and pulled high when initialization is complete. The external host device must be able to detect this low-to-high transition which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA[0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. In the PS scheme, the DATA[0] pin is tri-stated by default in user mode and must be driven by the external host device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified system frequency to ensure correct configuration (Figure 9–19 on page 9–42). No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If a configuration error occurs during configuration and the **Auto-restart configuration after error** option is turned on, the Cyclone III device family releases nSTATUS after a reset time-out period (a maximum of 230 μs). After nSTATUS is released and pulled high by a pull-up resistor, the external host device tries to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the external host device must generate a low-to-high transition (with a low pulse of at least 500 ns) on nCONFIG to restart the configuration process.

The external host device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the external device to detect errors and to determine when the programming is complete. If all configuration data is sent, but CONF_DONE or INIT_DONE has not gone high, the external device must reconfigure the target device.

Figure 9–15 shows how to configure multiple devices using an external host device. This circuit is similar to the PS configuration circuit for a single device, except that the Cyclone III device family is cascaded for multi-device configuration.

Figure 9–15. Multi-Device PS Configuration Using an External Host

Notes to Figure 9–15:

(1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or ground.

(5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

In a multi-device PS configuration, the nCE pin of the first device is connected to GND while its nCEO pin is connected to the nCE pin of the next device in the chain. The nCE input of the last device comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. The second device in the chain begins configuration in one clock cycle. Therefore, the transfer of data destinations is transparent to the external host device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

If any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured because all nSTATUS and CONF_DONE pins are tied together. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

You can have multiple devices that contain the same configuration data in your system. To support this configuration scheme, all device nCE inputs are tied to GND, while the nCEO pins are left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be of the same density and package. All devices start and complete configuration at the same time.

Figure 9–16 shows a multi-device PS configuration when both Cyclone III device family is receiving the same configuration data.

Figure 9–16. Multi-Device PS Configuration When Both Devices Receive the Same Data
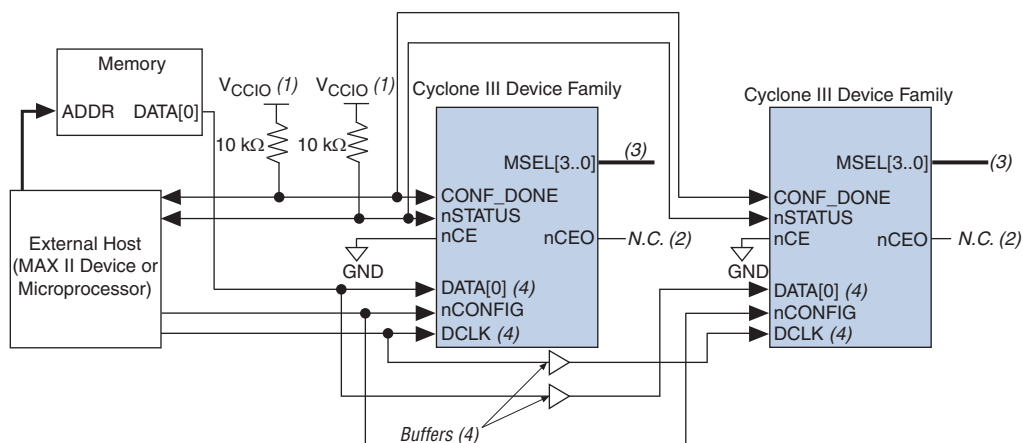
Notes to Figure 9–16:

(1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices are left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or ground.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

PS Configuration Timing

A PS configuration must meet the setup and hold timing parameters and the maximum clock frequency. When using a microprocessor or another intelligent host to control the PS interface, ensure that you meet these timing requirements.

Figure 9–17 shows the timing waveform for a PS configuration when using an external host device as an external host.

Figure 9–17. PS Configuration Timing Waveform [1]
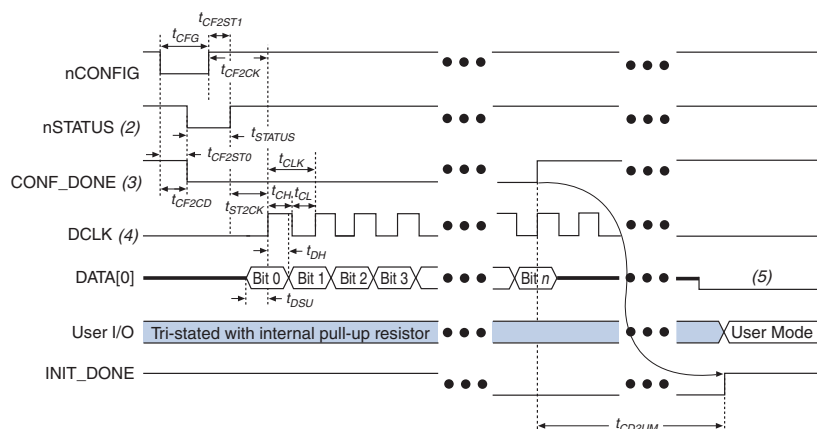
Notes to Figure 9–17:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Cyclone III device family holds nSTATUS low during POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) In user mode, drive DCLK either high or low when using the PS configuration scheme, whichever is more convenient. When using the AS configuration scheme, DCLK is a Cyclone III device family output pin and must not be driven externally.

(5) Do not leave the DATA[0] pin floating after configuration. Drive it high or low, whichever is more convenient.

Table 9–13 lists the PS configuration timing parameters for Cyclone III device family.

Table 9–13. PS Configuration Timing Parameters for Cyclone III Device Family (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	500	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	500	ns
t_{CFG}	nCONFIG low pulse width	500	—	ns
t_{STATUS}	nSTATUS low pulse width	45	800 [1]	μs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	800 [2]	μs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	800 [1]	—	μs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	Data setup time before rising edge on DCLK	5	—	ns
t_{DH}	Data hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	3.2	—	ns
t_{CL}	DCLK low time	3.2	—	ns
t_{CLK}	DCLK period	7.5	—	ns
f_{MAX}	DCLK frequency	—	100 [4]	MHz
t_{CD2UM}	CONF_DONE high to user mode [3]	300	650	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—

Table 9–13. PS Configuration Timing Parameters for Cyclone III Device Family (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2UMC}	CONF_DONE high to user mode with **CLKUSR** option on	t_{CD2CU} + (initialization clock cycles × CLKUSR period) [5]	—	—

Notes to Table 9–13:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding nSTATUS low.

(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting the device.

(4) Cyclone III devices can support a DCLK f_{MAX} of 133 MHz. Cyclone III LS devices can support a DCLK f_{MAX} of 100 MHz.

(5) For more information about the initialization clock cycles required in Cyclone III device family, refer to Table 9–5 on page 9–10.
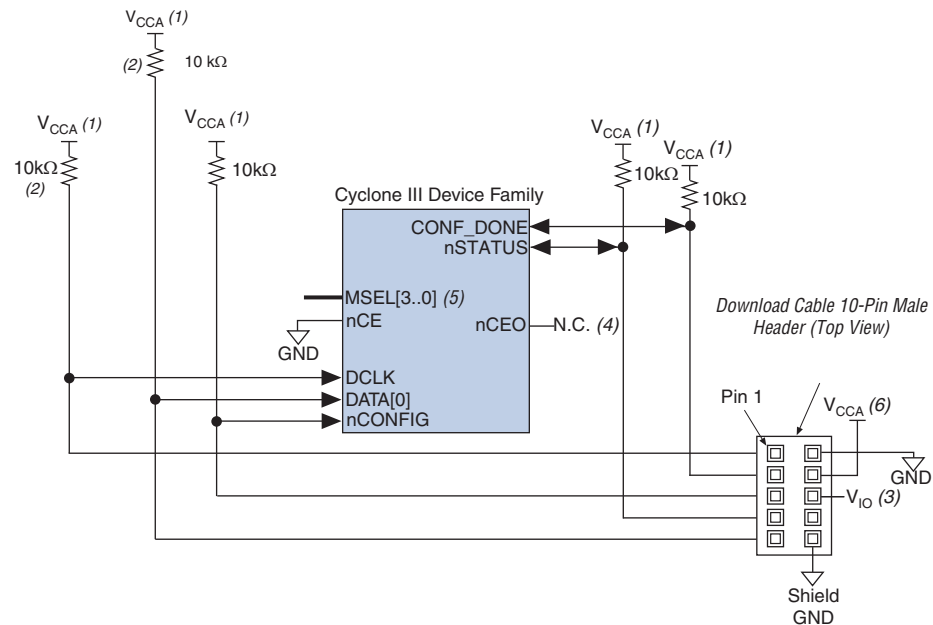
PS Configuration Using a Download Cable

In this section, the generic term "download cable" includes the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, the ByteBlasterMV™ parallel port download cable, and the Ethernet-Blaster communications cable.

In the PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the device using the download cable.

The programming hardware or download cable then places the configuration data one bit at a time on the DATA[0] pin of the device. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-kΩ pull-up resistor for the device to initialize.

When you use a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs. Additionally, the **Enable user-supplied start-up clock (CLKUSR)** option has no effect on the device initialization because this option is disabled in the **.sof** when programming the device using the Quartus II programmer and download cable. Therefore, if you turn on the **CLKUSR** option, you do not need to provide a clock on CLKUSR when you are configuring the device with the Quartus II programmer and a download cable.

Figure 9–18 shows PS configuration for Cyclone III device family using a download cable.

Figure 9–18. PS Configuration Using a USB-Blaster, MasterBlaster, ByteBlaster II, ByteBlasterMV, or Ethernet Blaster Cable
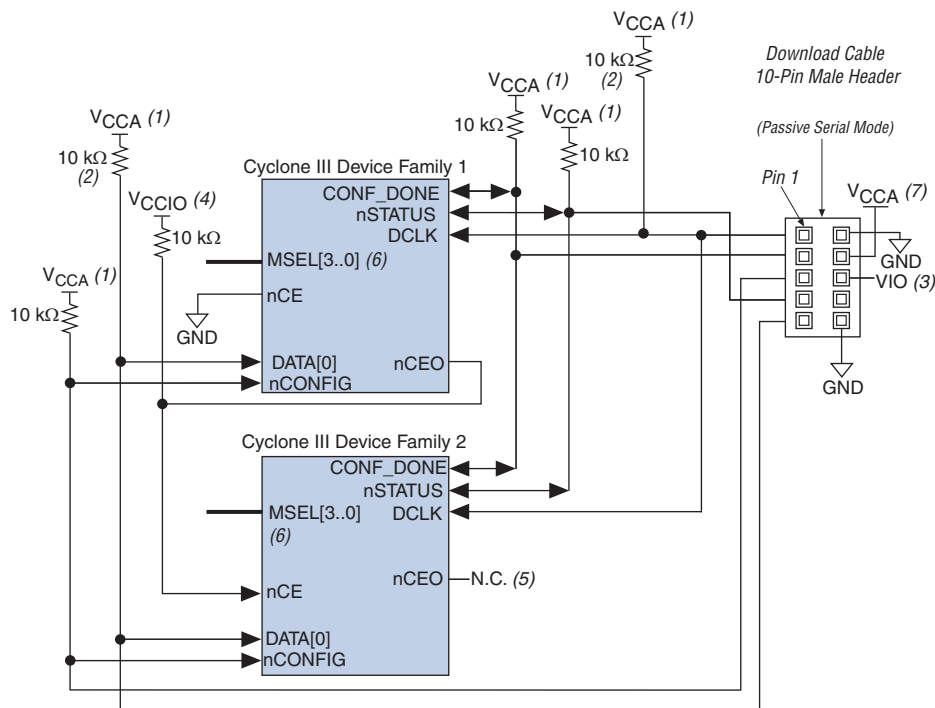

Notes to Figure 9–18:

(1) The pull-up resistor must be connected to the same supply voltage as the V_{CCA} supply.

(2) You only need the pull-up resistors on `DATA[0]` and `DCLK` if the download cable is the only configuration scheme used on your board. This is to ensure that `DATA[0]` and `DCLK` are not left floating after configuration. For example, if you are also using a configuration device, you do not need the pull-up resistors on `DATA[0]` and `DCLK`.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. For the USB Blaster, ByteBlaster II, ByteBlaster MV, and Ethernet Blaster, this pin is a no connect.

(4) The `nCEO` pin is left unconnected or used as a user I/O pin when it does not feed the `nCE` pin of another device.

(5) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 9–7 on page 9–11 for PS configuration schemes. Connect the MSEL pins directly to V_{CCA} or GND.

(6) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5- V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

You can use a download cable to configure multiple Cyclone III device family by connecting the `nCEO` pin of each device to the `nCE` pin of the subsequent device. The `nCE` pin of the first device is connected to GND while its `nCEO` pin is connected to the `nCE` pin of the next device in the chain. The `nCE` input of the last device comes from the previous device while its `nCEO` pin is left floating. All other configuration pins, `nCONFIG`, `nSTATUS`, `DCLK`, `DATA[0]`, and `CONF_DONE` are connected to every device in the chain. Because all `CONF_DONE` pins are tied together, all devices in the chain initialize and enter user mode at the same time.

In addition, the entire chain halts configuration if any device detects an error because the `nSTATUS` pins are tied together. The **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs.

Figure 9–19 shows PS configuration for multi Cyclone III device family using a MasterBlaster, USB-Blaster, ByteBlaster II, or ByteBlasterMV cable.

Figure 9–19. Multi-Device PS Configuration Using a USB-Blaster, MasterBlaster, ByteBlaster II, ByteBlasterMV, or Ethernet Blaster Cable

Notes to Figure 9–19:

(1) The pull-up resistor must be connected to the same supply voltage as the V_{CCA} supply.

(2) You only need the pull-up resistors on `DATA[0]` and `DCLK` if the download cable is the only configuration scheme used on your board. This is to ensure that `DATA[0]` and `DCLK` are not left floating after configuration. For example, if you are also using a configuration device, you do not need the pull-up resistors on `DATA[0]` and `DCLK`.

(3) Pin 6 of the header is a V_{IO} reference output voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In ByteBlasterMV, this pin is a no connect. In USB-Blaster, ByteBlaster II, and Ethernet Blaster, this pin is connected to `nCE` when it is used for AS programming. Otherwise, it is a no connect.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the `nCE` pin resides.

(5) The `nCEO` pin of the last device in the chain is left unconnected or used as a user I/O pin.

(6) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]` for PS configuration schemes, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(7) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5- V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

FPP Configuration

The FPP configuration in Cyclone III device family is designed to meet the increasing demand for faster configuration time. Cyclone III device family is designed with the capability of receiving byte-wide configuration data per clock cycle.

You can perform the FPP configuration of Cyclone III device family with an intelligent host, such as a MAX II device or microprocessor with flash memory. If your system already contains a CFI flash memory, you can use it for the Cyclone III device family configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone III device family. Both PS and FPP configuration schemes are supported using this PFL feature.

⌦ For more information about the PFL, refer to *Parallel Flash Loader Megafunction User Guide*.

☞ Cyclone III device family does not support enhanced configuration devices for PS or FPP configurations.

☞ FPP configuration is not supported in the E144 package of Cyclone III devices.

FPP Configuration Using an External Host

The FPP configuration using an external host provides a fast method to configure Cyclone III device family. In the FPP configuration scheme, you can use an external host device to control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device family. You can store configuration data in either an **.rbf**, **.hex**, or **.ttf** format. When using the external host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to the device, must be stored in the external host device. Figure 9–20 shows the configuration interface connections between the Cyclone III device family and an external device for single-device configuration.

Figure 9–20. Single-Device FPP Configuration Using an External Host
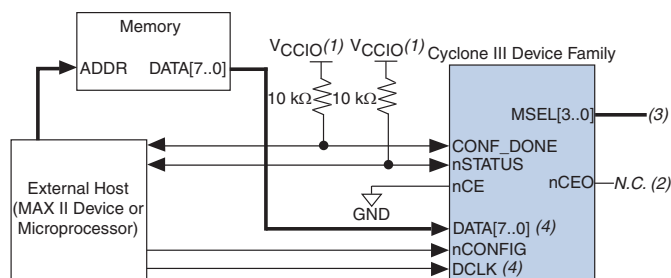
Notes to Figure 9–20:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

After nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the external host device places the configuration data one byte at a time on the DATA[7..0] pins.

Cyclone III device family receives configuration data on the DATA[7..0] pins and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high. The CONF_DONE pin goes high one byte early in FPP configuration mode. The last byte is required for serial configuration (AS and PS) modes.

☞   Two DCLK falling edges are required after CONF_DONE goes high to begin the initialization of the device.

Supplying a clock on CLKUSR does not affect the configuration process. After the CONF_DONE pin goes high, CLKUSR is enabled after the time specified as t_{CD2CU}. After this time period elapses, Cyclone III device family requires certain amount of clock cycles to initialize properly and enter user mode. For more information about the initialization clock cycles required in the Cyclone III device family, refer to Table 9–5 on page 9–10. For more information about the supported CLKUSR f_{MAX} value for Cyclone III device family, refer to Table 9–14 on page 9–47.

The INIT_DONE pin is released and pulled high when initialization is complete. The external host device must be able to detect this low-to-high transition which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.
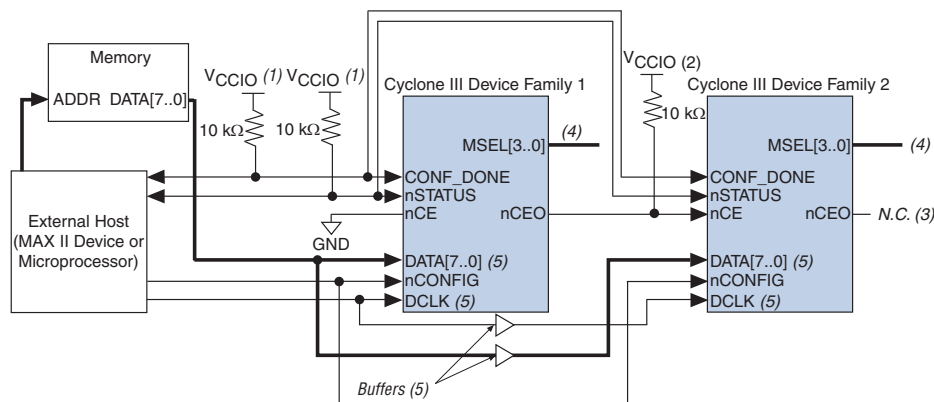
To ensure that DCLK and DATA[0] are not left floating at the end of the configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the FPP scheme in the Quartus II software, the DATA[0] pin is tri-stated by default in user mode and must be driven by the external host device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The DCLK speed must be below the specified system frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If a configuration error occurs during configuration and the **Auto-restart configuration after error** option is turned on, the Cyclone III device family releases nSTATUS after a reset time-out period (a maximum of 230 μs). After nSTATUS is released and pulled high by a pull-up resistor, the external host device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the external host device must generate a low-to-high transition (with a low pulse of at least 500 ns) on nCONFIG to restart the configuration process.

The external host device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the external device to detect errors and to determine when programming is complete. If all configuration data is sent but CONF_DONE or INIT_DONE has not gone high, the external device must reconfigure the target device.

Figure 9–21 shows how to configure multiple devices using a MAX II device. This circuit is similar to the FPP configuration circuit for a single device, except the Cyclone III device family is cascaded for a multi-device configuration.

Figure 9–21. Multi-Device FPP Configuration Using an External Host
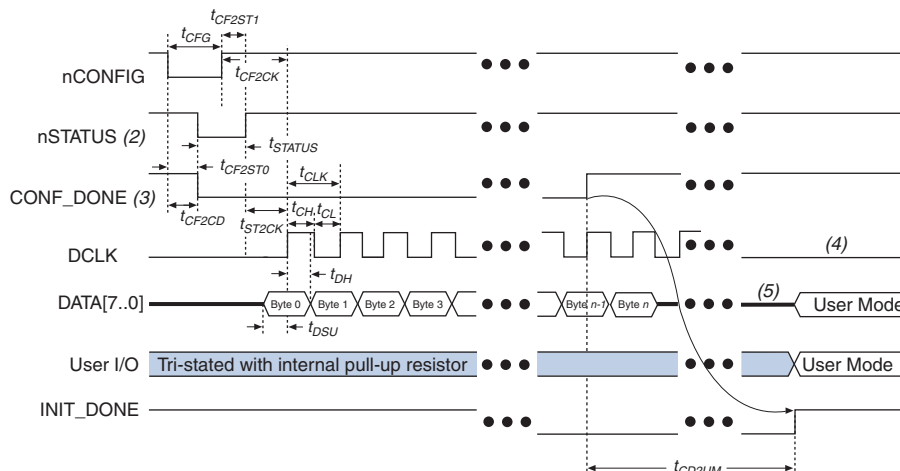

Notes to Figure 9–21:

(1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or ground.

(5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

In a multi-device FPP configuration, the nCE pin of the first device is connected to GND while its nCEO pin is connected to the nCE pin of the next device in the chain. The nCE input of the last device comes from the previous device while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. The second device in the chain begins configuration in one clock cycle; therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. All devices initialize and enter user mode at the same time because all device CONF_DONE pins are tied together.

All nSTATUS and CONF_DONE pins are tied together and if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

If a system has multiple devices that contain the same configuration data, tie all device nCE inputs to GND and leave nCEO pins floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be of the same density and package. All devices start and complete configuration at the same time.

Figure 9–22 shows multi-device FPP configuration when both Cyclone III device family is receiving the same configuration data.

Figure 9–22. Multi-Device FPP Configuration Using an External Host When Both Devices Receive the Same Data

Notes to Figure 9–22:

(1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices are left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

You can use a single configuration chain to configure Cyclone III device family with other Altera devices that support the FPP configuration. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device starts reconfiguration in all devices, tie all the device CONF_DONE and nSTATUS pins together.

For more information about configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera FPGA Chains* chapter in volume 2 of the *Configuration Handbook*.

FPP Configuration Timing

Figure 9–23 shows the timing waveform for FPP configuration when using an external host.

Figure 9–23. FPP Configuration Timing Waveform [1]

Notes to Figure 9–23:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Cyclone III device family holds nSTATUS low during POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. It must be driven high or low, whichever is more convenient.

(5) DATA[7..0] is available as user I/O pin after configuration; the state of the pin depends on the dual-purpose pin settings.

Table 9–14 lists the FPP configuration timing parameters for Cyclone III device family.

Table 9–14. FPP Timing Parameters for Cyclone III Device Family   (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	500	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	500	ns
t_{CFG}	nCONFIG low pulse width	500	—	ns
t_{STATUS}	nSTATUS low pulse width	45	230 [1]	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	230 [1]	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	230 [1]	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA setup time before rising edge on DCLK	5	—	ns
t_{DH}	DATA hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	3.2	—	ns
t_{CL}	DCLK low time	3.2	—	ns
t_{CLK}	DCLK period	7.5	—	ns
f_{MAX}	DCLK frequency	—	100 [3]	MHz
t_{CD2UM}	CONF_DONE high to user mode [2]	300	650	µs

Table 9–14. FPP Timing Parameters for Cyclone III Device Family   (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with **CLKUSR** option on	t_{CD2CU} + (initialization clock cycles × CLKUSR period) [4]	—	—

Notes to Table 9–14:

(1) This value is applicable if users do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting up the device.

(3) Cyclone III EP3C5, EP3C10, EP3C16, EP3C25, and EP3C40 devices support a DCLK f_{MAX} of 133 MHz. Cyclone III EP3C55, EP3C80, EP3C120 and all the Cyclone III LS devices support a DCLK f_{MAX} of 100 MHz.

(4) For more information about the initialization clock cycles required in Cyclone III device family, refer to Table 9–5 on page 9–10.

JTAG Configuration

JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. You can also use the JTAG circuitry to shift configuration data into the device. The Quartus II software automatically generates **.sof**s that are used for JTAG configuration with a download cable in the Quartus II software programmer.

For more information about JTAG boundary-scan testing, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

For the Cyclone III device, JTAG instructions have precedence over any other device configuration modes. Therefore, JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of a Cyclone III device during PS configuration, PS configuration terminates and JTAG configuration begins. If the Cyclone III device MSEL pins are set to AS mode, the Cyclone III device does not output a DCLK signal when JTAG configuration takes place.

☞ For the Cyclone III LS device, JTAG programming is disabled if the device was already configured using the PS or AS mode. After POR, the Cyclone III LS device allows only mandatory JTAG 1149.1 instructions (BYPASS, SAMPLE/RELOAD, EXTEST, and FACTORY). For more information, refer to "JTAG Instructions" on page 9–60.

The four required pins for a device operating in JTAG mode are TDI, TDO, TMS, and TCK. The TCK pin has an internal weak pull-down resistor while the TDI and TMS pins have weak internal pull-up resistors (typically 25 kΩ). The TDO output pin is powered by V_{CCIO} in I/O bank 1. All the JTAG input pins are powered by the V_{CCIO} pin. All the JTAG pins support only LVTTL I/O standard. All user I/O pins are tri-stated during JTAG configuration. Table 9–15 lists the function of each JTAG pin.

☞ The TDO output is powered by the V_{CCIO} power supply of I/O bank 1.

> For more information about how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

Table 9–15. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data shifts in on the rising edge of TCK. The TDI pin is powered by the V_{CCIO} supply. If the JTAG interface is not required on the board, the JTAG circuitry is disabled by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data shifts out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. The TDO pin is powered by V_{CCIO} in I/O bank 1. If the JTAG interface is not required on the board, the JTAG circuitry is disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions in the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. The TMS pin is powered by the V_{CCIO} supply. If the JTAG interface is not required on the board, the JTAG circuitry is disabled by connecting this pin to V_{CC}.
TCK	Test clock input	Clock input to the BST circuitry. Some operations occur at the rising edge while others occur at the falling edge. The TCK pin is powered by the V_{CCIO} supply. If the JTAG interface is not required on the board, the JTAG circuitry is disabled by connecting this pin to GND.

You can download data to the device on the PCB through the USB-Blaster, MasterBlaster, ByteBlaster II, ByteBlasterMV download cable, and Ethernet-Blaster communications cable during JTAG configuration. Configuring devices using a cable is similar to programming devices in-system. Figure 9–24 and Figure 9–25 show the JTAG configuration of a single Cyclone III device family.

For device V_{CCIO} of 2.5, 3.0, and 3.3 V, refer to Figure 9–24. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using V_{CCIO} of 2.5, 3.0, and 3.3 V, you must power up the V_{CC} of the download cable with a 2.5-V supply from V_{CCA}, and you must pull TCK to ground.

For device V_{CCIO} of 1.2, 1.5, and 1.8 V, refer to Figure 9–25. You can power up the V_{CC} of the download cabled with the supply from V_{CCIO}.

Figure 9–24. JTAG Configuration of a Single Device Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)
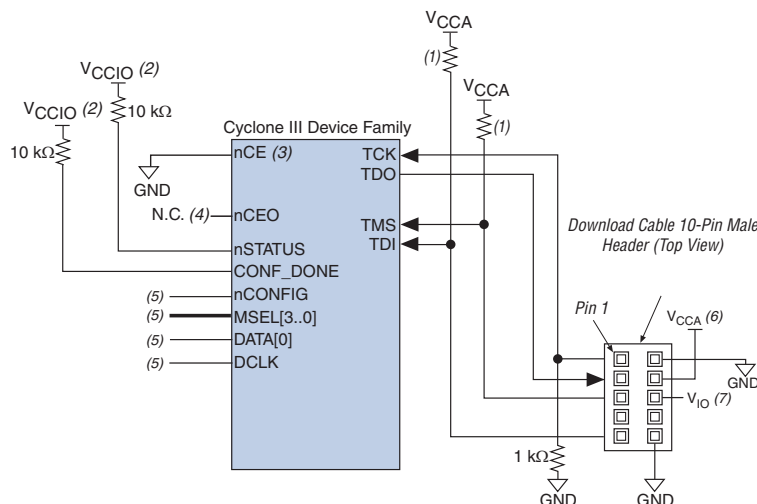
Notes to Figure 9–24:

(1) The resistor value can vary from 1 kΩ to 10 kΩ. Perform signal integrity analysis to select the resistor value for your setup.

(2) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(3) The nCE pin must be connected to GND or driven low for successful JTAG configuration.

(4) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(5) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] either high or low, whichever is convenient on your board.

(6) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, ByteBlasterMV, or Ethernet Blaster cable with a 2.5- V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

(7) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the device's V_{CCA}. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In USB-Blaster, ByteBlaster II, ByteBlasterMV, and Ethernet Blaster, this pin is a no connect.

Figure 9–25. JTAG Configuration of a Single Device Using a Download Cable (1.5-V or 1.8-V V$_{CCIO}$ Powering the JTAG Pins)
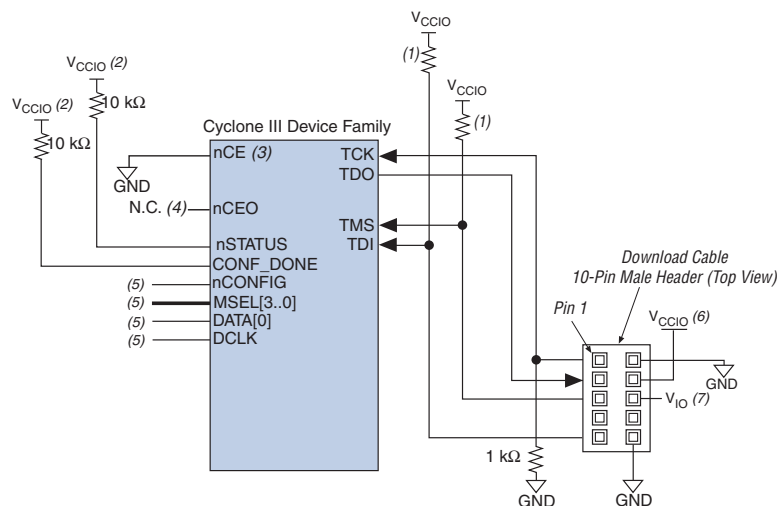
Notes to Figure 9–25:

(1) The resistor value can vary from 1 kΩ to 10 kΩ. Perform signal integrity analysis to select the resistor value for your setup.

(2) Connect these pull-up resistors to the V$_{CCIO}$ supply of the bank in which the pin resides.

(3) The nCE must be connected to GND or driven low for successful JTAG configuration.

(4) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(5) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] either high or low, whichever is convenient on your board.

(6) Power up the V$_{CC}$ of the ByteBlaster II, USB-Blaster, or Ethernet Blaster cable with supply from V$_{CCIO}$. The ByteBlaster II, USB-Blaster, and Ethernet Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the *ByteBlaster II Download Cable User Guide*, *USB-Blaster Download Cable User Guide* and *Ethernet Blaster Communications Cable User Guide*.

(7) In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming; otherwise it is a no connect.

To configure a single device in a JTAG chain, the programming software places all other devices in bypass mode. In bypass mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the TDO pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration upon completion. At the end of configuration, the software checks the state of CONF_DONE through the JTAG port. When the Quartus II software generates a **.jam** for a multi-device chain, it contains instructions to have all devices in the chain initialize at the same time. If CONF_DONE is not high, the Quartus II software indicates that configuration has failed. If CONF_DONE is high, the software indicates that configuration was successful. After the configuration bitstream is serially sent using the JTAG TDI port, the TCK port clocks an additional clock cycle to perform device initialization.

Cyclone III device family has dedicated JTAG pins that function as JTAG pins. You can perform JTAG testing on Cyclone III device family before, during, and after configuration. Cyclone III device family supports the BYPASS, IDCODE, and SAMPLE instructions during configuration without interrupting configuration. All other JTAG instructions can only be issued by first interrupting configuration and reprogramming I/O pins using the ACTIVE_DISENGAGE and CONFIG_IO instructions.

The CONFIG_IO instruction allows I/O buffers to be configured using the JTAG port and when issued after the ACTIVE_DISENGAGE instruction interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone III device family or waiting for a configuration device to complete configuration. Prior to issuing the CONFIG_IO instruction, you must issue the ACTIVE_DISENGAGE instruction. This is because in Cyclone III device family, the CONFIG_IO instruction does not hold nSTATUS low until reconfiguration, so you must disengage the active configuration mode controller when active configuration is interrupted. The ACTIVE_DISENGAGE instruction places the active configuration mode controllers in an idle state prior to JTAG programming. Additionally, the ACTIVE_ENGAGE instruction allows you to re-engage a disengaged active configuration mode controller.

☞ You must follow a specific flow when executing the CONFIG_IO, ACTIVE_DISENGAGE, and ACTIVE_ENGAGE JTAG instructions in Cyclone III device family. For more information about the instruction flow, refer to "JTAG Instructions" on page 9–60.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Cyclone III device family do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration, consider the dedicated configuration pins. Table 9–16 lists how these pins must be connected during JTAG configuration.

Table 9–16. Dedicated Configuration Pin Connections During JTAG Configuration

| Signal	Description
nCE	On all Cyclone III device family in the chain, nCE must be driven low by connecting it to ground, pulling it low using a resistor or driving it by some control circuitry. For devices that are also in multi-device AS, AP, PS, or FPP configuration chains, the nCE pins must be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Cyclone III device family in the chain, nCEO is left floating or connected to the nCE of the next device.
MSEL[3..0]	These pins must not be left floating. These pins support whichever non-JTAG configuration that is used in production. If you only use JTAG configuration, tie these pins to GND.
nCONFIG	Driven high by connecting to the V_CCIO supply of the bank in which the pin resides and pulling up using a resistor or driven high by some control circuitry.
nSTATUS	Pull to the V_CCIO supply of the bank in which the pin resides using a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin must be pulled up to the V_CCIO individually.
CONF_DONE	Pull to the V_CCIO supply of the bank in which the pin resides using a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin must be pulled up to the V_CCIO supply of the bank in which the pin resides individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Must not be left floating. Drive low or high, whichever is more convenient on your board.

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 9–26 and Figure 9–27 show a multi-device JTAG configuration.

For the device V_{CCIO} of 2.5, 3.0, and 3.3 V, refer to Figure 9–26. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using V_{CCIO} of 2.5, 3.0, and 3.3 V, you must power up the V_{CC} of the download cable with a 2.5-V supply from V_{CCA}.

For device V_{CCIO} of 1.2, 1.5, and 1.8 V, refer to Figure 9–27. You can power up the V_{CC} of the download cable with the supply from V_{CCIO}.

Figure 9–26. JTAG Configuration of Multiple Devices Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)
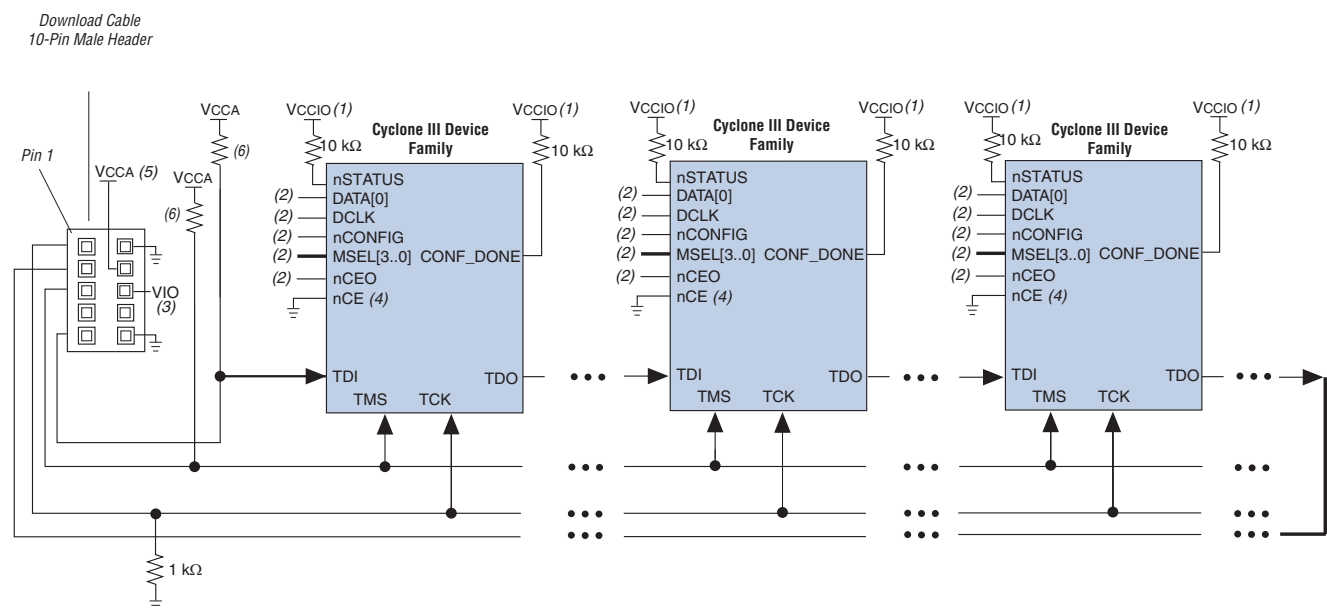
Notes to Figure 9–26:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) The nCE pin must be connected to ground or driven low for successful JTAG configuration.

(5) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5- V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications User Guide*.

(6) The resistor value can vary from 1 kΩ to 10 kΩ Perform signal integrity analysis to select the resistor value for your setup.

Figure 9–27. JTAG Configuration of Multiple Devices Using a Download Cable (1.2, 1.5, and 1.8-V V$_{CCIO}$ Powering the JTAG Pins)
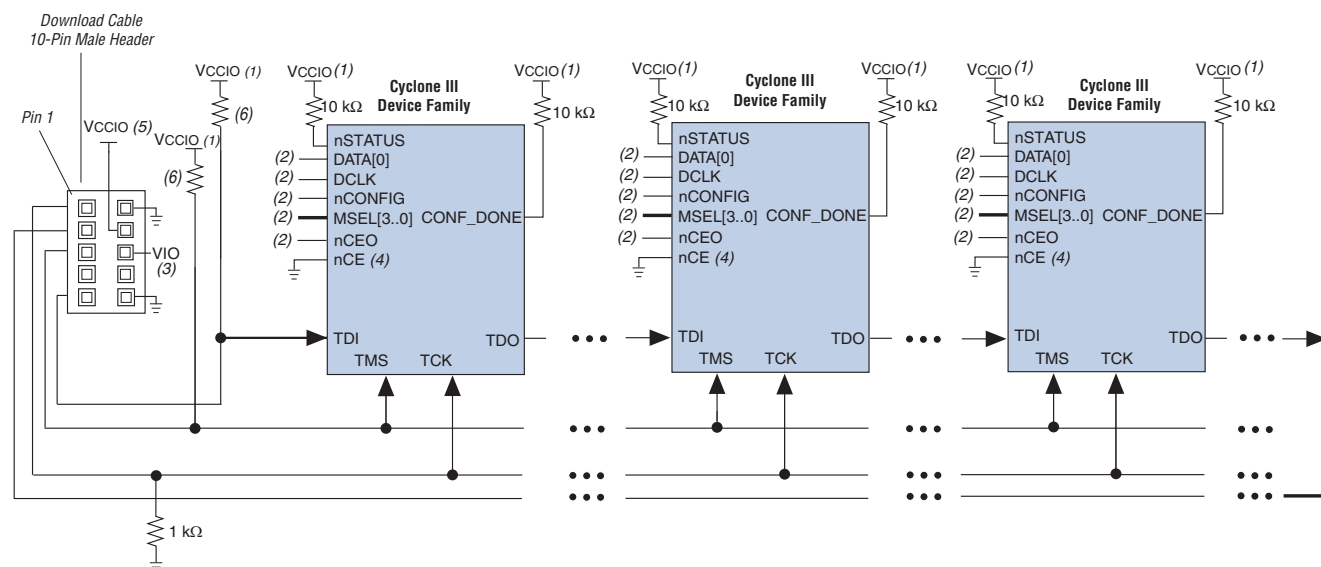
Notes to Figure 9–27:

(1) Connect these pull-up resistors to the V$_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] either high or low, whichever is convenient on your board.

(3) In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) The nCE pin must be connected to ground or driven low for successful JTAG configuration.

(5) Power up the V$_{CC}$ of the ByteBlaster II or USB-Blaster cable with supply from V$_{CCIO}$. The ByteBlaster II and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the *ByteBlaster II Download Cable User Guide* and the *USB-Blaster Download Cable User Guide*.

(6) The resistor value can vary from 1 kΩ to 10 kΩ. Perform signal integrity analysis to select the resistor value for your setup.

☞ All I/O inputs must maintain a maximum AC voltage of 4.1 V. If a non-Cyclone III device family is cascaded in the JTAG-chain, TDO of the non-Cyclone III device family driving into TDI of the Cyclone III device family must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

The nCE pin must be connected to GND or driven low during JTAG configuration. In multi-device AS, AP, PS, and FPP configuration chains, the nCE pin of the first device is connected to GND while its nCEO pin is connected to the nCE pin of the next device in the chain. The inputs of the nCE pin of the last device come from the previous device while its nCEO pin is left floating. In addition, the CONF_DONE and nSTATUS signals are shared in multi-device AS, AP, PS, and FPP configuration chains to ensure that the devices enter user mode at the same time after configuration is complete. When the CONF_DONE and nSTATUS signals are shared among all the devices, every device must be configured when you perform JTAG configuration.

If you only use JTAG configuration, Altera recommends that you connect the circuitry as shown in Figure 9–26 or Figure 9–27, in which each of the CONF_DONE and nSTATUS signals are isolated so that each device can enter user mode individually.

After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, ensure that the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multi-device configuration chain, the nCEO pin of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured. You can place other Altera devices that have JTAG support in the same JTAG chain for device programming and configuration.

☞ JTAG configuration allows an unlimited number of Cyclone III device family to be cascaded in a JTAG chain.

📝 For more information about configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera FPGA Chains* chapter in volume 2 of the *Configuration Handbook*.

Figure 9–28 shows JTAG configuration of a Cyclone III device family with a microprocessor.

Figure 9–28. JTAG Configuration of a Single Device Using a Microprocessor
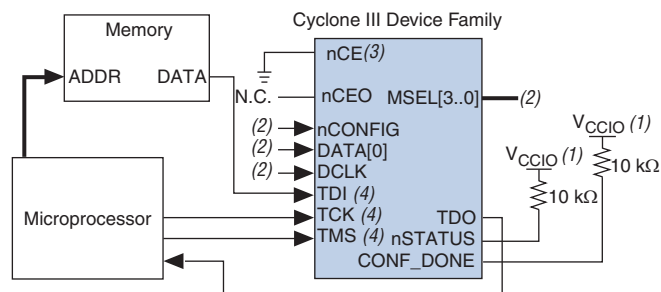
Notes to Figure 9–28:

(1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain.

(2) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] either high or low, whichever is convenient on your board.

(3) The nCE pin must be connected to GND or driven low for successful JTAG configuration.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into TDI, TMS, and TCK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 9–7.

Configuring Cyclone III Device Family with Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

📝 For more information about JTAG and Jam STAPL in embedded environments, refer to *AN 425: Using Command-Line Jam STAPL Solution for Device Programming*. To download the jam player, visit the Altera website (www.altera.com).

Configuring Cyclone III Device Family with the JRunner Software Driver

The JRunner software driver allows you to configure Cyclone III device family through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The supported programming input file is in **.rbf** format. The JRunner software driver also requires a Chain Description File (**.cdf**) generated by the Quartus II software. The JRunner software driver is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

☞ The **.rbf** used by the JRunner software driver cannot be a compressed **.rbf** because the JRunner software driver uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

👣 For more information about the JRunner software driver, refer to *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website at (www.altera.com).

Combining JTAG and AS Configuration Schemes

You can combine the AS configuration scheme with the JTAG-based configuration (Figure 9–29). This setup uses two 10-pin download cable headers on the board. One download cable is used in JTAG mode to configure the Cyclone III device family directly using the JTAG interface. The other download cable is used in AS mode to program the serial configuration device in-system using the AS programming interface. The MSEL[3..0] pins must be set to select AS configuration mode (Table 9–7 on page 9–11). If you try configuring the device using both schemes simultaneously, the JTAG configuration takes precedence and the AS configuration terminates.

Figure 9–29. Combining JTAG and AS Configuration Schemes
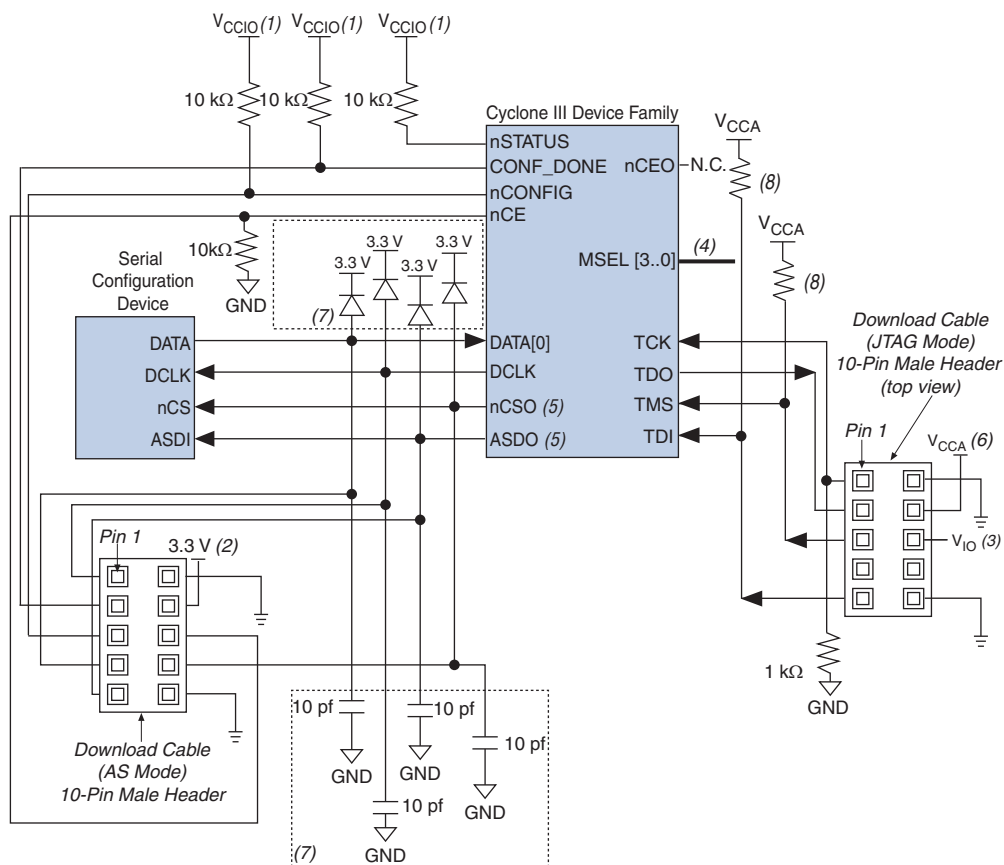
Notes to Figure 9–29:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or Ethernet Blaster cable with the 3.3-V supply.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In ByteBlasterMV, this pin is a no connect. In USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0] for AS configuration schemes, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. This nCSO pin functions as the FLASH_NCE pin in AP mode. The ASDO pin functions as the DATA[1] pin in other AP and FPP modes.

(6) Power up V_{CC} of the ByteBlaster II, USB-Blaster, ByteBlasterMV, or Ethernet Blaster cable with a 2.5- V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

(7) You must place the diodes and capacitors as close as possible to the Cyclone III device family. For effective voltage clamping, Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes. For more information about the interface guidelines using Schottky diodes, refer to *AN 523: Cyclone III Configuration Interface Guidelines with EPCS Devices*.

(8) The resistor value can vary from 1 kΩ to 10 kΩ. Perform signal integrity analysis to select the resistor value for your setup.

Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone III device family in a single-device or in a multiple-device chain supports in-system programming of a serial configuration device with the JTAG interface using the SFL design. The intelligent host or download cable of the board can use the four JTAG pins on the Cyclone III device family to program the serial configuration device in system, even if the host or download cable cannot access the configuration pins (DCLK, DATA, ASDI, and nCS pins).

The SFL design is a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the Cyclone III device family that uses its JTAG interface to access the EPCS JTAG Indirect Configuration Device Programming (**.jic**) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the SFL design.

In a multiple device chain, you must only configure the master device that controls the serial configuration device. When using this feature, the slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured. To use this feature successfully, set the MSEL[3..0] pins of the master device to select the AS configuration scheme (Table 9–7 on page 9–11). The serial configuration device in-system programming through the Cyclone III device family JTAG interface has three stages, which are described in the following sections:

- "Loading the SFL Design" on page 9–58
- "ISP of the Configuration Device" on page 9–59
- "Reconfiguration" on page 9–60

Loading the SFL Design

The SFL design is a design inside the Cyclone III device family that bridges the JTAG interface and the AS interface with glue logic.

The intelligent host uses the JTAG interface to configure the master device with a SFL design. The SFL design allows the master device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and active-low chip select (nCS) pins.

If you configure a master device with a SFL design, the master device enters user mode even though the slave devices in the multiple device chain are not being configured. The master device enters user mode with a SFL design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 9–30 shows the JTAG configuration of a single Cyclone III device family with a SFL design.

Figure 9–30. Programming Serial Configuration Devices In-System Using the JTAG Interface

Notes to Figure 9–30:
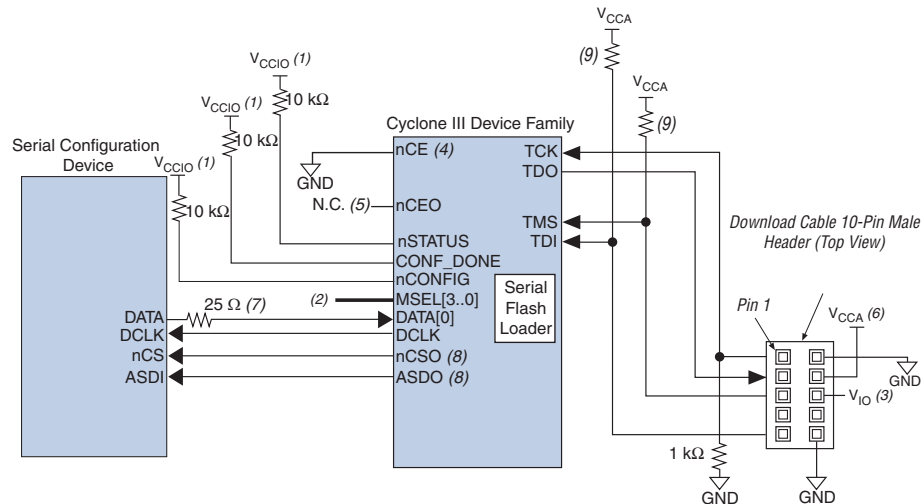
(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0] for AS configuration schemes, refer to Table 9–7 on page 9–11. Connect the MSEL pins directly to V_{CCA} or GND.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In ByteBlasterMV, this pin is a no connect. In USB-Blaster, ByteBlaster II, and Ethernet Blaster, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) The nCE pin must be connected to GND or driven low for successful JTAG configuration.

(5) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(6) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, ByteBlasterMV, or Ethernet Blaster cable with a 2.5-V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

(7) Connect the series resistor at the near end of the serial configuration device.

(8) These are dual-purpose I/O pins. The nCSO pin functions as the FLASH_nCE pin in AP mode. The ASDO pin functions as the DATA[1] pin in other AP and FPP modes.

(9) The resistor value can vary from 1 kΩ to 10 kΩ. Perform signal integrity analysis to select the resistor value for your setup.

ISP of the Configuration Device

In the second stage, the SFL design in the master device allows you to write the configuration data for the device chain into the serial configuration device with the Cyclone III device family JTAG interface. The JTAG interface sends the programming data for the serial configuration device to the Cyclone III device family first. The Cyclone III device family then uses the ASMI pins to send the data to the serial configuration device.

Reconfiguration

After the configuration data is successfully written into the serial configuration device, the Cyclone III device family does not reconfigure by itself. The intelligent host issues the PULSE_NCONFIG JTAG instruction to initialize the reconfiguration process. During reconfiguration, the master device is reset and the SFL design no longer exists in the Cyclone III device family and the serial configuration device configures all the devices in the chain with your user design.

For more information about SFL, refer to *AN 370: Using the Serial FlashLoader with Quartus II Software.*

JTAG Instructions

This section describes the instructions that are necessary for JTAG configuration for the Cyclone III device family. Table 9–17 lists the supported JTAG instructions.

Table 9–17. JTAG Instructions

JTAG Instruction	Cyclone III Device	Cyclone III LS Device
CONFIG_IO	✓	✓
ACTIVE_DISENGAGE	✓	✓
ACTIVE_ENGAGE	✓	✓
EN_ACTIVE_CLK	✓	—
DIS_ACTIVE_CLK	✓	—
APFC_BOOT_ADDR	✓	—
FACTORY [1]	—	✓
KEY_PROG_VOL [2]	—	✓
KEY_CLR_VREG [2]	—	✓

Notes to Table 9–17:

(1) In Cyclone III LS devices, the CONFIG_IO, ACTIVE_DISENGAGE, PULSE_NCONFIG, and PROGRAM instructions are supported, provided that the FACTORY instruction is executed. It is not necessary to execute the FACTORY instruction prior to the JTAG configuration in Cyclone III devices because this instruction is used for Cyclone III LS devices only.

(2) Use the KEY_PROG_VOL and KEY_CLR_VREG instructions for the design security feature. For more information, refer to "Design Security" on page 9–70.

For more information about the JTAG binary instruction code, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

For Cyclone III LS devices, the device can only allow mandatory JTAG 1149.1 instructions after POR. These instructions are BYPASS, SAMPLE/PRELOAD, EXTEST and FACTORY. To enable the access of other JTAG instructions, issue the FACTORY instruction. The FACTORY instruction puts the device in a state in which it is ready for in-house testing and board-level testing and it must be executed before configuration starts. When this instruction is executed, the CRAM bits content and volatile key are cleared and the device is reset.

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I/O Reconfiguration

Use the CONFIG_IO instruction to reconfigure the I/O configuration shift register (IOCSR) chain. This instruction allows you to perform board-level testing prior to configuring the Cyclone III device family or waiting for a configuration device to complete configuration. After the configuration is interrupted and JTAG testing is complete, the part must be reconfigured using the PULSE_NCONFIG JTAG instruction or by pulsing the nCONFIG pin low.

You can issue the CONFIG_IO instruction any time during user mode. The CONFIG_IO instruction cannot be issued when nCONFIG pin is asserted low (during power up) or immediately after issuing a JTAG instruction that triggers reconfiguration. For more information about the wait-time for issuing the CONFIG_IO instruction, refer to Table 9–18.

When using CONFIG_IO instruction, you must meet the following timing restrictions:

■ CONFIG_IO instruction cannot be issued during the nCONFIG pin low

■ Observe 230 µs minimum wait time after any of the following conditions are met:

   ■ nCONFIG pin goes high

   ■ Issuing the PULSE_NCONFIG instruction

   ■ Issuing the ACTIVE_ENGAGE instruction, before issuing the CONFIG_IO instruction

■ Wait 230 µs after power up with nCONFIG pin high before issuing the CONFIG_IO instruction (or wait for the nSTATUS pin to go high)

Table 9–18. Wait Time for Issuing the CONFIG_IO Instruction

Wait Time	Time
Wait time after the nCONFIG pin is released	230 µs
Wait time after PULSE_NCONFIG or ACTIVE_ENGAGE is issued	230 µs

Use the ACTIVE_DISENGAGE instruction with CONFIG_IO instruction to interrupt configuration. Table 9–19 lists the sequence of instructions to use for various CONFIG_IO usage scenarios.

Table 9–19. JTAG CONFIG_IO (without JTAG_PROGRAM) Instruction Flows [(1)] **(Part 1 of 2)**

JTAG Instruction	Configuration Scheme and Current State of the Cyclone III Device Family											
	Prior to User Mode (Interrupting Configuration)				User Mode				Power Up			
	PS	FPP	AS	AP [(4)]	PS	FPP	AS	AP [(4)]	PS	FPP	AS	AP [(4)]
FACTORY	NA	NA	NA	NA	NA	NA	NA	NA	R	R	R	NA
ACTIVE_DISENGAGE	0	0	0	0	0	0	0	0	—	—	—	—
CONFIG_IO	R	R	R	R	R	R	R	R	NA	NA	NA	NA
JTAG Boundary Scan Instructions (no JTAG_PROGRAM)	0	0	0	0	0	0	0	0	—	—	—	—

Table 9–19. JTAG CONFIG_IO (without JTAG_PROGRAM) Instruction Flows [1] **(Part 2 of 2)**

JTAG Instruction	Configuration Scheme and Current State of the Cyclone III Device Family											
	Prior to User Mode (Interrupting Configuration)				User Mode				Power Up			
	PS	FPP	AS	AP [4]	PS	FPP	AS	AP [4]	PS	FPP	AS	AP [4]
ACTIVE_ENGAGE	A	A	R [2]	R [2]	A	A	R [2]	R [2]	—	—	—	—
PULSE_NCONFIG			A [3]	A [3]			0	0	—	—	—	—
Pulse nCONFIG pin			A [3]	A [3]			0	0	—	—	—	—
JTAG TAP Reset	R	R	R	R	R	R	R	R	—	—	—	—

Notes to Table 9–19:

(1) "R" indicates that the instruction is to be executed before the next instruction, "O" indicates the optional instruction, "A" indicates that the instruction must be executed, and "NA" indicates that the instruction is not allowed in this mode.

(2) Required if you use ACTIVE_DISENGAGE.

(3) Neither of the instruction is required if you use ACTIVE_ENGAGE.

(4) AP configuration is for Cyclone III devices only.

The CONFIG_IO instruction does not hold the nSTATUS pin low until reconfiguration. You must disengage the active configuration controllers (AS and AP) by issuing the ACTIVE_DISENGAGE and ACTIVE_ENGAGE instructions when the active configuration is interrupted. You must issue the ACTIVE_DISENGAGE instruction alone or prior to the CONFIG_IO instruction if the JTAG_PROGRAM instruction is to be issued later (Table 9–20). This puts the active configuration controllers into the idle state. The active configuration controller is re-engaged after user mode is reached using JTAG programming (Table 9–20).

☞ While executing the CONFIG_IO instruction, all user I/Os are tri-stated.

If reconfiguration after interruption is performed using configuration modes (rather than using JTAG_PROGRAM), it is not necessary to issue the ACTIVE_DISENGAGE instruction prior to CONFIG_IO. You can start reconfiguration by either pulling the nCONFIG pin low for at least 500 ns, or issuing the PULSE_NCONFIG instruction. If the ACTIVE_DISENGAGE instruction was issued and the JTAG_PROGRAM instruction fails to enter user mode, you must issue the ACTIVE_ENGAGE instruction to reactivate the active configuration controller. Issuing the ACTIVE_ENGAGE instruction also triggers the reconfiguration in configuration modes; therefore, it is not necessary to pull the nCONFIG pin low or issue the PULSE_NCONFIG instruction.

ACTIVE_DISENGAGE

The ACTIVE_DISENGAGE instruction places the active configuration controller (AS and AP) into an idle state prior to JTAG programming. The active configuration controller is the AS controller when the MSEL pins are set to AS configuration scheme and the AP controller when the MSEL pins are set to the AP configuration scheme. The two purposes of placing the active controllers in an idle state are:

■ To ensure that they are not trying to configure the device in their respective configuration modes during JTAG programming

■ To allow the controllers to properly recognize a successful JTAG programming that results in the device reaching user mode

The ACTIVE_DISENGAGE instruction is required before JTAG programming regardless of the current state of the Cyclone III device family if the MSEL pins are set to an active configuration scheme (AS or AP). If the ACTIVE_DISENGAGE instruction is issued during a passive configuration scheme (PS or FPP), it has no effect on the Cyclone III device family. Similarly, the CONFIG_IO instruction is issued after an ACTIVE_DISENGAGE instruction, but is no longer required to properly halt configuration. Table 9–20 lists the required, recommended, and optional instructions for each configuration mode. The ordering of the required instructions is a hard requirement and must be met to ensure functionality.

Table 9–20. JTAG Programming Instruction Flows [1]

JTAG Instruction	Configuration Scheme and Current State of the Cyclone III Device											
	Prior to User Mode (Interrupting Configuration)				User Mode				Power Up			
	PS	**FPP**	**AS**	**AP** [2]	**PS**	**FPP**	**AS**	**AP** [2]	**PS**	**FPP**	**AS**	**AP** [2]
FACTORY	NA	NA	NA	NA	NA	NA	NA	NA	R	R	R	NA
ACTIVE_DISENGAGE	O	O	R	R	O	O	O	R	O	O	R	R
CONFIG_IO	Rc	Rc	O	O	O	O	O	O	NA	NA	NA	NA
Other JTAG instructions	O	O	O	O	O	O	O	O	O	O	O	O
JTAG_PROGRAM	R	R	R	R	R	R	R	R	R	R	R	R
CHECK_STATUS	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
JTAG_STARTUP	R	R	R	R	R	R	R	R	R	R	R	R
JTAG TAP Reset/ other instruction	R	R	R	R	R	R	R	R	R	R	R	R

Notes to Table 9–20:

(1) "R" indicates that the instruction is required to be executed before the next instruction, "O" indicates the optional instruction, "Rc" indicates the recommended instruction, and "NA" indicates that the instruction is not allowed to be executed in this mode.

(2) AP configuration is for Cyclone III devices only.

In AS or AP configuration schemes, the ACTIVE_DISENGAGE instruction puts the active configuration controllers into idle state. If a successful JTAG programming is executed, the active controllers are automatically re-engaged after user mode is reached using JTAG programming. This causes the active controllers to transition to their respective user mode states.

If JTAG programming fails to get the Cyclone III device family to enter user mode and re-engage active programming, there are available methods to achieve this for the AS or AP configuration schemes:

■ When in the AS configuration scheme, you can re-engage the AS controller by moving the JTAG TAP controller to the reset state or by issuing the ACTIVE_ENGAGE instruction.

■ When in the AP configuration scheme, the only way to re-engage the AP controller is to issue the ACTIVE_ENGAGE instruction. In this case, asserting the nCONFIG pin does not re-engage either active controller.

ACTIVE_ENGAGE

The `ACTIVE_ENGAGE` instruction allows you to re-engage a disengaged active controller. You can issue this instruction any time during configuration or user mode to re-engage an already disengaged active controller as well as trigger reconfiguration of the Cyclone III device family in the active configuration scheme specified by the MSEL pin settings.

The `ACTIVE_ENGAGE` instruction functions as the `PULSE_NCONFIG` instruction when the device is in passive configuration schemes (PS or FPP). The `nCONFIG` pin is disabled when the `ACTIVE_ENGAGE` instruction is issued.

☞ Altera does not recommend using the `ACTIVE_ENGAGE` instruction but it is provided as a fail-safe instruction for re-engaging the active configuration (AS or AP) controllers.

Changing the Start Boot Address of the AP Flash

In the AP configuration scheme, for Cyclone III devices only, you can change the default configuration boot address of the parallel flash memory to any desired address using the `APFC_BOOT_ADDR` JTAG instruction.

APFC_BOOT_ADDR

The `APFC_BOOT_ADDR` instruction is for Cyclone III devices only and allows you to define a start boot address for the parallel flash memory in the AP configuration scheme.

This instruction shifts in a start boot address for the AP flash. When this instruction becomes the active instruction, the `TDI` and `TDO` pins are connected through a 22-bit active boot address shift register. The shifted-in boot address bits get loaded into the 22-bit AP boot address update register, which feeds into the AP controller. The content of the AP boot address update register can be captured and shifted-out of the active boot address shift register from `TDO`.

The boot address in the boot address shift register and update register are shifted to the right (in the LSB direction) by two bits versus the intended boot address. The reason for this is that the two LSB of the address are not accessible. When this boot address is fed into the AP controller, two 0s are attached in the end as LSB, thereby pushing the shifted-in boot address to the left by two bits, which become the actual AP boot address the AP controller gets.

If you have enabled the remote update feature, the `APFC_BOOT_ADDR` instruction sets the boot address for the factory configuration only.

☞ The `APFC_BOOT_ADDR` instruction is retained after reconfiguration while the system board is still powered on. However, you must reprogram the instruction whenever you restart the system board.

Device Configuration Pins

Table 9–21 through Table 9–23 describe the connections and functionality of all the configuration-related pins on Cyclone III device family.

Table 9–21 lists the Cyclone III device family pin configuration.

Table 9–21. Cyclone III Device Family Configuration Pin Summary

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
1	FLASH_nCE, nCSO	Output	—	V_{CCIO}	AS, AP [2]
6	CRC_ERROR	Output	—	V_{CCIO}/Pull-up [1]	Optional, all modes
1	DATA[0]	Input	Yes	V_{CCIO}	PS, FPP, AS
		Bidirectional		V_{CCIO}	AP [2]
1	DATA[1], ASDO	Input	—	V_{CCIO}	FPP
		Output		V_{CCIO}	AS
		Bidirectional		V_{CCIO}	AP [2]
8	DATA[7..2]	Input	—	V_{CCIO}	FPP
		Bidirectional		V_{CCIO}	AP [2]
8	DATA[15..8]	Bidirectional	—	V_{CCIO}	AP [2]
6	INIT_DONE	Output	—	Pull-up	Optional, all modes
1	nSTATUS	Bidirectional	Yes	Pull-up	All modes
1	nCE	Input	Yes	V_{CCIO}	All modes
1	DCLK	Input	Yes	V_{CCIO}	PS, FPP
		Output		V_{CCIO}	AS, AP [2]
6	CONF_DONE	Bidirectional	Yes	Pull-up	All modes
1	TDI	Input	Yes	V_{CCIO}	JTAG
1	TMS	Input	Yes	V_{CCIO}	JTAG
1	TCK	Input	Yes	V_{CCIO}	JTAG
1	nCONFIG	Input	Yes	V_{CCIO}	All modes
6	CLKUSR	Input	—	V_{CCIO}	Optional
6	nCEO	Output	—	V_{CCIO}	Optional, all modes
6	MSEL[3..0]	Input	Yes	V_{CCINT}	All modes
1	TDO	Output	Yes	V_{CCIO}	JTAG
7	PADD[14..0]	Output	—	V_{CCIO}	AP [2]
8	PADD[19..15]	Output	—	V_{CCIO}	AP [2]
6	PADD[23..20]	Output	—	V_{CCIO}	AP [2]
1	nRESET	Output	—	V_{CCIO}	AP [2]
6	nAVD	Output	—	V_{CCIO}	AP [2]
6	nOE	Output	—	V_{CCIO}	AP [2]
6	nWE	Output	—	V_{CCIO}	AP [2]
5	DEV_OE	Input	—	V_{CCIO}	Optional, AP [2]
5	DEV_CLRn	Input	—	V_{CCIO}	Optional, AP [2]

Notes to Table 9–21:

(1) In Cyclone III devices, the CRC_ERROR pin is a dedicated output by default. Optionally, you can enable the CRC_ERROR pin as an open-drain output in the **CRC Error Detection** tab from the **Device and Pin Options** dialog box.

(2) AP configuration is for Cyclone III devices only.

Table 9–22 lists the dedicated configuration pins that must be connected properly on your board for successful configuration. Some of these pins may not be required for your configuration scheme.

Table 9–22. Dedicated Configuration Pins on Cyclone III Device Family (Part 1 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
MSEL [3..0]	N/A	All	Input	4-bit configuration input that sets the Cyclone III device family configuration scheme. These pins must be hardwired to V_{CCA} or GND. The MSEL[3..0] pins have internal 9-kΩ pull-down resistors that are always active. Some of the smaller devices or package options of Cyclone III devices do not have the MSEL[3] pin; therefore, the AP configuration scheme is not supported.
nCONFIG	N/A	All	Input	Configuration control input. Pulling this pin low with external circuitry during user mode causes the Cyclone III device family to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level starts a reconfiguration.
nSTATUS	N/A	All	Bidirectional open-drain	The Cyclone III device family drives nSTATUS low immediately after power-up and releases it after the POR time. ■ Status output. If an error occurs during configuration, nSTATUS is pulled low by the target device. ■ Status input. If an external source (for example, another Cyclone III device family) drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. Driving nSTATUS low after configuration and initialization does not affect the configured device. If you use a configuration device, driving nSTATUS low causes the configuration device to attempt to configure the device, but because the device ignores transitions on nSTATUS in user mode, the device does not reconfigure. To start a reconfiguration, nCONFIG must be pulled low.
CONF_DONE	N/A	All	Bidirectional open-drain	■ Status output. The target Cyclone III device family drives the CONF_DONE pin low before and during configuration. After all configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. ■ Status input. After all data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect bus holds or ADC to the CONF_DONE pin.

Table 9–22. Dedicated Configuration Pins on Cyclone III Device Family (Part 2 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the Cyclone III device family with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user-mode. In a single-device configuration, it must be tied low. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to the nCE pin of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the device.
nCEO	N/A if option is on. I/O if option is off.	All	Output open drain	Output that drives low when configuration is complete. In a single-device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In a multi-device configuration, this pin feeds the nCE pin of the next device. The nCEO of the last device in the chain is left floating or is used as a user I/O pin after configuration. If you use the nCEO pin to feed the nCE pin of the next device, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. If you use the nCEO pin as a user I/O pin after configuration, set the state of the pin on the **Dual-Purpose Pin** settings.
FLASH_nCE, nCSO [1], [2]	I/O	AS, AP [3]	Output	Output control signal from the Cyclone III device family to the serial configuration device in AS mode that enables the configuration device. This pin functions as the nCSO pin in AS mode and the FLASH_NCE pin in AP mode. Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash. Connects to the CE# pin on the Micron P30 or P33 flash. [3] This pin has an internal pull-up resistor that is always active.
DCLK [1], [2]	N/A	PS, FPP, AS, AP [3]	Input (PS, FPP). Output (AS, AP [3])	In PS and FPP configuration, DCLK is the clock input used to clock data from an external source into the target Cyclone III device family. Data is latched into the device on the rising edge of DCLK. In AS mode, DCLK is an output from the Cyclone III device family that provides timing for the configuration interface, it has an internal pull-up resistor (typically 25 kΩ) that is always active. In AP mode, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. [3] In active configuration schemes (AS or AP), this pin will be driven into an inactive state after configuration completes. Alternatively, in active schemes, you can use this pin as a user I/O during user mode. In passive schemes (PS or FPP) that use a control host, DCLK must be driven either high or low, whichever is more convenient. In passive schemes, you cannot use DCLK as a user I/O in user mode. Toggling this pin after configuration does not affect the configured device

Table 9–22. Dedicated Configuration Pins on Cyclone III Device Family (Part 3 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DATA[0] [1], [2]	I/O	PS, FPP, AS, AP [3]	Input (PS, FPP, AS). Bidirectional (AP) [3]	Data input. In serial configuration modes, bit-wide configuration data is presented to the target Cyclone III device family on the DATA[0] pin. In AS mode, DATA[0] has an internal pull-up resistor that is always active. After AS configuration, DATA[0] is a dedicated input pin with optional user control. After PS or FPP configuration, DATA[0] is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings. After AP configuration, DATA[0] is a dedicated bidirectional pin with optional user control. [3]
DATA[1], ASDO [1], [2]	I/O	FPP, AS, AP [3]	Input (FPP), Output (AS). Bidirectional (AP) [3]	Data input in non-AS mode. Control signal from the Cyclone III device family to the serial configuration device in AS mode used to read out configuration data. The DATA[1] pin functions as the ASDO pin in AS mode. In AS mode, DATA[1] has an internal pull-up resistor that is always active. After AS configuration, DATA[1] is a dedicated output pin with optional user control. In PS configuration scheme, DATA[1] functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA[1] is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings. In AP configuration scheme, which is for Cyclone III devices only, the byte-wide or word-wide configuration data is presented to the target Cyclone III device on DATA[7..0] or DATA[15..0], respectively. After AP configuration, DATA[1] is a dedicated bidirectional pin with optional user control. [3]
DATA[7..2]	I/O	FPP, AP [3]	Inputs (FPP). Bidirectional (AP) [3]	Data inputs. In AS or PS configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pin depends on the **Dual-Purpose Pin** settings. The byte-wide or word-wide configuration data is presented to the target Cyclone III device on DATA[7..0] or DATA[15..0], respectively, in the AP configuration scheme (for Cyclone III devices only). After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control. [3]
DATA[15..8]	I/O	AP [3]	Bidirectional	Data inputs. Word-wide configuration data is presented to the target Cyclone III device on DATA[15..0]. In PS, FPP, or AS configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15:8] are dedicated bidirectional pins with optional user control.

Table 9–22. Dedicated Configuration Pins on Cyclone III Device Family (Part 4 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
PADD[23..0]	I/O	AP [3]	Output	24-bit address bus from the Cyclone III device to the parallel flash in AP mode. Connects to the A[24:1] bus on the Micron P30 or P33 flash.
nRESET	I/O	AP [3]	Output	Active-low reset output. Driving the nRESET pin low resets the parallel flash. Connects to the RST# pin on the Micron P30 or P33 flash.
nAVD	I/O	AP [3]	Output	Active-low address valid output. Driving the nAVD pin low during a read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus. Connects to the ADV# pin on the Micron P30 or P33 flash.
nOE	I/O	AP [3]	Output	Active-low output enable to the parallel flash. Driving the nOE pin low during a read operation enables the parallel flash outputs (DATA[15..0]). Connects to the OE# pin on the Micron P30 or P33 flash.
nWE	I/O	AP [3]	Output	Active-low write enable to the parallel flash. Driving the nWE pin low during a write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid. Connects to the WE# pin on the Micron P30 or P33 flash.

Note to Table 9–22:

(1) If you are accessing the EPCS device with the ALTASMI_PARALLEL megafunction or your own user logic in user mode, in the **Device and Pin Options** window of the Quartus II software, in the **Dual-Purpose Pins** category, select **Use as regular I/O** for this pin.

(2) To tri-state the AS configuration pins in user mode, turn on the **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box in the **Configuration** tab. This option tri-states the DCLK, DATA0, nCSO, and ASDO pins.

(3) AP configuration scheme is for Cyclone III devices only.

Table 9–23 lists the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 9–23. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	Optional user-supplied clock input synchronizes the initialization of one or more devices. This pin is enabled by turning on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Status pin used to indicate when the device has initialized and is in user-mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. After the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software. The functionality of this pin changes if the **Enable OCT_DONE** option is enabled in the Quartus II software. This option controls whether the INIT_DONE signal is gated by the OCT_DONE signal, which indicates the Power-Up OCT calibration is complete. If this option is turned off, the INIT_DONE signal is not gated by the OCT_DONE signal
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the **Enable device-wide output enable (DEV_OE)** option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset (DEV_CLRn)** option in the Quartus II software.

Design Security

The design security feature is for Cyclone III LS devices only. The design security feature is not supported in Cyclone III devices.

Cyclone III LS Design Security Protection

Cyclone III LS device designs are protected from copying, reverse engineering, and tampering using configuration bitstream encryption and anti-tamper features.

Security Against Copying

The volatile key is securely stored in the Cyclone III LS device and cannot be read out through any interfaces. The information of your design cannot be copied because the configuration file read-back feature is not supported in Cyclone III LS devices.

Security Against Reverse Engineering

Reverse engineering from an encrypted configuration file is very difficult and time consuming because Cyclone III LS configuration file formats are proprietary and the file contains million of bits which require specific decryption. Reverse engineering the Cyclone III LS device is just as difficult because the device is manufactured on the advanced 60-nm process technology.

Security Against Tampering

Cyclone III LS devices support the following anti-tamper features:

- Ability to limit JTAG instruction set and provides protection against configuration data readback over the JTAG port

- Ability to clear contents of FPGA logic, configuration memory, user memory, and volatile key

- Error detection (ED) cycle indicator to core Cyclone III LS devices provide a pass or fail indicator at every ED cycle and visibility over intentional or unintentional change of CRAM bits.

For more information about anti-tamper protection for Cyclone III LS devices, refer to *AN 593: Anti-Tamper Protection for Cyclone III LS Devices*.

For more information about the implementation of secure configuration flow in Quartus II, refer to *AN 589: Using Design Security Feature in Cyclone III LS Devices*.

AES Decryption Block

The main purpose of the AES decryption block is to decrypt the configuration bitstream prior to entering configuration. Prior to receiving encrypted data, you must enter and store the 256-bit volatile key in the device with battery backup. The key is scrambled prior to storing it in the key storage to make it more difficult for anyone to retrieve the stored key using de-capsulation of the device.

Key Storage

Cyclone III LS devices support volatile key programming. Table 9–24 lists the volatile key features.

Table 9–24. Security Key Features   (Part 1 of 2)

Volatile Key Features	Description
Key programmability	Reprogrammable and erasable
External battery	Required
Key programming method [(1)]	On-board

Table 9–24. Security Key Features   (Part 2 of 2)

Volatile Key Features	Description
Design protection	Secure against copying, reverse engineering, and tampering

Note to Table 9–24:

(1) Key programming is carried out using the JTAG interface.

AES volatile key zeroization is supported in Cyclone III LS devices. The volatile key clear and key program JTAG instructions from the device core is supported to protect Cyclone III LS devices against tampering. You can clear and reprogram the key from the device core whenever tampering attempt is detected by executing the KEY_CLR_VREG and KEY_PROG_VOL JTAG instructions to clear and reprogram the volatile key, and then reset the Cyclone III LS device by pulling the nCONFIG pin low for at least 500 ns. When nCONFIG returns to a logic-high level and nSTATUS is released by the Cyclone III LS device, reconfiguration begins to configure the Cyclone III LS device with a benign or unencrypted configuration file. After configuration is successfully completed, observe the cyclecomplete signal from error detection block to ensure that reconfigured CRAM bits content is correct for at least one error detection cycle. You can also observe the cyclecomplete and crcerror signals for any unintentional CRAM bits change.

☞ cyclecomplete is a signal that is routed from the error detection block to the core for the purpose of every complete error detection cycle. You must include the cycloneiiils_crcblock WYSIWYG atom in your design to use the cyclecomplete signal. For more information about the SEU mitigation, refer to the *SEU Mitigation in Cyclone III Devices* chapter.

V_{CCBAT} is a dedicated power supply for the volatile key storage and not shared with other on-chip power supplies, such as V_{CCIO} or V_{CC}. V_{CCBAT} continuously supplies power to the volatile register regardless of the on-chip supply condition. The nominal voltage for this supply is 3.0 V, while its valid operating range is from 1.2 to 3.3 V. If you do not use the volatile security key, you may connect the V_{CCBAT} to a 1.8-V, 2.5-V, or 3.0-V power supply.

☞ After power-up, wait for 200 ms (Standard POR) or 9 ms (Fast POR) before beginning the key programming to ensure that V_{CCBAT} is at its full rail.

☞ As an example, BR1220 (-30°C to +80°C) and BR2477A (-40 C to +125°C) are lithium coin-cell type batteries used for volatile key storage purposes.

☞ For more information about the battery specifications, refer to the *Cyclone III LS Device Data Sheet* chapter.

Cyclone III LS Design Security Solution

Cyclone III LS devices are SRAM-based devices. To provide design security, Cyclone III LS devices require a 256-bit volatile key for configuration bitstream encryption.

The Cyclone III LS design security feature provides routing architecture optimization for design separation flow with the Quartus II software. Design separation flow achieves both physical and functional isolation between design partitions.

For more information about the design separation flow, refer to *AN 567: Quartus II Design Separation Flow.*

You can carry out secure configuration in Steps 1–3, as shown in Figure 9–31:

1. Generate the encryption key programming file and encrypt the configuration data.

   The Quartus II configuration software uses the user-defined 256-bit volatile keys to generate a key programming file and an encrypted configuration file. The encrypted configuration file is stored in an external memory, such as a flash memory or a configuration device.

2. Program the volatile key into the Cyclone III LS device.

   Program the user-defined 256-bit volatile keys into the Cyclone III LS device through the JTAG interface.

3. Configure the Cyclone III LS device.

   At system power-up, the external memory device sends the encrypted configuration file to the Cyclone III LS device.

Figure 9–31. Cyclone III LS Secure Configuration Flow [1]
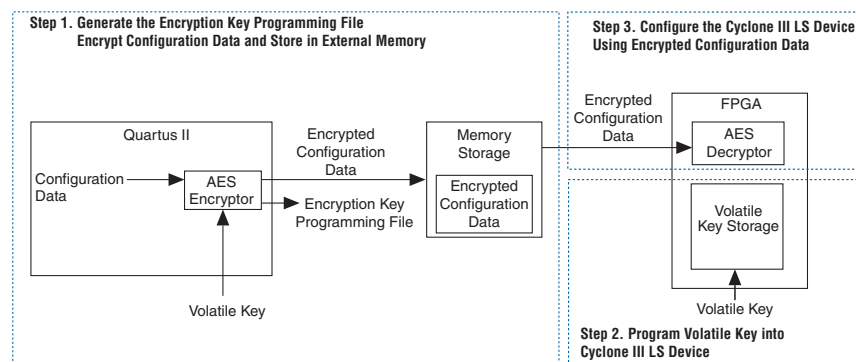
Note to Figure 9–31:

(1) Step 1, Step 2, and Step 3 correspond to the procedure detailed in "Cyclone III LS Design Security Solution".

Available Security Modes

There are several security modes available on Cyclone III LS devices, they are:

■ Volatile Key

■ No Key Operation

■ FACTORY Mode

Volatile Key

Secure operation with volatile key programmed and required external battery—this mode accepts both encrypted and unencrypted configuration bitstreams. Use the unencrypted configuration bitstream support for board-level testing only.

No Key Operation

Only unencrypted configuration bitstreams are allowed to configure the device.

FACTORY Mode

After power up, Cyclone III LS devices must be in FACTORY mode to program the volatile key. The FACTORY private JTAG instruction must be issued after the device successfully exits from POR and before the device starts loading the core configuration data to enable access to all other instructions from the JTAG pins. The device configuration data and AES volatile key are cleared if the FACTORY instruction is executed.

Table 9–25 lists the configuration bitstream and the configuration mode supported for each security mode.

Table 9–25. Security Modes Supported

Mode	Function	Configuration File	Allowed Configuration Mode
Volatile Key	Secure	Encrypted	PS with AES (without decompression).
			FPP with AES (without decompression).
			Remote update fast AS with AES (without decompression).
			Fast AS (without decompression).
	Board-Level Testing	Unencrypted	All configuration modes that do not engage the design security feature.
No Key	—	Unencrypted	All configuration modes that do not engage the design security feature.
FACTORY	Volatile Key Programming	—	—

Remote System Upgrade

Cyclone III devices support remote system upgrade in AS and AP configuration schemes. Cyclone III LS devices support remote system upgrade in the AS configuration scheme only. Remote system upgrade can also be implemented with advanced Cyclone III features such as real-time decompression of configuration data in the AS configuration scheme.

■ The serial configuration device uses the AS configuration scheme to configure Cyclone III or Cyclone III LS devices

■ The supported parallel flash uses the AP configuration scheme to configure Cyclone III devices

■ Remote system upgrade is not supported in the multi-device configuration chain for any configuration scheme.

Functional Description

The dedicated remote system upgrade circuitry in Cyclone III device family manages remote configuration and provides error detection, recovery, and status information. User logic or a Nios® II processor implemented in the Cyclone III device family logic array provides access to the remote configuration data source and an interface to the configuration memory.

☞ Configuration memory refers to serial configuration devices (EPCS) or supported parallel flash memory, and depends on the configuration scheme that you use.

The remote system upgrade process of Cyclone III device family involves the following steps:

1. A Nios II processor (or user logic) implemented in the Cyclone III device family logic array receives new configuration data from a remote location. The connection to the remote source is a communication protocol such as the transmission control protocol/Internet protocol (TCP/IP), peripheral component interconnect (PCI), user datagram protocol (UDP), universal asynchronous receiver/transmitter (UART), or a proprietary interface.

2. The Nios II processor (or user logic) writes this new configuration data into a configuration memory.

3. The Nios II processor (or user logic) starts a reconfiguration cycle with the new or updated configuration data.

4. The dedicated remote system upgrade circuitry detects and recovers from any error that might occur during or after the reconfiguration cycle, and provides error status information to the user design.

Figure 9–32 shows the steps required for performing remote configuration updates (the numbers in Figure 9–32 coincide with steps 1–4).

Figure 9–32. Functional Diagram of Cyclone III Device Family Remote System Upgrade
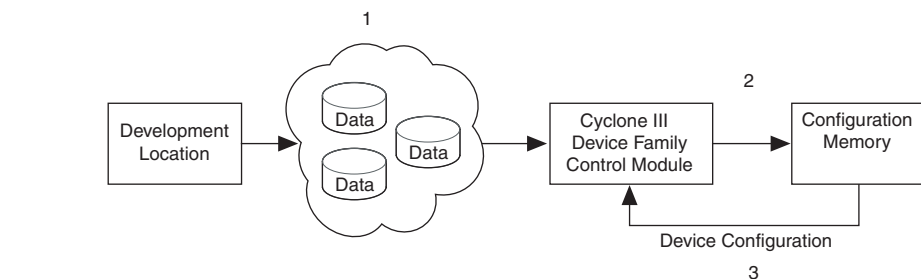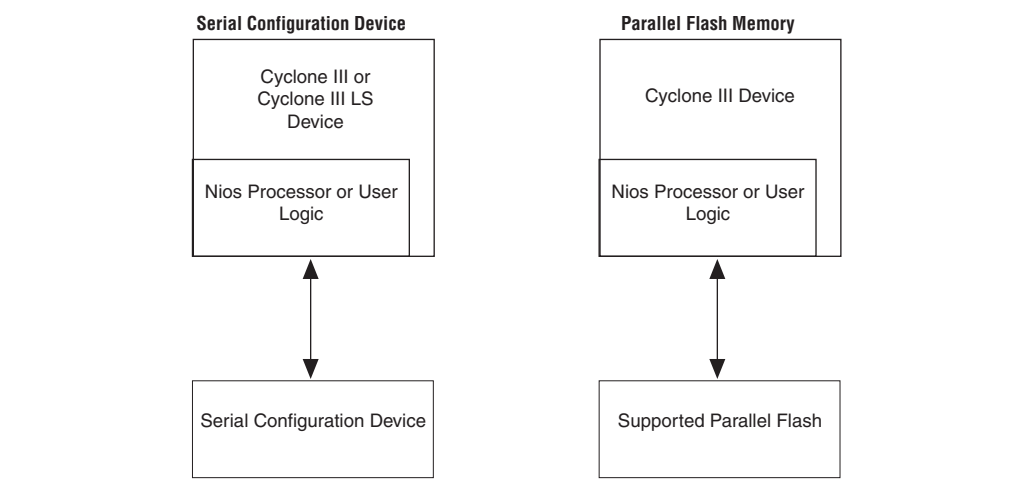
Figure 9–33 shows the block diagrams to implement remote system upgrade with the AS and AP configuration schemes.

Figure 9–33. Remote System Upgrade Block Diagrams for AS and AP Configuration Schemes

☞ Remote system upgrade only supports single-device configuration.

When using remote system upgrade in Cyclone III devices, you must set the mode select pins (MSEL [3.0]) to the AS or AP configuration scheme. When using remote system upgrade in Cyclone III LS devices, you must set MSEL [3..0] to the AS configuration scheme. The MSEL pin setting in remote system upgrade mode is the same as standard configuration mode. Standard configuration mode refers to normal Cyclone III device family configuration mode with no support for remote system upgrades, and the remote system upgrade circuitry is disabled. When using remote system upgrade in Cyclone III device family, you must enable the **remote update mode** option setting in the Quartus II software. For more information, refer to "Enabling Remote Update" on page 9–76.

Enabling Remote Update

You can enable or disable remote update for Cyclone III device family in the Quartus II software before design compilation (in the Compiler Settings menu). To enable remote update in the compiler settings of the project, perform the following steps in the Quartus II software:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.

2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.

3. Click the **Configuration** tab.

4. From the **Configuration Mode** list, select **Remote**.

5. Click **OK**.

6. In the **Settings** dialog box, click **OK**.

Configuration Image Types

When using remote system upgrade, Cyclone III device family configuration bitstreams are classified as factory configuration images or application configuration images. An image, also referred to as a configuration, is a design loaded into the device that performs certain user-defined functions. Each device in your system requires one factory image with the addition of one or more application images. The factory image is a user-defined fall-back, or safe, configuration and is responsible for administering remote updates with dedicated circuitry. Application images implement user-defined functionality in the target Cyclone III device family. You can include the default application image functionality in the factory image.

Remote System Upgrade Mode

In remote update mode, the Cyclone III device family loads the factory configuration image after power-up. The user-defined factory configuration determines which application configuration is to be loaded and triggers a reconfiguration cycle. The factory configuration can also contain application logic.

When used with configuration memory, remote update mode allows an application configuration to start at any flash sector boundary. Additionally, the remote update mode features a user watchdog timer that can detect functional errors in an application configuration.

Remote Update Mode

When a Cyclone III device family is first powered up in remote update in the AS configuration scheme, it loads the factory configuration located at address `boot_address[23:0] = 24b'0`. Altera recommends storing the factory configuration image for your system at boot address `24b'0` when using the AS configuration scheme. A factory configuration image is a bitstream for Cyclone III device family in your system that is programmed during production and is the fall-back image when an error occurs. This image is stored in non-volatile memory and is never updated or modified using remote access. This corresponds to the start address location 0x000000 in the serial configuration device.

When you use the AP configuration in Cyclone III devices, the Cyclone III device loads the default factory configuration located at the following address after device power-up in remote update mode:

boot_address[23:0] = 24'h010000 = 24'b1 0000 0000 0000 0000

You can change the default factory configuration address to any desired address using the `APFC_BOOT_ADDR` JTAG instruction. The factory configuration image is stored in non-volatile memory and is never updated or modified using remote access. This corresponds to the default start address location 0x010000 represented in 16-bit word addressing (or the updated address if the default address is changed) in the supported parallel flash memory. For more information about the application of the `APFC_BOOT_ADDR` JTAG instruction in AP configuration scheme, refer to "JTAG Instructions" on page 9–60.

The factory configuration image is user designed and contains soft logic (Nios II processor or state machine and the remote communication interface) to:

■ Process any errors based on status information from the dedicated remote system upgrade circuitry

■ Communicate with the remote host and receive new application configurations and store the new configuration data in the local non-volatile memory device

■ Determine which application configuration is to be loaded into the Cyclone III device family

■ Enable or disable the user watchdog timer and load its time-out value (optional)

■ Instruct the dedicated remote system upgrade circuitry to start a reconfiguration cycle

Figure 9–34 shows the transitions between the factory and application configurations in remote update mode.

Figure 9–34. Transitions Between Configurations in Remote Update Mode
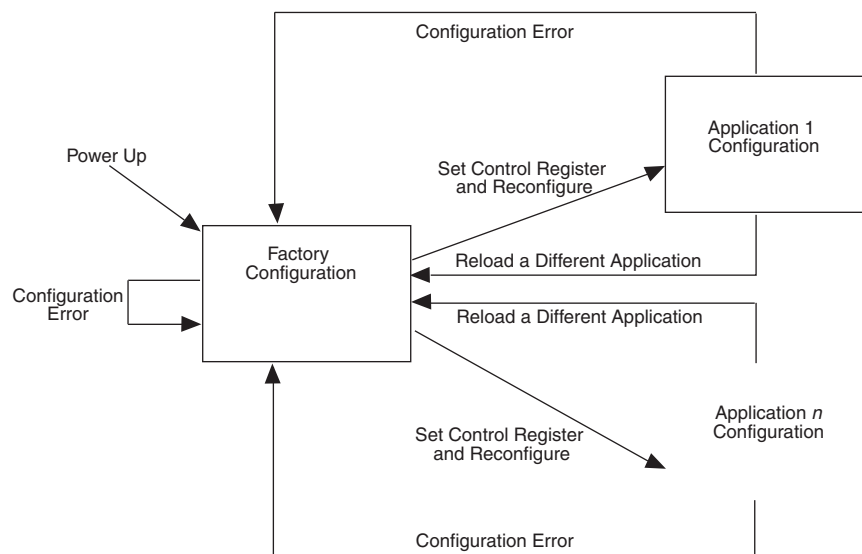
After power up or a configuration error, the factory configuration logic writes the remote system upgrade control register to specify the address of the application configuration to be loaded. The factory configuration also specifies whether or not to enable the user watchdog timer for the application configuration and, if enabled, specifies the timer setting.

☞ Only valid application configurations designed for remote update mode include the logic to reset the timer in user mode. For more information about the user watchdog timer, refer to "User Watchdog Timer" on page 9–85.

If there is an error while loading the application configuration, the remote system upgrade status register is written by the dedicated remote system upgrade circuitry of the Cyclone III device family, specifying the cause of the reconfiguration.

The following actions cause the remote system upgrade status register to be written:

■ `nSTATUS` driven low externally

■ Internal CRC error

■ User watchdog timer time-out

■ A configuration reset (logic array `nCONFIG` signal or external `nCONFIG` pin assertion)

Cyclone III device family automatically load the factory configuration located at address `boot_address[23:0] = 24'b0` for the AS configuration scheme, and default address `boot_address[23:0] = 24'h010000` (or the updated address if the default address is changed) for the AP configuration scheme. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for reconfiguration. Then the factory configuration takes the appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

When Cyclone III device family successfully load the application configuration, the devices enter user mode. In user mode, the soft logic (Nios II processor or state machine and the remote communication interface) assists the Cyclone III device family in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device, and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and starts system reconfiguration.

Dedicated Remote System Upgrade Circuitry

This section explains the implementation of the Cyclone III device family remote system upgrade dedicated circuitry. The remote system upgrade circuitry is implemented in hard logic. This dedicated circuitry interfaces to the user-defined factory application configurations implemented in the Cyclone III device family logic array to provide the complete remote configuration solution. The remote system

upgrade circuitry contains the remote system upgrade registers, a watchdog timer, and state machines that control those components. Figure 9–35 shows the data path of the remote system upgrade block.

Figure 9–35. Remote System Upgrade Circuit Data Path [(1)]
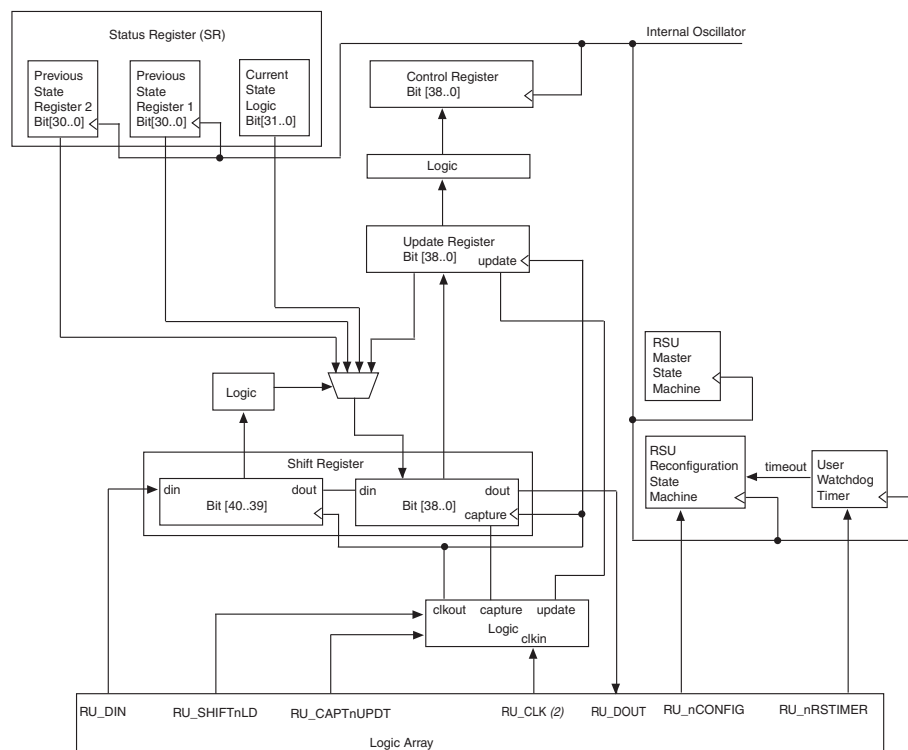
Notes to Figure 9–35:

(1) `RU_DOUT`, `RU_SHIFTnLD`, `RU_CAPTnUPDT`, `RU_CLK`, `RU_DIN`, `RU_nCONFIG`, and `RU_nRSTIMER` signals are internally controlled by the ALTREMOTE_UPDATE megafunction.

(2) `RU_CLK` refers to ALTREMOTE_UPDATE megafunction block "clock" input. For more information, refer to the *Remote Update Circuitry (ALTREMOTE_UPDATE) Megafunction User Guide*.

Remote System Upgrade Registers

The remote system upgrade block contains a series of registers that stores the configuration addresses, watchdog timer settings, and status information. These registers are listed in Table 9–26.

Table 9–26. Remote System Upgrade Registers   (Part 1 of 2)

Register	Description
Shift register	This register is accessible by the logic array and allows the update, status, and control registers to be written and sampled by user logic. Write access is enabled in remote update mode for factory configurations to allow writes to the update register. Write access is disabled for all application configurations in remote update mode.
Control register	This register contains the current configuration address, the user watchdog timer settings, one option bit for checking early `CONF_DONE`, and one option bit for selecting the internal oscillator as the startup state machine clock. During a read operation in an application configuration, this register is read into the shift register. When a reconfiguration cycle is started, the contents of the update register are written into the control register.

Table 9–26. Remote System Upgrade Registers (Part 2 of 2)

Register	Description
Update register	This register contains data similar to that in the control register. However, it can only be updated by the factory configuration by shifting data into the shift register and issuing an update operation. When a reconfiguration cycle is triggered by the factory configuration, the control register is updated with the contents of the update register. During a read in a factory configuration, this register is read into the shift register.
Status register	This register is written to by the remote system upgrade circuitry on every reconfiguration to record the cause of the reconfiguration. This information is used by the factory configuration to determine the appropriate action following a reconfiguration. During a capture cycle, this register is read into the shift register.

The control and status registers of the remote system upgrade are clocked by the 10-MHz internal oscillator (the same oscillator that controls the user watchdog timer). However, the shift and update registers of the remote system upgrade are clocked by the maximum frequency of 40-MHz user clock input (RU_CLK). There is no minimum frequency for RU_CLK.

Remote System Upgrade Control Register

The remote system upgrade control register stores the application configuration address, the user watchdog timer settings, and option bits for application configuration. In remote update mode for the AS configuration scheme, the control register address bits are set to all zeros (24'b0) at power up to load the AS factory configuration. In remote update mode for the AP configuration scheme, the control register address bits are set to 24'h010000 (24'b1 0000 0000 0000 0000) at power up to load the AP default factory configuration. However, for the AP configuration scheme, you can change the default factory configuration address to any desired address using the APFC_BOOT_ADDR JTAG instruction. Additionally, a factory configuration in remote update mode has write access to this register.

The control register bit positions are shown in Figure 9–36 and listed in Table 9–27. In the figure, the numbers show the bit position of a setting in a register. For example, bit number 35 is the enable bit for the watchdog timer.

Figure 9–36. Remote System Upgrade Control Register

38	37	36	35	34	33	12	11	0
Rsv2	Cd_early	Osc_int	Wd_en	Rsv1	Ru_address[21..0]		Wd_timer[11..	

When enabled, the early CONF_DONE check (Cd_early) option bit ensures that there is a valid configuration at the boot address specified by the factory configuration and that it is of the proper size. If an invalid configuration is detected or CONF_DONE pin is asserted too early, the device resets and then reconfigures the factory configuration image. The internal oscillator, as startup state machine clock (Osc_int) option bit, ensures a functional startup clock to eliminate the hanging of startup when enabled. When all option bits are turned on, they provide complete coverage for the programming and startup portions of the application configuration. It is strongly recommended that you turn on both the Cd_early and Osc_int option bits.

☞   The `Cd_early` and `Osc_int` option bits for the application configuration must be turned on by the factory configuration.

Table 9–27. Remote System Upgrade Control Register Contents

Control Register Bit	Value	Definition
`Wd_timer[11..0]`	12'b000000000000	User watchdog time-out value (most significant 12 bits of 29-bit count value: {`Wd_timer[11..0]`,17'b1000})
`Ru_address[21..0]`	22'b0000000000000000000000	Configuration address (most significant 22 bits of 24-bit boot address value: `boot_address[23:0]` = {`Ru_address[21..0]`,2'b0})
`Rsv1`	1'b0	Reserved bit
`Wd_en`	1'b1	User watchdog timer enable bit
`Osc_int` [(1)]	1'b1	Internal oscillator as startup state machine clock enable bit
`Cd_early` [(1)]	1'b1	Early `CONF_DONE` check
`Rsv2`	1'b1	Reserved bit

Note to Table 9–27:

(1) Option bit for the application configuration.

Remote System Upgrade Status Register

The remote system upgrade status register specifies the reconfiguration trigger condition. The various trigger and error conditions include:

■ Cyclical redundancy check (CRC) error during application configuration

■ `nSTATUS` assertion by an external device due to an error

■ Cyclone III device family logic array triggered a reconfiguration cycle, possibly after downloading a new application configuration image

■ External configuration reset (`nCONFIG`) assertion

■ User watchdog timer time out

Table 9–28 lists the contents of the current state logic in the status register, when the remote system upgrade master state machine is in factory configuration or application configuration accessing the factory information or application information respectively, and the MSEL pin setting is set to AS or AP configuration scheme. The status register bit in Table 9–28 lists the bit positions in a 32-bit logic.

Table 9–28. Remote System Upgrade Current State Logic Contents In Status Register [(1)]

Current State Logic	Status Register Bit	Definition	Description
Factory information [(2)]	31:30	Master State Machine current state	The current state of the RSU master state machine
	29:24	Reserved bits	Padding bits that are set to all 0's
	23:0	Boot address	The current 24-bit boot address that was used by the configuration scheme as the start address to load the current configuration.

Table 9–28. Remote System Upgrade Current State Logic Contents In Status Register [1]

Current State Logic	Status Register Bit	Definition	Description
Application information part 1 [3]	31:30	Master State Machine current state	The current state of the RSU master state machine
	29	User watchdog timer enable bit	The current state of the user watchdog enable, which is active high
	28:0	User watchdog timer time-out value	The current entire 29-bit watchdog time-out value
Application information part 2 [3]	31:30	Master State Machine current state	The current state of the RSU master state machine
	29:24	Reserved bits	Padding bits that are set to all 0's
	23:0	Boot address	The current 24-bit boot address that was used by the configuration scheme as the start address to load the current configuration

Notes to Table 9–28:

(1) The MSEL pin setting is in the AS or AP configuration scheme.

(2) The RSU master state machine is in factory configuration.

(3) The RSU master state machine is in application configuration.

The previous two application configurations are available in the previous state registers (previous state register 1 and previous state register 2), but only for debugging purposes.

Table 9–29 lists the contents of the previous state register 1 and previous state register 2 in the status register when the MSEL pin setting is set to the AS or AP scheme. The status register bit in Table 9–29 shows the bit positions in a 31-bit register. The previous state register 1 and previous state register 2 have the same bit definitions. The previous state register 1 reflects the current application configuration and the previous state register 2 reflects the previous application configuration.

Table 9–29. Remote System Upgrade Previous State Register 1 and Previous State Register 2 Contents in Status Register [1] **(Part 1 of 2)**

Status Register Bit	Definition	Description
30	`nCONFIG` source	One-hot, active-high field that describes the reconfiguration source that caused the Cyclone III device family to leave the previous application configuration. If there is a tie, the higher bit order indicates precedence. For example, if `nCONFIG` and remote system upgrade `nCONFIG` reach the reconfiguration state machine at the same time, the `nCONFIG` precedes the remote system upgrade `nCONFIG`.
29	CRC error source	
28	`nSTATUS` source	
27	User watchdog timer source	
26	Remote system upgrade `nCONFIG` source	
25:24	Master state machine current state	The state of the master state machine during reconfiguration causes the Cyclone III device family to leave the previous application configuration.

Table 9–29. Remote System Upgrade Previous State Register 1 and Previous State Register 2 Contents in Status Register [(1)] **(Part 2 of 2)**

Status Register Bit	Definition	Description
23:0	Boot address	The address used by the configuration scheme to load the previous application configuration.

Note to Table 9–29:

(1) The MSEL pin settings are in the AS configuration scheme.

If a capture is inappropriately done, for example, capturing a previous state before the system has entered remote update application configuration for the first time, a value will output from the shift register to indicate that the capture was incorrectly called.

Remote System Upgrade State Machine

The remote system upgrade control and update registers have identical bit definitions, but serve different roles (Table 9–26 on page 9–81). While both registers can only be updated when the device is loaded with a factory configuration image, the update register writes are controlled by the user logic, and the control register writes are controlled by the remote system upgrade state machine.

In factory configurations, the user logic should send the option bits (Cd_early and Osc_int), the configuration address, and watchdog timer settings for the next application configuration bit to the update register. When the logic array configuration reset (RU_nCONFIG) goes high, the remote system upgrade state machine updates the control register with the contents of the update register and starts system reconfiguration from the new application page.

☞ To ensure the successful reconfiguration between the pages, assert RU_nCONFIG signal for a minimum of 250 ns. This is equivalent to strobing the reconfig input of the ALTREMOTE_UPDATE megafunction high for a minimum of 250 ns.

If there is an error or reconfiguration trigger condition, the remote system upgrade state machine directs the system to load a factory or application configuration (based on mode and error condition) by setting the control register accordingly.

Table 9–30 lists the contents of the control register after such an event occurs for all possible error or trigger conditions.

The remote system upgrade status register is updated by the dedicated error monitoring circuitry after an error condition but before the factory configuration is loaded.

Table 9–30. Control Register Contents After an Error or Reconfiguration Trigger Condition

Reconfiguration Error/Trigger	Control Register Setting In Remote Update
nCONFIG reset	All bits are 0
nSTATUS error	All bits are 0
CORE triggered reconfiguration	Update register
CRC error	All bits are 0
Wd time out	All bits are 0

User Watchdog Timer

The user watchdog timer prevents a faulty application configuration from stalling the device indefinitely. The system uses the timer to detect functional errors after an application configuration is successfully loaded into the Cyclone III device family.

The user watchdog timer is a counter that counts down from the initial value loaded into the remote system upgrade control register by the factory configuration. The counter is 29-bits wide and has a maximum count value of 2^{29}. When specifying the user watchdog timer value, specify only the most significant 12 bits. Remote system upgrade circuitry appends 17'b1000 to form the 29 bits value for the watchdog timer. The granularity of the timer setting is 2^{17} cycles. The cycle time is based on the frequency of the 10-MHz internal oscillator.

Table 9–31 lists the operating range of the 10-MHz internal oscillator.

Table 9–31. 10-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Unit
5	6.5	10	MHz

The user watchdog timer begins counting after the application configuration enters device user mode. This timer must be periodically reloaded or reset by the application configuration before the timer expires by asserting RU_nRSTIMER. If the application configuration does not reload the user watchdog timer before the count expires, a time-out signal is generated by the remote system upgrade dedicated circuitry. The time-out signal tells the remote system upgrade circuitry to set the user watchdog timer status bit (Wd) in the remote system upgrade status register and reconfigures the device by loading the factory configuration.

☞ To allow remote system upgrade dedicated circuitry to reset the watchdog timer, you must assert the RU_nRSTIMER signal active for a minimum of 250 ns. This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for a minimum of 250 ns.

The user watchdog timer is not enabled during the configuration cycle of the device. Errors during configuration are detected by the CRC engine. Also, the timer is disabled for factory configuration. Functional errors must not exist in the factory configuration because it is stored and validated during production and is never updated remotely.

☞ By default, the user watchdog timer is disabled in factory configurations and enabled in user-mode application configurations. If you do not want to use the watchdog timer feature, disable this feature in the factory configuration.

Quartus II Software Support

Implementation in your design requires a remote system upgrade interface between the Cyclone III device family logic array and the remote system upgrade circuitry. You must also generate configuration files for production and remote programming of the system configuration memory. The Quartus II software provides these features.

The two implementation options, the ALTREMOTE_UPDATE megafunction and the remote system upgrade atom, are for the interface between the remote system upgrade circuitry and the device logic array interface. Using the megafunction block instead of creating your own logic saves design time and offers more efficient logic synthesis and device implementation.

For more information about the ALTREMOTE_UPDATE megafunction, refer to the *Remote Update Circuitry (ALTREMOTE_UPDATE) Megafunction User Guide*.

Document Revision History

Table 9–32 lists the revision history for this document.

Table 9–32. Document Revision History

Date	Version	Changes
August 2012	2.2	Updated Micron P30 and P33 Parallel NOR flash devices.
July 2012	2.1	Finalized Table 9–3, Table 9–13, and Table 9–14.
December 2011	2.0	■ Updated "Configuration Features" on page 9–2, "Reset" on page 9–8, "AS Configuration (Serial Configuration Devices)" on page 9–12, "Single-Device AS Configuration" on page 9–13, "AP Configuration Supported Flash Memory" on page 9–24, "Single-Device AP Configuration" on page 9–25, "JTAG Configuration" on page 9–48, and "User Watchdog Timer" on page 9–85. ■ Removed the "Overriding the Internal Oscillator" section from "JTAG Configuration". ■ Updated Figure 9–11, Figure 9–24, Figure 9–25, Figure 9–26, Figure 9–27, Figure 9–29, Figure 9–30. ■ Updated Table 9–13, Table 9–18, and Table 9–22. ■ Replaced links to *AN 386: Using the Parallel Flash Loader with the Quartus II Software* links to *Parallel Flash Loader Megafunction User Guide.*
December 2009	1.2	■ Updated Table 9–7, Table 9–10, Table 9–22, and Table 9–28. ■ Updated Figure 9–23 and Figure 9–30. ■ Updated the "Programming Serial Configuration Devices" and "Security Against Tampering" sections. ■ Minor changes to the text.
July 2009	1.1	Made a minor correction to the part number.
June 2009	1.0	Initial release.