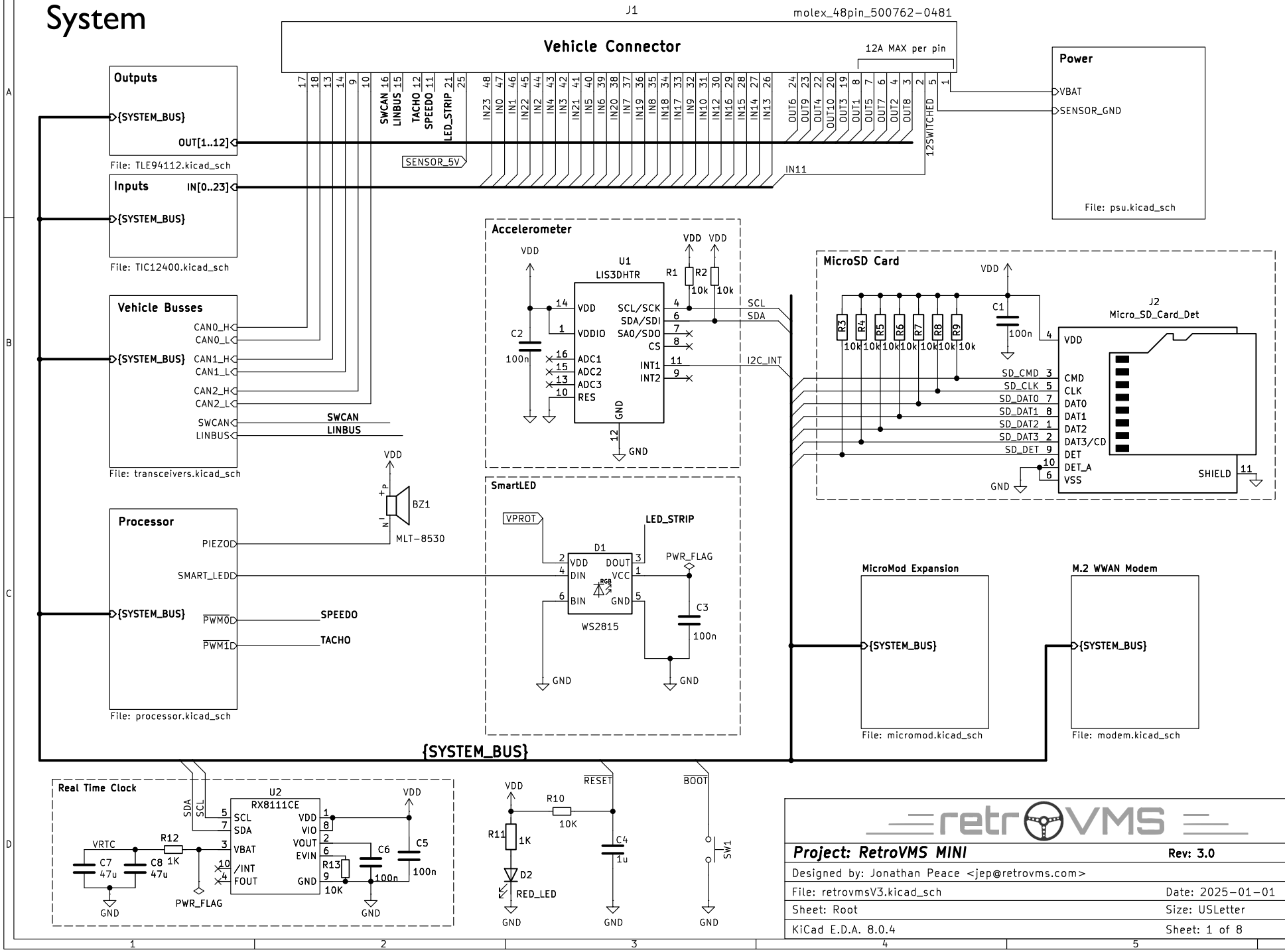
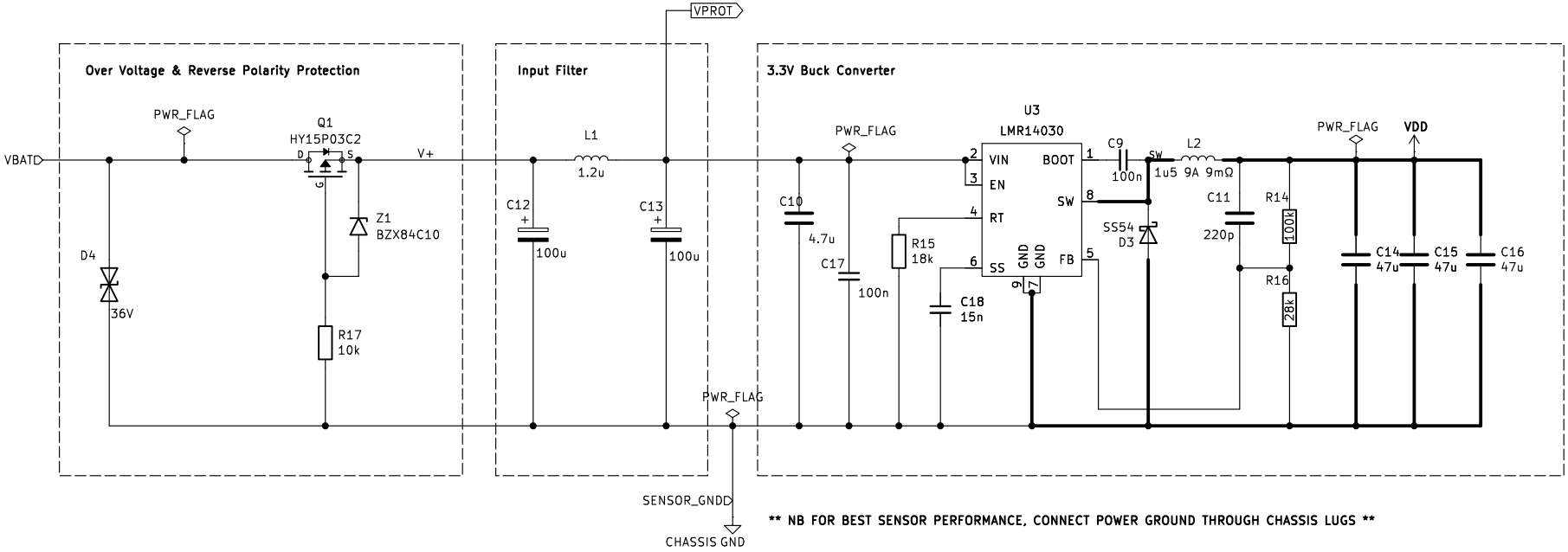
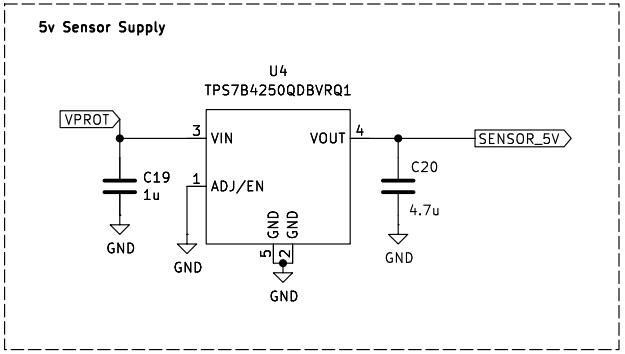
System

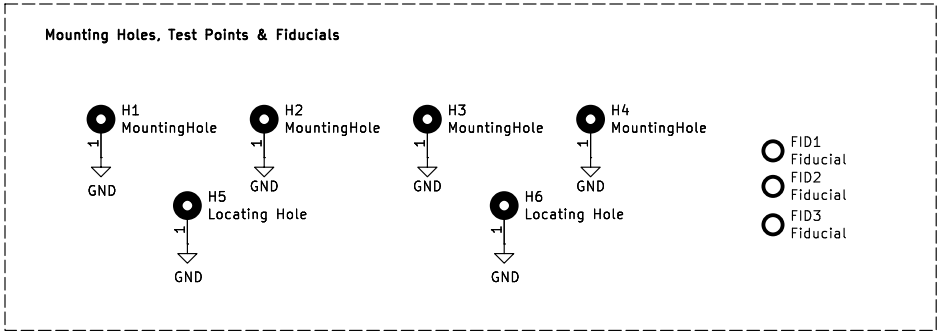


Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: retrovmsV3.kicad_sch	Date: 2025-01-01
Sheet: Root	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 1 of 8

Power

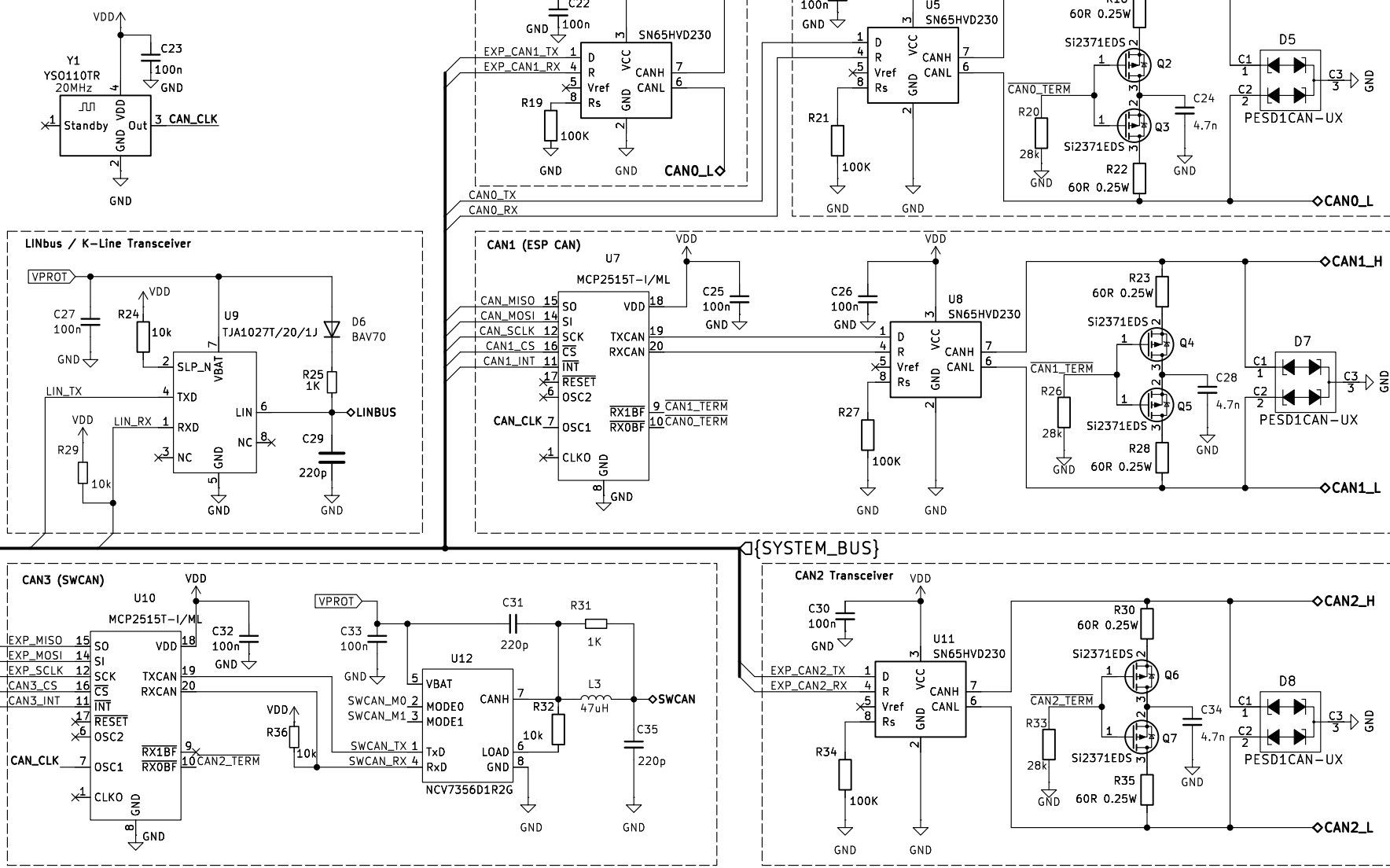






Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: psu.kicad_sch	Date: 2025-01-01
Sheet: Power	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 2 of 8

Vehicle Busses



CAN BUS ASSIGNMENT

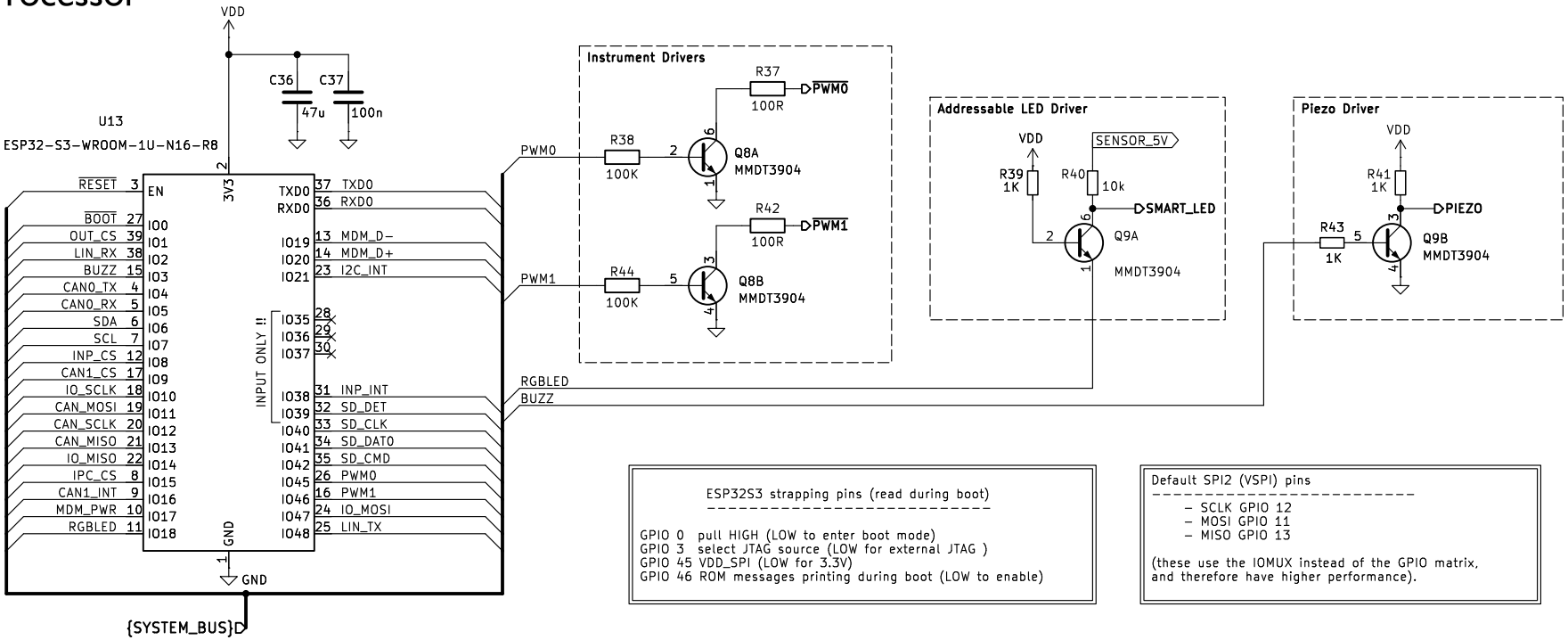
CAN0 – Dual connected PHYs allows main and expansion processors to communicate using their internal CAN MACs
CAN1 – External MAC (MCP2515) via ESP32 SPI2 (VSPI) + PHY
CAN2 – PHY connected to 2nd expansion processor internal MAC
CAN3 – External MAC (MCP2515) via EXPANSION SPI2 + SWCAN PHY

CAN Terminations are controlled by MCP2515 GPIO

retroVMS

Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: transceivers.kicad_sch	Date: 2025-01-01
Sheet: Vehicle Busses	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 3 of 8

Processor



ESP32S3 strapping pins (read during boot)

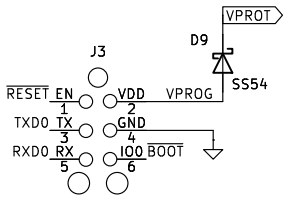
GPIO 0 pull HIGH (LOW to enter boot mode)
GPIO 3 select JTAG source (LOW for external JTAG)
GPIO 45 VDD_SPI (LOW for 3.3V)
GPIO 46 ROM messages printing during boot (LOW to enable)

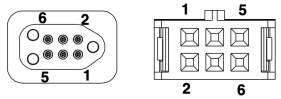
Default SPI2 (VSPI) pins

- SCLK GPIO 12
- MOSI GPIO 11
- MISO GPIO 13

(these use the IOMUX instead of the GPIO matrix, and therefore have higher performance).

Programming header for ESPprog
- dual foot print 6-pin TagConnect with 0.127 header



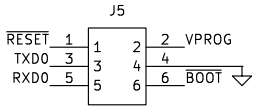


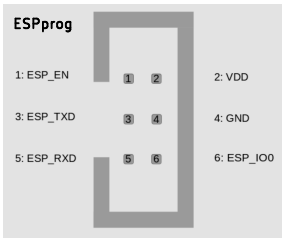
TAG 6 PIN	IDC 6 PIN
1	1
2	2
3	3
4	4
5	5
6	6

ESP32 Programming Header

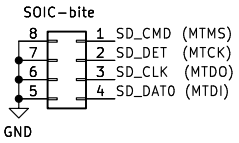
IO0 = 1 : boot from flash
IO0 = 0 : bootloader

EN = 0 : Reset

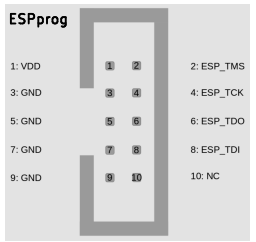




ESP32 JTAG ESPPROG debug
- uses SOICbite or 6P 1.27mm clip on probe



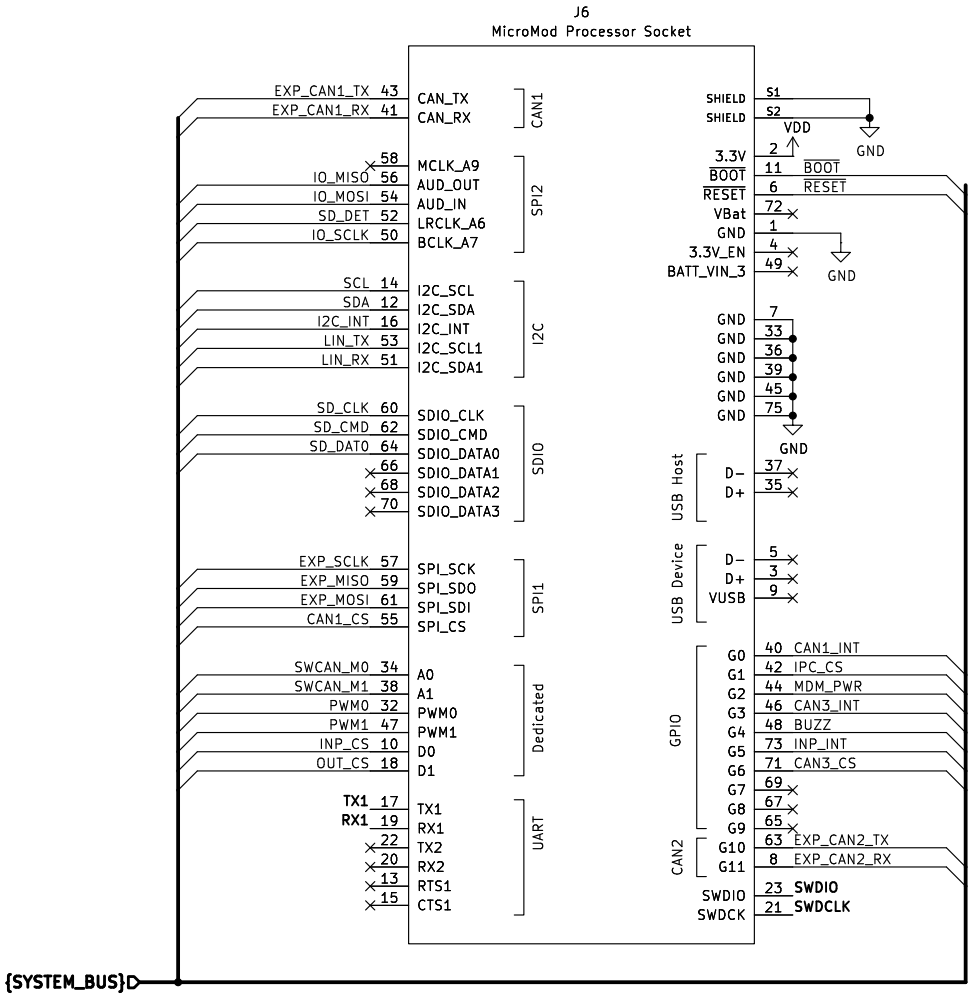
ESP32-S3 Pin	JTAG Signal
MTDO / GPIO40	TDO
MTDI / GPIO41	TDI
MTCK / GPIO39	TCK
MTMS / GPIO42	TMS



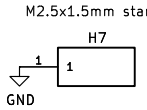
** use USB C 15W cable to power ESPprog **

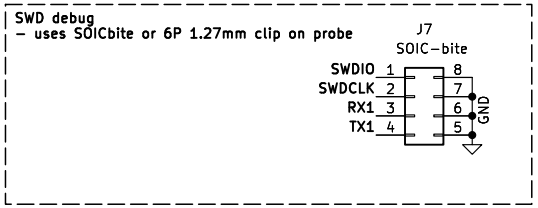
Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: processor.kicad_sch	Date: 2025-01-01
Sheet: Processor	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 4 of 8

Micromod M.2 Processor/Expansion socket



	MicroModule (M.2) Pinout v1.0		
	An Input is into the module. The module controls Outputs.		
		GND	75
74	3.3V	G5 / BUS5	73
72	RTC_3V_BATT	G6 / BUS6	71
70	SPI_CS1# / SDIO_DATA3 (I/O)	G7 / BUS7	69
68	SDIO_DATA2 (I/O)	G8	67
66	SDIO_DATA1 (I/O)	G9 / ADC_D- / CAM_HSYNC	65
64	SPI_CIPO1 / SDIO_DATA0 (I/O)	G10 / ADC_D+ / CAM_VSYNC	63
62	SPI_COPI1 / SDIO_CMD (I/O)	SPI_CIPO (I)	61
60	SPI_SCK1 / SDIO_CLK (O)	SPI_COPI (O)	59
58	AUD_MCLK (O)	SPI_SCK (O)	57
56	AUD_OUT / PCM_OUT / I2S_OUT / CAM_MCLK	SPI_CS#	55
54	AUD_IN / PCM_IN / I2S_IN / CAM_PCLK	I2C_SCL1 (I/O)	53
52	AUD_LRCLK / PCM_SYNC / I2S_WS / PDM_DATA (I/O)	I2C_SDA1 (I/O)	51
50	AUD_BCLK / PCM_CLK / I2S_SCK / PDM_CLK (I/O)	BATT_VIN/3 (I - ADC) (0/3.3V)	49
48	G4 / BUS4	PWM1	47
46	G3 / BUS3	GND	45
44	G2 / BUS2	CAN_TX	43
42	G1 / BUS1	CAN_RX	41
40	G0 / BUS0	GND	39
38	A1	USBHOST_D-	37
36	GND	USBHOST_D+	35
34	A0	GND	33
32	PWM0	Module Key	31
30	Module Key	Module Key	29
28	Module Key	Module Key	27
26	Module Key	Module Key	25
24	Module Key	SWDIO	23
22	UART_TX2 (O)	SWDCK	21
20	UART_RX2 (I)	UART_RX1 (I)	19
18	D1 / CAM_TRIG	UART_TX1 (O)	17
16	I2C_INT# (I)	UART_CTS1 (I)	15
14	I2C_SCL (I/O)	UART_RTS1 (O)	13
12	I2C_SDA (I/O)	BOOT (I - Open Drain)	11
10	D0	USB_VIN	9
8	G11 / SWDSWO	GND	7
6	RESET# (I - Open Drain)	USB_D-	5
4	3.3V_EN	USB_D+	3
2	3.3V	GND	1

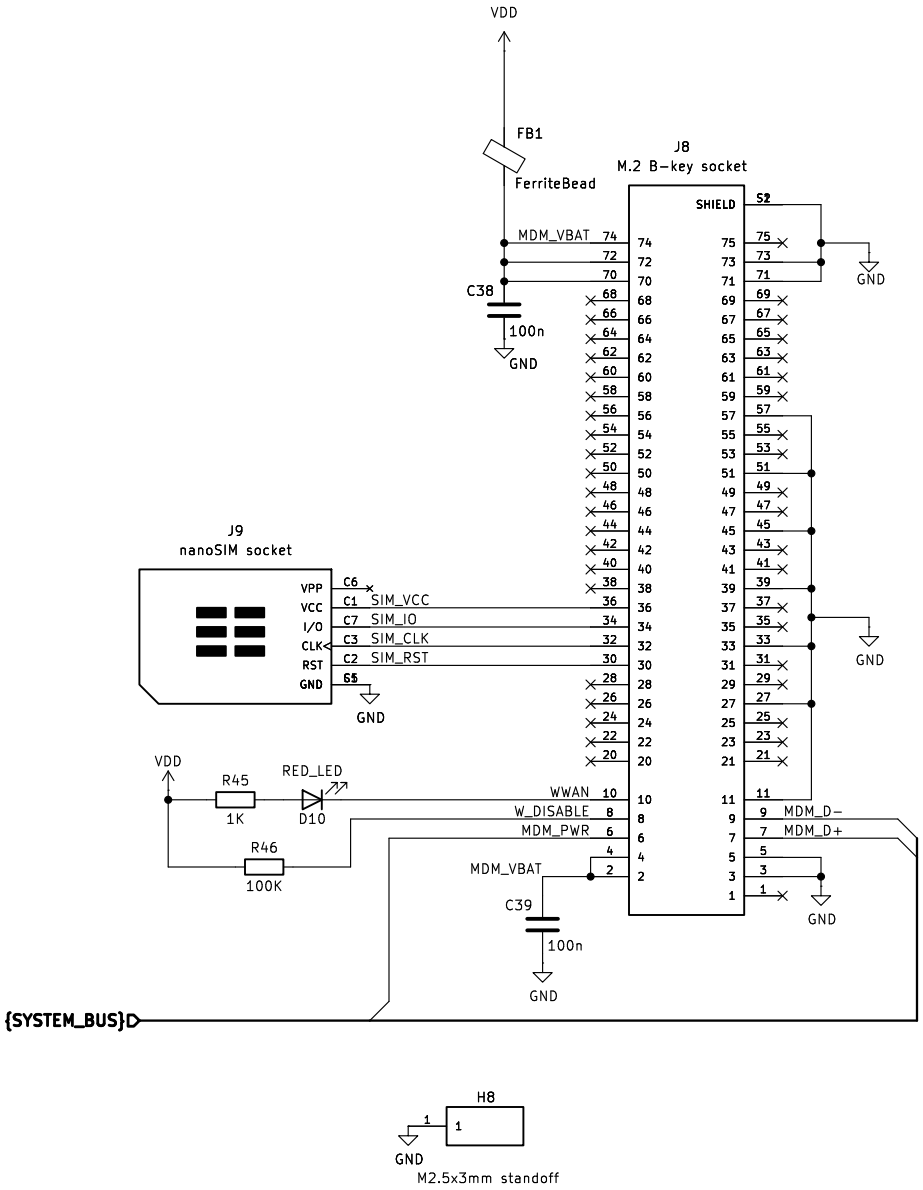




retroVMS

Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: micromod.kicad_sch	Date: 2025-01-01
Sheet: MicroMod Expansion	Size: A4
KiCad E.D.A. 8.0.4	Sheet: 5 of 8

4G GSM/GNSS M.2 module socket



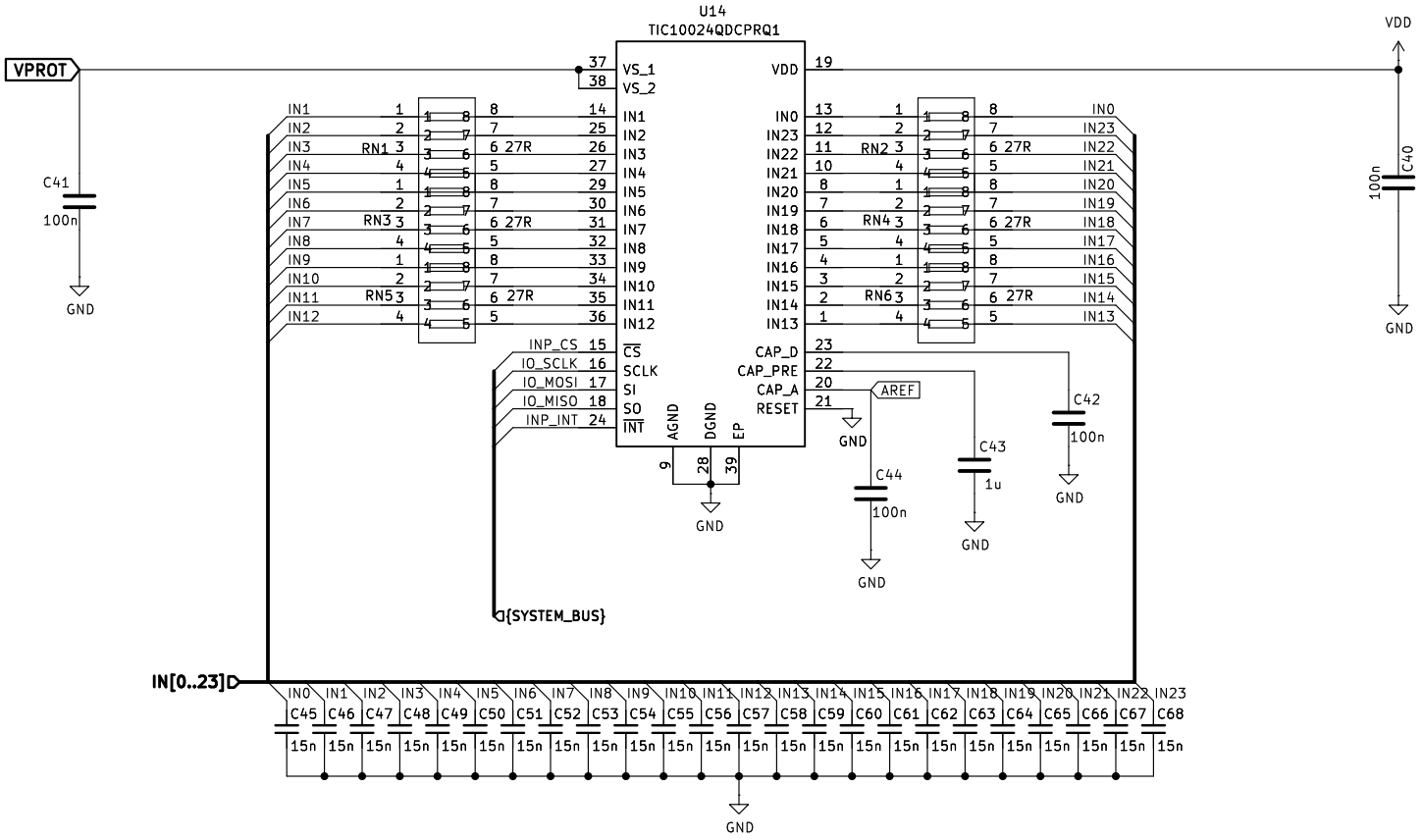
SIM7600X-M2 pinout

74	VBAT	CONFIG_2=GND	75
72	VBAT	GND	73
70	VBAT	GND	71
68	NC	CONFIG_1=GND	69
66	USIM_DET(I)(1.8V)	RESET#(I)(1.8V)	67
64	GPIO3(IO)(1.8V)	ANTCTL3(O)(1.8V)	65
62	GPIO77(IO)(1.8V)	ANTCTL2(O)(1.8V)	63
60	UART_TXD(O)(1.8V)	ANTCTL1(O)(1.8V)	61
58	UART_RXD(I)(1.8V)	ANTCTL0(O)(1.8V)	59
56	UART_CTS(O)(1.8V)	GND	57
54	UART_RTS(I)(1.8V)	NC	55
52	UART_DTR(I)(1.8V)	NC	53
50	GPIO40(IO)(1.8V)	GND	51
48	GPIO41(IO)(1.8V)	NC	49
46	GPIO43(IO)(1.8V)	NC	47
44	GPIO44(IO)(1.8V)	GND	45
42	I2C_SDA(IO/OD)(1.8V)	NC	43
40	I2C_SCL(O/OD)(1.8V)	NC	41
38	NC	GND	39
36	USIM_VDD	NC	37
34	USIM_DATA	NC	35
32	USIM_CLK	GND	33
30	USIM_RST	NC	31
28	PCM_CLK(O)(1.8V)	NC	29
26	W_DISABLE2_N(I)(3.3V)	GND	27
24	PCM_OUT(O)(1.8V)	DPR(I)(1.8V)	25
22	PCM_IN(I)(1.8V)	WoWWAN(OD)(1.8V/3.3V)	23
20	PCM_SYNC(O)(1.8V)	CONFIG_0=GND	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#(OD)(3.3V)	GND	11
8	W_DISABLE1_N(I)(3.3V)	USB_D-	9
6	FUL_CARD_POWER_OFF#(I)(1.8/3.3V)	USB_D+	7
4	VBAT	GND	5
2	VBAT	GND	3
		CONFIG_3=NC	1

retroVMS

Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: modem.kicad_sch	Date: 2025-01-01
Sheet: M.2 WWAN Modem	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 6 of 8

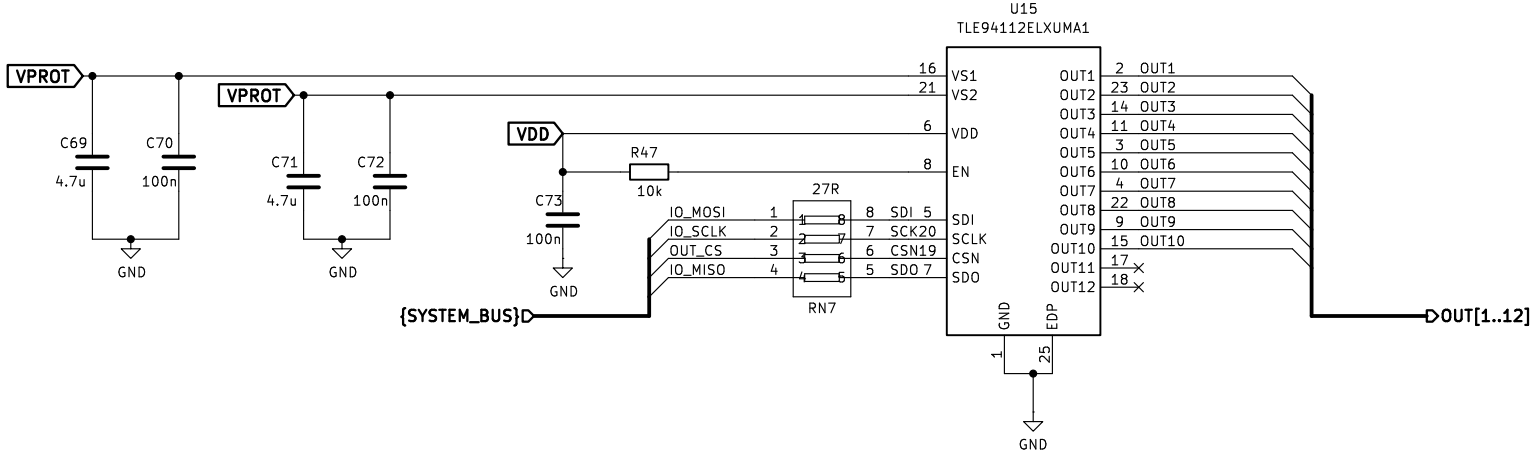
Inputs - 24-channel protected Analog/Digital inputs



retroVMS	
Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: TIC12400.kicad_sch	Date: 2025-01-01
Sheet: Inputs	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 7 of 8

Outputs - 12channel LS/HS/PWM driver

Per datasheet:
Series resistors between the microcontroller and the signal pins of the TLE94112 are recommended if a MOSFET is used to protect VS1 and VS2 pins.
These resistors limit the current between the microcontroller and the device during negative transients on VBAT (e.g. ISO/TR 7637 pulse 1)



Project: RetroVMS MINI	**Rev: 3.0**
Designed by: Jonathan Peace <jep@retrovms.com>	
File: TLE94112.kicad_sch	Date: 2025-01-01
Sheet: Outputs	Size: USLetter
KiCad E.D.A. 8.0.4	Sheet: 8 of 8