EE5811 : FPGA LAB

P V Aishwarya IS21MTECH14004

Problem

Question 5) c) from papers/icse/cs/2018.pdf Simplify the following expression using Boolean Laws :

A.(
$$A' + B$$
).C.($A + B$)

Implement above program in FPGA.

Solution

Truth Table

A	B	C	LHS	RHS
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 1: Truth table for A.(A' + B).C.(A + B) = A.B.C

Implemented the above truth table in FPGA. The inputs A,B,C are taken in through three wires and its LHS output is displayed on RED LED and its RHS output is displayed on Seven segment. Steps:

- 1. In Ubuntu, write verilog program.
- 2. Compile and Run it on FPGA.