This article describes charge storage memory constructed using a semiconducting single walled nanotube transistor which is highly mobile making it suitable for storage memory. This type of memory contributes in decreasing the power utilization for read and write and erase and gives advantage of storing over quasi continuous quantities of charge. The authors explain the main drawing force behind the high mobility as the reverse injected charge when removed from the dielectic by applying a moderate range voltage across the dielectric. Their work is justified with equations, atomic force topograph, drain current graph and voltage graph for read write cycles as compared to other silicon FETs. The authors also concluded that storage memory can be improved with shorted storage gates and suitable charge straps. Since cache memory is significant in any fast processing device, I think that this technology can help in improving the cache memory processing. This article helps clearify the concept of Nano RAM to a great extend.