Name: Aishwarya Gandhi

SBU ID:111424452

Email: aishwarya.gandhi@stonybrook.edu

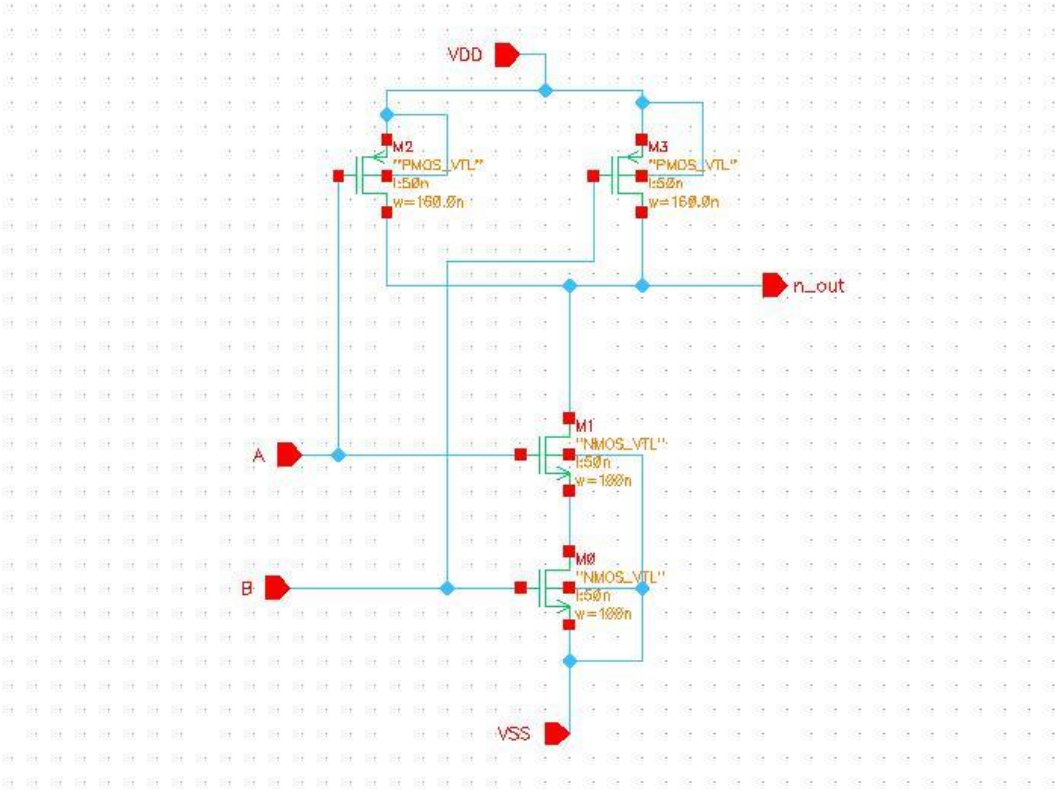
ESE 555 ASSIGNMENT 3

Objective:

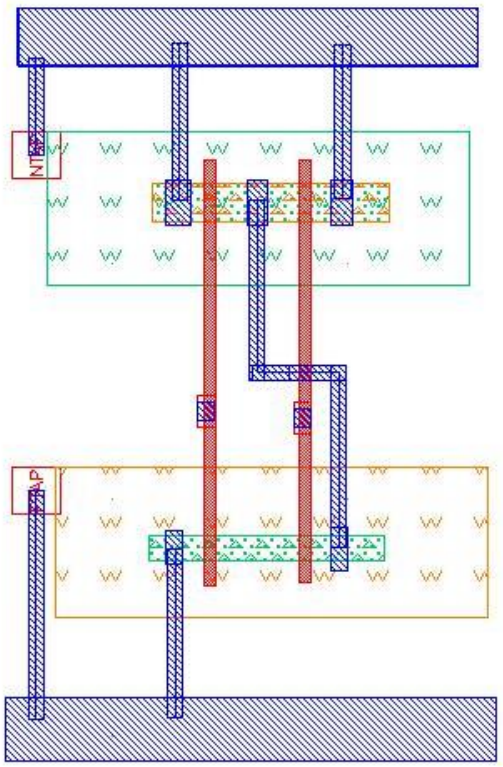
i) Design and verify a CMOS positive (rising) edge triggered master-slave D type flip-flop with an asynchronous reset.

ii) To verify the functionality of the flip-flop by designing a simple data path.

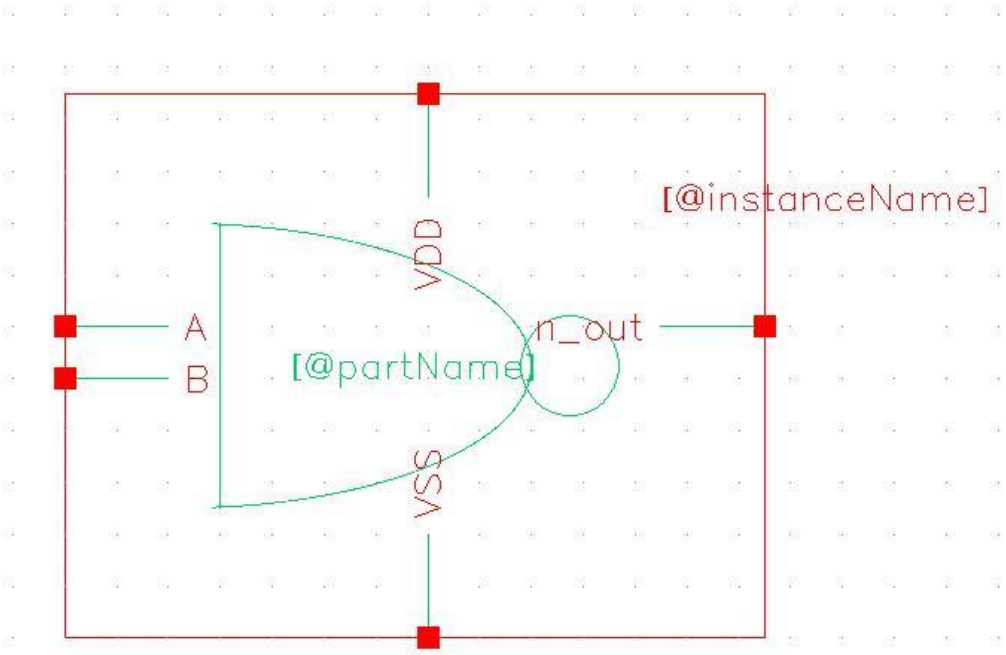
NAND SCHEMATIC



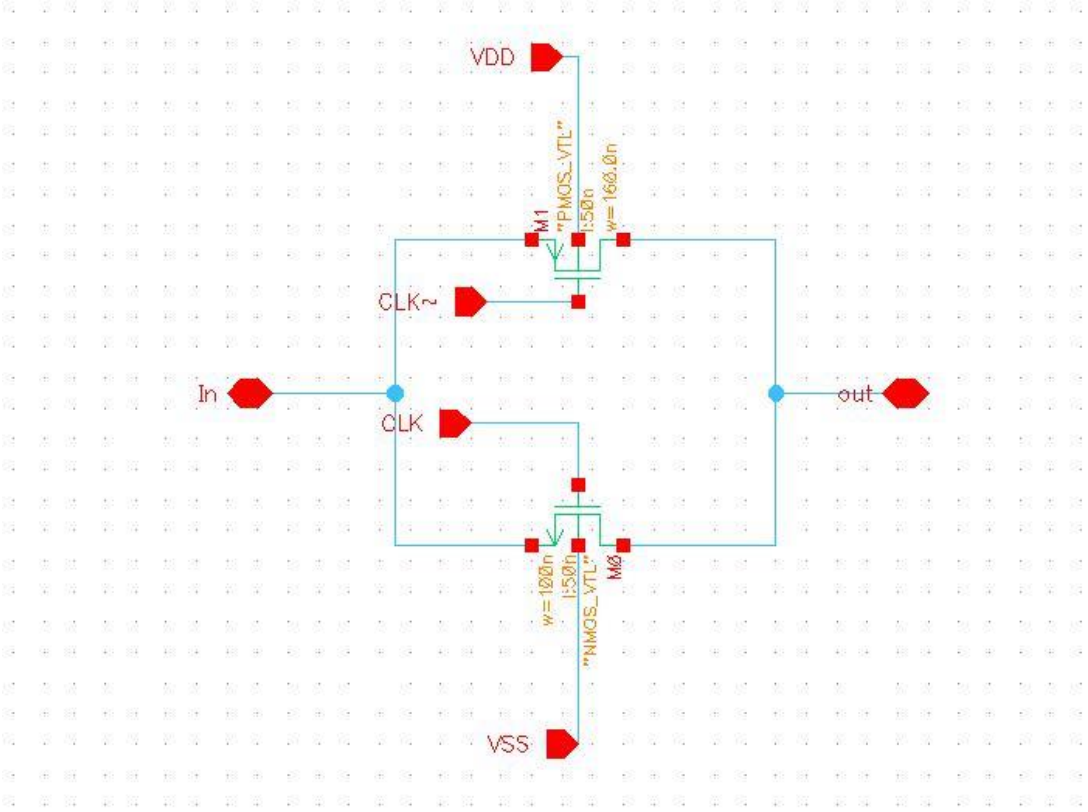
NAND LAYOUT:



NAND SYMBOL



TRANSMISSION GATE SCHEMATIC



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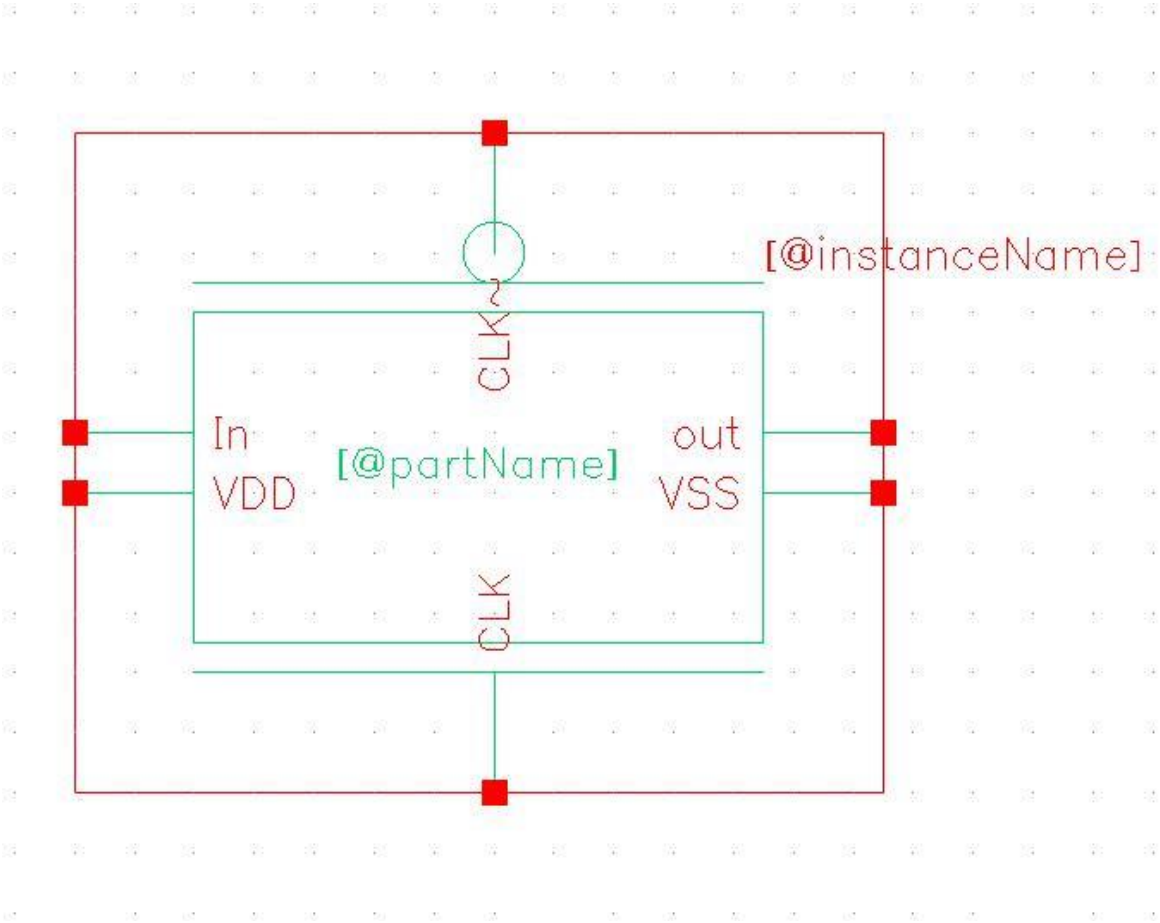
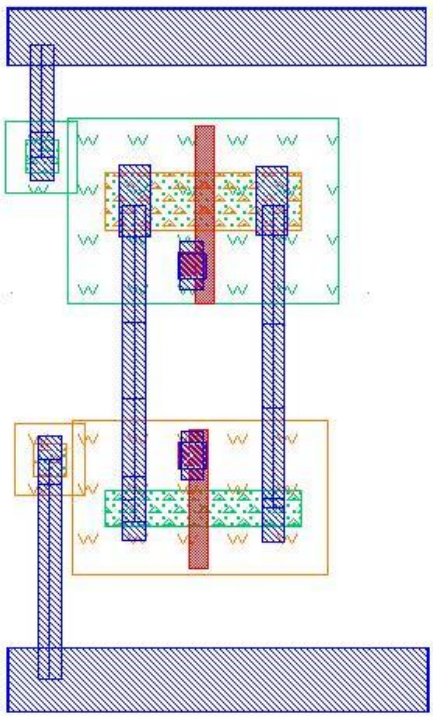
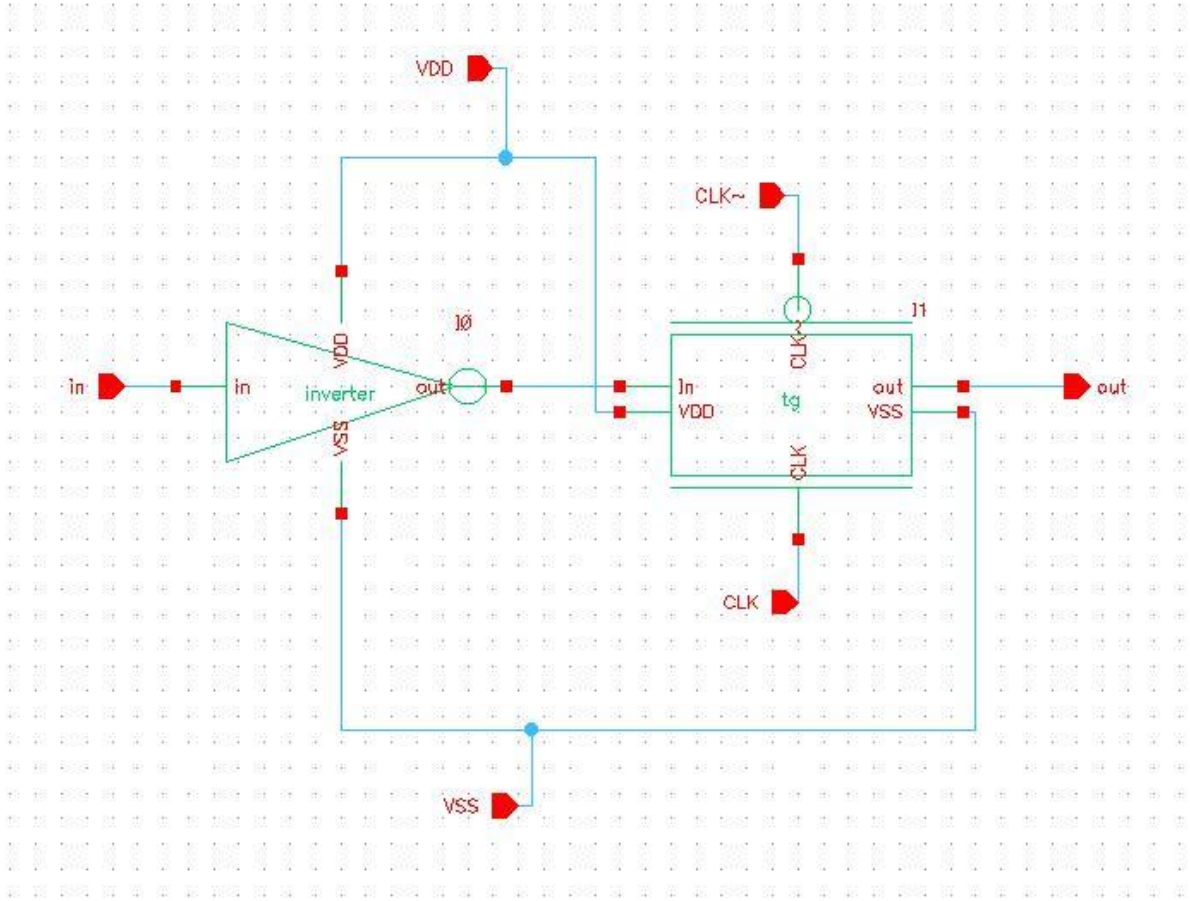
TRANSMISSION GATE SYMBOL



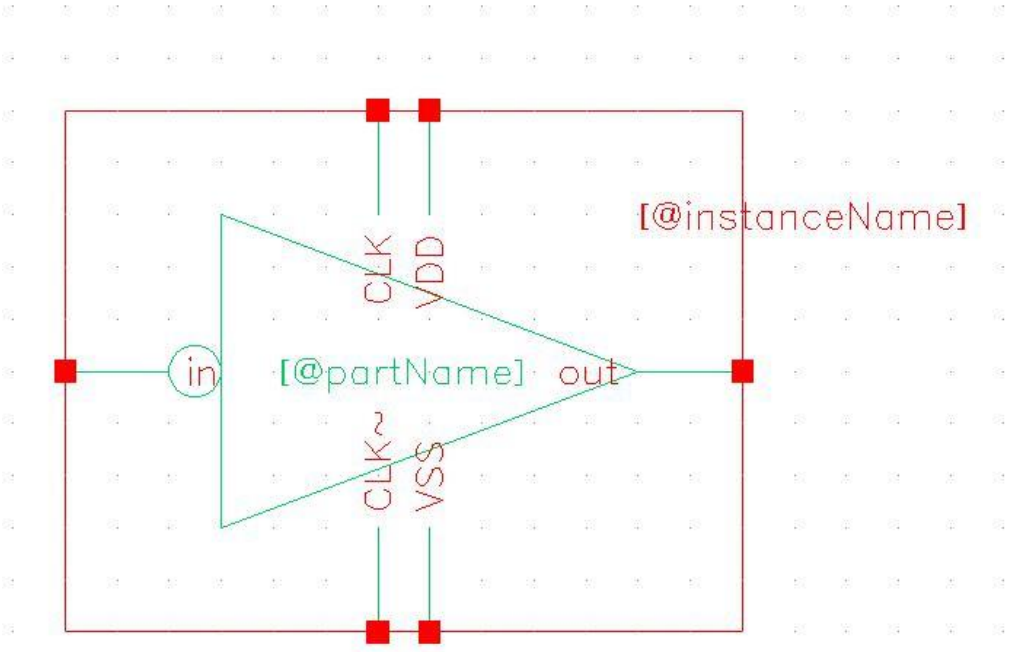
TRANSMISSION GATE LAYOUT:



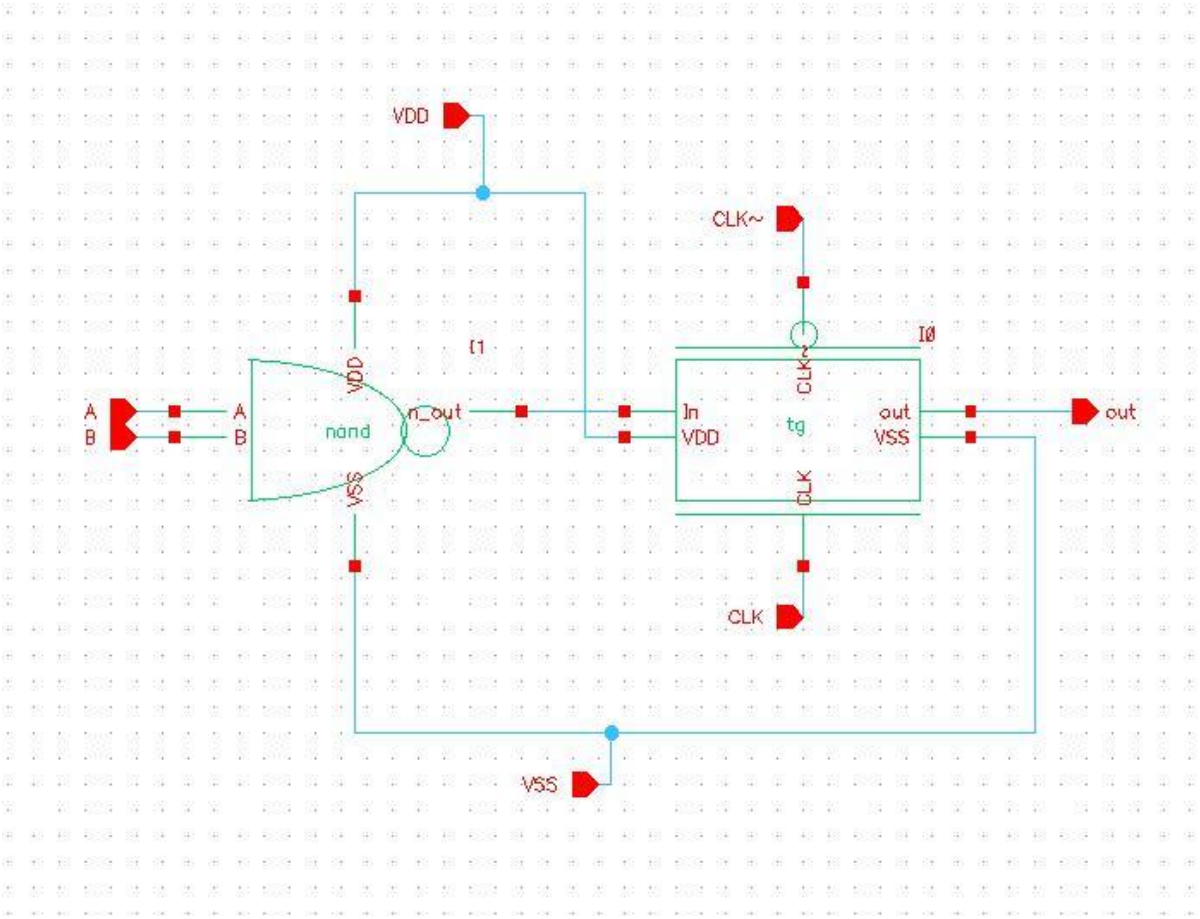
TRISTATE INVERTER SCHEMATIC



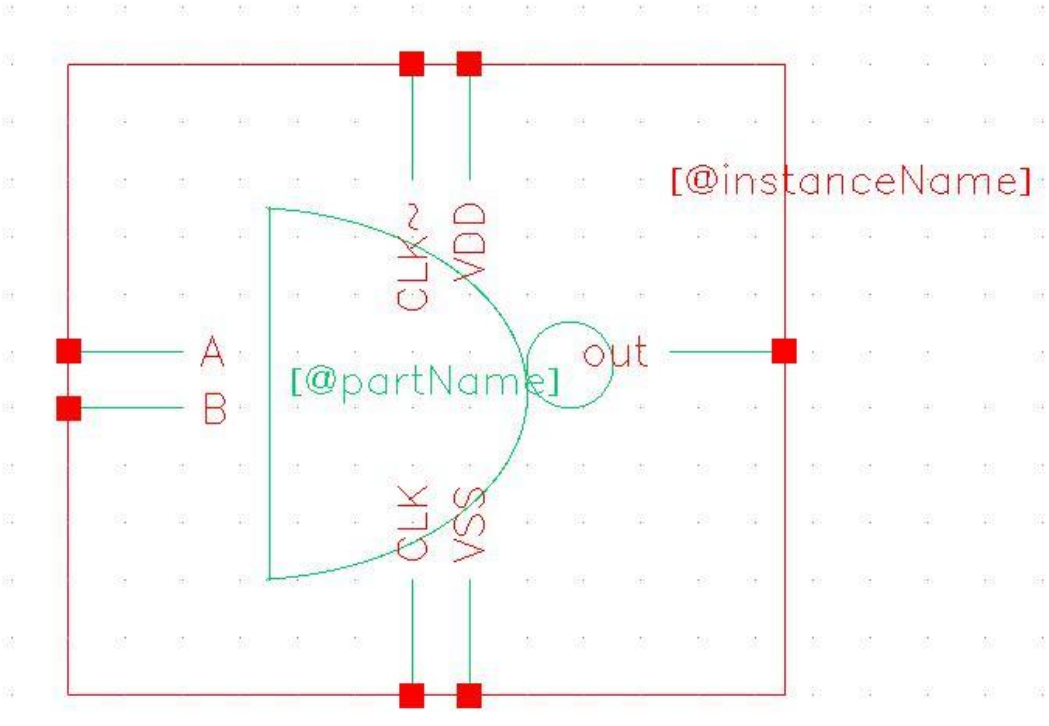
TRISTATE INVERTER SYMBOL



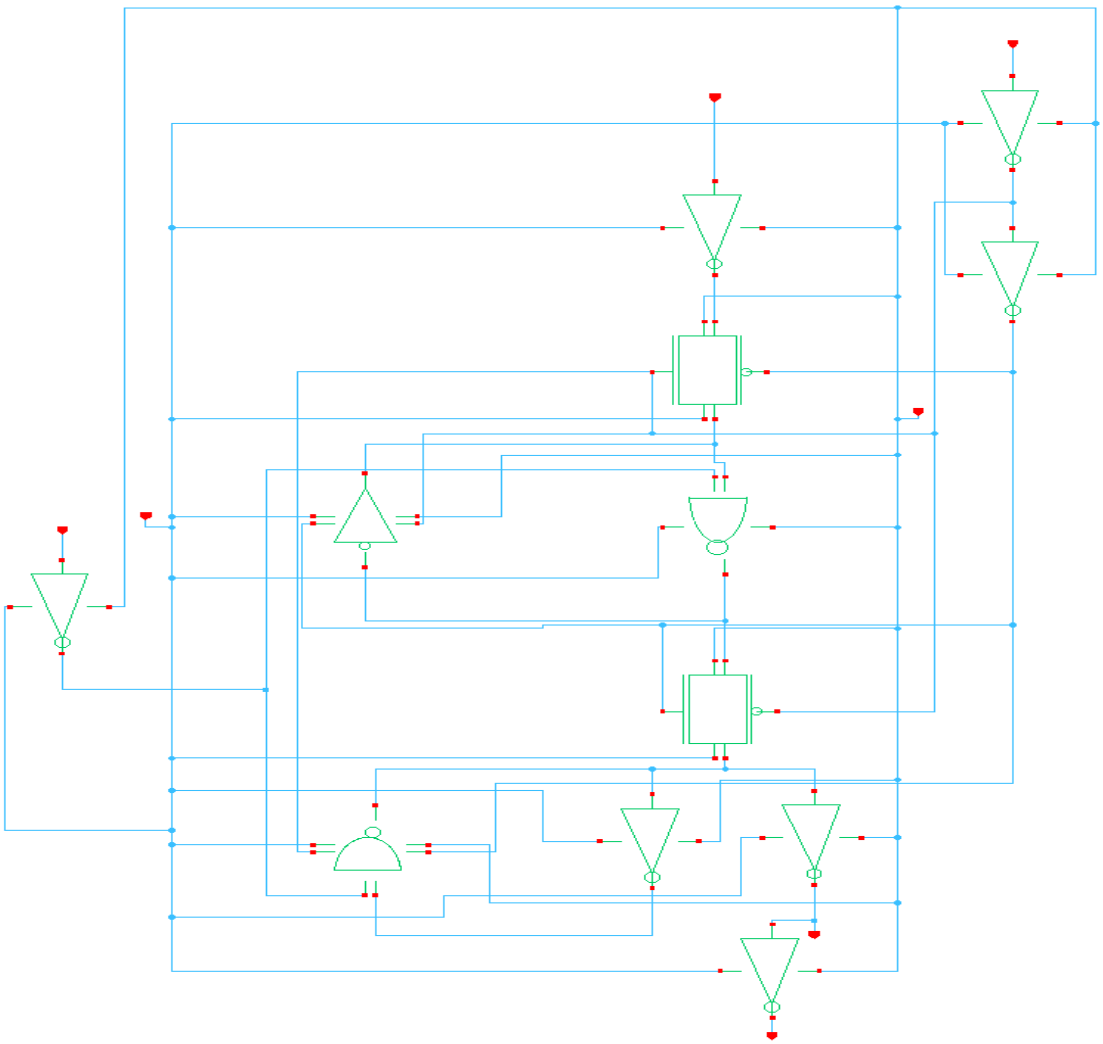
TRISTATE NAND SCHEMATIC



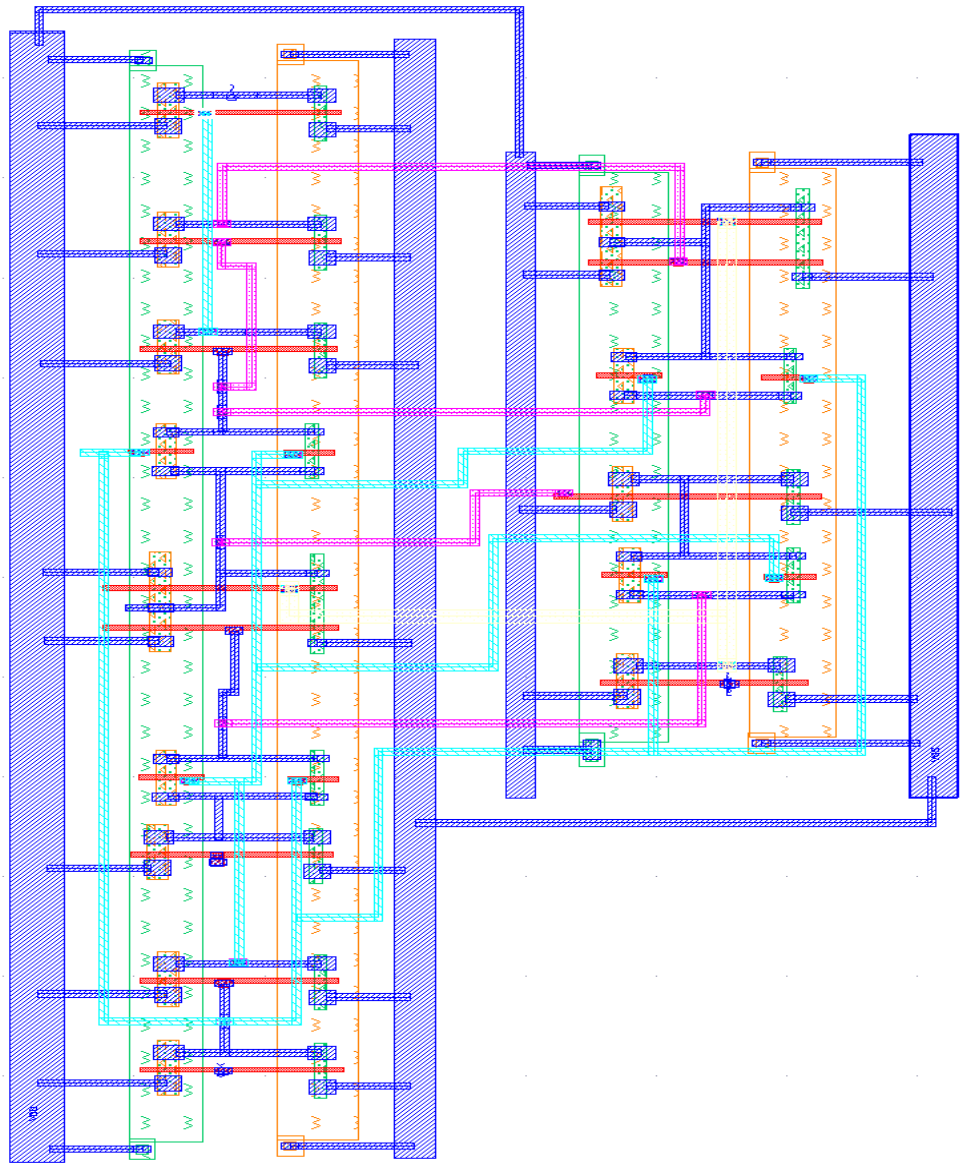
TRISTATE NAND SYMBOL



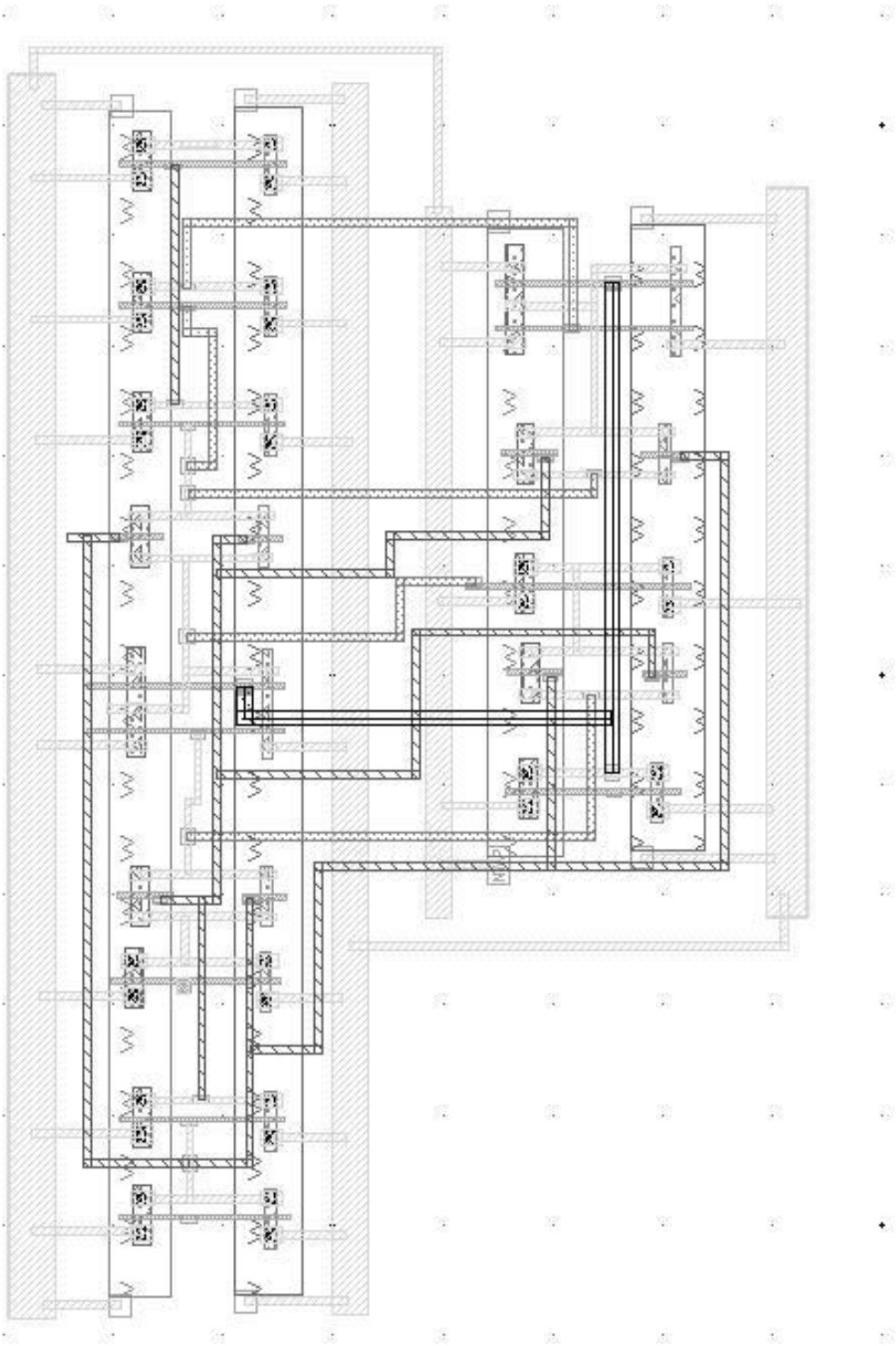
D FLIP-FLOP SCHEMATIC



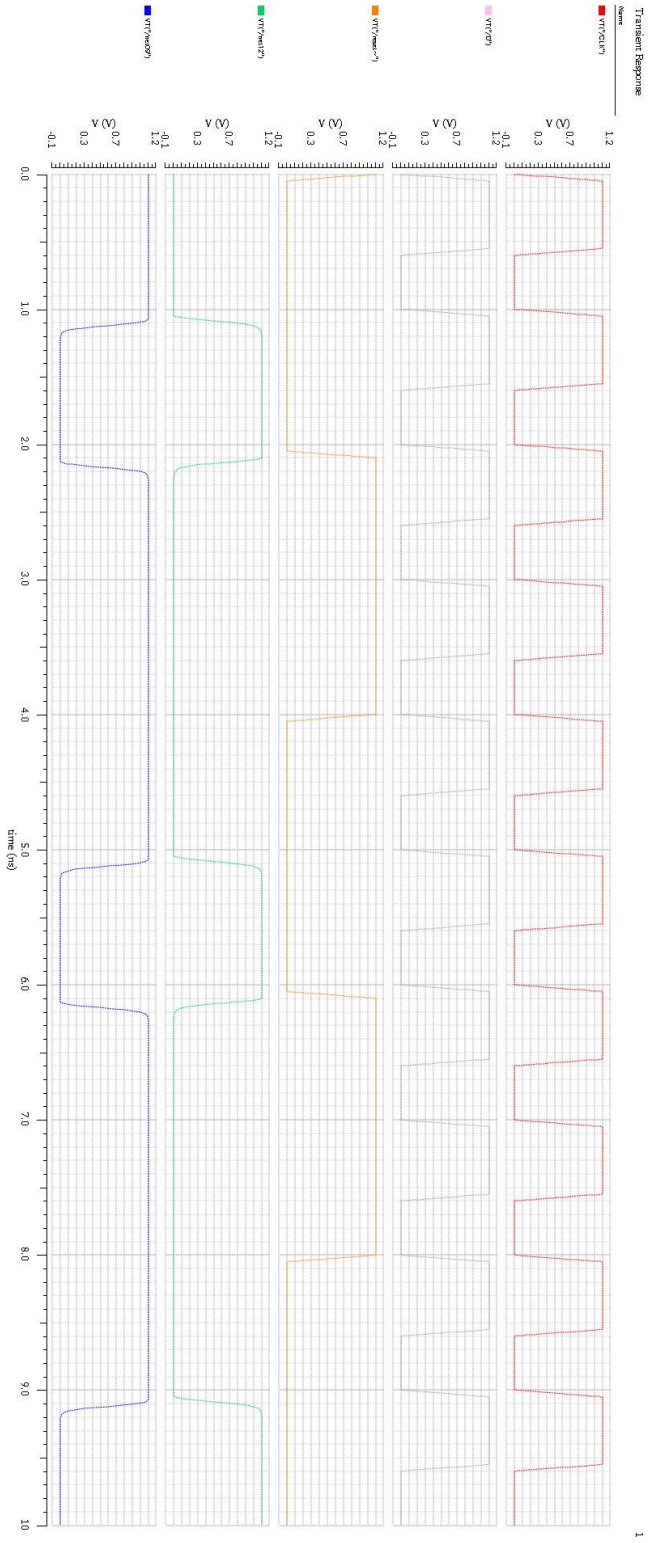
D FLIP-FLOP LAYOUT



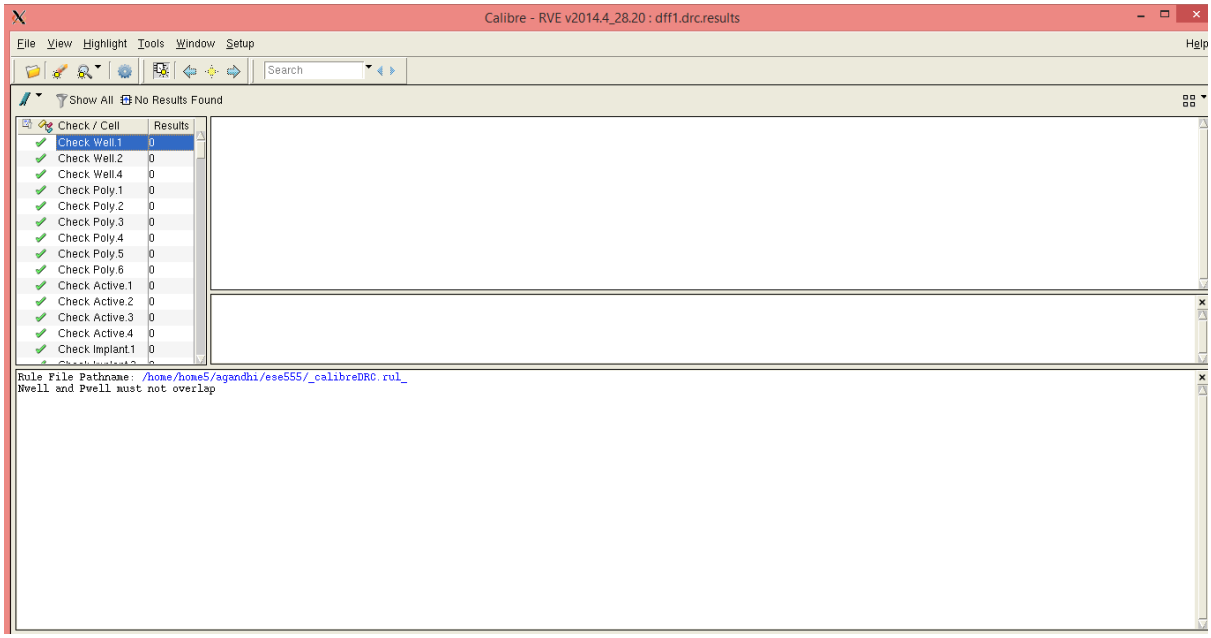
D FLIP-FLOP LAYOUT



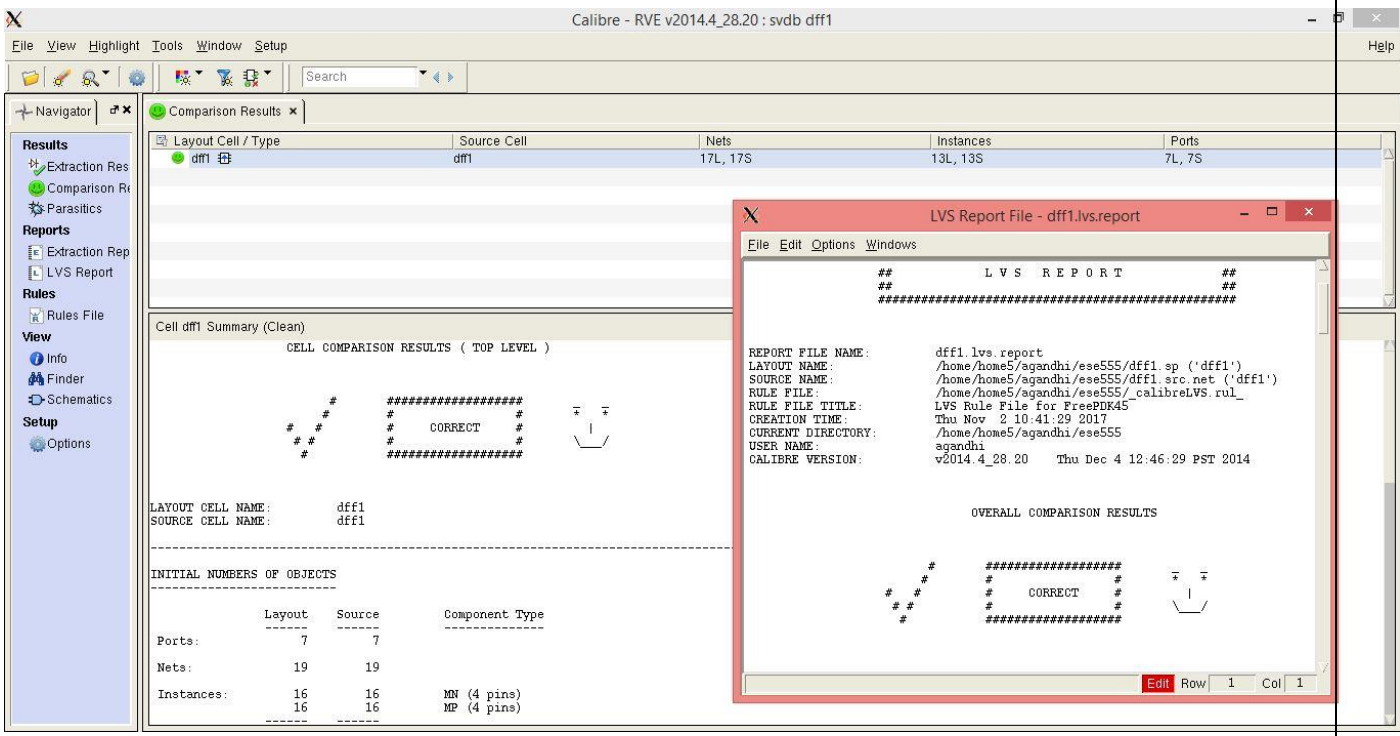
TRANSIENT ANALYSIS OF D FLIP-FLOP



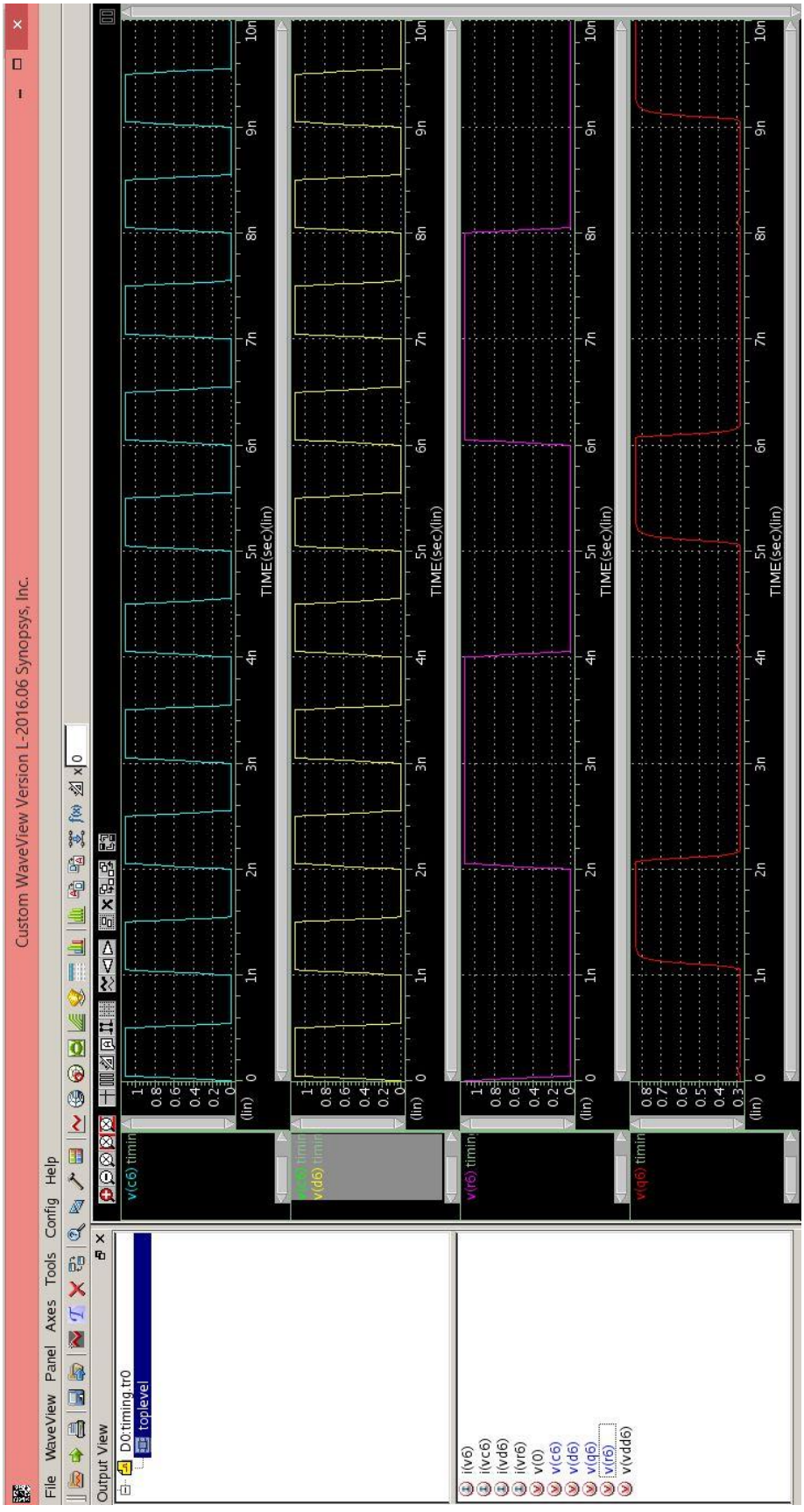
DRC SUCCESSFUL



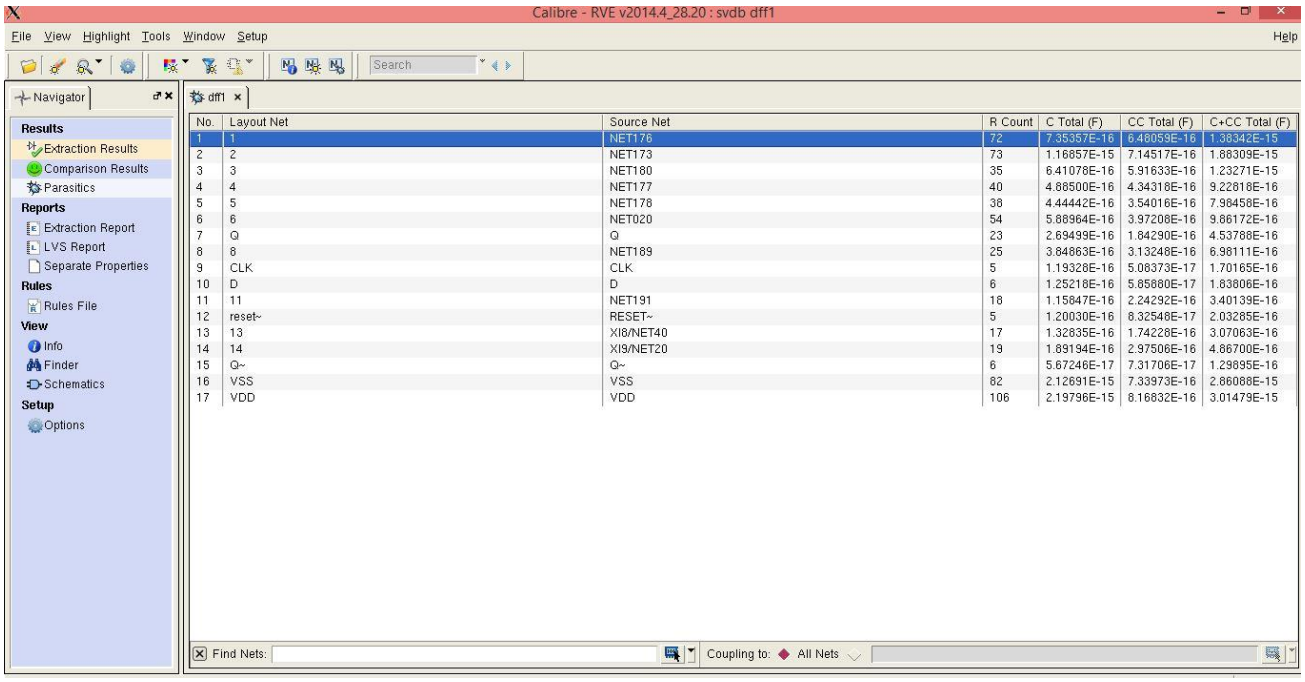
LVS SUCCESSFUL



POST LAYOUT SIMULATION OF D FLIP-FLOP:

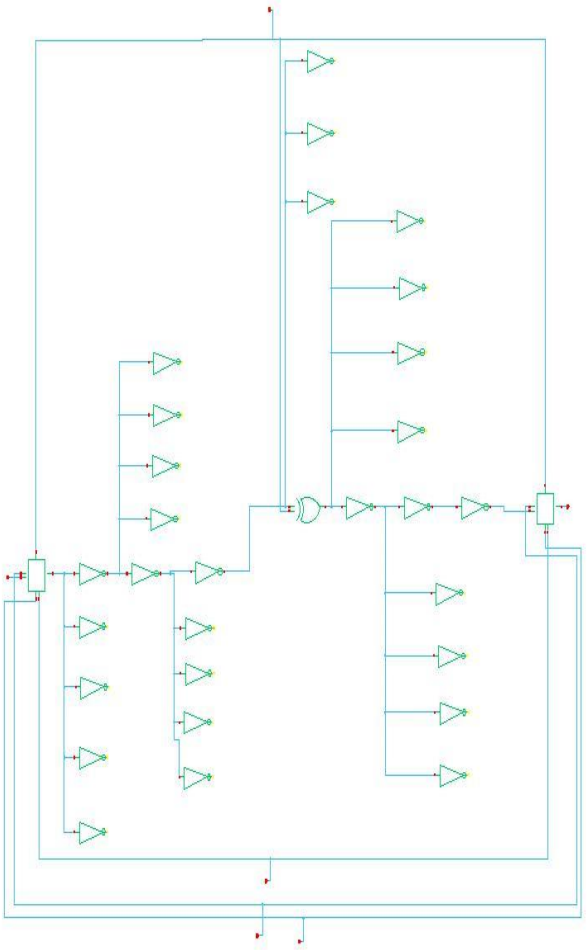


PARASITIC REPORT:



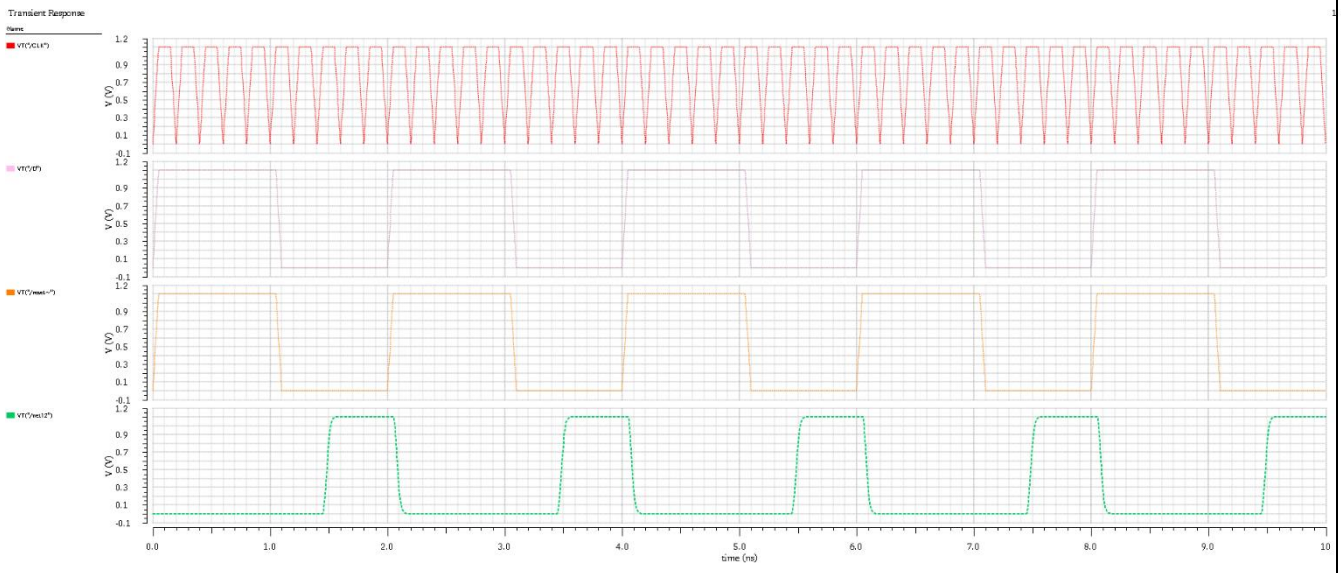
No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	1	NET176	72	7.35357E-16	6.48059E-16	1.38342E-15
2	2	NET173	73	1.16857E-15	7.14517E-16	1.88309E-15
3	3	NET180	35	6.41078E-16	5.91633E-16	1.23271E-15
4	4	NET177	40	4.86500E-16	4.34318E-16	9.22818E-16
5	5	NET178	38	4.44442E-16	3.54016E-16	7.98458E-16
6	6	NET020	54	5.88964E-16	3.97208E-16	9.86172E-16
7	Q	Q	23	2.69499E-16	1.84290E-16	4.53788E-16
8	8	NET189	25	3.84863E-16	3.13248E-16	6.98111E-16
9	CLK	CLK	5	1.19328E-16	5.08373E-17	1.70165E-16
10	D	D	6	1.25218E-16	5.85880E-17	1.83806E-16
11	11	NET191	18	1.15847E-16	2.24292E-16	3.40139E-16
12	reset~	RESET~	5	1.20030E-16	8.32548E-17	2.03285E-16
13	13	XI8/NET40	17	1.32835E-16	1.74228E-16	3.07063E-16
14	14	XI9/NET20	19	1.89194E-16	2.97506E-16	4.86700E-16
15	Q~	Q~	6	5.67246E-17	7.31706E-17	1.29895E-16
16	VSS	VSS	82	2.12691E-15	7.33973E-16	2.86088E-15
17	VDD	VDD	106	2.19796E-15	8.16832E-16	3.01479E-15

DATA PATH DESIGN

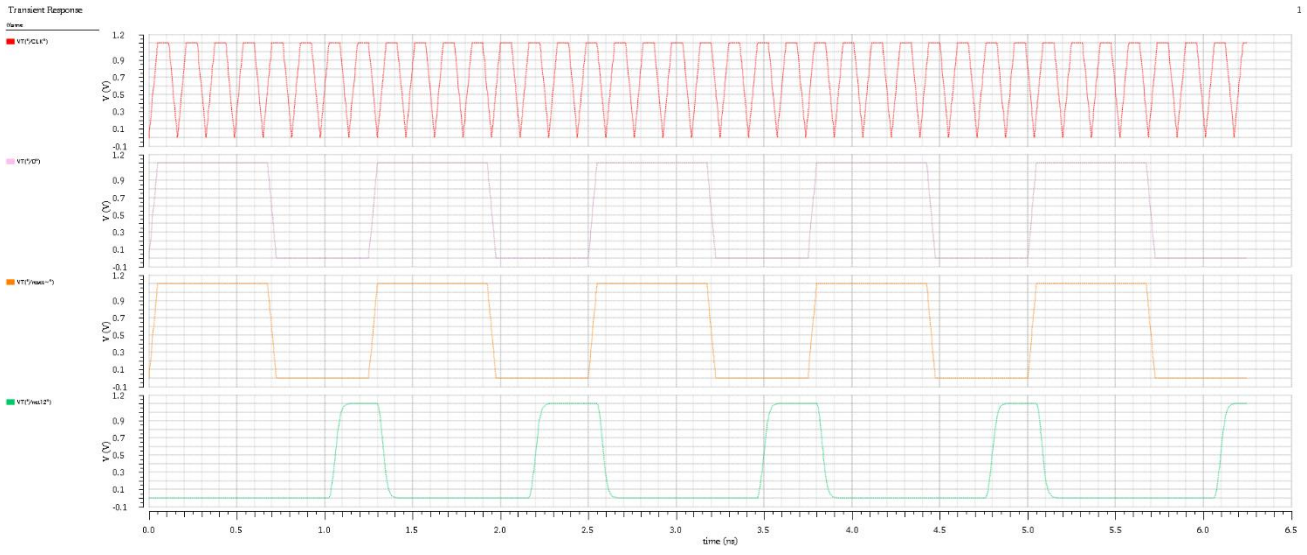


CORRECT OPERATION OF DATA PATH:

Clock frequency: 5Ghz
Data frequency: 500Mhz

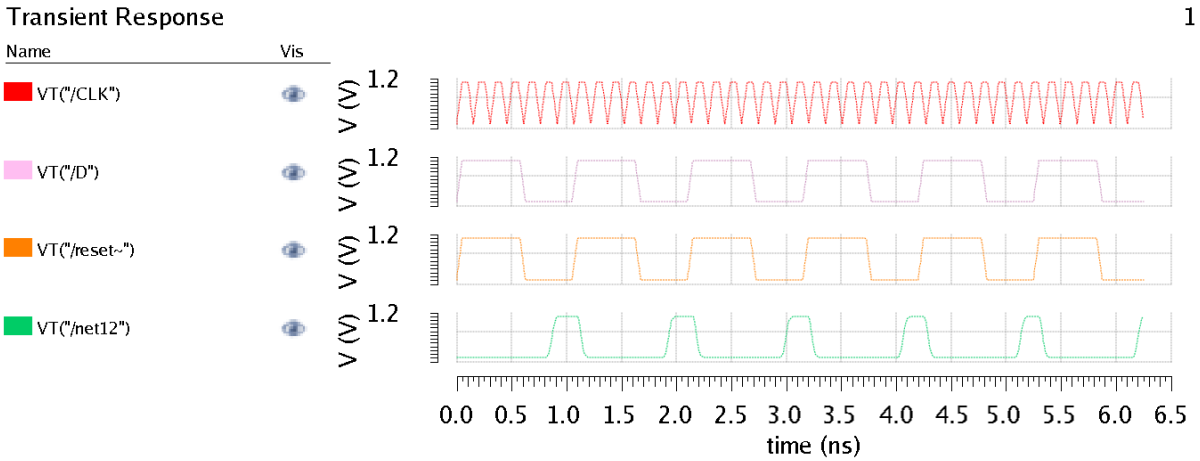


Clock frequency: 8Ghz
Data frequency: 800Mhz

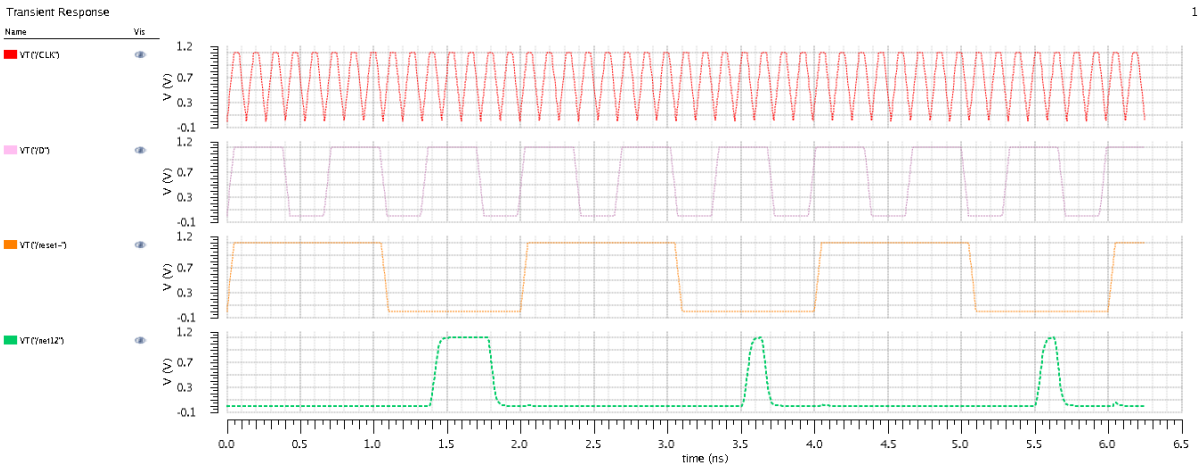


CORRECT OPERATION OF DATA PATH:

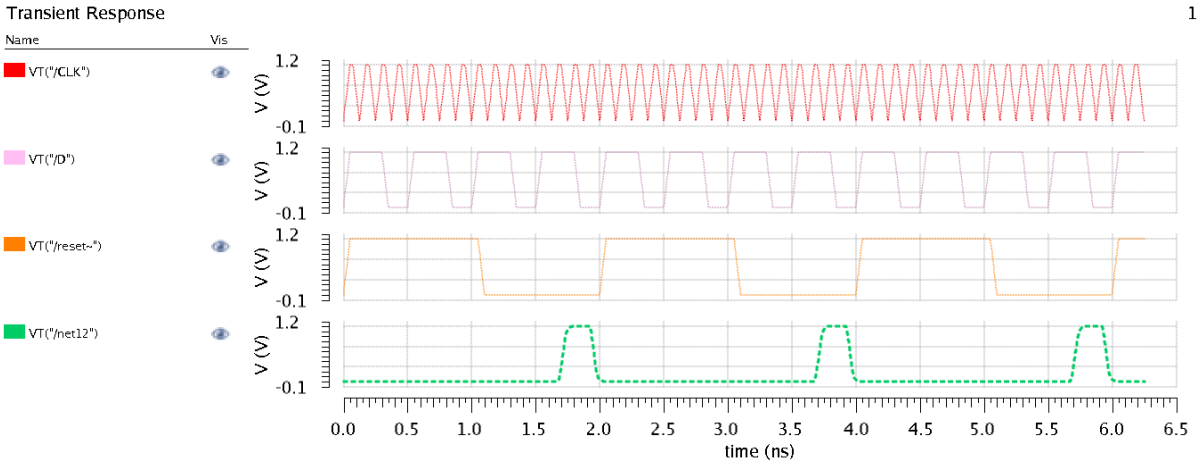
Clock frequency: 9.5Ghz
Data frequency: 950MhZ



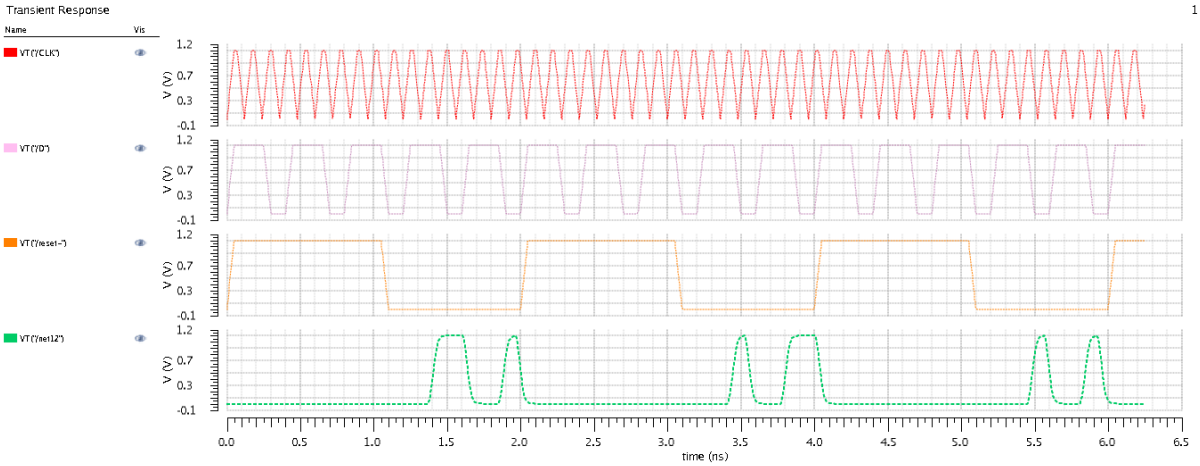
Clock frequency: 15Ghz
Data frequency: 1.5GhZ



Clock frequency: 20Ghz
Data frequency: 2GhZ



Clock frequency: 30Ghz
Data frequency: 3GHz

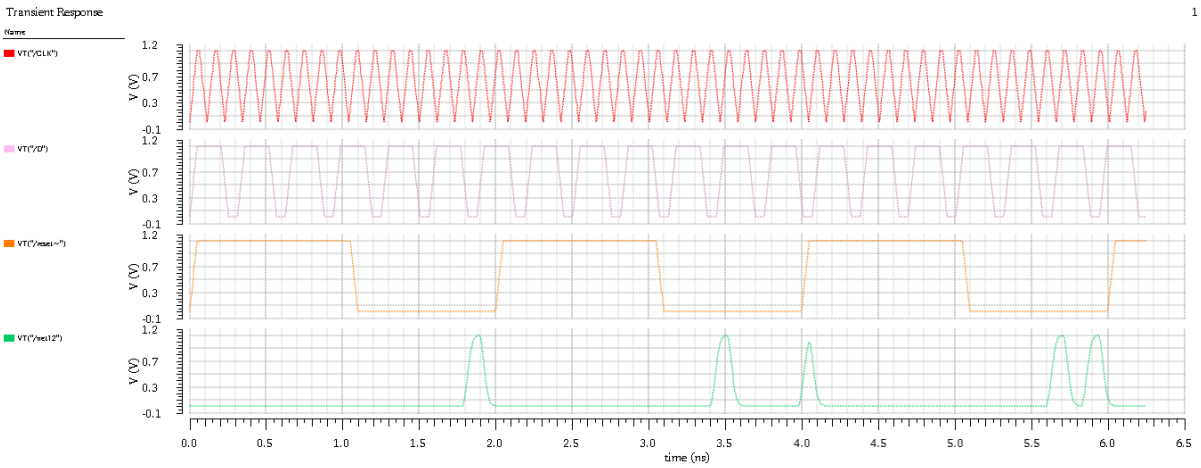


- MAXIMUM CLOCK FREQUENCY OF OPERATION: **30GHz**

FAILURE OF DATA PATH OPERATION

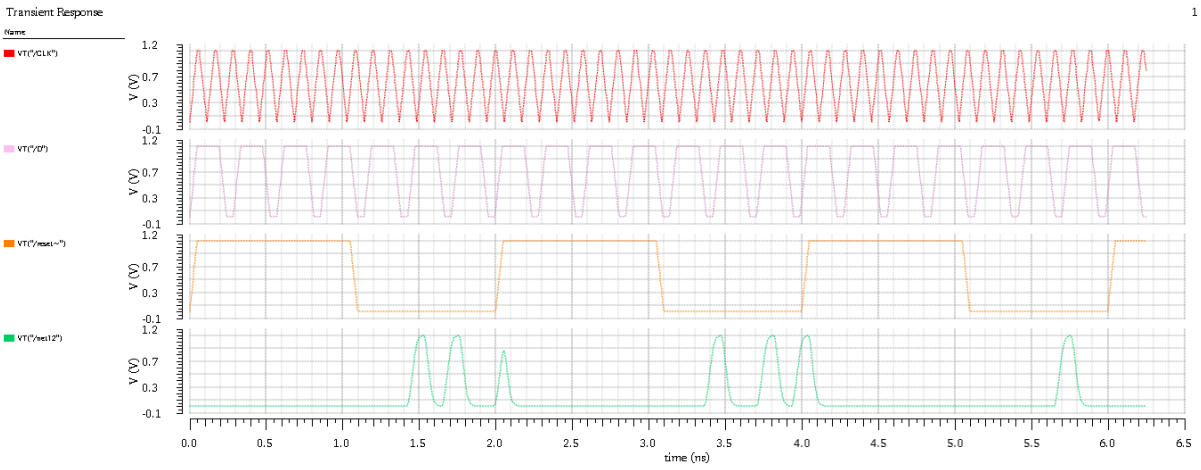
Clock frequency: 31Ghz

Data frequency: 3.1GhZ



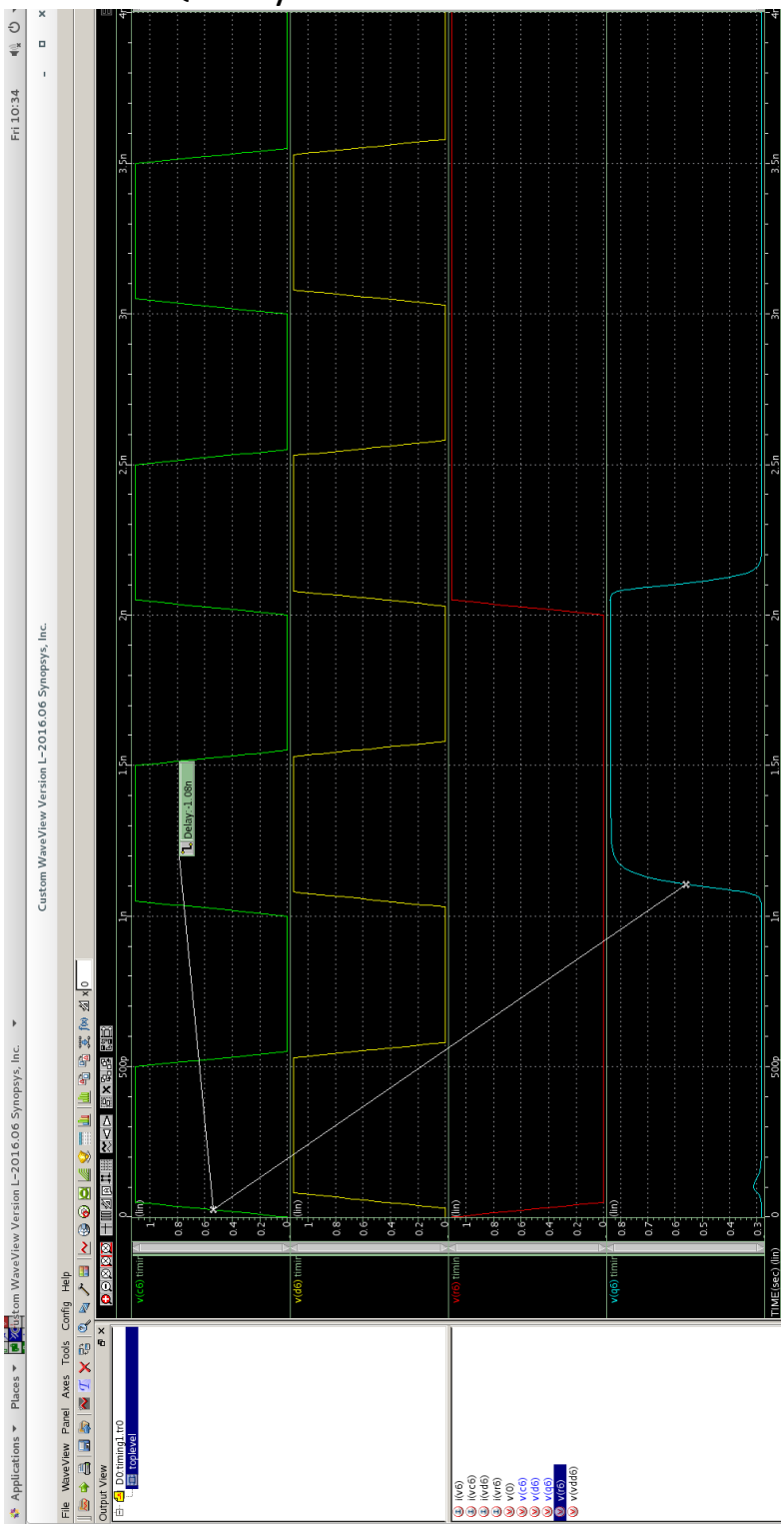
Clock frequency: 35Ghz

Data frequency: 3.5GhZ



Clock-to-Q delay:

For latching logic high,
Clock-to-Q delay: 1.09ns

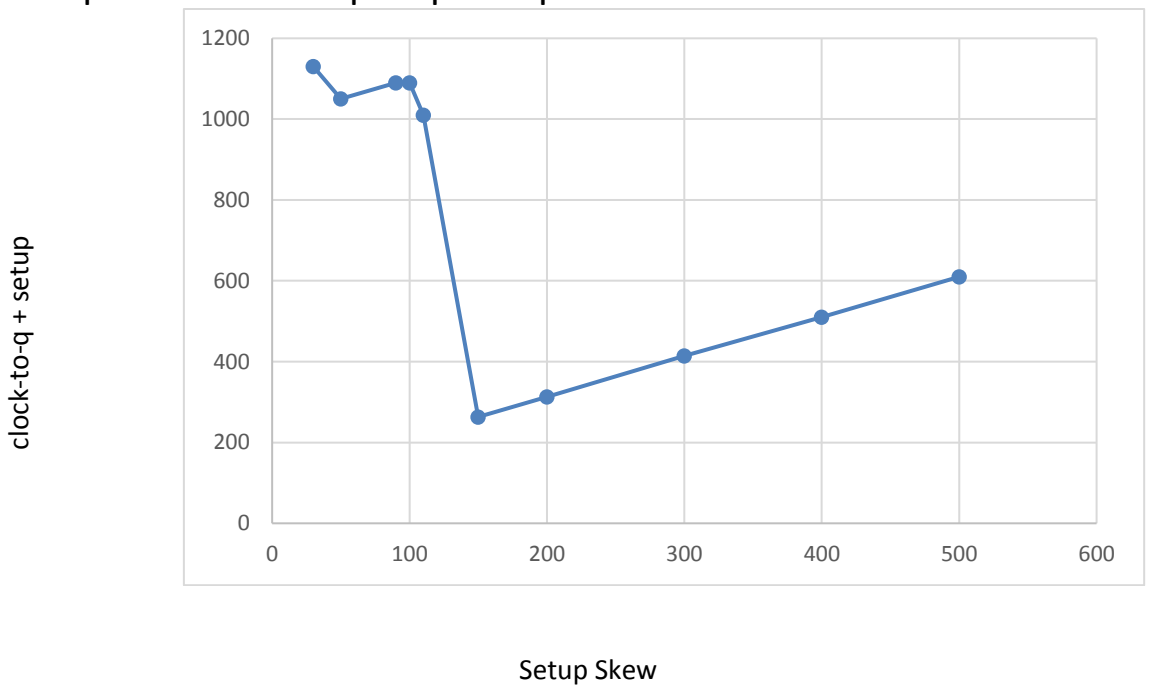


For latching logic low,
Clock-to-Q delay: 1.12ns

Setup time:

Setup skew(ps)	Clock-to-q delay(ps)	setup+clock-q-delay
500	82	582
400	82.2	482.2
300	83	383
200	83.3	283.3
150	83.3	233.3
110	900	1010
100	990	1090
90	1000	1090
50	1000	1050
30	1100	1130

Setup time of the flip-flop: 150ps



Hold time:

Hold skew(ps)	clock-to-q delay(ps)
500	1080
400	1080
300	1080
200	1080
150	1080
110	1080
100	1080
90	1080
50	1080
30	1080
0	1080

Could not observe any change in clock-to-q delay for decreasing hold time.