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Assignment 1

Assume a CMOS inverter designed in a 45 nm technology with the following transistor sizes.
a. (W/L)n = 100 nm / 50 nm
b. (W/L)p = 200 nm / 50 nm

Q1. Assuming that this inverter drives a capacitive load of 2 fF (C_{load} = 2 fF), calculate the low-to-high and high-to-low propagation delays using the following parameters. Note that the nominal power supply voltage for this technology is 1 Volt. Assume that the input is a step function.
a. $(V_{th})n$ = 0.4106 Volts
b. $(V_{th})p$ = -0.3842 Volts
c. μ_n = 270 cm^2 / (V-s)
d. μ_p = 70 cm^2 / (V-s)
e. $\varepsilon_{ox} = 3.97 \times \varepsilon_0$
f. $\varepsilon_0 = 8.85 \times 10^{-12}$ (F/m)
g. $T_{ox,\ nmos} = 1.14 \times 10^{-9}$ (m)
h. $T_{ox,\ pmos} = 1.26 \times 10^{-9}$ (m)

Solution:

$$\{ \quad k_n = \left[\mu_{\boldsymbol{n}} \frac{\varepsilon_{\boldsymbol{ox}}}{t_{\boldsymbol{ox,nmos}}} \frac{W_n}{L_{\boldsymbol{n}}}\right] \qquad k_p = \left[\mu_{\boldsymbol{p}} \frac{\varepsilon_{\boldsymbol{ox}}}{t_{\boldsymbol{ox,pmos}}} \frac{W_p}{L_{\boldsymbol{p}}}\right]$$

$$k_n = \mathbf{1.66 \times 10^{-3}} \qquad k_p = \mathbf{0.78 \times 10^{-3}} \quad \}$$

$$t_{PHL} = \frac{C_{load}}{k_n\,(V_{DD} - V_{T,n})}\left[2\frac{V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

$$= \frac{2\times10^{-15}}{1.66\times10^{-3}\times0.5894}\left[\frac{2\times0.4106}{0.5894} + \ln\left(\frac{4\times0.5894}{1} - 1\right)\right]$$

$$= \mathbf{3.47\ ps}$$

$$t_{PLH} = \frac{C_{load}}{k_p\,(V_{DD} - |V_{T,p}|)}\left[2\frac{|V_{T,n}|}{V_{DD} - |V_{T,n}|} + ln\left(\frac{4\left(V_{DD} - |V_{T,n}|\right)}{V_{DD}} - 1\right)\right]$$

$$= \frac{2\times10^{-15}}{0.78\times10^{-3}\times0.6158}\left[\frac{2\times0.3842}{0.6158} + \ln\left(\frac{4\times0.6158}{1} - 1\right)\right]$$

$$= \mathbf{6.78\ ps}$$

Answer:

High-to-low propagation delay: 3.47ps

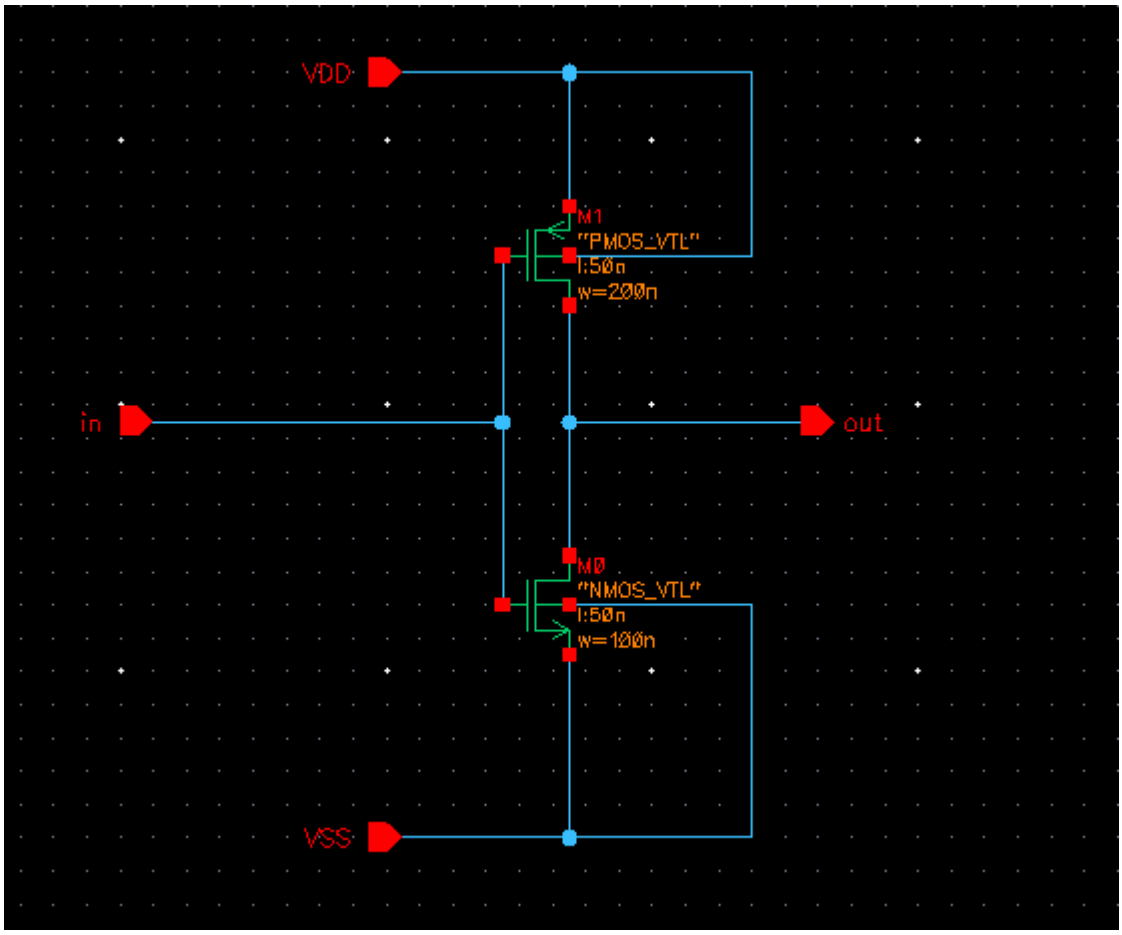
Low-to-high propagation delay: 6.78ps

2. Start Cadence and open a new schematic window named “inverter” under the main library. Design this inverter using Cadence schematic view. Generate a symbol. Next, start another schematic window named “inverter_test” under the same library to simulate (transient analysis) the inverter. Provide a pulse waveform as the input with a period of 2 nm and 50% duty cycle. Verify correct functionality. Next, simulate (perform transient analysis for 5 clock cycles, equal to 10 ns) the schematic netlist and determine both the low-to-high and high-to-low propagation delays for the following two cases:

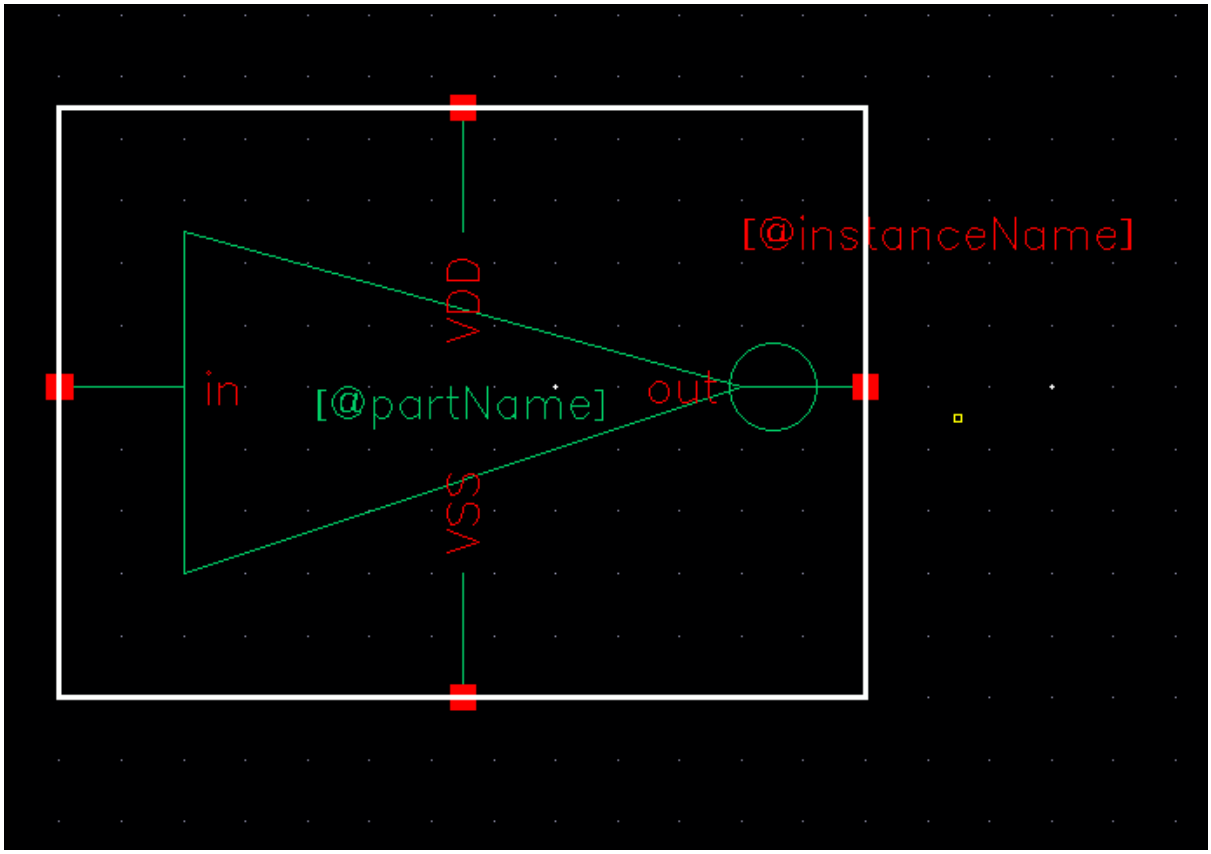
a. Rise/fall times of the input signal is 1 ps (practically step input)
b. Rise/fall times of the input signal is 200 ps
c. Compare the simulation results with the calculation results in Step 1 (Discuss the differences)

Solution:

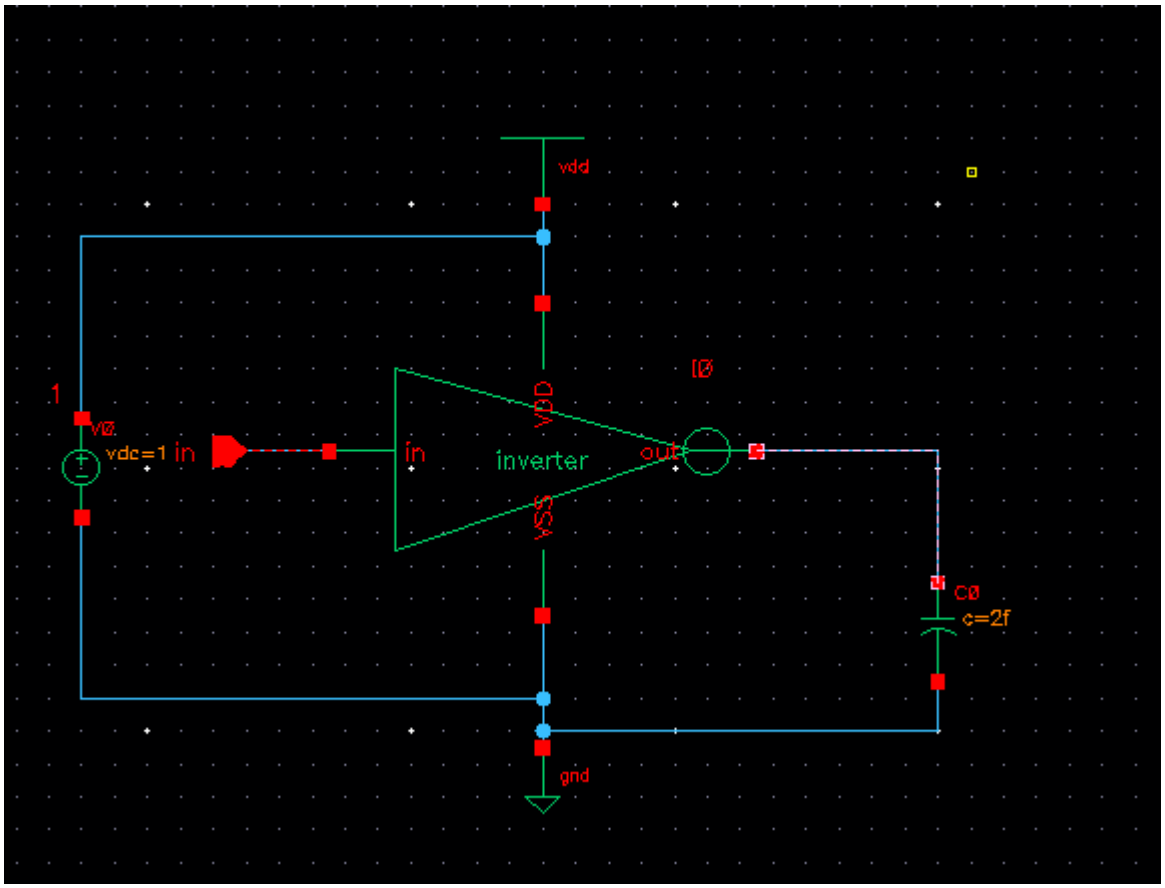
Schematic View:



Symbol view:

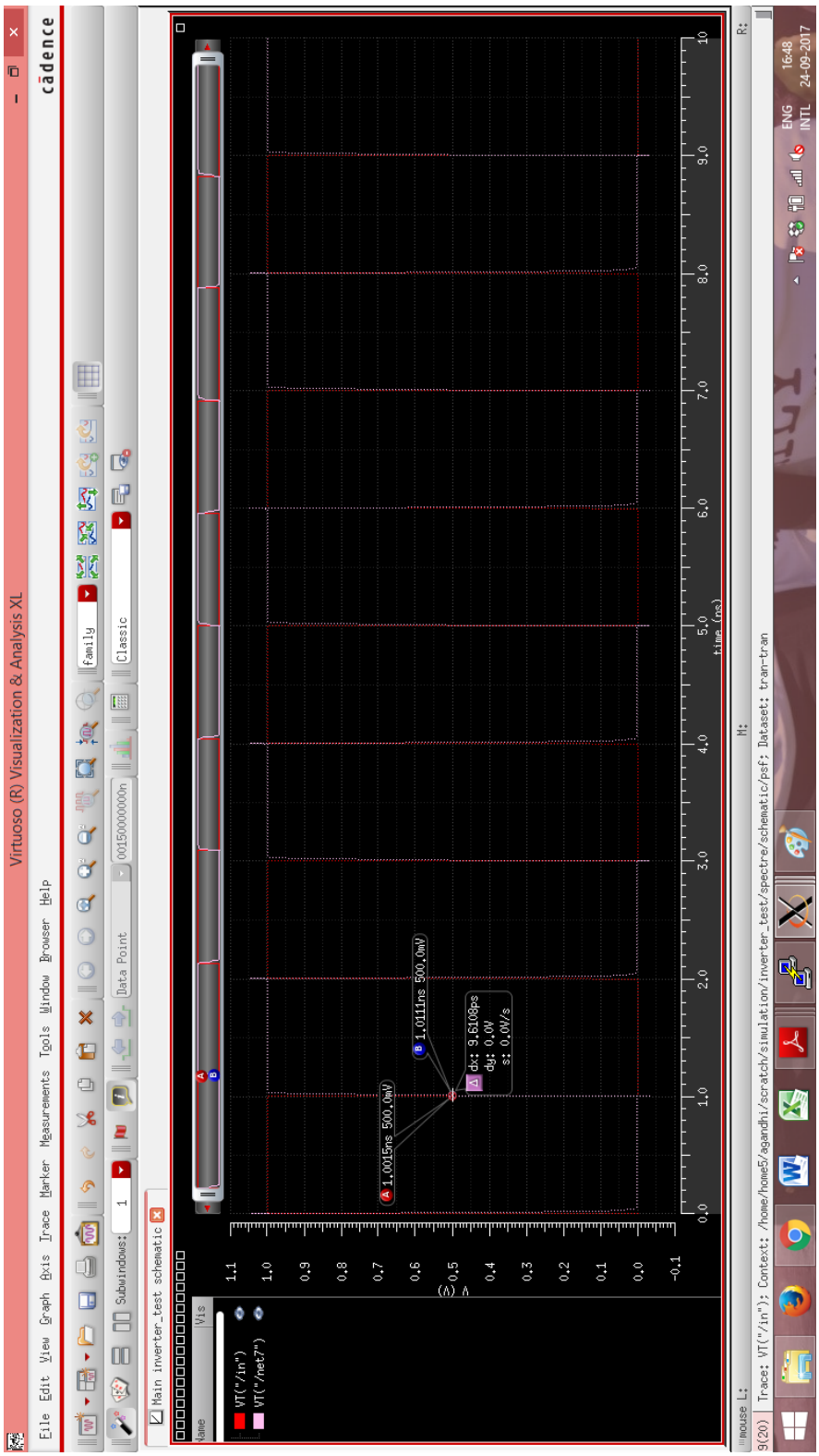


Schematic of inverter_test:

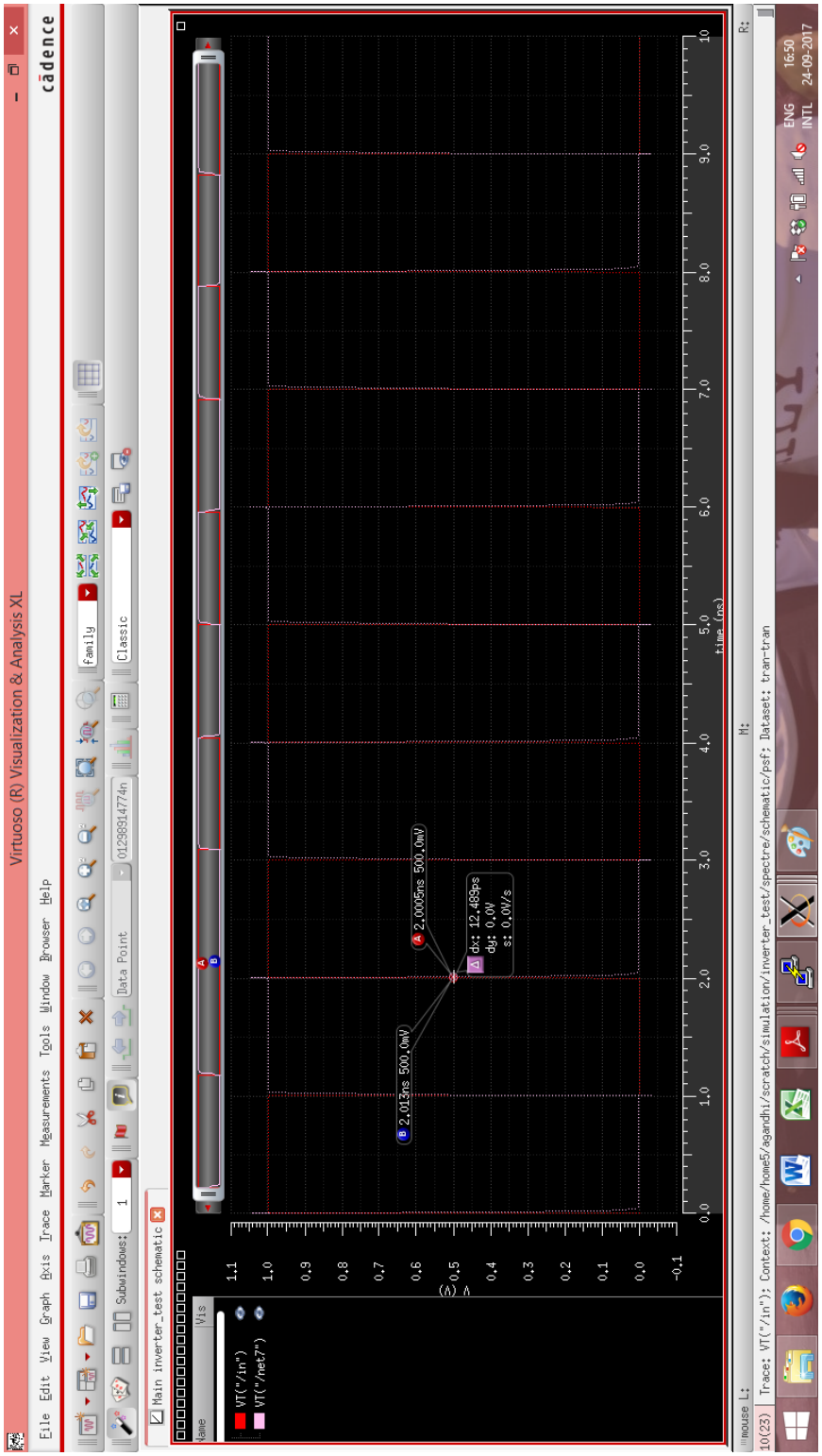


Case a:

Rise/fall times of the input signal is 1 ps



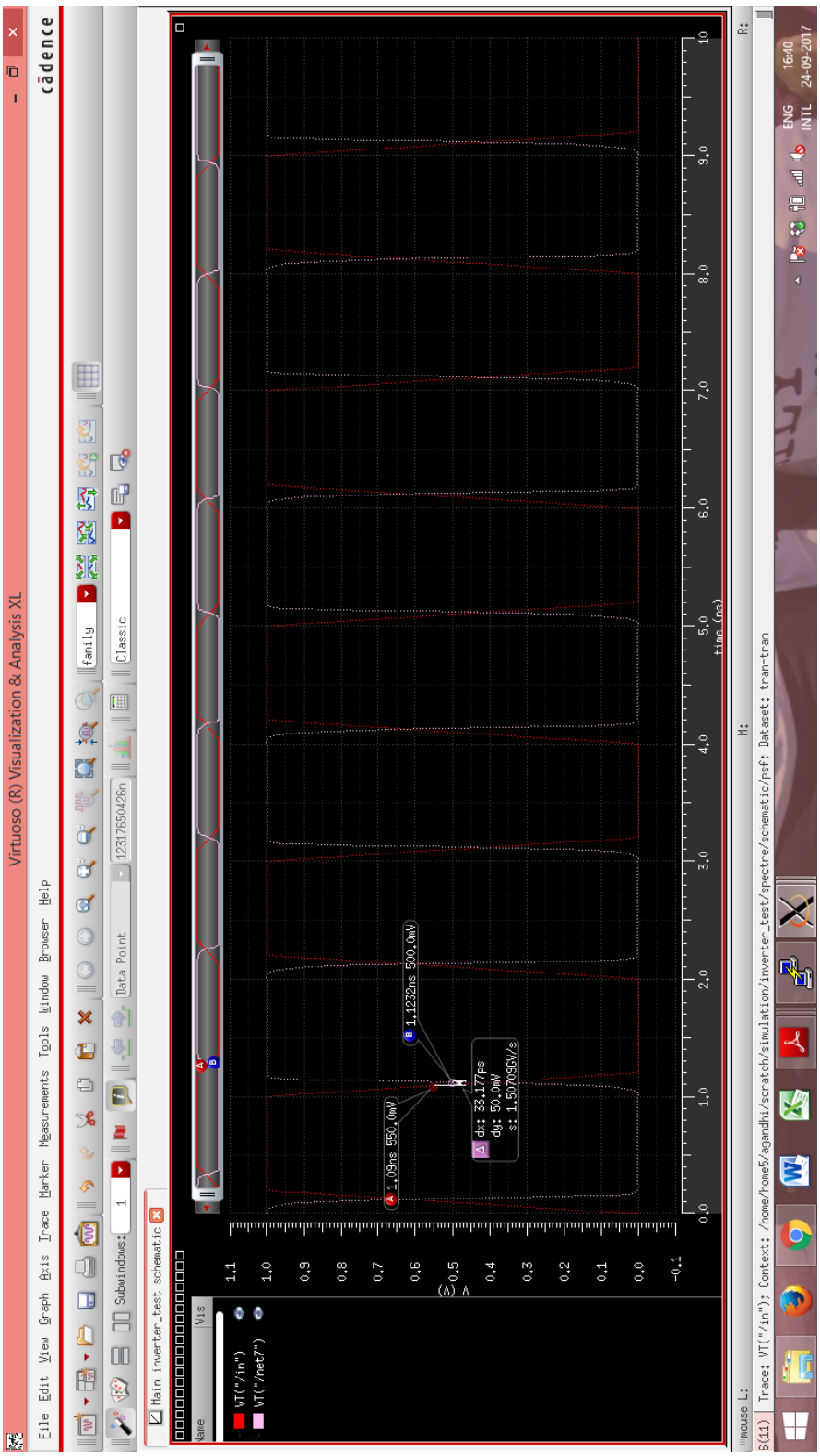
Low to high propagation delay: 9.61ps



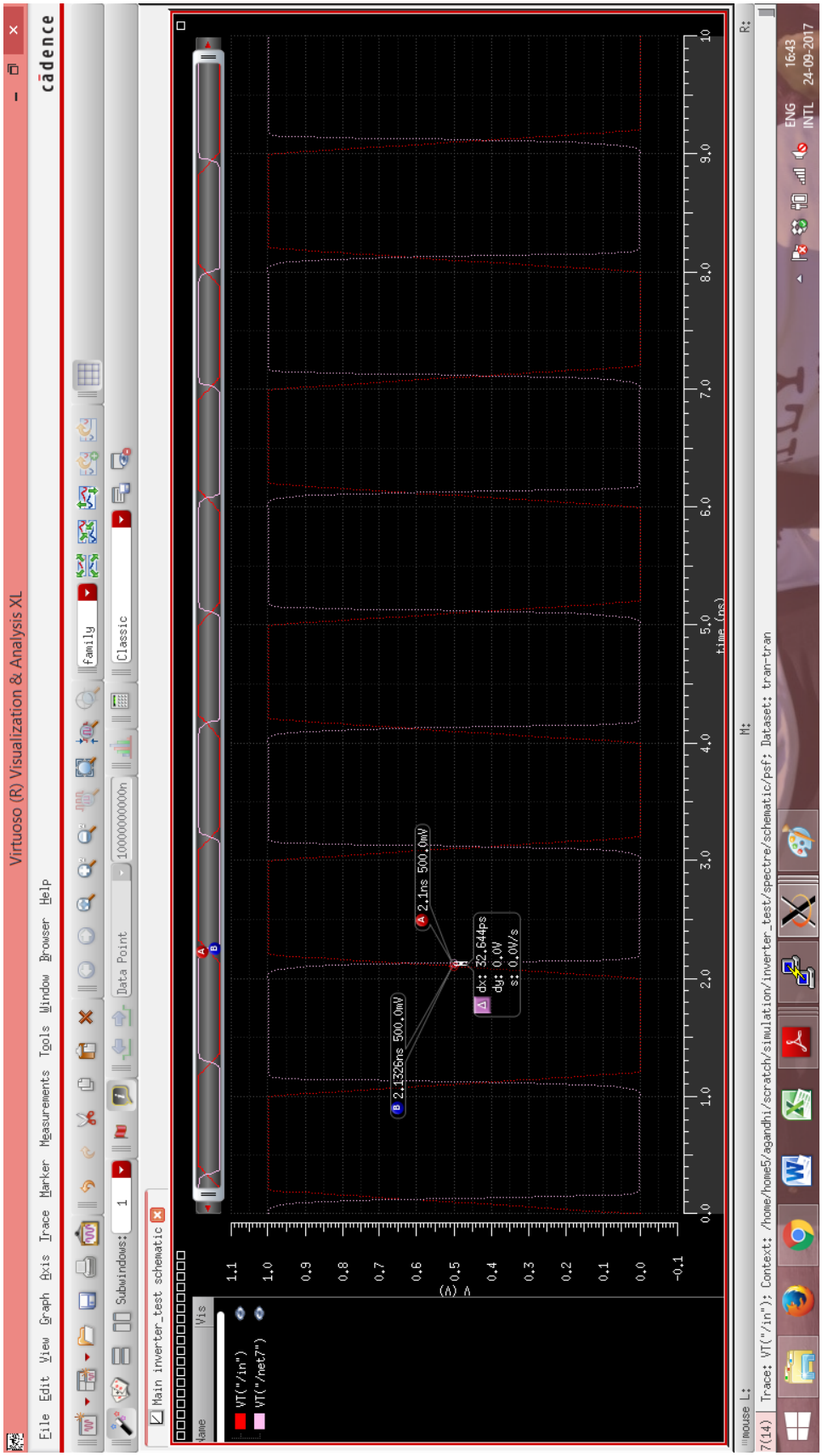
High to low propagation delay: 12.489ps

Case b:

Rise/fall times of the input signal is 200 ps



Low to high propagation delay: 33.17ps



High to low propagation delay: 32.644ps

Case c:

Compare the simulation results with the calculation results in Step 1:

By calculations,

High-to-low propagation delay: 3.47ps

Low-to-high propagation delay: 6.78ps

By transient analysis,

For, Rise/fall times of the input signal is 1 ps

High-to-low propagation delay: 12.489ps

Low-to-high propagation delay: 9.6108ps

For, Rise/fall times of the input signal is 200 ps

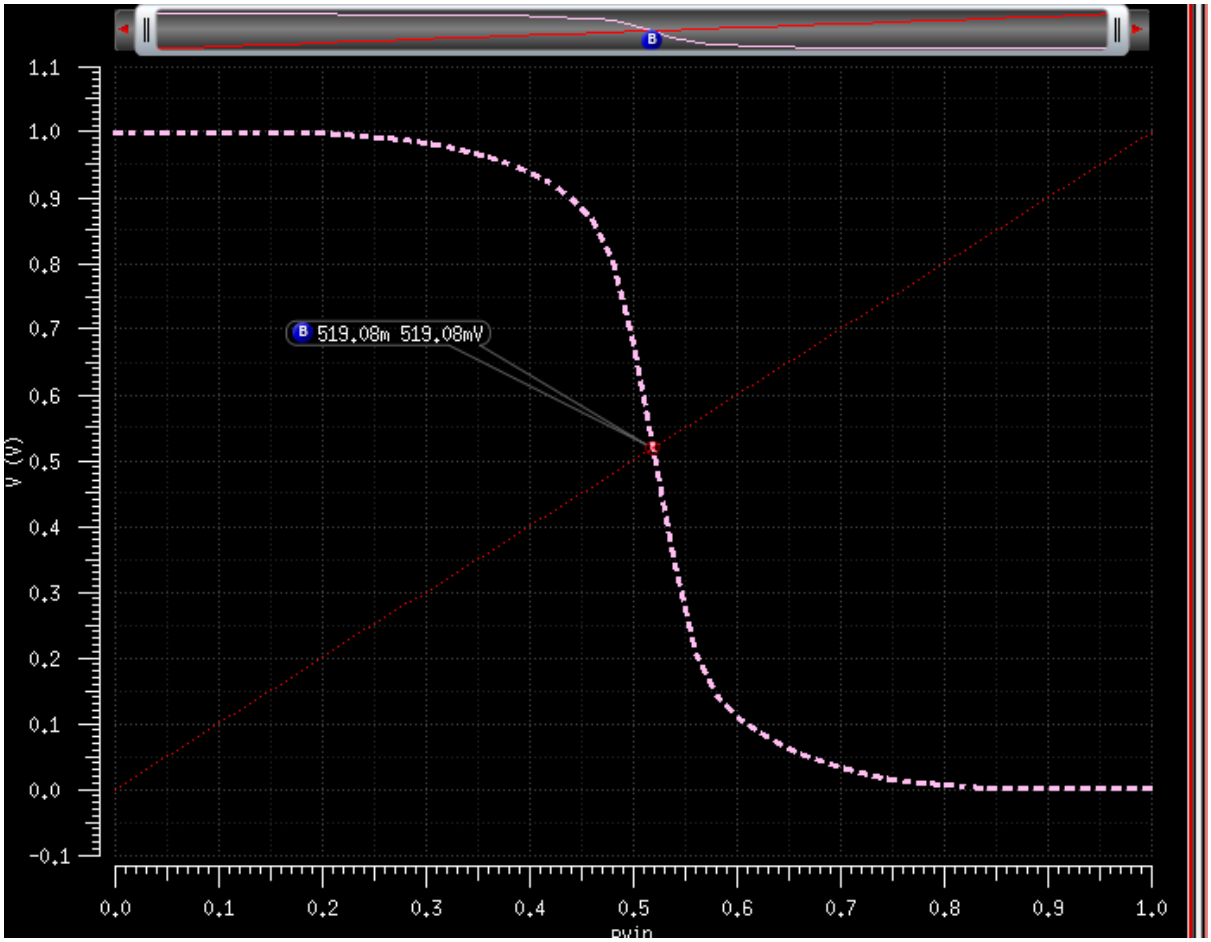
High-to-low propagation delay: 32.644ps

Low-to-high propagation delay: 33.177ps

As there is a difference in threshold voltage when calculated theoretically and practically, there is a difference in the propagation delays.

3. Obtain the DC transfer characteristic of the inverter by performing a DC analysis in Spectre. In DC analysis, a large signal at the input node will be swept from VSS to VDD and output will be analyzed for each input value. From the DC characteristics, determine if the inverter operation is symmetric. If not, resize the transistors to ensure that the DC transfer curve is symmetric (e.g., Vin=Vout line intersects the transfer function curve at half VDD). Re-perform the transient analysis to determine both low-to-high and high-to-low propagation delays again.

DC Analysis:

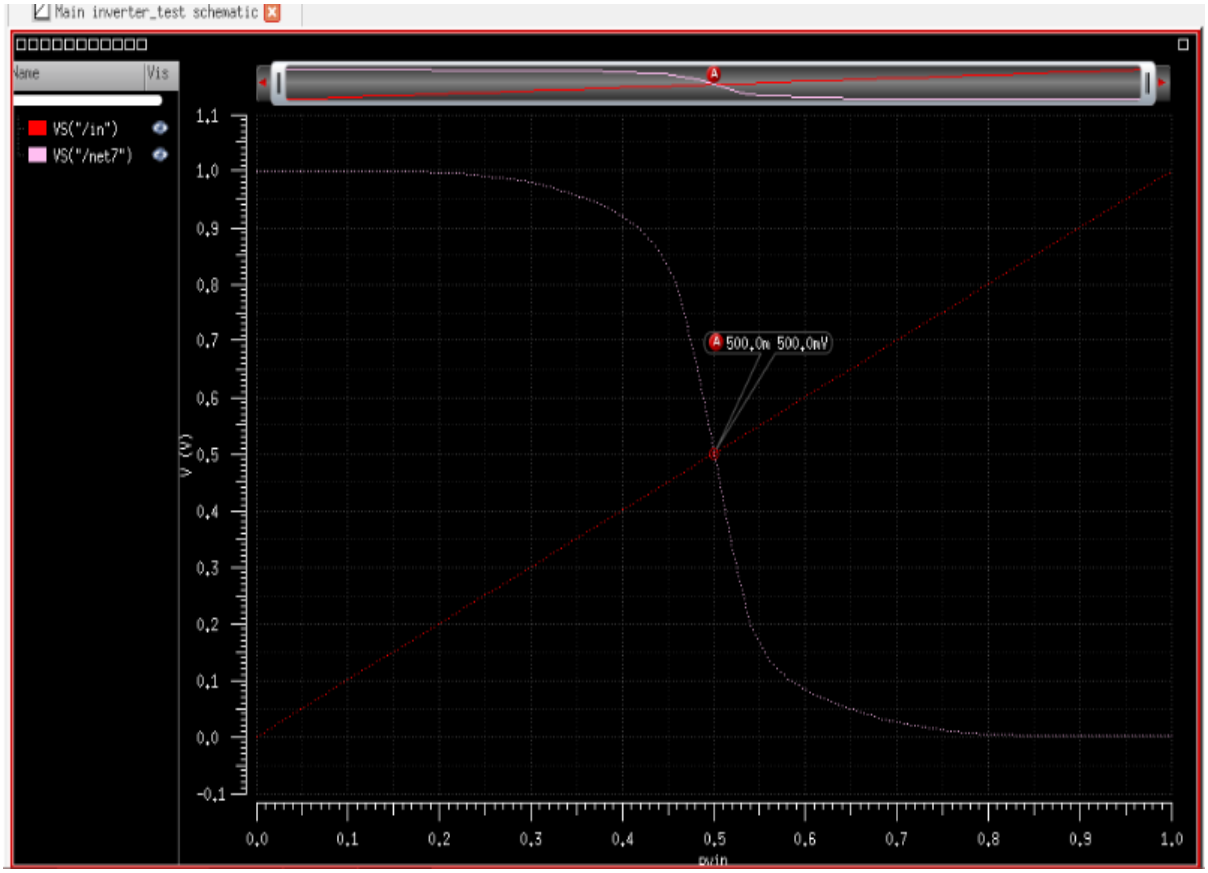


At $\frac{V_{DD}}{2}$,

$V_{in} \neq V_{out}$

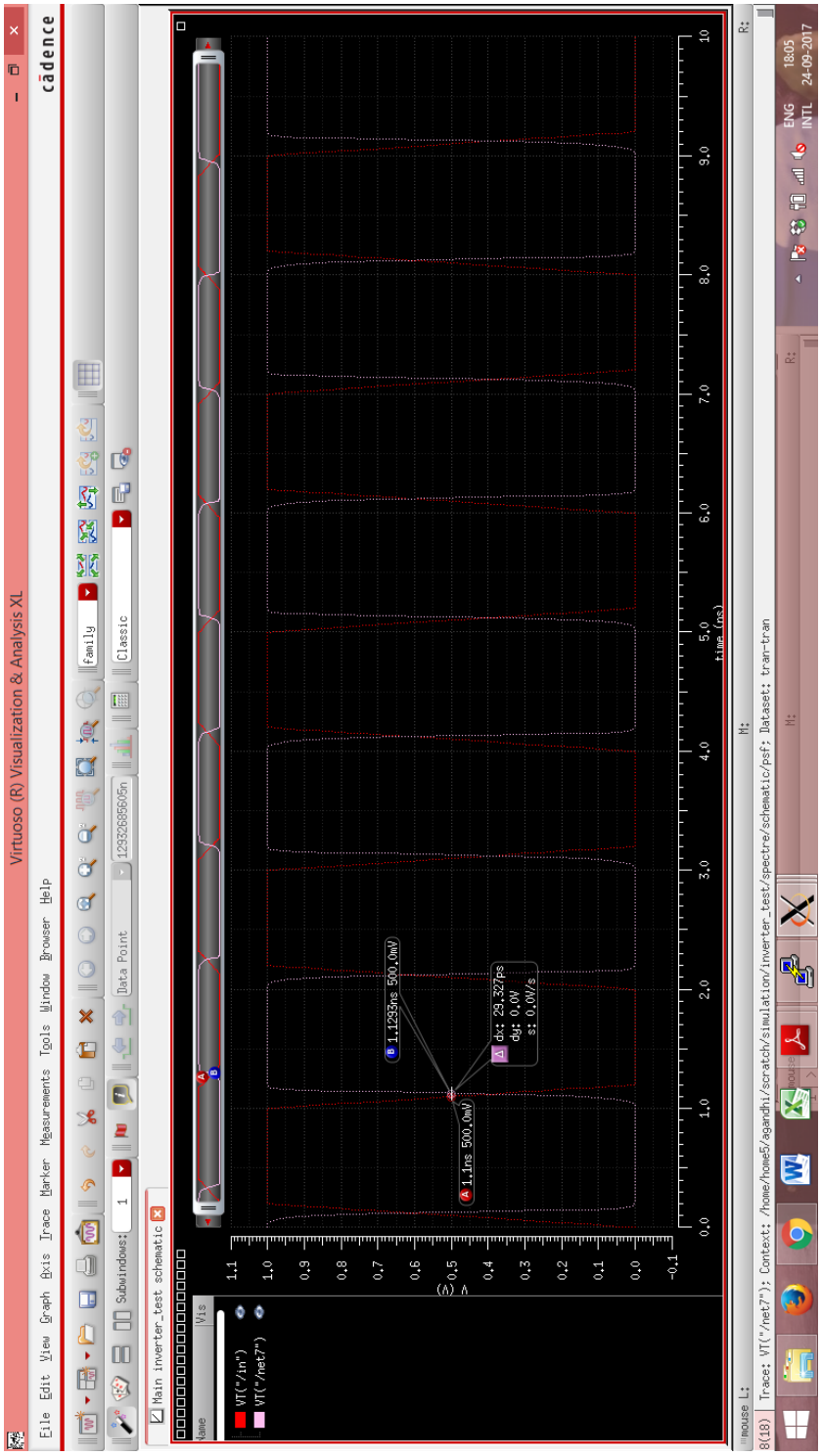
Thus, Inverter operation is asymmetric.

DC Analysis after resizing the transistors:
(Wp=160nm, Lp=50nm
Wn=100nm, Ln=50nm)



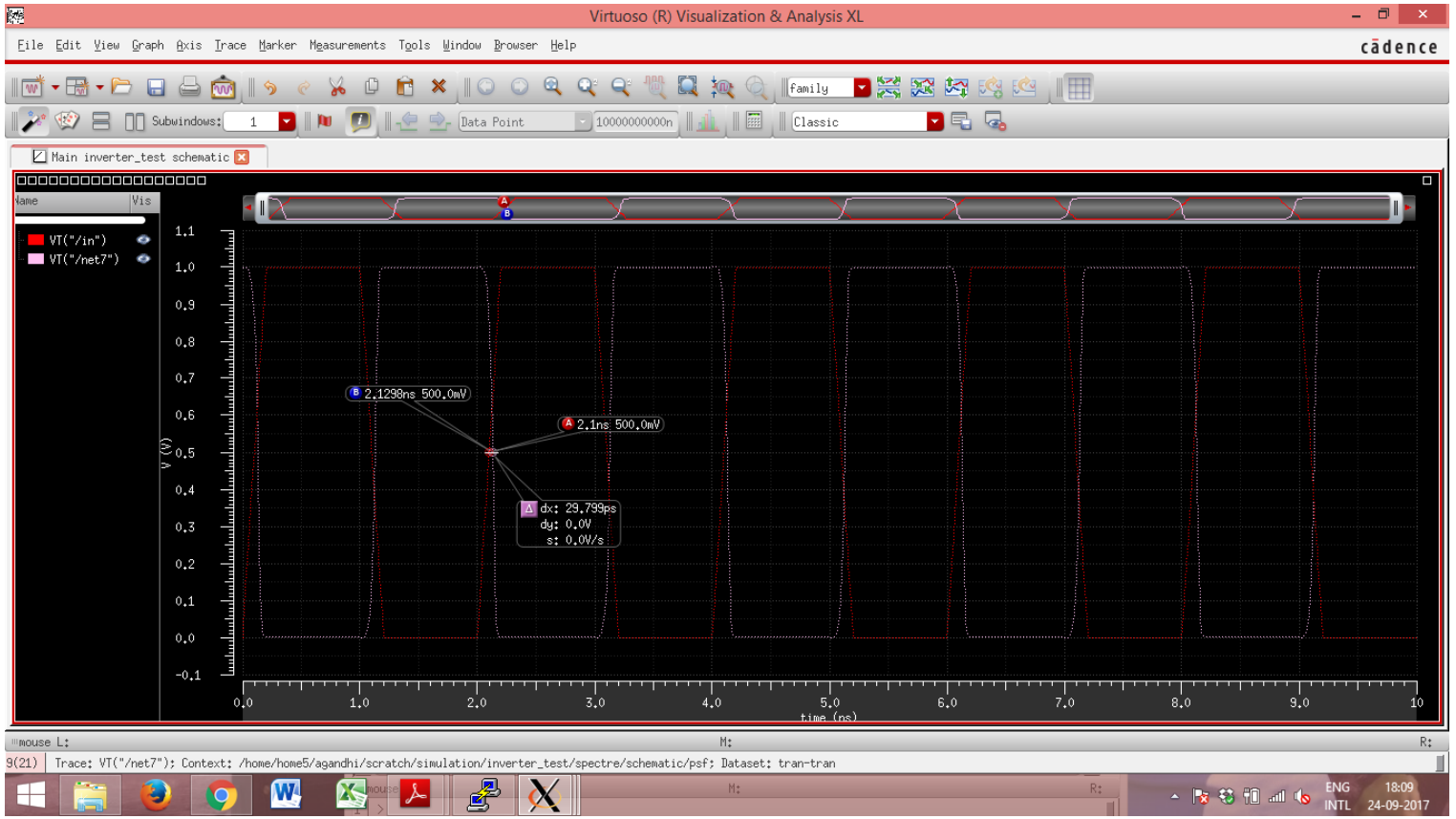
At $\frac{V_{DD}}{2}$,
$V_{in} = V_{out}$
DC analysis is symmetric.

Re-performing Transient Analysis :
(Wp=160nm, Lp=50nm
Wn=100nm, Ln=50nm,
Rise/fall time=200ps)



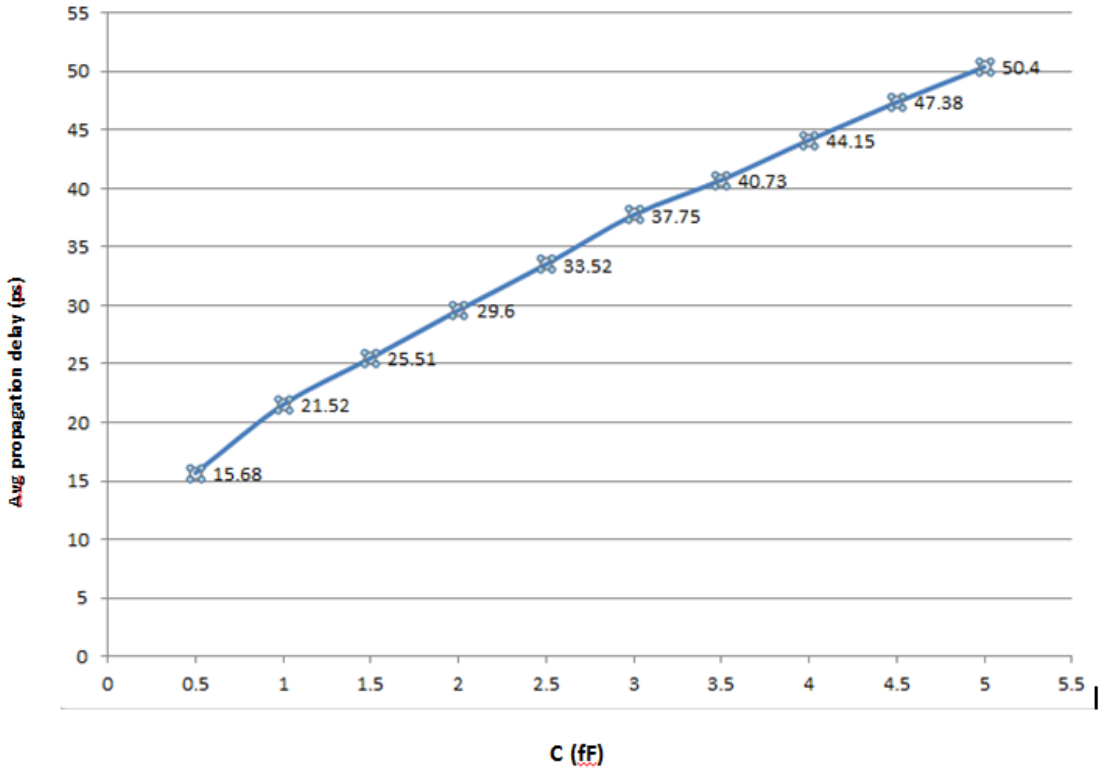
Low to high propagation delay: 29.327ps

High to low propagation delay: 29.799



4. After adjusting the sizes in the previous step, sweep the load capacitance from 0.5 fF to 5 fF in steps of 0.5 fF. Perform transient analysis to determine low-to-high and high-tolow propagation delays. Plot average propagation delay ({low-to-high+high-to-low}/2) versus output load capacitance.

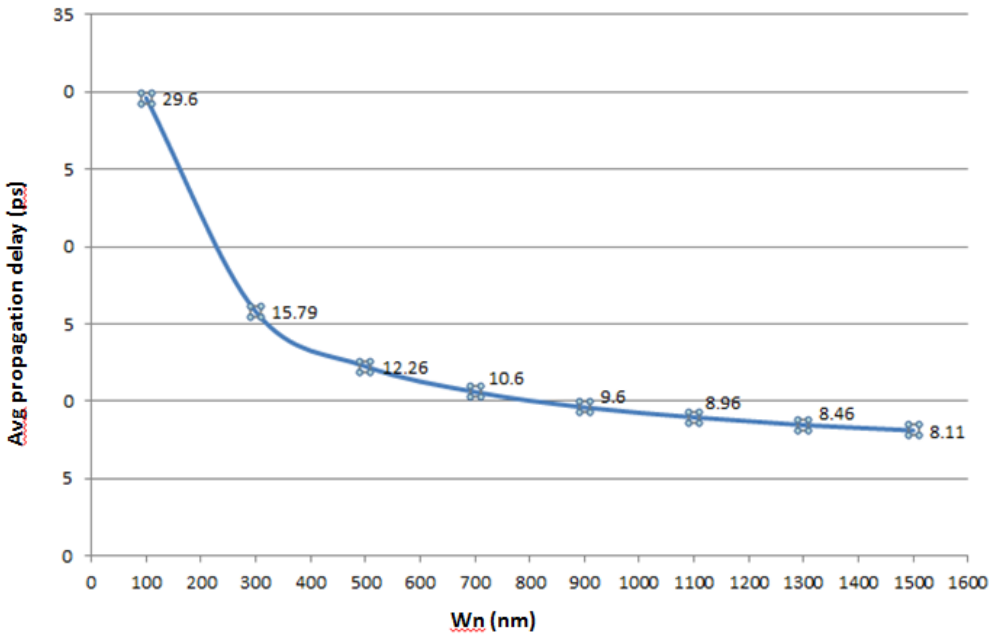
Solution:



As load capacitance increases, average propagation delay also increases.

5. Keep the output load constant at 2 fF. Also keep the Wp/Wn ratio you found in Step 3 constant. Sweep Wn until 1.5 um (with step size of 200 nm) while keeping Wp/Wn ratio constant, so for each Wn, Wp also changes. Perform transient analysis to determine low-to-high and high-to-low propagation delays. Plot average propagation delay ({lowto-high+high-to-low}/2) versus Wn.

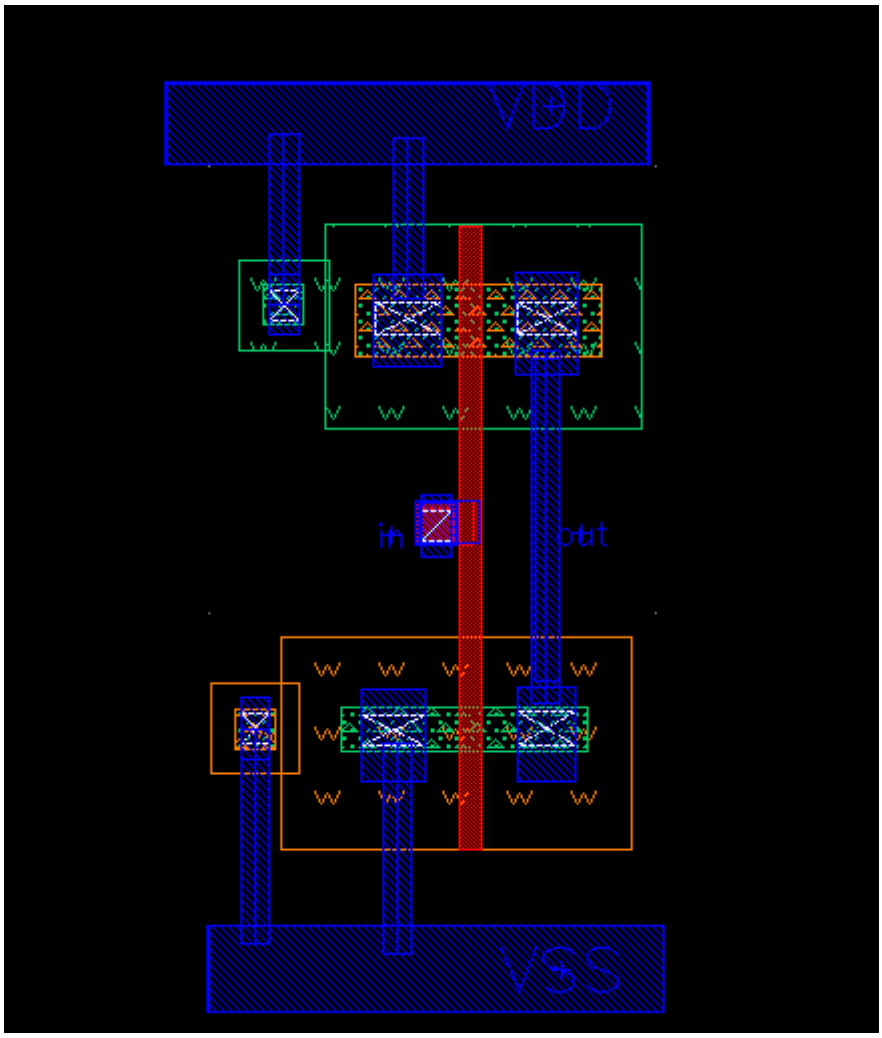
Solution:



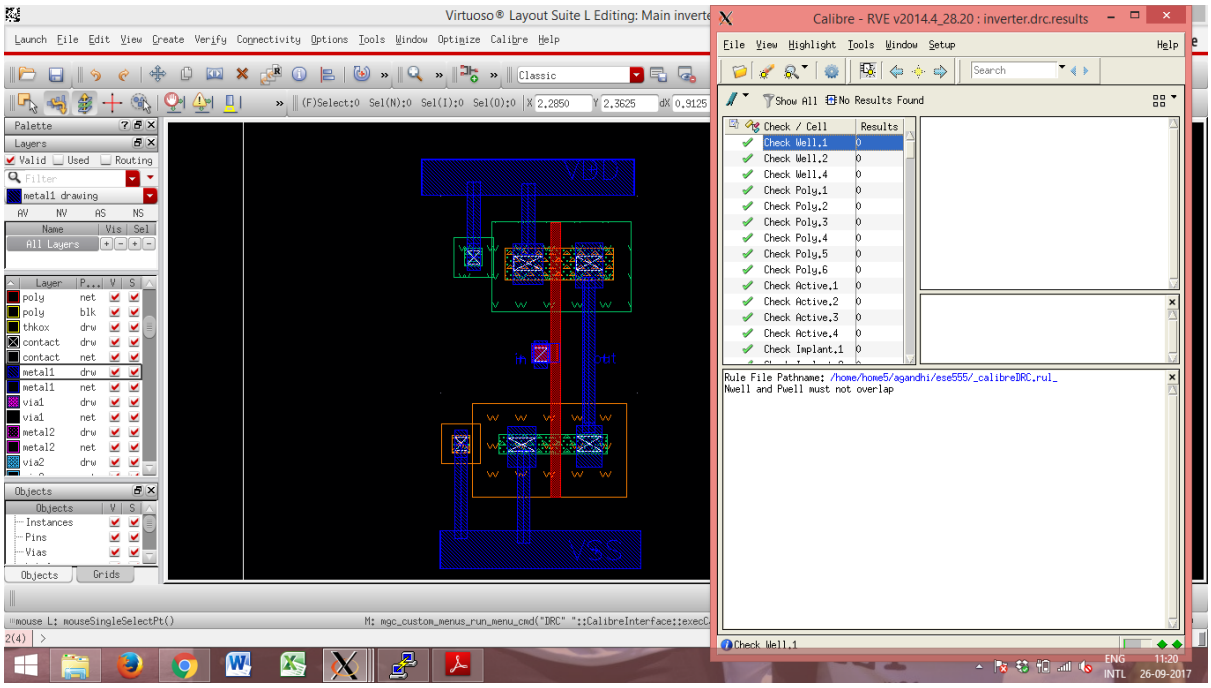
As Wn increases, average propagation delay decreases.

6. Change Wp and Wn back to the values determined in Step 3. Draw a physical layout of the final inverter using Cadence Virtuoso. Successfully pass DRC and LVS.

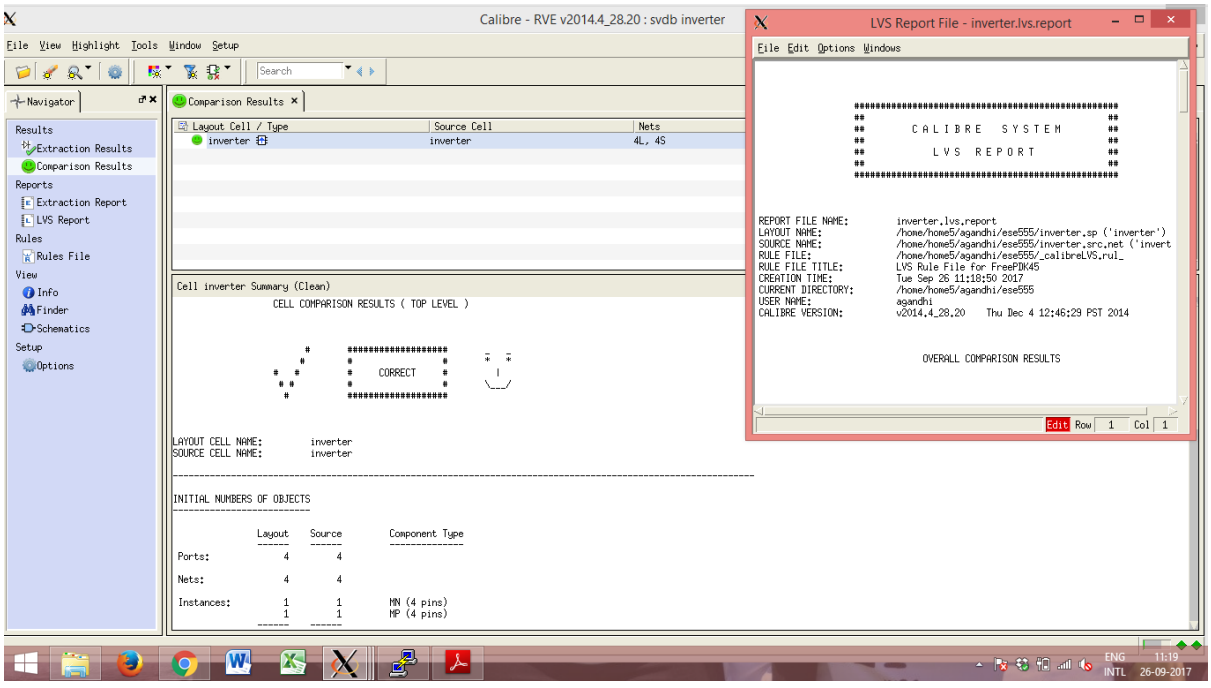
Layout view:



DRC:


Virtuoso® Layout Suite L Editing: Main inverter
Calibre - RVE v2014.4_28.20 : inverter.drc.results
Check Well.1
Check Well.2
Check Well.4
Check Poly.1
Check Poly.2
Check Poly.3
Check Poly.4
Check Poly.5
Check Poly.6
Check Active.1
Check Active.2
Check Active.3
Check Active.4
Check Implant.1
Rule File Pathname: /home/home5/agandhi/ese555/_calibreDRC.rul_
Nwell and Pwell must not overlap
VDD
VSS

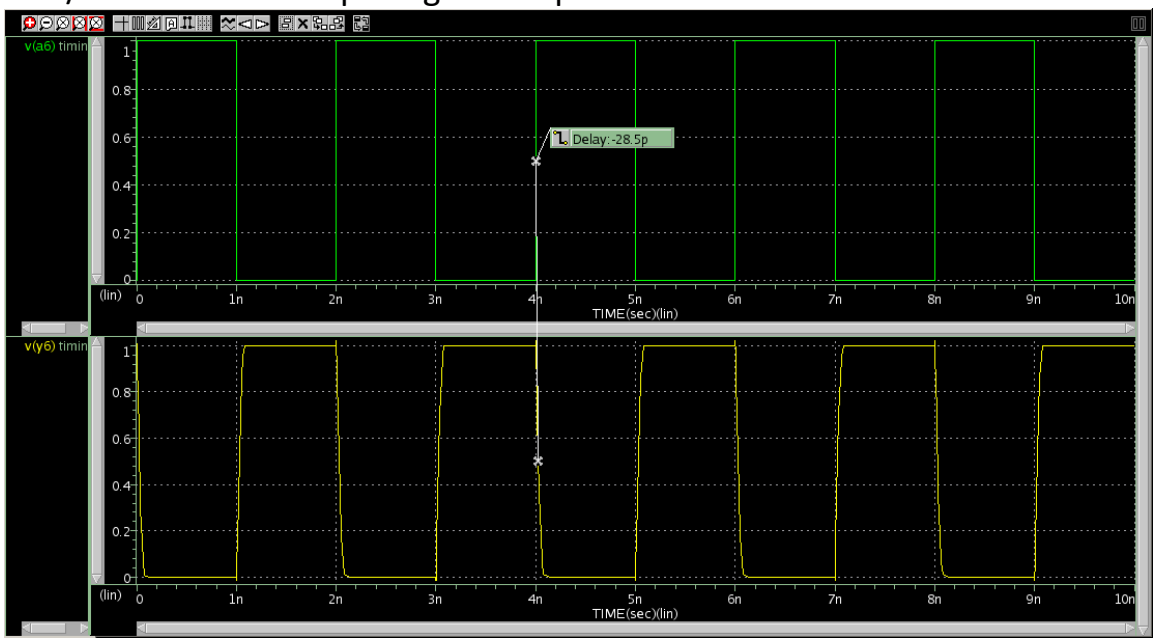
LVS:


Calibre - RVE v2014.4_28.20 : svdb inverter
LVS Report File - inverter.lvs.report
CALIBRE SYSTEM
LVS REPORT
REPORT FILE NAME: inverter.lvs.report
LAYOUT NAME: /home/home5/agandhi/ese555/inverter.sp ('inverter')
SOURCE NAME: /home/home5/agandhi/ese555/inverter.src.net ('invert
RULE FILE: /home/home5/agandhi/ese555/_calibreLVS.rul_
RULE FILE TITLE: LVS Rule File for FreePDK45
CREATION TIME: Tue Sep 26 11:18:50 2017
CURRENT DIRECTORY: /home/home5/agandhi/ese555
USER NAME: agandhi
CALIBRE VERSION: v2014.4_28.20 Thu Dec 4 12:46:29 PST 2014
OVERALL COMPARISON RESULTS
Cell inverter Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: inverter
SOURCE CELL NAME: inverter
INITIAL NUMBERS OF OBJECTS
Ports: 4 4
Nets: 4 4
Instances: 1 1 NN (4 pins)
1 1 MP (4 pins)

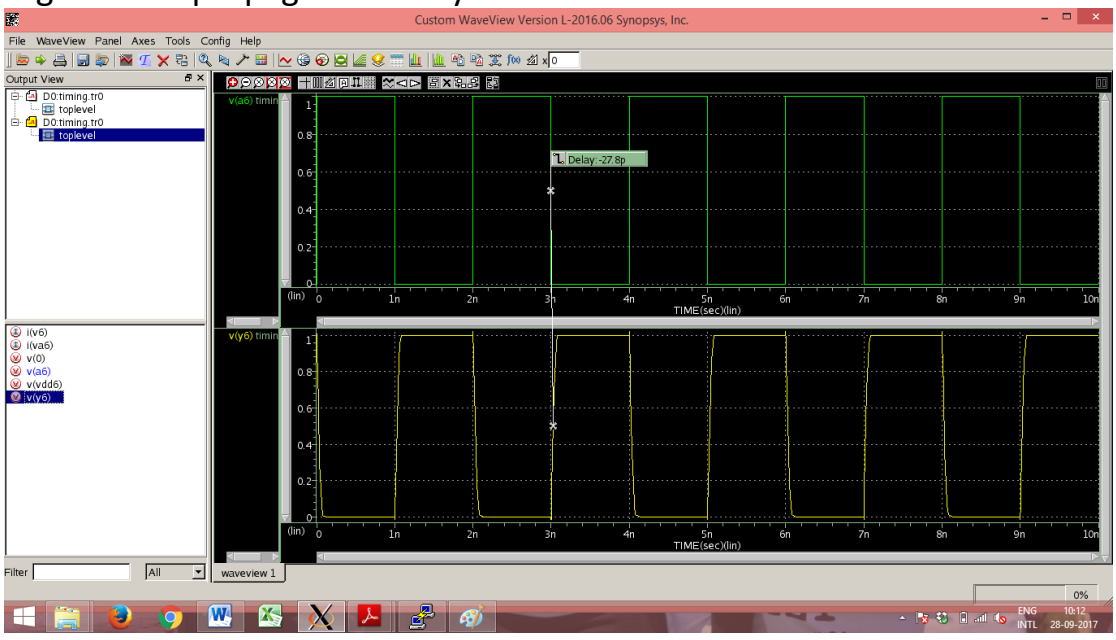
7. Extract the layout and simulate (perform transient analysis for 5 clock cycles) in HSPICE the extracted netlist to verify functionality. Also simulate both the low-to-high and high-to-low propagation delays for the following two cases:
a. Rise/fall times of the input signal is 1 ps (practically step input)
b. Rise/fall times of the input signal is 200 ps
c. Compare the simulation results (transient analysis) of the extracted netlist with that of the schematic netlist

Case a:

Rise/fall time of the input signal is 1 ps



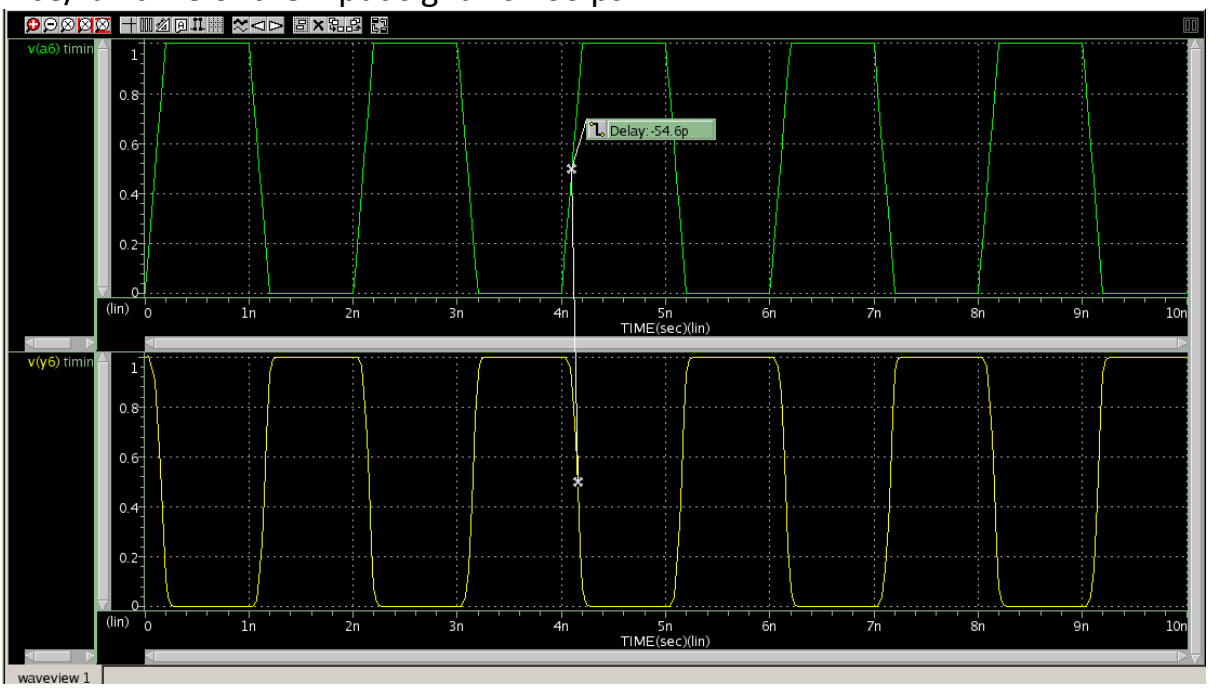
High-to-low propagation delay: 28.5



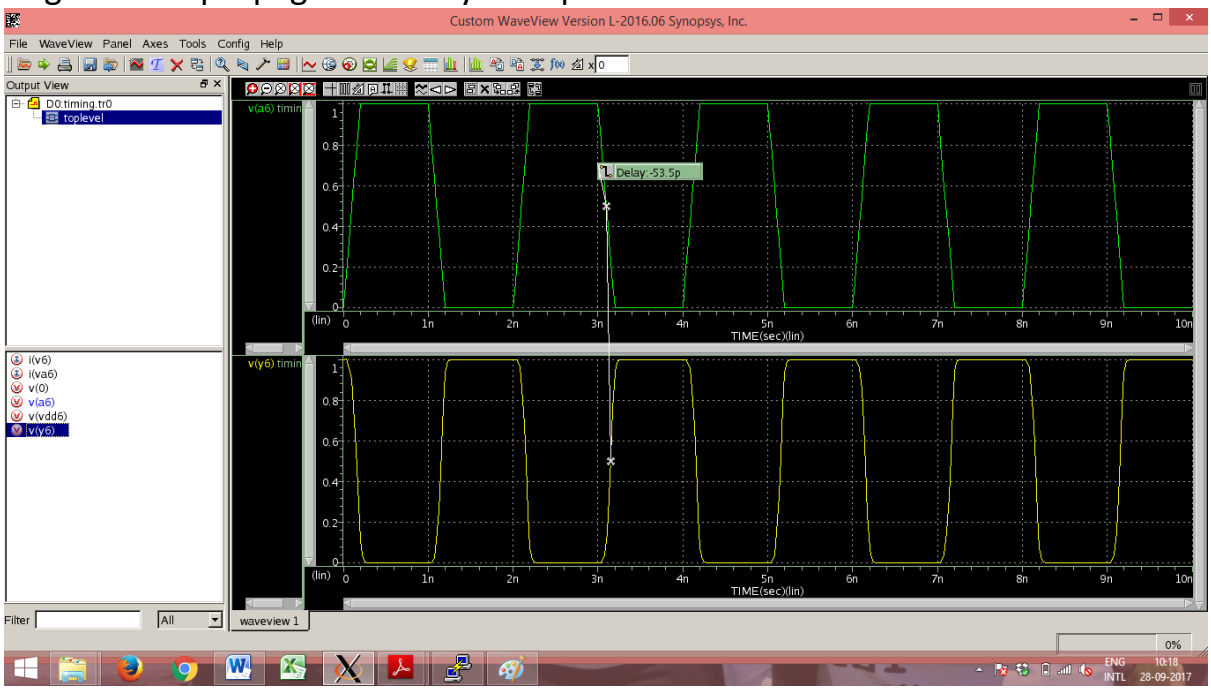
Low-to-high propagation delay: 27.8

Case b:

Rise/fall time of the input signal is 200 ps.

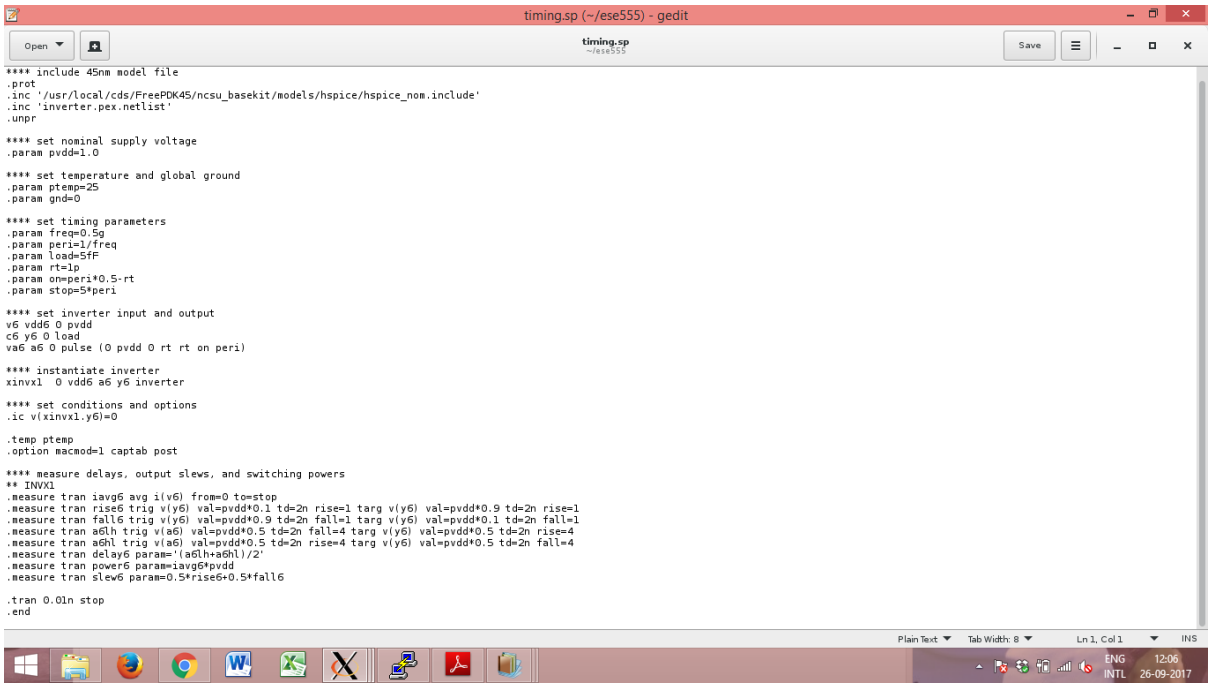


High-to-low propagation delay: 54.6ps



Low-to-high propagation delay: 53.5ps

Timing.sv file:



c. Compare the simulation results (transient analysis) of the extracted netlist with that of the schematic netlist.

Simulation results of schematic netlist:

For, Rise/fall times of the input signal is 1 ps

High-to-low propagation delay: 12.489ps

Low-to-high propagation delay: 9.6108ps

For, Rise/fall times of the input signal is 200 ps

High-to-low propagation delay: 32.644ps

Low-to-high propagation delay: 33.177ps

Simulation results of extracted netlist:

For, Rise/fall times of the input signal is 1 ps

High-to-low propagation delay: 28.5ps

Low-to-high propagation delay: 27.8ps

For, Rise/fall times of the input signal is 200 ps

High-to-low propagation delay: 54.6ps

Low-to-high propagation delay: 53.5