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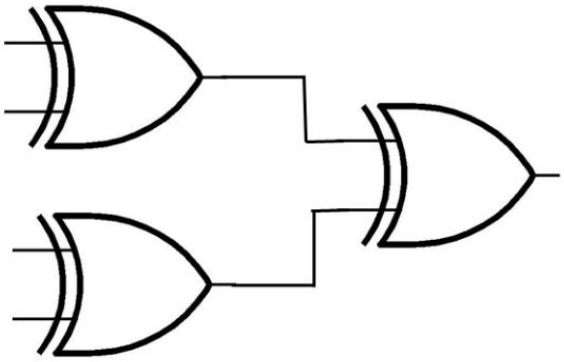
ESE 555 ASSIGNMENT 2

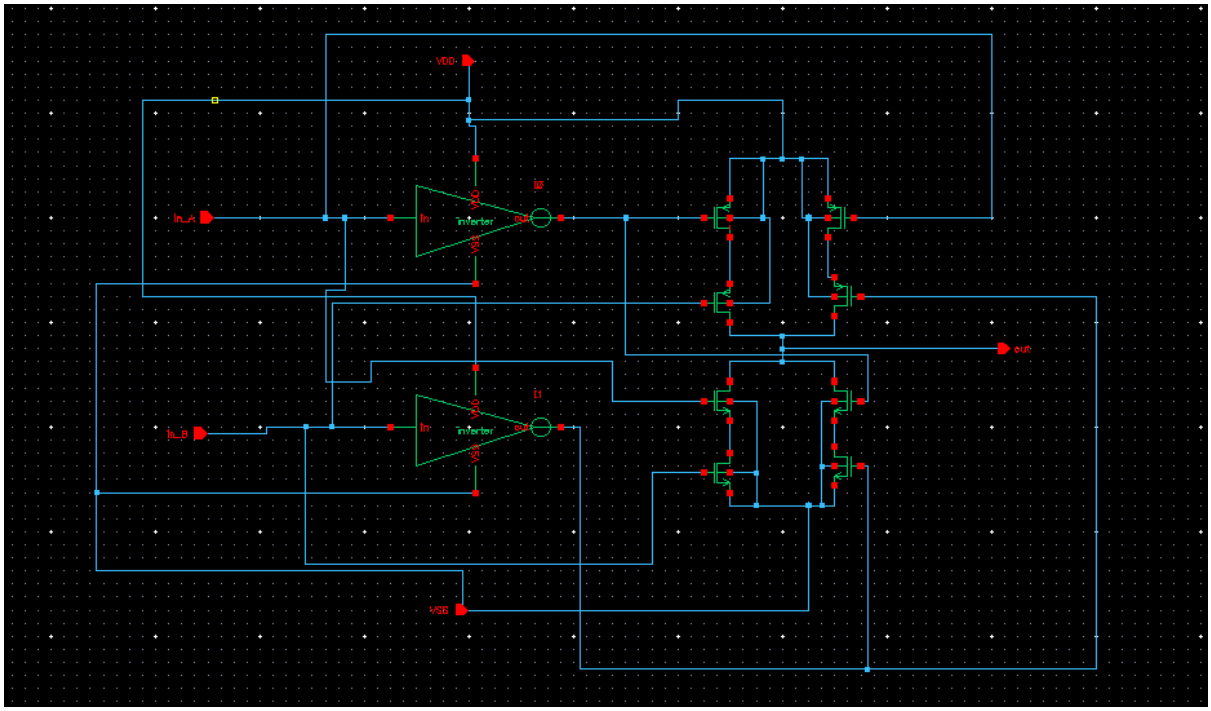
Objective: Design and verify a four-input parity generator consisting of three XOR gates in the 45 nm CMOS technology.



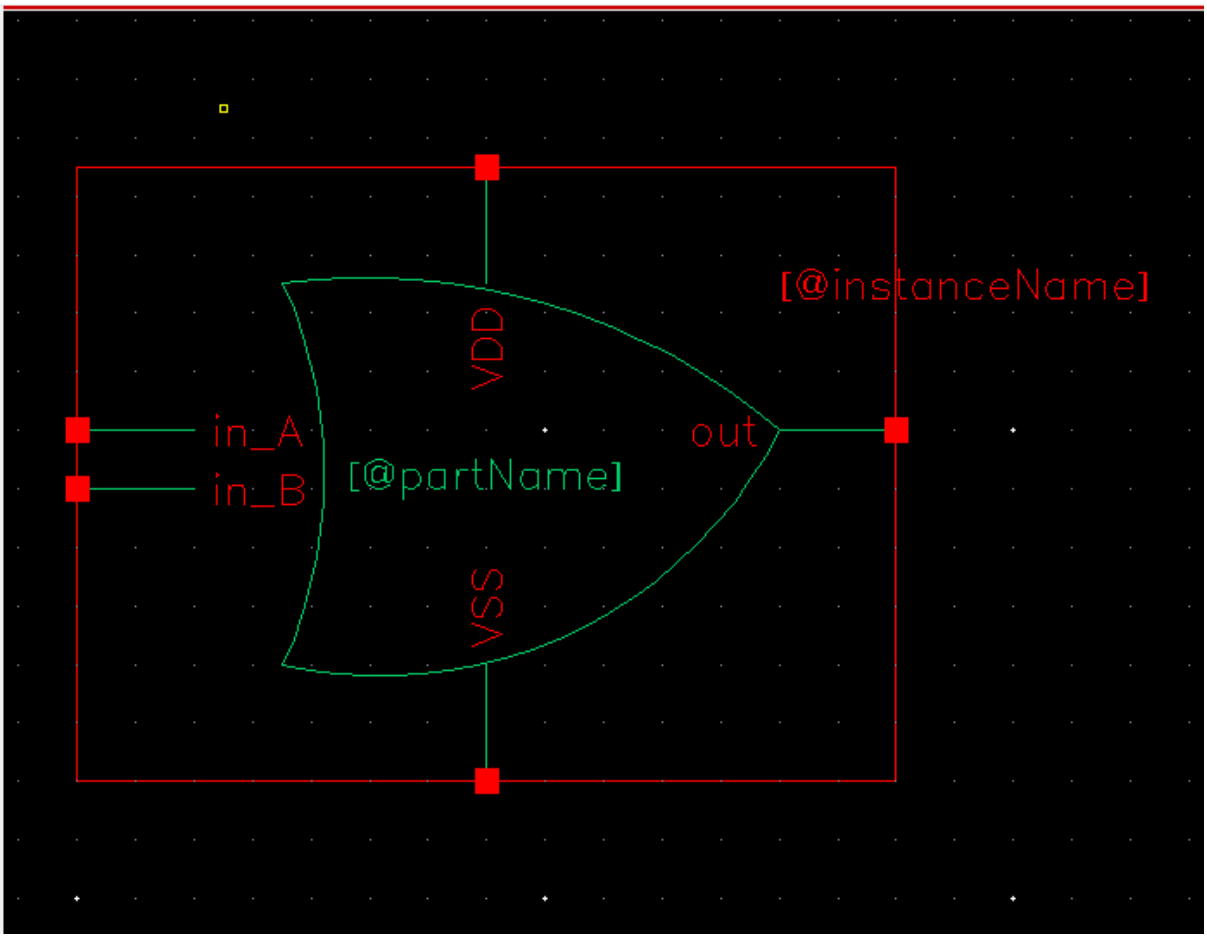
Design Objective:

- Minimize the power delay product
- Worst case propagation delay < 200ps

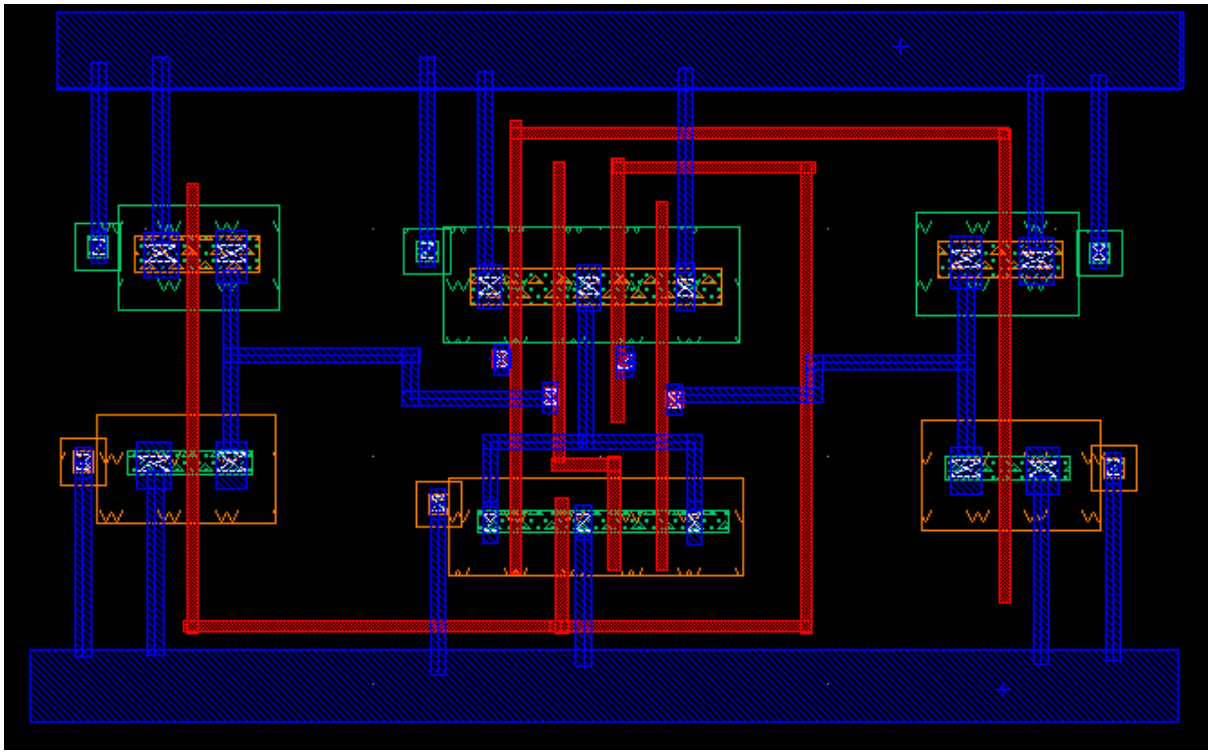
XOR Gate Design [Circuit Schematic]:



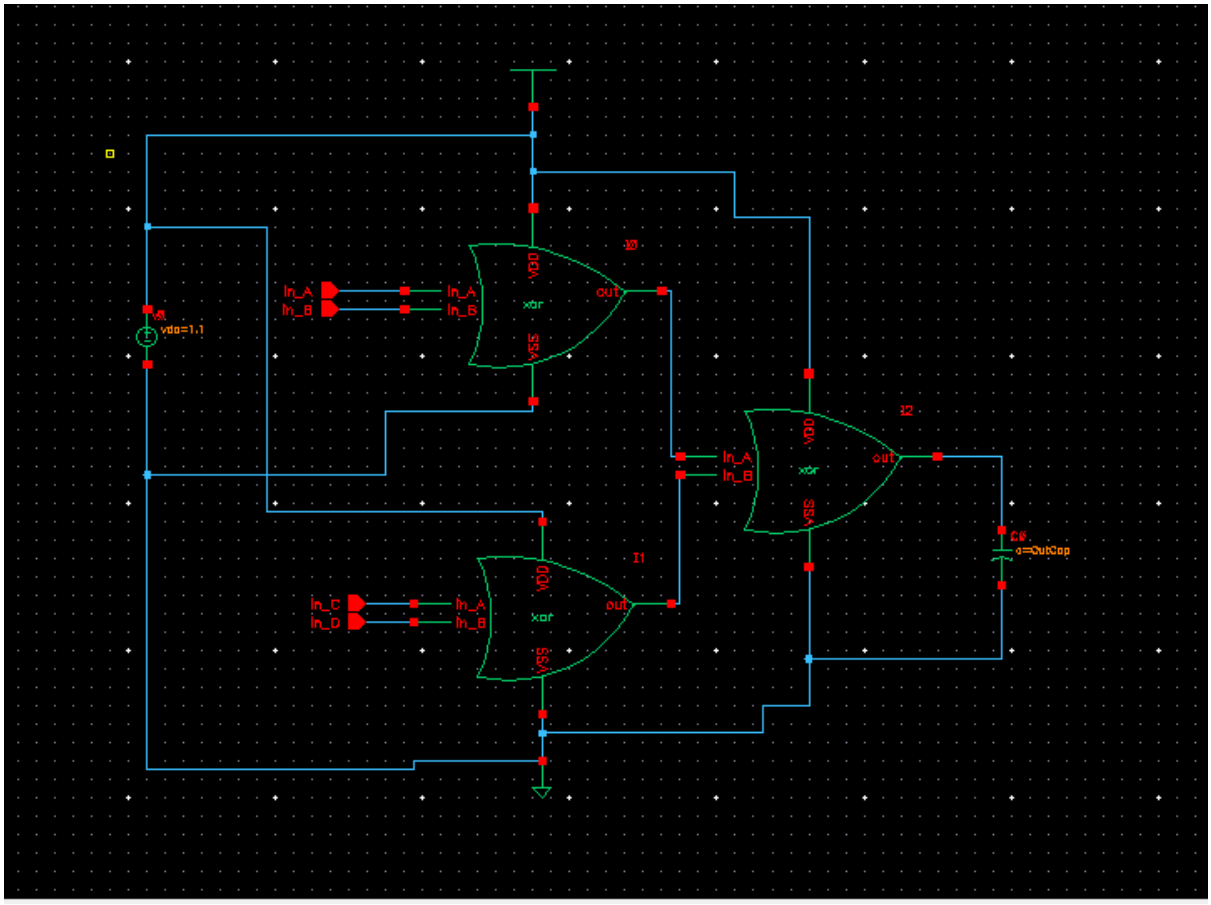
XOR Symbol:



XOR Gate Design[Layout]:



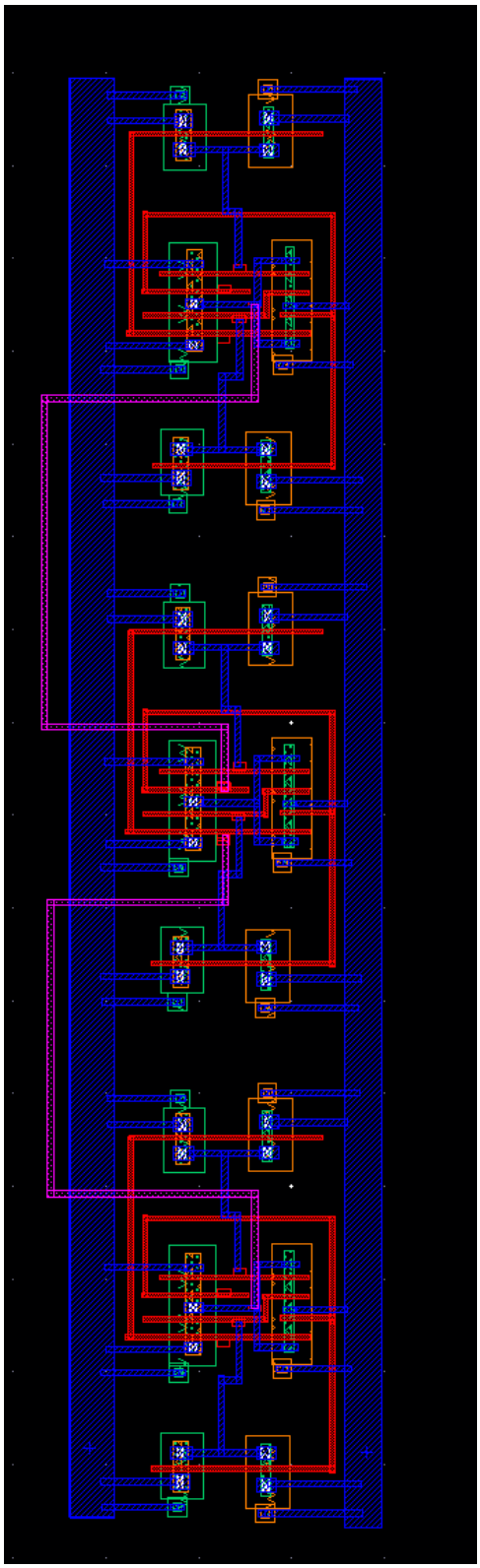
Parity Generator [Circuit Schematic]:



Wp= 160nm Lp=50nm

Wn=100nm Ln=50nm

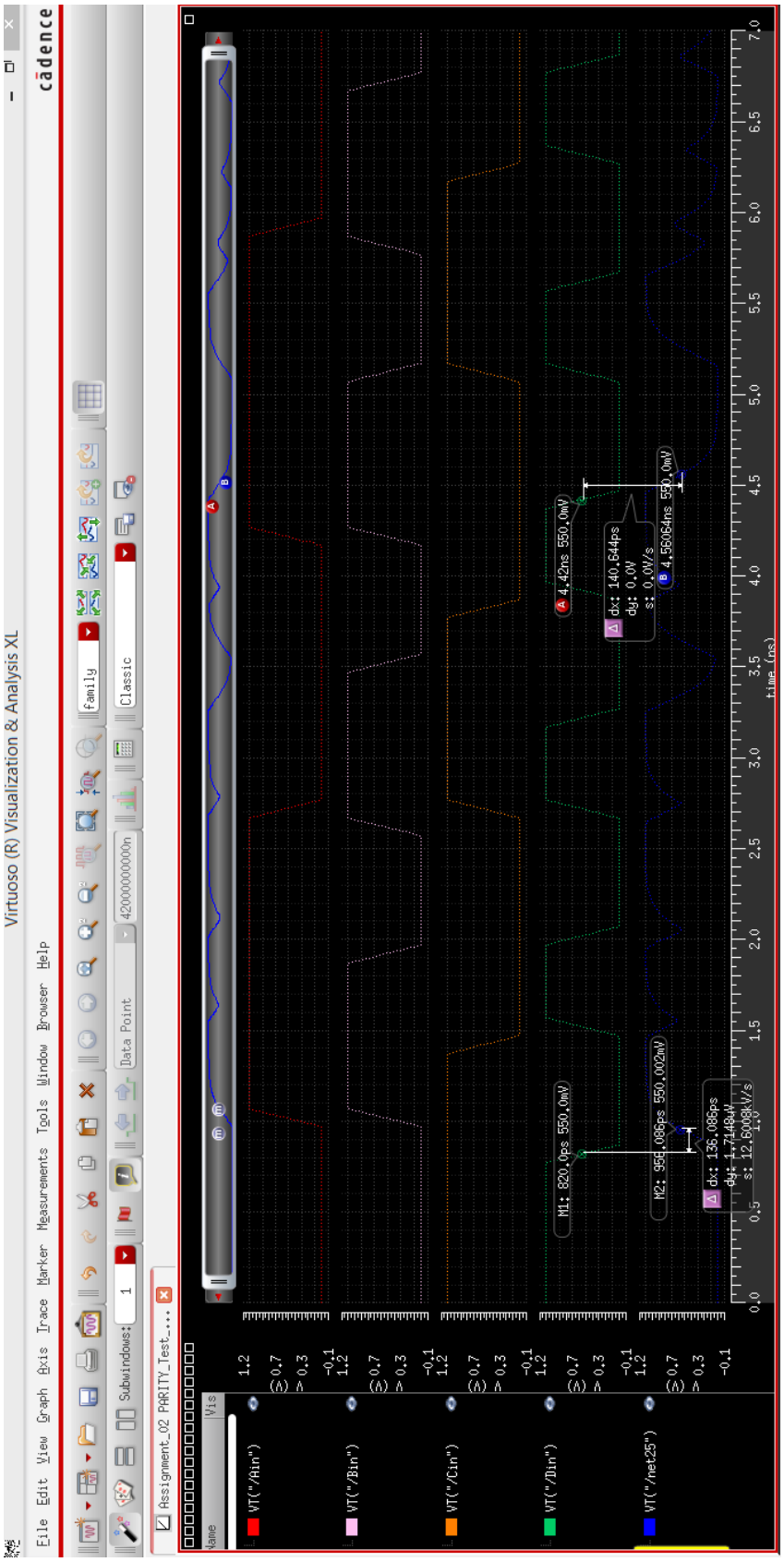
Parity Generator[Layout]:



Wp= 160nm Lp=50nm

Wn=100nm Ln=50nm

Transient Simulation:



Average propagation delay= **138.4ps**

Estimating Wn and Wp for least power delay product:

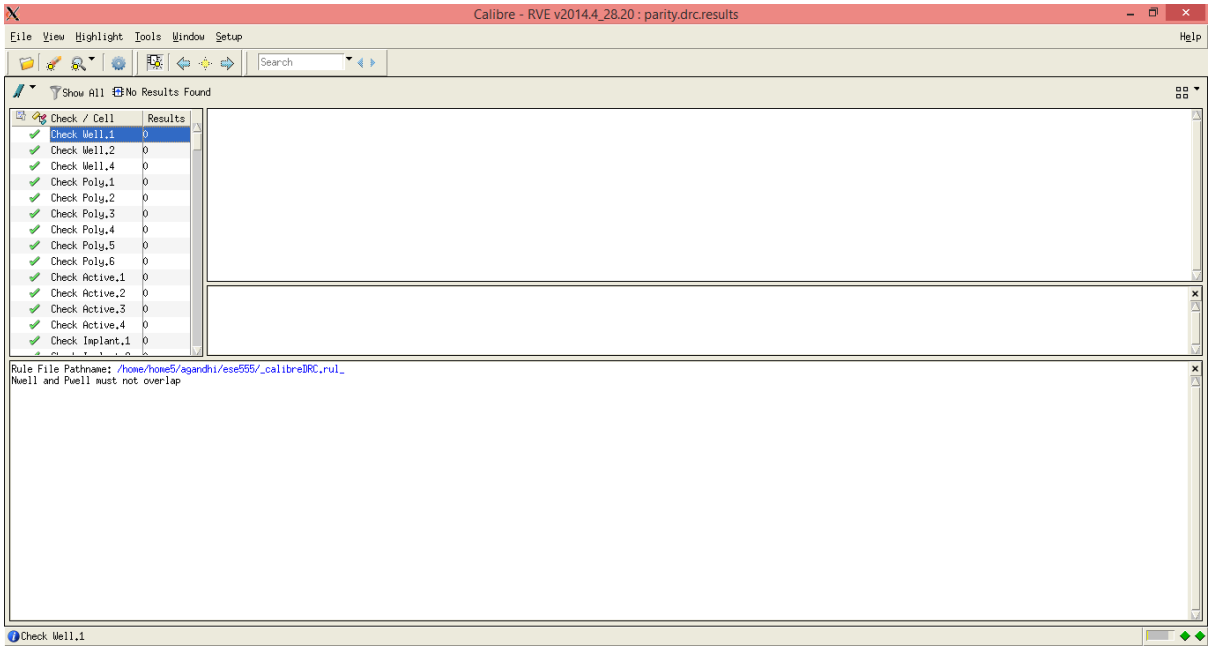
Wp (nm)	Wn (nm)	Propagation delay low-high (ps)	Propagation delay high-low(ps)	Avg. delay (ps)	Current (µA)	Power (µW)	Power delay product (Ws * 10^{-18})
180	90	120.97	156.03	138.5	27.62	30.38	4207.54
170	90	128.31	154.20	141.25	27.09	29.79	4208.52
160	90	133.04	157.51	145.26	26.49	29.14	4232.59
170	100	127.12	145.19	136.15	28.16	30.98	4217.47
160	100	136.086	140.64	138.4	27.59	30.34	4199.66
150	100	141.16	145.02	143.09	27.00	29.70	4249.88

Power delay product is minimum for Wp=160nm Wn=100nm.

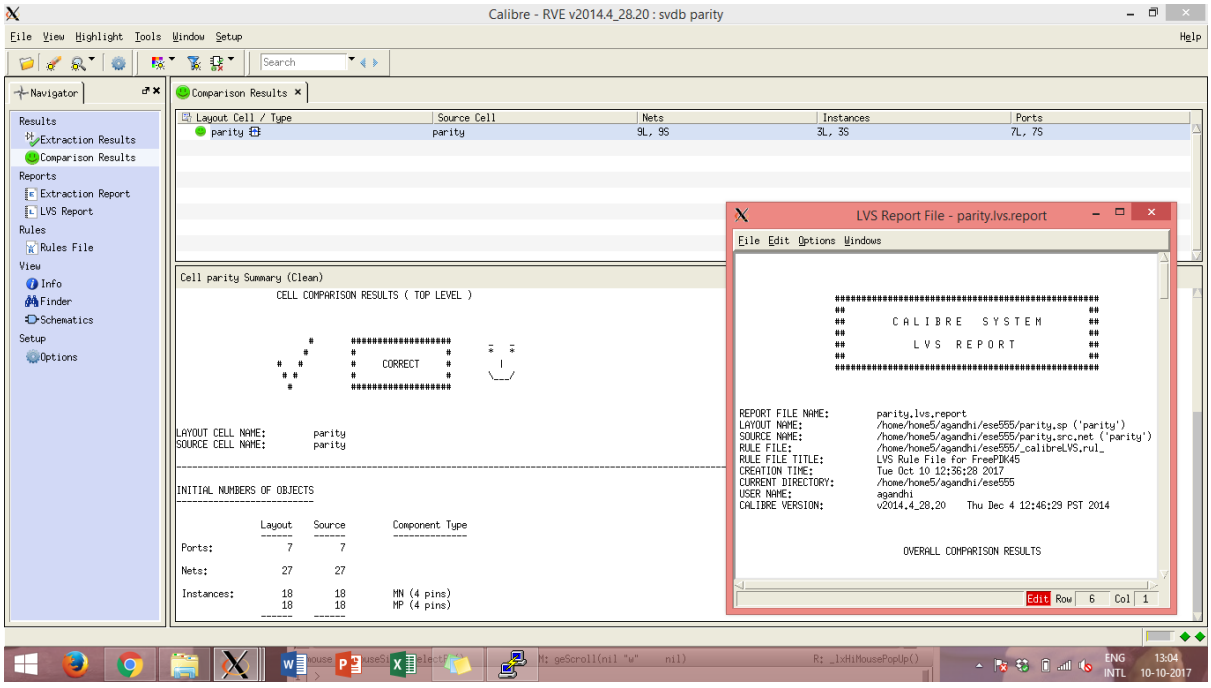
Thus, **Wp= 160nm Lp=50nm**

Wn=100nm Ln=50nm is selected for the design.

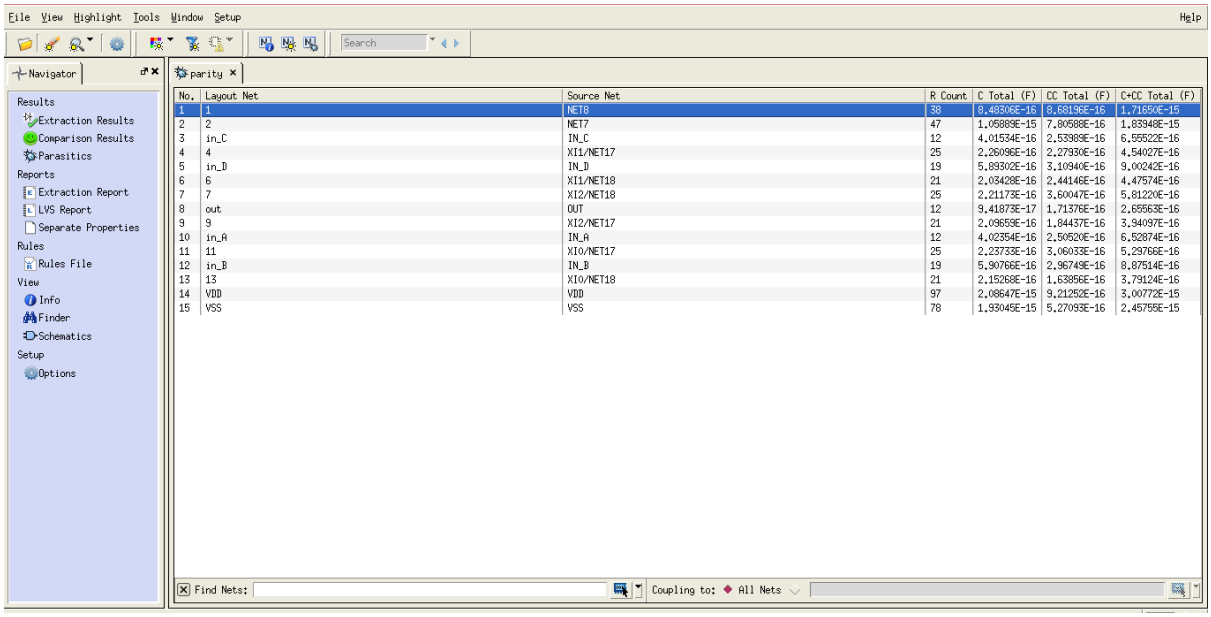
Successful DRC Results:



Successful LVS Results:

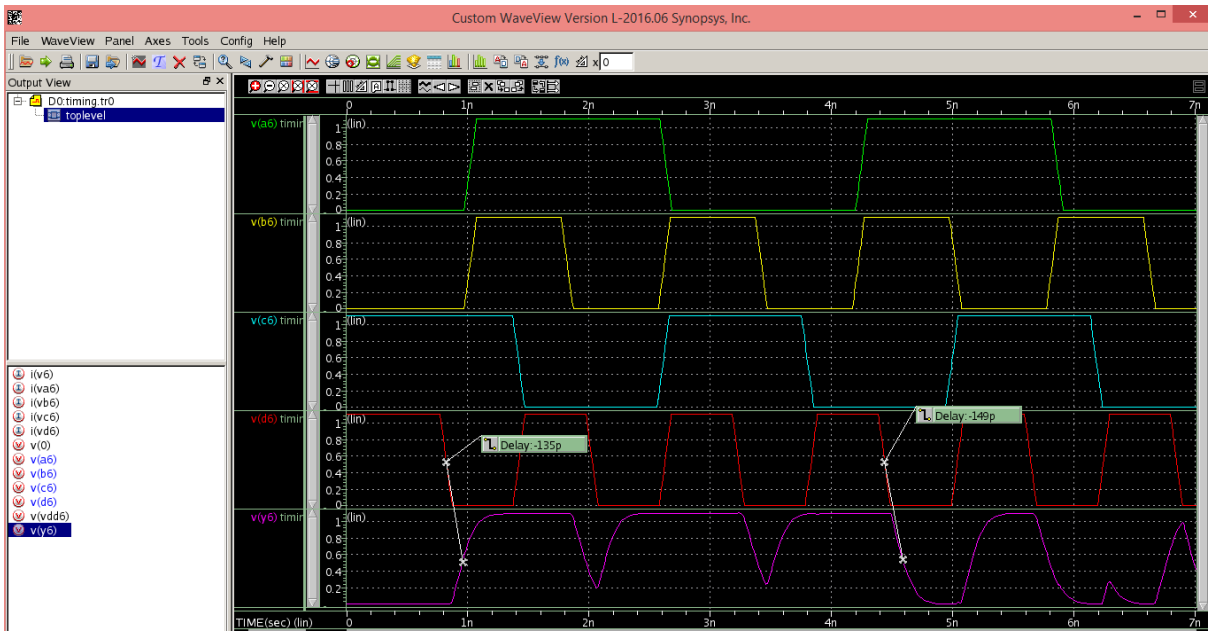


Parasitic Report:



No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	1	NET8	38	8.48306E-16	8.68196E-16	1.71650E-15
2	2	NET7	47	1.05889E-15	7.80588E-16	1.83948E-15
3	in_C	IN_C	12	4.01534E-16	2.53989E-16	6.55522E-16
4	4	XI1/NET17	25	2.26096E-16	2.27930E-16	4.54027E-16
5	in_D	IN_D	19	5.89302E-16	3.10940E-16	9.00242E-16
6	6	XI1/NET18	21	2.03428E-16	2.44146E-16	4.47574E-16
7	7	XI2/NET18	25	2.21173E-16	3.60047E-16	5.81220E-16
8	out	OUT	12	9.41873E-17	1.71376E-16	2.65563E-16
9	9	XI2/NET17	21	2.09659E-16	1.84437E-16	3.94097E-16
10	in_A	IN_A	12	4.02354E-16	2.50520E-16	6.52874E-16
11	11	XI0/NET17	25	2.23733E-16	3.06033E-16	5.29766E-16
12	in_B	IN_B	19	5.90766E-16	2.96749E-16	8.87514E-16
13	13	XI0/NET18	21	2.15268E-16	1.63856E-16	3.79124E-16
14	VDD	VDD	97	2.08647E-15	9.21252E-16	3.00772E-15
15	VSS	VSS	78	1.93045E-15	5.27093E-16	2.45755E-15

Post-layout simulation data:



Average propagation delay= **142ps**