ESE 555 CAD ASSIGNMENT 3
Due November 3

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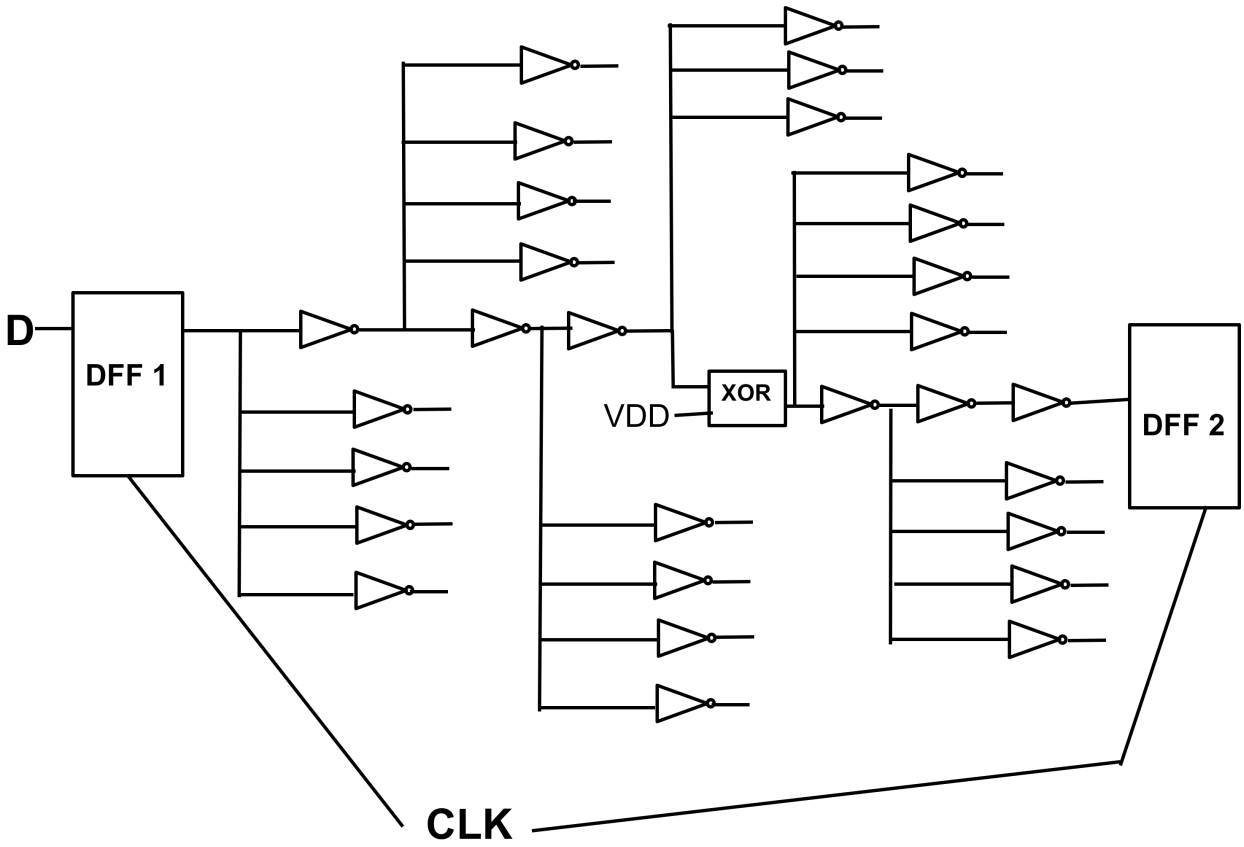
Design and verify a CMOS positive (rising) edge triggered master-slave D type flip-flop with an asynchronous reset (active at logic high) using 45 nm static CMOS technology. Flip-flop should have three inputs (data, clock, and reset) and two outputs (Q and Q bar). The supply voltage is set to 1.1 Volts. The flip-flop should drive an external load of 5 fF in addition to the internal parasitic capacitances that exist at the output stage. Assume 50 ps of rise/fall times for the data and clock signals. Assume 50% duty cycle for both signals. Both signals should be periodic.

Note that you need to obtain the clock bar signal internally. In industrial D flip-flops, the input clock signal goes through two inverters. The output of the first inverter acts as your internal clock bar signal and the output of the second inverter acts as your internal clock signal. Obey to this principle in your design.

To verify the functionality of the flip-flop, design a simple data path at the schematic level as follows:



The incoming data is provided to the D input of DFF1. The Q output of DFF1 goes through multiple inverters (you can use the inverter you designed in CAD1). The output of one of those inverters is an input to another inverter and so forth. The output of some of the inverters may be floating. These inverters are added to increase the output load. There is also an XOR gate (you can use the XOR you designed in CAD2). The output of DFF2 should drive a capacitance of 5 fF. Both DFFs are clocked by the same clock signal.

The incoming data should be at 1/10 the frequency of the clock signal (for example, if clock is running at 100 MHz, Data should run at 10 MHz). In the first rising clock edge, D should be latched by DFF1. It will then propagate through the combinational logic and should be latched by DFF2 during the second rising clock edge. **Verify this functionality for 5 cycles of the data signal. Also verify the operation of asynchronous reset.**

Design constraints: The data path shown above should work at a minimum of 2 GHz clock signal (200 MHz data signal). Iteratively increase the clock frequency (and also data frequency) to determine the maximum frequency at which the data path can still work. At a certain frequency, the data path will fail, meaning that DFF2 will be unable to latch the input signal (output of the final inverter) at the second rising edge of the clock signal. Thus, the data path suffers from a max delay constraint violation.

Deliverables for the schematic level simulation:

1) Demonstration of correct operation of the data path at 2 GHz clock frequency (for 5 data cycles, show waveforms), also verify the asynchronous reset
2) Maximum frequency of operation
3) Waveforms showing failure if the maximum frequency is exceeded

Draw the layout of only the DFF cell and pass DRC, LVS.

From post layout simulations, determine the following data:

4) Clock-to-Q delay for both cases (latching logic-low and latching logic-high)
5) Setup time of the flip-flop
6) Hold time of the flip-flop

When characterizing the flip-flop for setup time, obtain clock-to-Q delay as a function of setup skew when driving a load of 5 fF. Construct clock and data waveforms as a single pulse, as discussed in the class. Assume the flip-flop is latching a logic-high. Assume very large hold skew. Plot [setup skew] versus [setup skew +clock-to-Q delay]. Choose the setup time that minimizes this summation (y axis). In practice, setup time is characterized separately for both latching logic-high and logic-low. In this case, you will perform only one of them (latching logic-high).

When characterizing the flip-flop for hold time, obtain clock-to-Q delay as a function of hold skew when driving a load of 5 fF. Assume very large setup skew. Construct clock and data waveforms as a single pulse, as discussed in the class. Choose hold time that produces 10%

increase in the nominal clock-to-Q delay. In practice, hold time is characterized separately for both latching logic-high and logic-low. In this case, you will perform only one of them (latching logic-high).

When you sweep setup skew for setup time characterization (and hold skew for hold time characterization), make sure your step size is reasonable. As the setup skew (or hold skew) is reduced, you will need to reduce your step size because clock-to-Q delay will start to be more sensitive to setup (and hold) skews.

REPORT: In your report, include the data for items 1 to 6 above including waveforms when necessary. For the final design, include screen snapshots showing, layout, successful DRC and LVS results, and post layout simulation data.