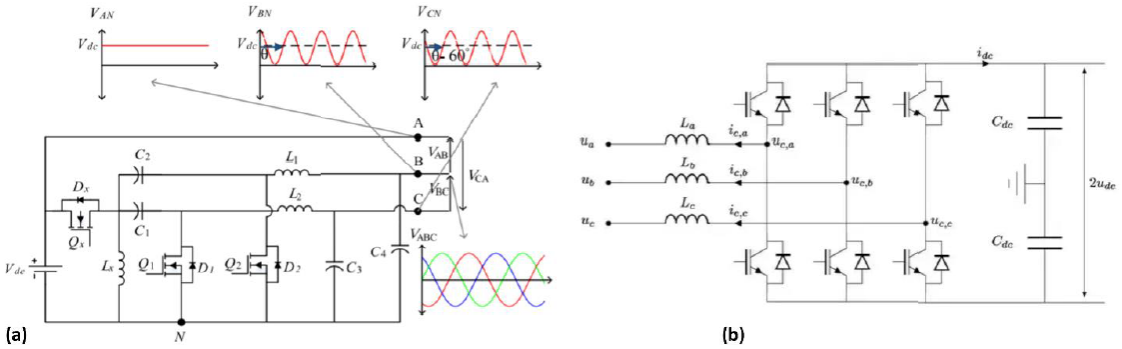
Modelling and Control of a Three-Switch, Three-Phase DC to AC Converter



Authors:
Flavius Alexandru Luntrasu
Frederik Sabro Valeur
Gintaras Zubavicius
Pere Izquierdo
Peter Kærgaard Magnussen

Supervisors:
Dezso Séra
Tamas Kerekes
João Pedro Rodrigues Martins

AALBORG UNIVERSITY
DENMARK

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Introduction 1

1.1 Problem Analysis

In recent years, the penetration of renewable energy in power grids worldwide has been substantially increasing. This is especially true of wind and solar energy, as illustrated in figures 1.1 and 1.2, respectively.

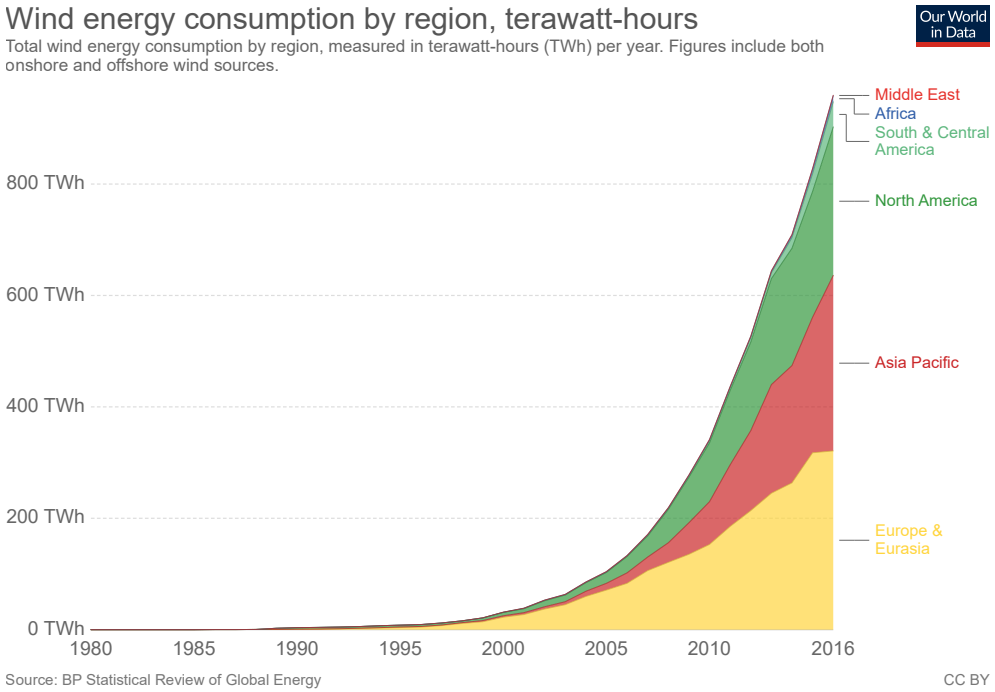

Figure 1.1: Global wind energy consumption from 1980 to 2016. [2]

Renewable energy sources are often subject to constraints outside human control, most notably climate and weather conditions. Therefore, they are less reliable than most conventional energy sources: one of the main concerns regarding their widespread implementation is their ability to comply with grid standards and requirements. These are imposed by grid operators with the aim to maintain grid stability.

As both wind and photovoltaic power generators must be connected to the grid through power converters, the control of these devices becomes crucial in meeting the desired criteria. In order to allow the source to inject power into the grid, such a power converter must at the very least be able to match its output voltage, frequency, and phase with the grid parameters. Ensuring this is the first step for the design of any converter control scheme. However, the increasingly demanding grid codes require further capabilities from

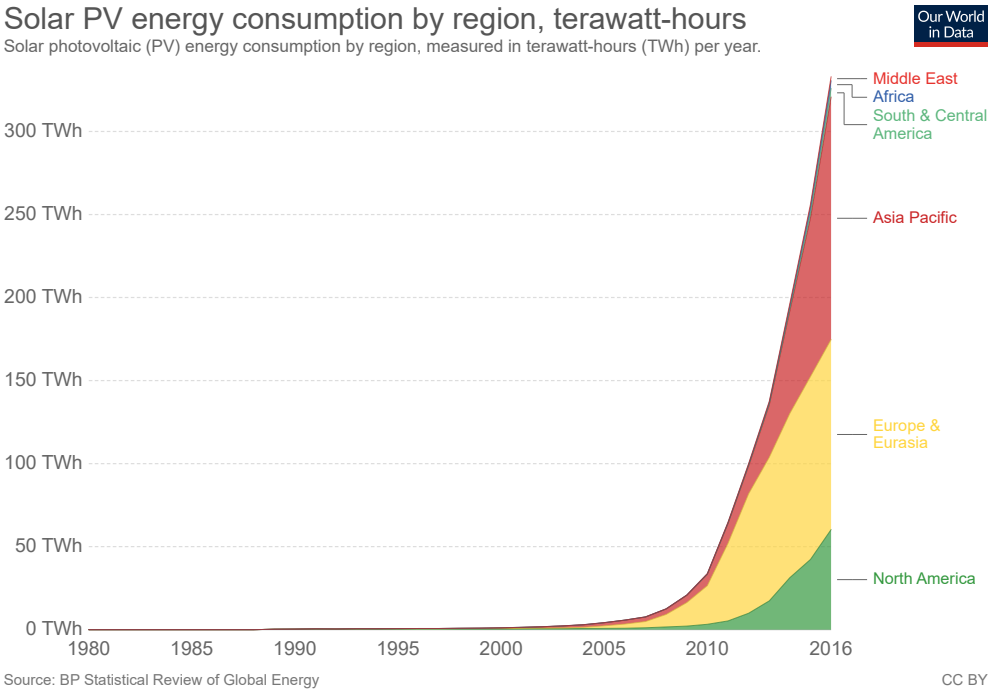

Figure 1.2: Global photovoltaic energy consumption from 1980 to 2016. [2]

the converter, such as allowing for dynamic control of active and reactive power and minimizing injected current harmonics.

The strictness of grid codes reflects the issues that power grids are currently facing regarding power electronics. As power loads become increasingly non-linear due to the wider use of electronics, the harmonic content of the grid increases. Moreover, generation interfaced with the grid through power electronics also increases its harmonic content. Harmonics in the grid are undesirable, as they increase losses in certain loads such as ac motors, and can make electronic loads not work as intended.

Traditional power generation is usually based on large synchronous machines. These provide stability to grid by being reliable and able to store energy in their rotor in the form of inertia. Therefore, in case of a grid fault or voltage drop, this energy is accessed to compensate for the lack of power in the grid. This is not the case for photovoltaic power generation, where no energy is stored mechanically, and limited in the case of wind turbines, where the topology of the generator may limit its power compensation capabilities. The control of power converters is therefore fundamental for adequate grid operation.

This project focuses on the development of control schemes for power converters that implement some of the functions that have been proven desirable for grid-connected renewable power sources. Most applications rely on dc-to-ac converters to ensure adequate grid injection characteristics, although other converters are often used to couple the power source with the dc-to-ac converter. In most photovoltaic applications, where direct current is obtained from the solar panels, a dc-to-dc converter is used to ensure maximum power and control the input voltage of the dc-to-ac converter. A general diagram for such a topology is shown in figure 1.3.

In a similar manner, wind power systems also employ a converter to couple the generator

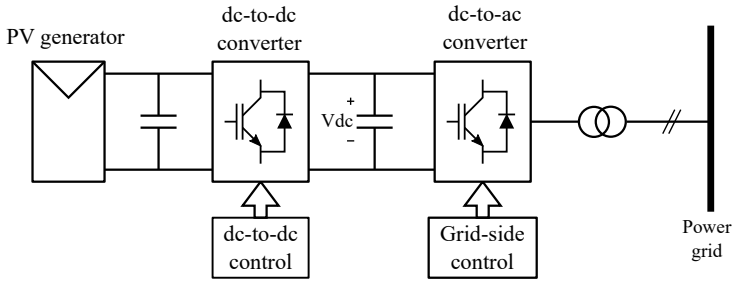

Figure 1.3: General photovoltaic topology.

side with the dc-to-ac power converter. In this case, however, this converter is an ac-to-dc rectifier, as the electrical machines used for wind power generation are almost always based on alternating current. A general topology for such a system is shown in figure 1.4.

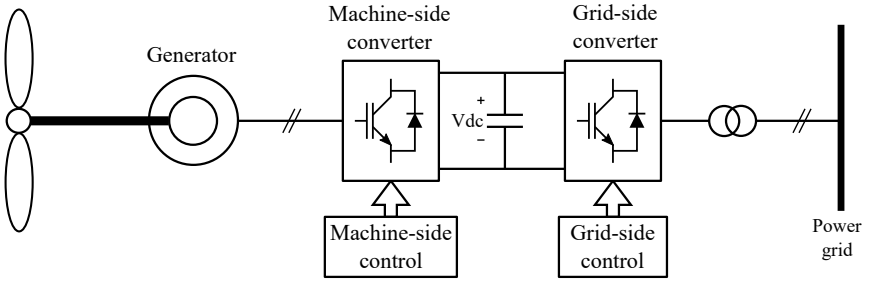

Figure 1.4: General wind power generation topology.

The basics behind both photovoltaic and wind power systems are thus quite similar: a generator block outputs an electrical current that is then conditioned by a first converter; a second converter then adapts the output of the first converter to allow for grid injection. The control scheme of the first converter is usually tasked with optimizing the power output of the source, using maximum power point tracking (MPPT) algorithms, as well as maintaining adequate characteristics for the input of the grid-side converter. These general characteristics are shared with many renewable power generation systems, but this project mostly refers to wind and photovoltaic generation, as they are the most widespread - excluding hydro power, which often does not rely on power electronics.

The focus of this project is on the grid-side converter: its main goal is the development of a control scheme allowing for power injection to the grid under varying undesirable conditions. For a suitable control scheme to be developed, a particular converter topology must be selected and studied.

In this report, two dc-to-ac three-phase converter topologies are analyzed: the most widely used scheme consisting of six switching devices, and a newly proposed topology consisting of only three switching devices, as proposed by Farhadi and Abapour [1].

The choice of three-phase over single-phase converters stems from the fact that three-phase power systems are more commonly used by power generators. Three-phase systems offer many advantages over single-phase ones: most notably, constant power, lower conductor material requirements, and in closer connection to this project, lower number of switching devices required for power converters at the same power level.

The motivation behind the analysis of the three-switch converter is the possibility that such a topology potentially presents lower power losses than the conventional six-switch topology. This is due to the fact that switching losses occur in each of the switching devices, because of their non-ideal behavior: current and voltage cannot have their values changed instantly.

Therefore, the more switching devices that a converter uses, the higher its potential switching losses. It should be noted that this is broadly simplified, as switching losses depend on other parameters such as switching frequency and circuit characteristics, so the fact that a topology uses a lower number of switching devices is not enough to conclude that it will always present lower switching losses. Moreover, topologies that aim to reduce the number of switching devices most often rely on the use of passive components, which can in turn increase parasitic losses in the circuit. Larger passive component requirements may also increase costs. Reducing the number of switches may, however, increase converter reliability and improve both converter cost and size.

1.2 Problem Statement and Methodology

1.2.1 Problem 1: How to control a grid connected converter in order to comply with grid codes?

1. Develop a suitable control scheme to control the current flow between the grid and converter.
2. Investigate a compensation method for the harmonic content of the grid.
3. Develop a method that is capable of providing voltage support to the grid using reactive power.

1.2.2 Problem 2: Investigate the possibility of reducing the number of switches of the converter from 6 to 3, using the topology proposed in [1].

1. Develop a simple and intuitive modulation strategy using circuit analysis and PLECS simulations.
2. Test the open-loop control in the lab by emulating the three-switch inverter.
3. Develop a state-space model of the converter for the implementation of model predictive control.
4. Assemble the power stage of the three-switch inverter for experimental tests.
5. Compare the results obtained for the two converters.

System Description 2

The following project is using the resources and laboratory facilities provided by Aalborg University. Therefore some considerations and limitations that come with these facilities will be described in this chapter as it also influences the measurements and rationals used in the technical implementations presented in this report.

2.1 Grid-Converter Connection Setup

The laboratory provides a physical Danfoss 4kW DC to AC converter connected to the grid via a transformer and LC filter.

The setup can be seen in figure 2.1. The figure itself does a good job of highlighting each component individually - DC power supply, Danfoss inverter, filter and transformer and the LEM modules, which are the voltage and current sensors, that provide the necessary data to the control interface - as well as the connections.

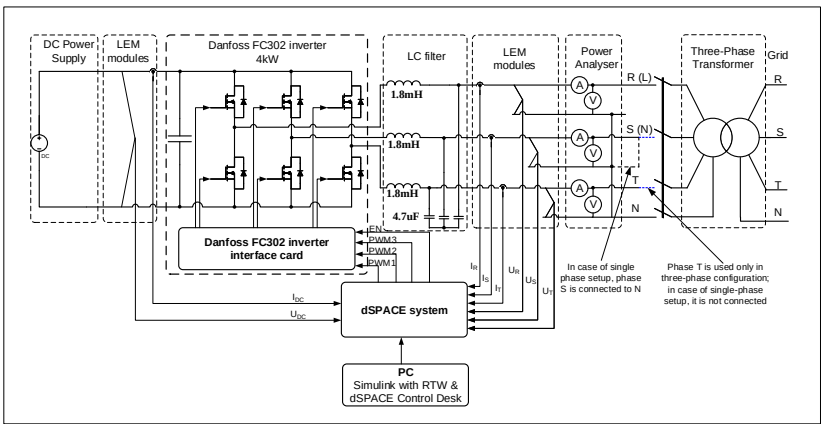

Figure 2.1: Setup for grid connected converter.

Some important considerations need to be made:

- For the purpose of current control, the transformer is seen as an inductor, therefore, the connection between converter and grid is considered to be done via an LCL filter where the grid side inductor is represented by the transformer. The project will refer to it as such.
- The three phase measurements take place before the transformer - as seen from converter side - therefore, for reactive power compensation, the grid side inductance will also include the transformer's inductance.

- Although there is a neutral wire present on the primary side of the transformer it is worth pointing out that it's only used in single-phase configurations (which is not the case here) and for phase voltage measurements. Therefore, for analysis purposes there are only three wires on the primary side, with no neutral connection (either delta, or star without neutral wire).
- I_R, I_S, I_T are the phase currents and U_R, U_S, U_T are the phase-to-neutral voltages. R,S,T is one of the labelling conventions used for three phase wires. In this project, R,S,T will be replaced by A,B,C.
- I_{DC} and U_{DC} are the power supply's current and voltage.
- $PWM1$, $PWM2$, $PWM3$ - are the three power width modulation signals corresponding to one of each converter leg.
- EN allows for boolean type signals to be passed to the inverter card, that can be used for a turn ON/OFF logic implementation.

2.2 Control Interface

In order to ensure the communication between the control model and the physical inverter, a dSPACE system will be used. This system provides an user-controllable interface between the physical setup described at section 2.1 and a Simulink model with implemented control strategy.

One of the features of a dSPACE system is Rapid Control Prototyping (RCP). This allows for control algorithms, to be taken from a mathematical model - in this case, a Simulink model - and to be implemented as a real-time application, allowing for the control strategies to be tested on a real target model directly from Simulink. For this purpose Simulink is used as the simulation and input tool and the Simulink Coder enables the code generation while the dSPACE system consists of a hardware component (seen in figure 2.2), which allows for the data processing and signal transfer and a software environment (dSPACE ControlDesk - figure 2.3) which represents the real-time interface, allowing for control and human interaction.

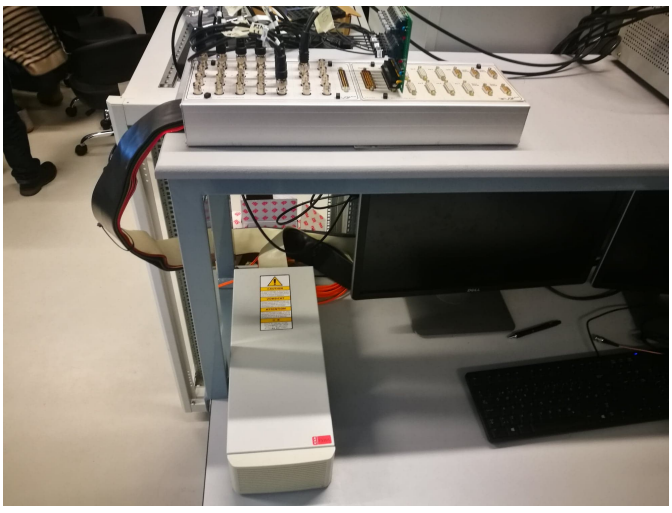

Figure 2.2: dSPACE Hardware component.

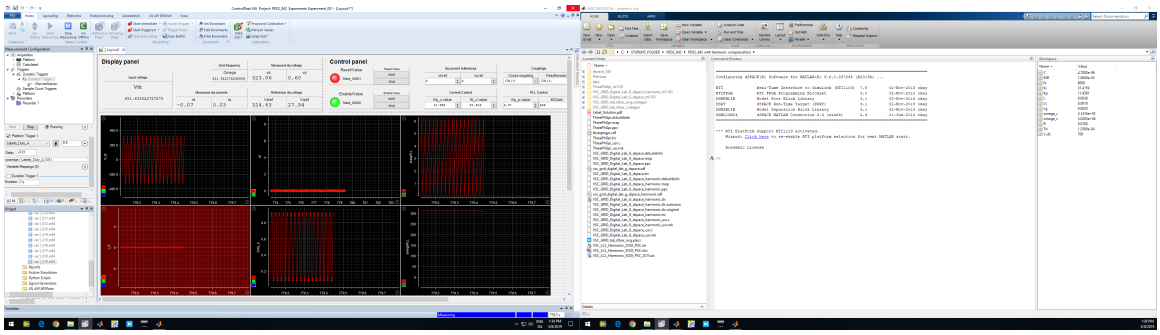

Figure 2.3: dSPACE ControlDesk environment.

It is also worth mentioning that the communication between Simulink and dSPACE ControlDesk happens via a Simulink library with custom made blocks for dSPACE data sharing.

2.3 Real-Time Simulator

Due to the fact that errors in a real grid connected converter can result in the converter tripping or getting damaged, understanding the causes and efficiently troubleshooting them can prove to be quite cumbersome.

In order to get familiarized with the whole system and to detect possible problems that can occur during experimentation without over-stressing the physical setup, the control strategy will be first tested on a real time simulator prior to moving it to the real setup. The main advantage of such a simulator is that it provides data to the user even in the case of over-current or any disturbance that would an interruption or tripping of the hardware. This allows for proper understanding of how the real setup behaves. Adding to that it allows for getting accustomed with wire connection and the physical communication between the control interface and the hardware.

One such simulator that will be used is the Plexim RT box; this piece of hardware, seen in figure 2.4, allows for what is known as, Hardware-in-the-loop (HIL) simulation. In HIL, a simulator mimics the environment in which the electronic control unit will function. This type of simulations come with the benefit that errors can be detected and fixed much faster and in a safer and more time-efficient way. In this situation, a grid connected converter PLECS model will be uploaded in the RT box and as such, the RT box will mimic the actual grid connection.

Figure 2.4: PLECS RT box.[3]

The communication between the control interface and the simulator is done via analog output signals, for the current and voltage measurements and via the digital channels for the PWM input signals; thus a bidirectional data flow is provided between the PLECS RT box and the dSPACE control interface.

The control interface used will also be the one mentioned in section 2.2. This way the whole control setup can be accurately validated.

Analysis and Design 3

This chapter presents the analysis and design procedure needed to comply with the objectives described in Section 1.2.

3.1 Proposed Converter

In this section the analysis process of the proposed converter shown in figure 3.1 is presented. Analysis to implement an open-loop and a Model Predictive Control (MPC) control approaches are carried out. The provided paper [1] is used as fundamental basis for the analysis of the converter.

It is important to note that [1] does not provide a comprehensive approach to open-loop modulation of the proposed inverter. Instead, it directly proposes a modulation strategy based on closed-loop model predictive control, which will be expanded upon in the following sections. Another point to note is the fact that, at the time of writing this report and to the author's best knowledge, the aforementioned paper [1] is the only available reference for the analysis of this particular topology of three-switch, three-phase inverter. However, references for other three-switch inverter topologies are available, especially for the so-called Delta inverter [4] [5], which has found uses in motor drive applications. The main drawback of this topology is the fact that it requires three separate dc voltage sources connected in series with each of the transistors, which must be perfectly balanced. Many sources are also available for three-switch three-phase rectifiers [6] [7] [8] [9], but to our best knowledge the proposed topologies are unidirectional, and so cannot be used to convert from dc to ac. Other three-phase dc-to-ac converter topologies with a reduced number of switches have been widely discussed in the literature, most notably the four-switch converter [10] [11]. Although this appears to be the topology most similar to the three-switch converter analyzed here, we have not been able to translate the proposed modulation strategies for the four-switch to the three-switch converter.

The schematic of the proposed three-switch converter is shown in figure 3.1.

The main concept behind this converter is to achieve dc-biased sine waves at nodes B and C with a 60° phase difference. In this manner, assuming that the dc bias is equal to the source voltage, the line to line voltages would result in a balanced three-phase system, as detailed in the following section.

Although this topology might appear to differ from the one presented in [1], the two circuits are in fact completely equivalent. By drawing the schematic in this manner, the converter can be interpreted in a more straightforward manner: inductors L_1 and L_2, together with capacitors C_3 and C_4 provide filtering to the output phase voltages. The left side of the

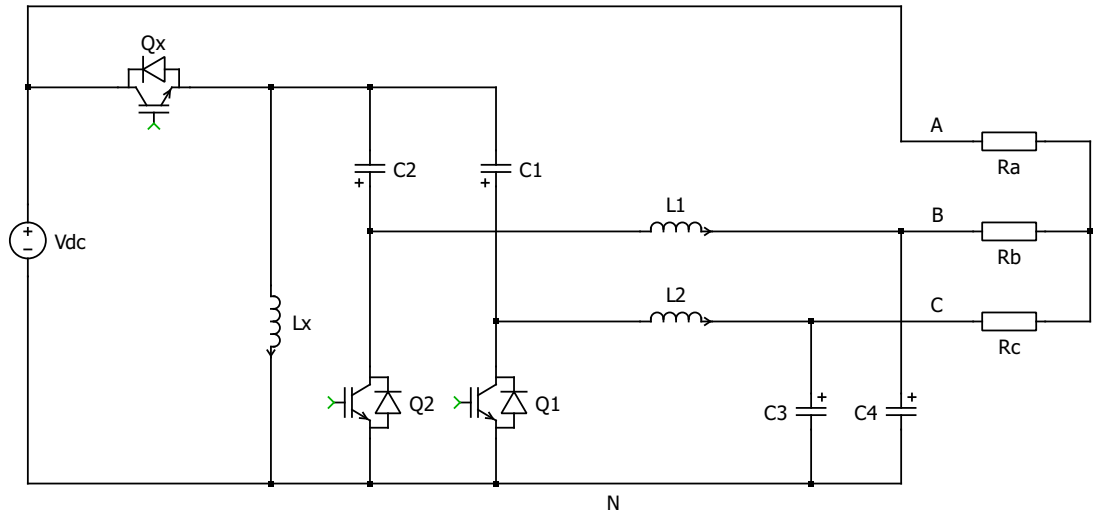

Figure 3.1: Three switch converter schematic.

converter, conforming V_{dc}, Q_x, and L_x, is equivalent to that of a conventional buck-boost converter, where the switching device is connected in series with the voltage source, and the storage inductor is connected in parallel with it. This would suggest that the proposed converter uses this left part to control the voltage applied across the intermediate capacitors C_1 and C_2 and the leg switches Q_1 and Q_2, thus becoming capable of producing the desired biased sinusoidal voltages by controlling the two leg switches.

The first approach to the modulation scheme of the three-switch converter was open-loop analysis through trial and error. This was done by investigating the required switching patterns to achieve a three-phase AC output or signals containing the desired fundamental sine waves at the output.

3.1.1 PLECS analysis

This first investigation was carried out using the circuit-oriented simulation software PLECS. The goal was to achieve, as stated in the paper [1], two biased sinusoidal phase voltages along with a constant dc output. This would lead to three balanced line to line voltages at the output of the converter. The corresponding equations for the desired phase and line output voltages are given respectively in equations 3.1 and 3.2.

$$\begin{aligned} V_{AN} &= V_{dc} \\ V_{BN} &= V_{dc} + V_m sin(\omega t) \\ V_{CN} &= V_{dc} + V_m sin(\omega t - \frac{\pi}{3}) \end{aligned} \tag{3.1}$$

Therefore, the line voltages become a balanced three-phase system:

$$\begin{aligned}
V_{AB} &= V_{AN} - V_{BN} = V_{dc} - V_{dc} - V_m \sin(\omega t) = V_m \sin(\omega t + \pi) \\
V_{BC} &= V_{BN} - V_{CN} = V_{dc} + V_m \sin(\omega t) - V_{dc} - V_m \sin(\omega t - \frac{\pi}{3}) \\
&= V_m(\sin(\omega t) - \sin(\omega t - \frac{\pi}{3})) = 2V_m \cos(\frac{\omega t + \omega t - \frac{\pi}{3}}{2}) \sin(\frac{\omega t - \omega t + \frac{\pi}{3}}{2}) \\
&= 2V_m \cos(\omega t - \frac{\pi}{6}) \sin(\frac{\pi}{6}) = V_m \cos(\omega t - \frac{\pi}{6}) = V_m \sin(\frac{\pi}{2} - \omega t + \frac{\pi}{6}) \\
&= V_m \sin(-\omega t + \frac{2\pi}{3}) = V_m \sin(\omega t + \frac{\pi}{3}) \\
V_{CA} &= V_{CN} - V_{AN} = V_{dc} + V_m \sin(\omega t - \frac{\pi}{3}) - V_{dc} = V_m \sin(\omega t - \frac{\pi}{3})
\end{aligned} \tag{3.2}$$

Where V_m is denoting the amplitude of the voltage. In order to achieve the desired output, different approaches were investigated.

Duty cycles

[1] propose instantaneous duty cycles for switch Q_1 and Q_2, obtained through equation 3.3.

$$\begin{aligned}
D(t) &= \frac{V_{out}}{V_{in} + V_{out}} \\
D_B(t) &= \frac{V_{dc} + V_m \sin(\omega t - \frac{\pi}{3})}{2V_{dc} + V_m \sin(\omega t - \frac{\pi}{3})} \\
D_C(t) &= \frac{V_{dc} + V_m \sin(\omega t)}{2V_{dc} + V_m \sin(\omega t)}
\end{aligned} \tag{3.3}$$

Where V_{out} is the phase voltage and V_{in} is the DC input. Applying equation 3.3 a switching pattern can be obtained for switch Q_1 (D_C) and Q_2 (D_B). By comparing the switching patterns with a carrier wave, the pulse-width modulated switching signals can be obtained.

Although the paper [1] provide instantaneous duty cycles for Q_1 and Q_2, no scheme is provided for the control of Q_x. Moreover, the control scheme used for experimental tests and simulations as detailed by the authors is always based on model predictive control, which does not require any references for the duty cycles. Therefore, it is possible that the switching signals that were used in the testing were not as described by equations 3.3, especially during transient periods.

Now, the choice of whether Q_x should be controlled in an independent or dependent manner with Q_1 and Q_2 is not specified in the paper, so attempts were made using both options. Figure 3.2 and 3.3 show the PLECS schematic with two modulation schemes for Q_x; dependently and independently with respect to Q_1 and Q_2. The dependent scheme shown in the figure uses an *OR* logic gate to turn on Q_x every time that either Q_1 or Q_2 (or both) are on. The independent switching scheme simply sends a pulse signal with a constant duty ratio to Q_x.

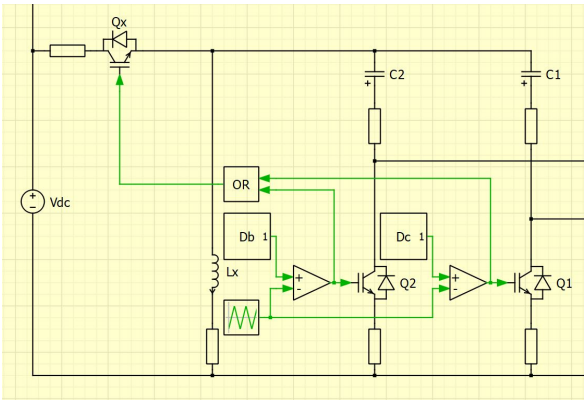

Figure 3.2: Q_x dependent of Q_1 and Q_2

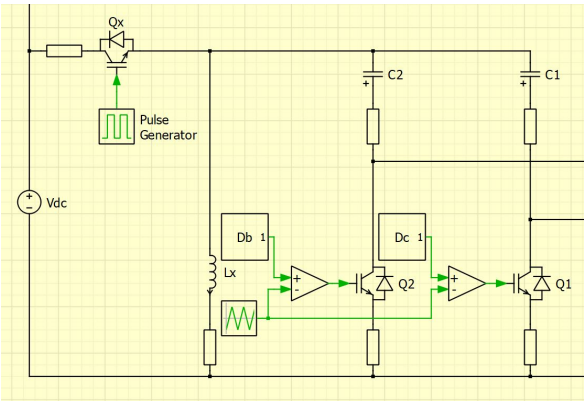

Figure 3.3: Q_x independent of Q_1 and Q_2.

The subsystems *Db* and *Dc* act as reference duty cycle generators, which along with a carrier wave assemble the pulses for Q_1 and Q_2. The two subsystems are based on equation 3.3.

To achieve the desired output when operating the switch Q_x dependently, as in figure 3.2, the passive components were adjusted over a wide range of values. However, no matter the effort taken into this setup, no promising results were obtained. The DC bias for the phase voltages was especially challenging to achieve. Moreover, the amplitude of the phase voltages also differed from its desired value.

By controlling Q_x independently, as in figure 3.3, it was possible to control the DC bias by adjusting the switching patterns for Q_x, Q_1 and Q_2. By increasing the duty cycle for Q_x and lowering it for Q_1 and Q_2, more energy is provided into the circuit, hence raising the DC bias for phase B and C. Moreover, by adjusting the modulation index, from the linear range, i.e $m_a \leq 1$ to overmodulation, $m_a > 1$, the DC bias was improved for the phase voltages. However, a known consequence of this is the presence of more low-frequency harmonics in the output voltage [12].

Passive components

Regarding the passive components it was found that the values proposed in the paper were not adequate for our analysis. With the stated values it was not possible to obtain any kind of sinusoidal output. Improvements were obtained by adjusting the output capacitors C_3 and C_4 from 1 μF to approximately 1 mF. Additionally, all other components were adjusted randomly in order to obtain the desired output. A trade off was discovered between having the same amplitude for the phase voltages, the correct phase angle, a proper DC bias and having few harmonics at the output. In figure 3.4 it was chosen to reflect the best sinusoidal output for the phase voltages, regardless of the lack of a correct dc bias and similar voltage amplitude. figure 3.4 is based on the independent control of Q_x as shown in figure 3.3. figure 3.5 presents the corresponding Fourier spectrum of the phase voltages.

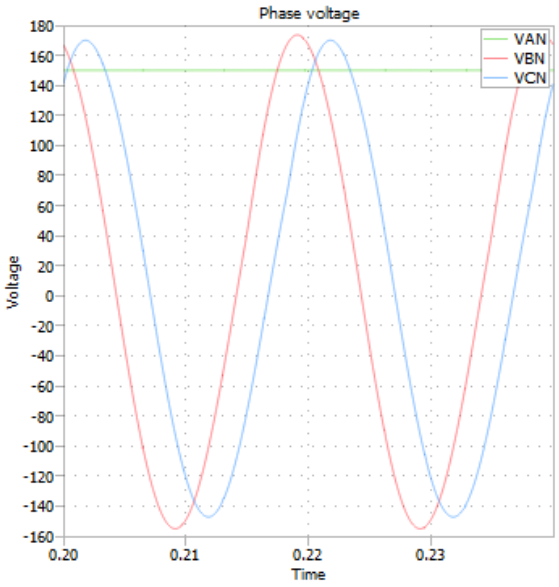

Figure 3.4: Arbitrary phase voltages for proposed converter. Biased approximately around 0V

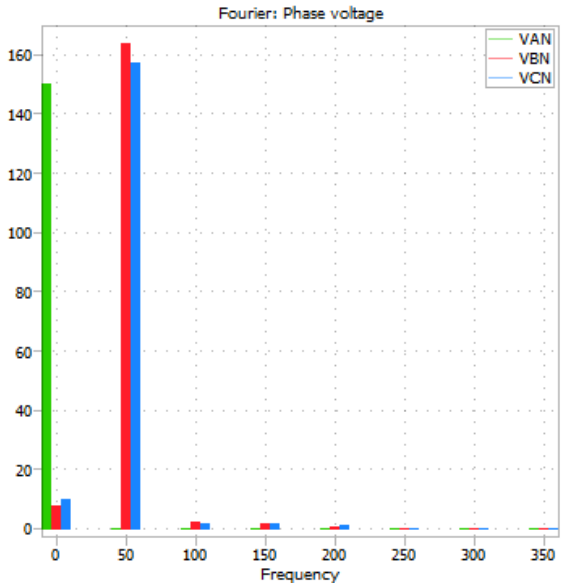

Figure 3.5: Fourier spectrum of phase voltages

The Fourier spectrum reveals the low DC bias for phase B and C and a smaller amount of lower order harmonics. The phase voltages appear acceptable. However, using equations 3.2 they reveal a different picture for the line voltages, which are visualized in figure 3.6

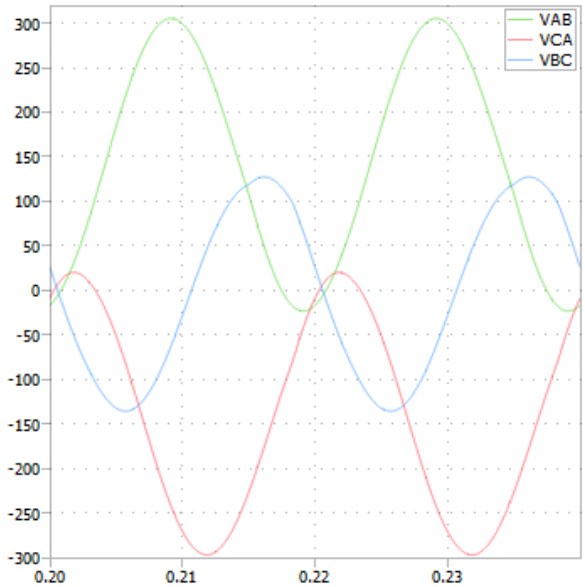

Figure 3.6: Corresponding line voltages

The line voltage are roughly displaced by 120°. However, bias and amplitude differs significantly. As been mentioned, working with this proposed converter revealed a trade off between the desired properties. Figure 3.4 shows a slightly distorted pair of phase

voltages, which was chosen to be presented in this project. Yet, it could have been chosen to present other output scenarios.

To sum up, it has been found that the proposed converter is tricky to manage. Even though components and inputs are adjusted, no sufficient output has been achieved. In addition to the PLECS analysis an attempt was made, trying to construct a model predictive control algorithm for the converter.

3.1.2 Converter modelling considerations

Seeing how, as discussed in the previous section, no satisfactory results were obtained using the attempted open-loop modulation schemes, a different approach needed to be undertaken. Therefore, replicating the procedure used by Farhadi and Abapour [1], we attempted to expand our knowledge of the operation of the three-switch converter by developing a state-space model that accurately represents it.

The paper [1] already provides a state-space model of the three-switch converter. However, it is apparent that the provided model contains several mistakes. Most notably, the coefficient matrix G is missing a term in row 5, column 2, which relates the derivative of output inductor current $\frac{di_{L2}}{dt}$ to output voltage V_{CN}. This is immediately evident, as an equivalent term is present relating $\frac{di_{L1}}{dt}$ to V_{BN}. An inductance also appears to be missing in row 3, column 3, for the term relating $\frac{di_{Lx}}{dt}$ to its value i_{Lx}. Without this inductance, units do not match.

It is also worth noting that the choice of states and inputs performed in the paper is, to our best knowledge, unconventional. When modelling power converters using a state-space approach, states should be associated to the energy levels of the storage components; i.e. states are defined as capacitor voltages and inductor currents. The model provided in the paper instead considers the voltage levels of capacitors 1 and 2 as inputs instead of states, thus eliminating the need to obtain their derivatives: this translates to not updating their values during simulation, and instead relying on previous data or measured values. Our best guess is to assume that the control scheme implemented by Farhadi and Abapour feeds the measured values of V_{C1} and V_{C2} back to the control system, using them to update the possible values of the other states. However, the precise approach taken by the authors is never specifically mentioned in the paper.

Instead of defining V_{C3} and V_{C4} as states, the model uses V_{BN} and V_{CN}. However, this change is much more straightforward, as $V_{BN} = V_{C4}$ and $V_{CN} = V_{C3}$ if the two output capacitors are assumed to contain to parasitic resistance. When considering these parasitic, output and capacitor voltages can be simply related using voltage divider expressions.

The authors of this project contacted one of the authors of the paper [1] with questions regarding the unconventional state definition, apparent errors in the modelling, control scheme, and choice of passive components, among others, but no satisfactory answer was given to most of the questions.

In conclusion, we did not find the state-space model of the three-switch converter presented in [1] to be accurate, or at least not completely. However, the control scheme for the three-switch converter proposed in the paper uses the aforementioned state-space model

to implement model predictive control (MPC), with seemingly promising results.

3.1.3 Model predictive control (MPC)

MPC is a control method in which a model of the system to be controlled is used to predict its future behavior over a range of possible control signals. Optimality criteria are then used in order to select the most appropriate control action. In practice, these criteria are often expressed in the form of a cost function, which can be numerically evaluated. The optimum control action is then chosen by minimizing this cost function.

The main advantages of MPC are the easy inclusions of constraints and non-linearities to the control scheme, together with very good performance in most scenarios, assuming that the model accurately represents the real system. Having direct access to the cost function allows the designer to make decisions on the control scheme in a much more direct way than other control methods that rely on the tuning of parameters. On the other hand, the computational burden that MPC demands of the control system processor can be large. This is due to the fact that for every prediction that is made, ramifications for future predictions appear exponentially. Thus, an adequate balance must be found between performance and computational requirements.

The large computational requirements of MPC have made it find limited applications in power converter control and drive systems, as the small sampling times used in these fields are often incompatible with solving the optimization problem online. An approach for implementing MPC for power converters is to take advantage of their inherently discrete nature. As power converters have a limited number of switching states, predictions can be made only for each of the possible states; which can then be evaluated in the cost function. The state with minimum cost is then selected and generated. Since the possible control actions (switching states) are finite, this approach is known as Finite Control Set MPC (FCS-MPC). This method has been successfully applied to a wide range of power converter and drive applications [13].

FCS-MPC is the control method used by Farhadi and Abapour for the proposed three-switch converter. Using a provided state-space model, state values for future sampling instants can be calculated and then used in a cost function. Details on the definition, discretization, and solutions of a general linear state-space model, as used in FCS-MPC schemes, can be found in Appendix A. The cost function used by the authors of the paper is defined as:

$$J = \sum_{i\in\{B,C\}} \Big(\sum_{j=1}^{N_P} (V_{iN}(k+j) - V_{Ref,iN}(k+j))^2 \Big) + \sum_{p\in\{x,1,2\}} \lambda_p (i_{Lp}(k) - \beta_p i_{Sat,p})^2 \quad (3.4)$$

Where N_P is the predict horizon, k is the current sampling instant, β is the upper bound for inductor currents, and λ is the Lagrange multiplier determining the weight of inductor current saturation with respect to voltage error within the cost function. The first term of equation 3.4 represents the error between the future reference voltages $V_{Ref,BN}, V_{Ref,CN}$ and their predicted values; while the second term accounts for inductor saturation. Therefore, by minimizing this cost function, the obtained optimum state is that which ensures both accurate matching of the output voltage references and minimum

inductor saturation. Minimizing inductor saturation ensures that the converter will work without significant inductance drops, maintaining the accuracy of the used model and thus its predictions. The Lagrange multiplier (λ) determines the balance between the two terms when calculating costs.

Both the prediction horizon (N_P) and the Lagrange multiplier (λ) can be tuned to achieve different results. Increasing the prediction horizon allows the controller to select the optimum state considering further future results, thus reducing output voltage error. However, it also significantly increases computational load. On the other hand, increasing the value of the Lagrange multiplier prevents inductor over-saturation, at the cost of lower output voltage accuracy. These expected effects are verified experimentally in [1], where total harmonic distortion (THD) is shown to be directly proportional to λ and inversely proportional to N_P. The cost function can be simplified to not account for inductor saturation:

$$J = \sum_{i \in \{B,C\}} \Big(\sum_{j=1}^{N_P} (V_{iN}(k+j) - V_{Ref,iN}(k+j))^2 \Big) \tag{3.5}$$

This is equivalent to giving a value of 0 to the Lagrange multiplier. For simulation purposes this is the cost function that will be implemented first, as the inductors used are initially set to be ideal and thus not capable of saturation.

Although the paper provides a state-space model of the converter, a procedure for its discretization and solution, and the cost function to be used in MPC, our attempts to simulate the three-switch converter using the proposed control scheme have proven to not be fruitful. As discussed in section 3.1.2, we believe that the state-space model provided by the paper is not accurate, and have therefore concluded this to be at least one of the reasons why the MPC scheme does not appear to work in our attempts to replicate it.

Therefore, we decided to attempt to develop our own state-space model of the three-switch converter, both to gain further insight into its operation which could potentially lead to the development of a suitable open-loop modulation scheme, and to implement a modified version of the MPC scheme proposed in [1]. As prior to this project our knowledge of state-space modelling of power converters was quite limited, we decided to begin our analysis by studying the procedures used to develop a state-space model of a well-known power converter: for this purpose we chose the Ćuk converter. This topology was chosen as a starting point due to the fact that it constitutes a good middle ground between the complexity of the three-switch converter and the simplicity of the more basic dc-to-dc converters: the Ćuk converter contains four passive energy storage components (two inductors and two capacitors) and a single switch. Moreover, there is extensive literature on the state-space modelling of the Ćuk converter [14].

Modelling of the Ćuk converter

Our modelling of the Ćuk converter is based on Slobodan Ćuk's PhD thesis [14]. In it, the author details the procedure for the derivation of state-space equations for power converters, and the final model of the Ćuk converter is provided. However, the model does not take into account passive component parasitics. In our approach to the modelling,

we have decided to include them, as detailed in Appendix B. The topology of the Ćuk converter is shown in figure 3.7.

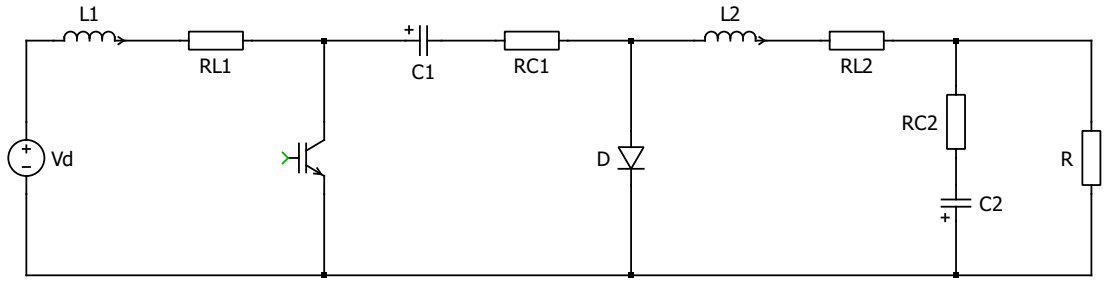

Figure 3.7: Ćuk converter schematic.

The main guidelines for state-space modelling of power converters, as illustrated in Appendix B can be summarized as:

- Define states as the variable associated with the stored energy level of all passive components: inductor current and capacitor voltage.
- Derive the differential equations describing the circuit in each of its switching states, using the expressions $v_L = L\frac{di_L}{dt}$ and $i_C = C\frac{dv_C}{dt}$ and Kirchoff's voltage and current laws. For a linear state-space model, the derivative of each of the states must be found only in terms of other states and inputs; the derivatives of other states or inputs and independent terms cannot be included without linearization.
- The equations must be expressed in the general matrix form described in Appendix A.
- Outputs can be defined as desired, as a combination of states and inputs.

If desired, the state-space models obtained for each state can be joined together into a state-average model, turning the coefficient matrices into functions of the switch duty cycles. The accuracy of such a model depends on circuit topology and switching frequency, and must be carefully evaluated. In our experience, the state-average model of a Ćuk converter starts to accurately reflect its behavior at a switching frequency of approximately 15 kHz, with 1 mH ideal inductors and 5 μF ideal capacitors.

In the case of the three-switch inverter, state-averaging is not used by Farhadi and Abapour, as the proposed MPC scheme controls the converter in terms of optimum discrete switching states and not optimum duty cycles.

The averaged state-space model developed as described in Appendix B has been tested by implementing and running the model and Simulink and comparing the obtained results with those of a PLECS simulation. The obtained waveforms are shown in figure 3.8, for a Ćuk converter with the parameters: $D = 0.8$, $L_1 = L_2 = 1\,mH$, $C1 = C2 = 5\,\mu F$, $V_d = 10\,V$, $R = 5\,\Omega$, $R_{L1} = R_{L2} = 0.1\,\Omega$, and $R_{C1} = R_{C2} = 0.05\,\Omega$.

From figure 3.8 it becomes clear that the state-space model with parasitics matches steady-state simulation values almost perfectly, and quite accurately during the initial transient period. The differences with the ideal circuit model are also apparent. The expected ideal

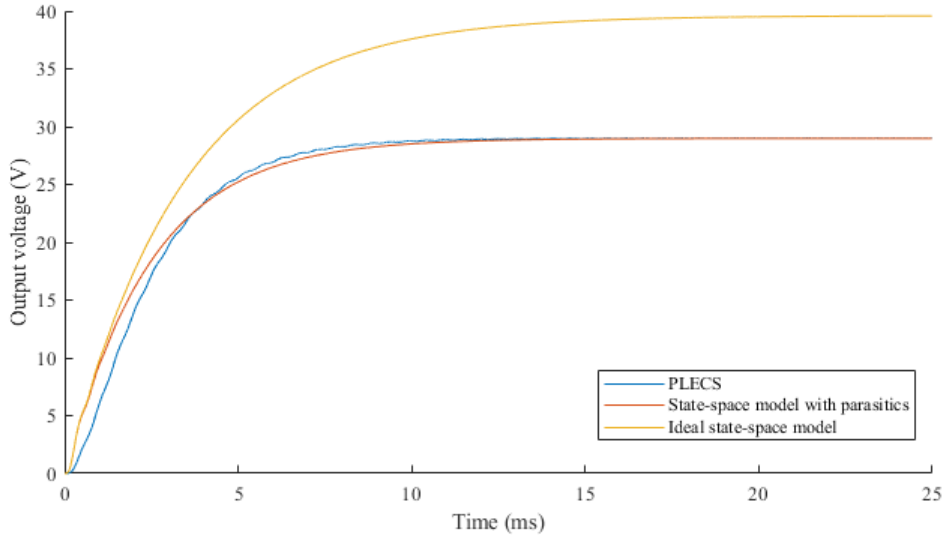

Figure 3.8: Ćuk converter output voltage transient waveforms.

output voltage, as obtained through steady state analysis, is calculated as:

$$V_{out} = \frac{D}{1-D} V_d = \frac{0.8}{0.2} \cdot 10 = 40\,V \tag{3.6}$$

This value matches the ideal state-space model steady-state result.

It should be noted that the derivation of state-space models becomes increasingly complex for circuits with several switching devices: every switch multiplies by 2 the number of states for which models must be developed. Therefore, the three-switch converter has 8 distinct switching states. To avoid tackling the modelling of the three-switch converter directly an intermediate step is proposed, consisting on simplifying the circuit.

Modelling of the simplified two-switch converter

By removing one of the output legs of the three switch inverter, the circuit should be able to generate a single-phase ac voltage. Due to the symmetry of the three-switch converter, this simplification should be valid. The details and results of the modelling process are shown in Appendix C. The topology of this reduced two-switch converter is shown in figure 3.9.

The figure reveals that this simplified topology is remarkably similar to that of the Ćuk converter: by swapping the inductor L_x with the switch Q_x and exchanging the switch Q_1 for a diode, the two topologies become equal. Therefore, the approach taken to model the three-switch converter is almost identical to the one used for the Ćuk converter, while adding two more switching states.

Simulations of the state-space model in Simulink prove that the results obtained for single switching states accurately match those from PLECS simulations; but they do not completely match those obtained when switching between states. This problem was found again when modelling the three-switch converter: further details are provided in the following section.

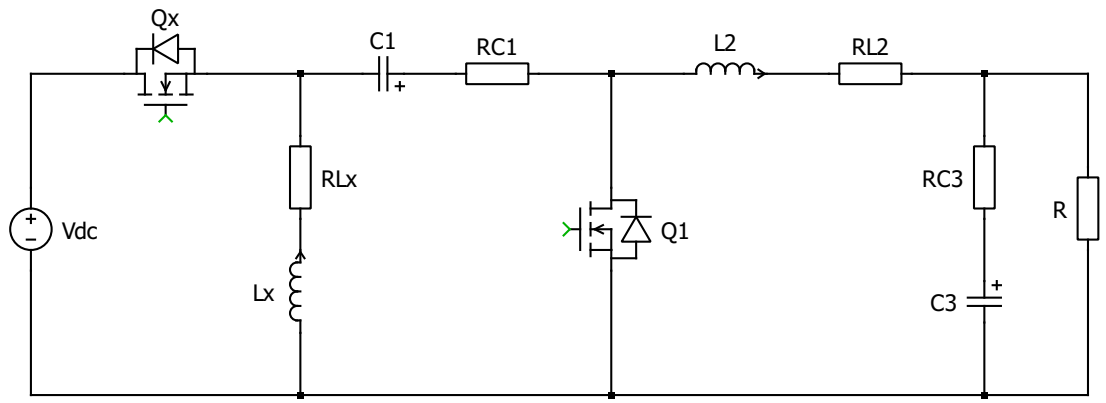

Figure 3.9: Two switch converter schematic.

As no satisfactory results were obtained for this simplified topology, we decided to attempt to model the three-switch converter directly, as the paper by Farhadi and Abapour [1] can be used as a reference.

3.1.4 Modelling of the three-switch converter

The state-space modelling of the proposed three-switch converter is detailed in Appendix D. Our approach mainly differs from that of Farhadi and Abapour in defining capacitor voltages v_{C1} and v_{C2} as states instead of inputs. In order to reduce its complexity, the model is developed neglecting all passive component parasitics. However, as for the reduced two-switch converter, the results obtained from simulation of the model do not completely match those from PLECS simulations when switching between states.

In order to verify the validity of the model, PLECS is used to extract the state-space models that the software uses; as PLECS is also based on switching state-space models. To do so, a small script is executed after the circuit has been designed. By defining the state of each of the switches (switching mode), the software outputs the coefficient matrices that it uses for the simulation of that particular mode. By comparing these results with those obtained from our state-space modelling, we found that the models match for all of the switching states except for mode 8, which has all three switches in off state. This should verify that our modelling is correct, at least for the first 7 switching modes. The schematic of the three-switch converter is shown again in figure 3.10, for reference purposes.

The issue with mode 8 is that to obtain the equations describing the derivatives of inductor currents, no current loop exists that does not come across either two inductors or a diode. Therefore, in our modelling, one of the diodes had to be assumed to be conducting.

However, the coefficient matrix for mode 8 extracted from PLECS shows that the calculation of the three inductor current derivatives is done using all four capacitor voltages. To our best knowledge, this appears to be the result of a numerical linearization process. Therefore, the model used by PLECS is not exactly equivalent to the one that we obtained.

Although the first 7 modes perfectly match those used by PLECS, the results obtained from the model do not match those of the PLECS simulations when switching between modes, even when mode 8 is deliberately left out of the simulation. This suggests that

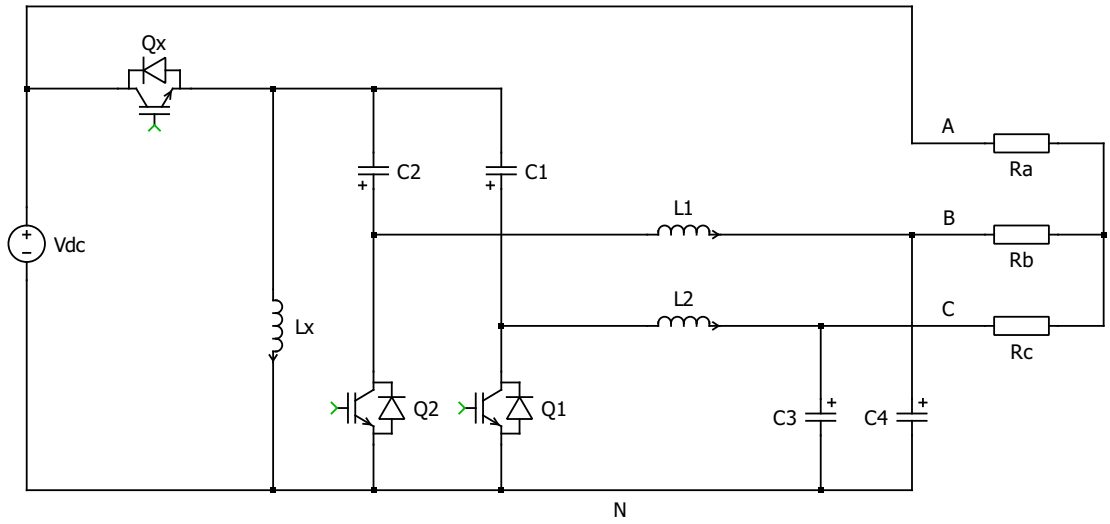

Figure 3.10: Three-switch converter schematic.

PLECS uses more information for its state-space model simulation than it makes available; even when running a model built from the numerical coefficient matrices given by PLECS the results still differ from the circuit simulation. Therefore, we have concluded that the proposed three-switch inverter cannot be accurately modelled by a linear state-space model as defined in this report.

A possible explanation as to why this miss-match occurs is that PLECS uses different coefficient matrices depending not only on the state of the switches but also on the state of the anti-parallel diodes. Accounting for all possible states with conducting diodes would, however significantly increase the complexity of the model. Not only would we have to derive the coefficient matrices for all possible diode state combinations, but for simulation purposes we would also have to implement further logic statements to switch between circuit states depending on diode voltage polarities. We have therefore decided that the amount of work that such a process would require, without ensuring the obtention of a working model, falls outside of the scope of this project.

Another possible explanation for the miss-match between results is the fact that the state-coefficient matrices obtained through our modelling process do not have full rank in several of the switching states. This implies that their inverse matrix does not exist for these states. Therefore, the equations derived in Appendix A for the solution of state-space models cannot be applied directly, as equation A.22 requires the use of the inverse state coefficient matrix. Conceptually, this would imply that the modes without a full rank coefficient matrix do not have unique solutions to some of the state derivative values.

This issue can be overcome by substituting the inverse matrix for a pseudo-inverse one. We attempted to implement the Moore-Penrose inverse, which retains some of the properties of the inverse matrix. When solving a system of equations containing some linearly dependent equations (as would be the case), using the Moore-Penrose inverse results in the obtention of a singular solution that minimizes Euclidean norm between all solutions: this can be interpreted as the least-squares solution. We do not know, however, if this is the approach used by PLECS when encountering such a problem, so different results may still

be obtained when using this procedure, assuming the models to perfectly match.

It should be noted that the inclusion of passive component parasitics in the modelling process allows for the use of the proper inverse matrix, as the coefficient matrix then becomes full-rank for all of the switching modes. However, simulations run with the numerical matrices extracted from PLECS including parasitics still do not yield satisfactory results.

Attempts at the implementation of MPC for simulation purposes have been carried out, but with little success. Presumably, our implementation of the basic MPC algorithm is correct, and thus the problem lies in the inaccuracy of the state-space model that it uses. Several state-space models were implemented in the MPC algorithm: the one provided in the paper by Farhadi and Abapour [1], with and without our suggested corrections, the one obtained through our modelling process as described in Appendix D, and the numerical ones obtained directly from the PLECS environment, both with and without parasitic components. However, none of the attempts proved fruitful.

A final attempt to figure out a possible control scheme for the converter was carried out. A PLECS/Simulink model was built containing independent PLECS circuit simulations for each of the switching states. A Matlab script is then run, which generates the output voltage references and receives output voltage simulation outputs for each of the 8 modes. Comparing the outputs of each of the simulated circuits with their references, the mode that most accurately matches the desired values is selected and its state values stored. For the next sampling instant, the values of the states are fed back to the circuits and the process is repeated until desired. Limited success was achieved with this approach, but we could not derive any consistent switching pattern from it.

Due to the many difficulties encountered in the control of the proposed three-switch converter, as detailed in this section, the main focus of the project was moved from the three-switch converter to the traditional six-switch one.

3.2 Traditional 6-Switch Converter

3.2.1 Circuit Analysis and Modulation

Unlike the three-switch converter, the traditional 6-switch converter has been studied for decades, so its behavior is well understood and thus many modulation techniques have been developed to suit different applications. A general schematic of this three-phase converter is shown in figure 3.11.

Assuming the switching devices and diodes to be ideal, the circuit analysis is very straightforward. It is important to keep in mind that a voltage source cannot be short-circuited, as it would then be providing ideally infinite current to the circuit. In a practical case, the large current spike would likely destroy the switching devices. Therefore, regardless of how the switching devices are to be controlled, the two switches of each leg must always be in opposite states, i.e. the pairs S1-S4, S3-S6, and S5-S2 must always have one device on and the other off. This reduces the number of possible states of the circuit from $2^6 = 64$ to $2^3 = 8$, which simplifies the analysis. For the purposes of this project,

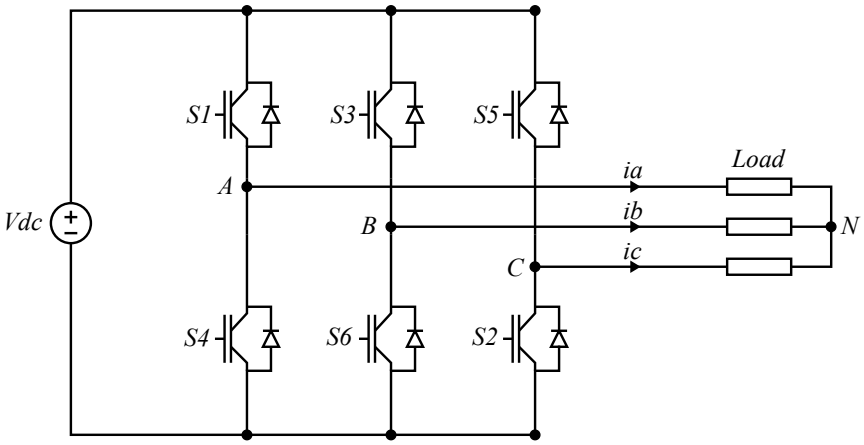

Figure 3.11: Six-switch traditional converter schematic.

the main concern is converter output current, as converter output voltage is fixed by the grid, with very limited possibilities for the converter to modify its values. The values of output voltage for each of the possible states of the converter, both line-to-neutral and line-to-line, are shown in table 3.1.

States	S_1	S_3	S_5	V_{AN}	V_{BN}	V_{CN}	V_{AB}	V_{BC}	V_{CA}
0	0	0	0	0	0	0	0	0	0
1	1	0	0	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	V_{dc}	0	$-V_{dc}$
2	1	1	0	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0	V_{dc}	$-V_{dc}$
3	0	1	0	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-V_{dc}$	V_{dc}	0
4	0	1	1	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-V_{dc}$	0	V_{dc}
5	0	0	1	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	0	$-V_{dc}$	V_{dc}
6	1	0	1	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	V_{dc}	$-V_{dc}$	0
7	1	1	1	0	0	0	0	0	0

Table 3.1: States of the three-phase, six-switch dc-to-ac converter.

A method must then be used to control the switching devices in such a way that the converter output currents can match their given references. This method is referred to as modulation scheme. In this project, the modulation scheme must be able to synthesize its voltage references, obtained from the desired current values. Therefore, the modulation scheme must be able to produce sinusoidal currents at a frequency of around 50 Hz, with the desired amplitude and phase, while minimizing non-fundamental harmonic amplitude. The modulation method used in this project is space vector modulation (SVM).

The main idea behind all modulation schemes is to use the switching devices of the inverter to make the output voltage transition between its possible voltage levels. As an example: switching between states 1 and 4 would result in V_{AN} becoming a square wave with a minimum value of $-\frac{2}{3}V_{dc}$ and a maximum value of $\frac{2}{3}V_{dc}$. For a three-phase inverter, however, all three phases must become balanced ac signals, so switching between two states is not sufficient. A way to obtain such an output is by simply following the sequence

from states 1 to 6 as detailed in table 3.1. This would generate output voltages as the ones illustrated in figure 3.12, for a single period of 50 Hz voltage.

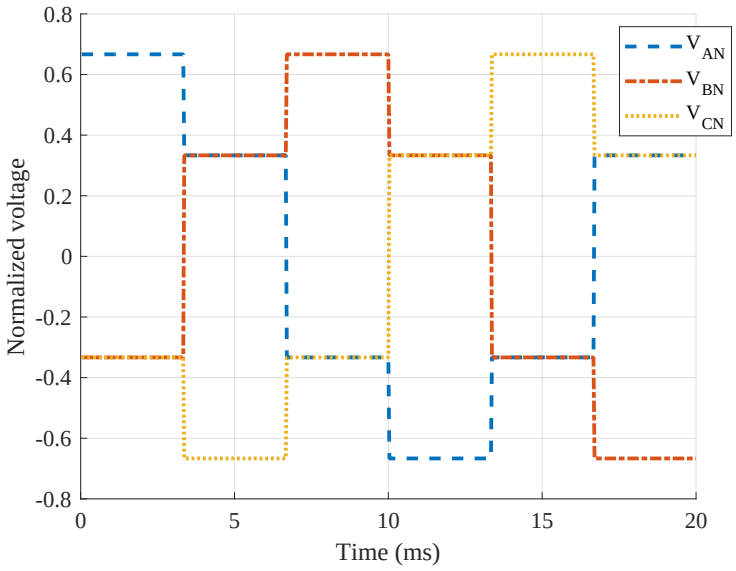

Figure 3.12: Phase to neutral voltages for a generic simplified modulation scheme.

4 Although these waveforms could be acceptable for some applications, their undesired harmonic content is too large for most purposes, as it is clear that they are far from pure sine waves. It is therefore needed to filter out these undesired harmonics. With the scheme described above, these undesired harmonics are found at low frequencies close to the fundamental, so the physical realization of the filter can become very challenging. By modifying the modulation scheme, however, these undesired harmonics can be pushed to higher frequencies. This can be done by switching between two adjacent states several times per period, as well as making use of the two zero states.

In order to minimize undesired harmonics while also minimizing switching instances (which result in power losses), the optimal state sequence to follow is state 0, followed by two active states, followed by state 7. This is illustrated in figure 3.13.

The figure assumes that the frequency of the carrier wave is much higher than that of the reference waves, which have approximately the same frequency as the grid voltage (50 Hz). Therefore, in a single switching period, as represented in the figure, the references can be assumed to be constant. The main concern of the modulation scheme is then to synthesize adequate reference voltages for each of the phases: v_a^{**}, v_b^{**}, and v_c^{**}. The horizontal axis of figure 3.13 shows the time spent in each of the switching states for sector 1, which is defined as the zone where the inverter is switching between state 1 and 2.

By making the reference voltages pure sinusoidal waves with equal frequency and 120° out of phase between each other, adequate harmonic performance can be achieved. However, the scheme can be improved further. One of the main concerns of inverter control is achieving the maximum possible output voltage without compromising the harmonic

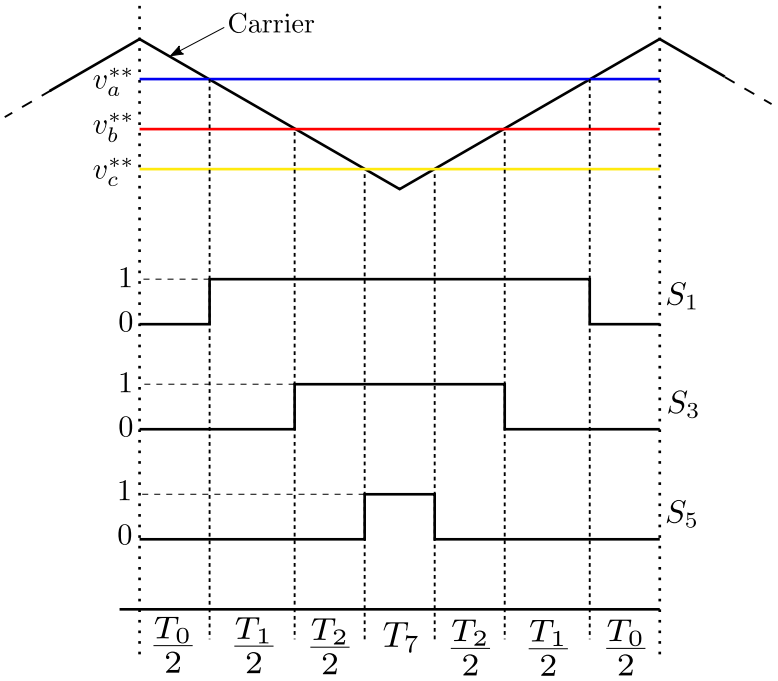

Figure 3.13: Switching sequence for the first sector of space vector modulation.

performance of the inverter. When the amplitude of the carrier wave is larger than the amplitude of the references, the converter operates in linear operation range, where output voltage is defined as the dc input voltage times the amplitude modulation factor m_a; which is defined as the ratio between reference voltage amplitude and carrier wave amplitude. Outside of this range, there are whole switching periods where some or all of the switching devices do not change their states. Output voltage can still increase at this point, at the cost of poorer harmonic performance and non-linearity. At infinite m_a, the output voltages would become square waves, which have the largest possible amplitude of their fundamental harmonic.

One way to increase the linear range of the converter is by making use of the zero-sequence component. In a balanced three-phase system, any voltage that is equally present in all three phases is cancelled out. Making use of this property, an option is to introduce a voltage at three times the fundamental frequency. Aligning it properly, the peaks of the reference voltages will be decreased, improving the linear range. As previously mentioned, this third harmonic is cancelled out. It has been concluded that a third harmonic with an amplitude of 1/4 that of the fundamental yields the optimum results, increasing the linear range of the inverter by about 15.5% [15].

Space vector modulation is based on a modification of this idea: instead of synthesizing a new third harmonic wave, it uses the already existing references to generate the zero sequence component. To do so, the three pure sinusoidal references are manipulated to obtain an almost triangular wave at three times the fundamental sequence. This signal is obtained by extracting the reference voltage that falls between the other two at every point in time. This is illustrated in figure 3.14.

Figure 3.14 shows that three pure sinusoidal references v_a^*, v_b^*, and v_c^* with a normalized

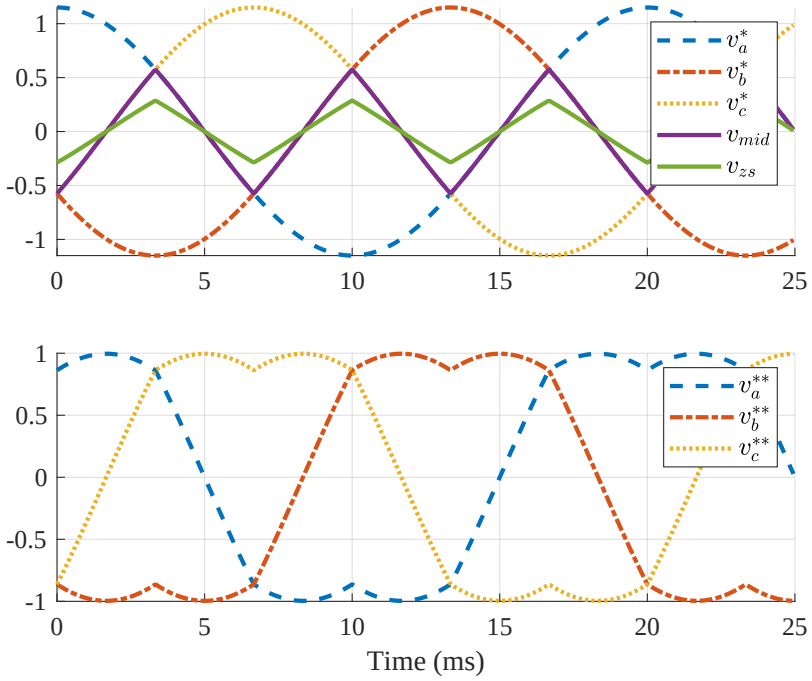

Figure 3.14: Reference generation for space vector modulation.

amplitude of $2/\sqrt{3}$ result in references v_a^{**}, v_b^{**}, and v_c^{**} with an amplitude of 1 after the calculated zero sequence v_{zs} is added to them. This is how SVM improves the voltage modulation capabilities of the converter with respect to the simpler pure sine-wave comparison method. To understand why $v_{zs} = 0.5v_{mid}$, further derivations must be provided [16] [17].

In sector I, $T_s = T_0 + T_1 + T_2 + T_7$, as shown in figure 3.13. By selecting the distribution of the zero states T_0 and T_7, different modulation strategies can be obtained. The distribution of these times can be defined as:

$$T_7 = k_0 T_{zero} \tag{3.7}$$

$$T_0 = (1 - k_0) T_{zero} \tag{3.8}$$

$$T_{zero} = T_s - T_1 - T_2 \tag{3.9}$$

T_0 corresponds to the time during which the upper switching devices S_1, S_3, and S_5 are all off, as seen in figure 3.13; this corresponds to the time during which the carrier wave is below all three reference sine waves. Similarly, T_7 corresponds to the time during which the carrier wave is above all three references. Therefore, the zero sequence component to be introduced to the references can be calculated as:

$$v_{zs} = k_0(1 - v_{max}^*) + (1 - k_0)(-1 - v_{min}^*) \tag{3.10}$$

For sector I:

$$v_{zs} = k_0(1 - v_a^*) + (1 - k_0)(-1 - v_c^*) \tag{3.11}$$

By choosing the value of k_0, different space vector modulation schemes can be achieved. Conventional space vector modulation uses $k_0 = 1/2$, which amounts to equal distribution between the two zero states, resulting in a symmetrical scheme. This yields the closest output to pure sinusoidal waveforms out of all possible values of k_0 [15]. Therefore, the zero sequence component becomes:

$$v_{zs} = \frac{1}{2}[(1 - v^*_{max}) + (-1 - v^*_{min})] = -\frac{1}{2}(v^*_{max} + v^*_{min}) \tag{3.12}$$

As the sinusoidal references form a balanced three-phase system, the expression for the zero sequence can be further simplified to:

$$v_{zs} = \frac{1}{2}v^*_{mid} \tag{3.13}$$

The final references can then be simply calculated as:

$$v^{**}_a = v^*_a + v_{zs} \tag{3.14}$$
$$v^{**}_b = v^*_b + v_{zs} \tag{3.15}$$
$$v^{**}_c = v^*_c + v_{zs} \tag{3.16}$$

Space vector modulation derives its name from the fact that the switching sequences to be applied to the converter can be calculated by representing the balanced three-phase reference voltages as a rotating space vector and using trigonometric identities and properties. In this way, the modulation scheme of the converter can determine the optimum switching state at any point in time by applying an algorithm with simple numerical calculations. This is the most commonly used approach because it removes the need to synthesize a carrier wave, thus further reducing the computational requirements of the control scheme. Therefore, such a method only requires the amplitude and phase of the space vector to modulate the inverter with satisfactory performance for most application.

In this project the carrier-based approach to SVM described in this section is used instead, due to its simplicity. The reference voltages are generated as described previously and then compared with a carrier triangular wave oscillating at a much higher frequency. The results obtained are completely equivalent to those obtained with a conventional SVM algorithm, and no issues with computational time were encountered in the implementation of the method for experimental tests.

3.2.2 Grid Synchronization

In order to control the current flow between the inverter and the grid, it is necessary to continuously extract the fundamental positive sequence magnitude and frequency/phase from the grid. Referring to the current control section, the current control is done in the rotating dq0 frame. Therefore, the instantaneous phase of the grid voltage is required to perform the reference frame transformation. Although current control can be performed through other means that avoid the use of reference frame transformations, this information is still required. This is the case for proportional-resonant controllers, another commonly used method for current control.

Several different methods can be used to obtain the phase information from the grid [18]. One approach is based on the Fourier transform: by performing this operation on the grid signal, its complete harmonic spectrum can be obtained. Then, the frequency of the fundamental harmonic can be extracted. Variations of the Fourier transform can be implemented as discrete adaptive filters running in real time, but achieving sufficient accuracy often implies too large a computational burden for the algorithm to be run in real time at the switching frequency of the converter.

A simpler method to measure grid frequency consists on zero-crossing detection: by determining the instants when the polarity of the voltage is reversed, and assuming the signal to be perfectly sinusoidal, phase and frequency can be obtained. The downside of this method is that higher order harmonics and non-linearities can result in additional zero-crossings to be detected in a single cycle of the fundamental; the zero-crossings of the fundamental signal do not necessarily match those of the measured voltage.

A third method is the phase-locked loop. A phase-locked loop is a closed loop system that uses the measured grid voltage as a feedback to obtain its phase information. This is the method that will be used in this project, as it avoids the issues presented by the previous two methods. Figure 3.15 shows the basic block diagram of a phase-locked loop structure.

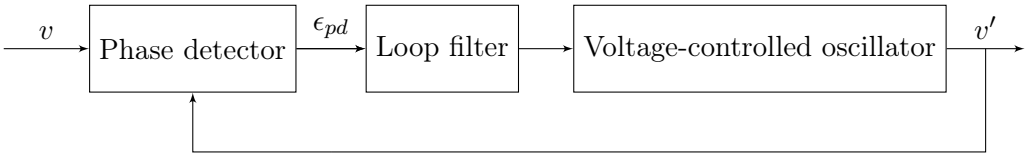

Figure 3.15: General PLL block diagram.

The blocks shown in the PLL diagram can be implemented in several different ways. A common method is to multiply the reference and measured sinusoids to obtain an error signal that can be used for the obtention of the phase. For the purposes of this project, the method chosen is based on reference frame transformations: this method has the advantage of not generating the oscillations in phase that appear in the phase-angle error signal at twice the fundamental frequency of the grid when using the simple multiplication method [18]. This results in better performance, as the frequency of these oscillations would be too close to that of the fundamental, thus complicating the design of the loop filter to avoid interactions.

Due to this fact, a synchronous reference frame phase-locked loop topology (SRF-PLL) is chosen, where the grid information is extracted directly in the rotating frame. A linearized model of the SRF-PLL is developed, which allow for an analytical design of the control system using classical control theory. Subsequently, the design is verified through simulation in Simulink.

SRF-PLL Design Based on Linearized Model

The basic idea of the SRF-PLL is to use a control loop acting on the voltage phase angle θ in order to force $v_q = 0$. This is done by using the output v_q of the dq0 transformation (T_{dq0}) as the error signal of the control loop. When $v_q = 0$, the space vector v_{pcc} is located

on the d-axis and θ is equal to angle of the grid, as a direct consequence. Note, that the d-axis output of the dq0 transformation is not utilized in the SRF-PLL control loop. The relationship between v_q and the angle/frequency difference between the grid and the PLL is shown mathematically in the following section:

$$T_{dq0} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.17}$$

$$\begin{bmatrix} V_m \cos(\omega_{pcc} t) \\ V_m \cos(\omega_{pcc} t + \frac{2\pi}{3}) \\ V_m \cos(\omega_{pcc} t - \frac{2\pi}{3}) \end{bmatrix} \cdot T_{dq0} = \begin{bmatrix} V_m \cos(\omega_{pcc} t - \theta) \\ -(V_m \sin(\theta - \omega_{pcc} t)) \\ 0 \end{bmatrix} \tag{3.18}$$

Substituting $\theta = \omega_{pll} \cdot t$ and rewriting using trigonometric identities yields:

$$v_q = V_m \sin(\omega_{pcc} - \omega_{pll})t \tag{3.19}$$

The non-linear equation 3.19 is linearized to:

$$v_q = V_m(\omega_{pcc} - \omega_{pll}) \tag{3.20}$$

A block diagram of the linearized system is illustrated in figure 3.16. With $PI = K_p + \frac{K_p}{T_i s}$ and neglecting the voltage amplitude of the grid (V_m), the closed loop transfer function is:

$$G_{CL}(s) = \frac{K_p s + \frac{K_p}{T_i}}{s^2 + K_p s + \frac{K_p}{T_i}} \tag{3.21}$$

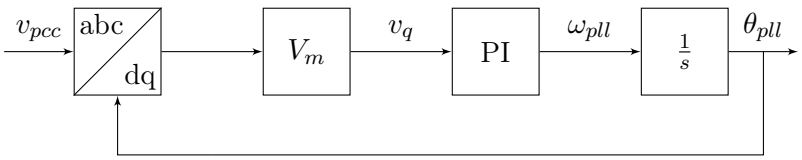

Figure 3.16: Linearized SRF-PLL block diagram

Equation 3.21 is similar to a general second order system with a zero:

$$G(s) = \frac{2\zeta\omega_n + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.22}$$

Ignoring the zero, the settling time and overshoot can be approximated using the standard relationships for a second order system:

$$\omega_n = \sqrt{\frac{K_p}{T_i}} \tag{3.23}$$

$$\zeta = \frac{\sqrt{K_p T_i}}{2} \tag{3.24}$$

ζ is set to 0.707 for a overshoot of 5% and settling time (T_s) is set to 20ms. From figure 3.17, it is evident that two responses differ to a certain degree. This could be due to the linearization and the zero from equation 3.21. Nevertheless, the settling times are correlating within a reasonable range, which indicates that the linearized model is valid for approximating the bandwidth of the SRF-PLL.

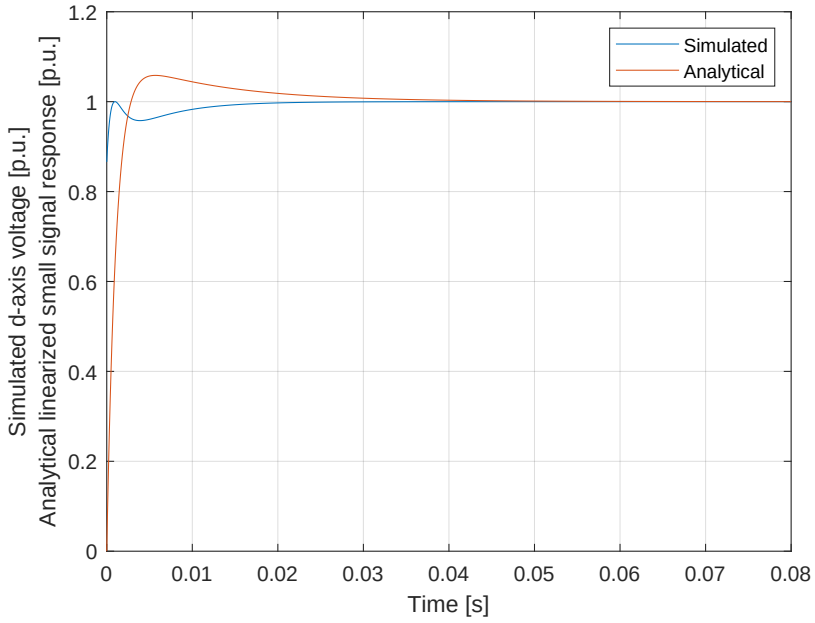

Figure 3.17: Comparison of analytical and simulated step response in the continuous domain.

The speed of the system determined by the T_s, is a trade off between noise/harmonic rejecting and synchronization speed [19]. This is shown in figure 3.18, where the grid is superimposed with a 25'th harmonic with a 0.1 pu amplitude. From figure 3.18, it is clear that high frequency harmonics can be rejected from the phase tracking by lowering the bandwidth.

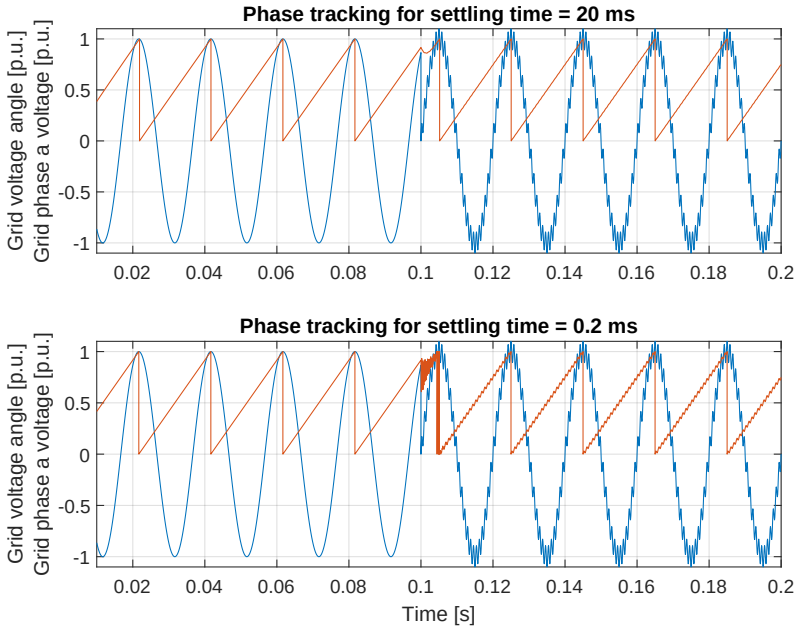

Figure 3.18: Harmonic rejection with different T_s for the SRF-PLL in the continuous domain.

From the figure 3.18, it is evident that high frequency distortions and harmonics can be rejected from the phase tracking by changing the bandwidth of the SRF-PLL through the PI. But, the basic SRF-PLL from figure 3.16 is not able to reject low order harmonics (eg. third and fifth harmonics) and negative sequence voltages. This problem is visualized in figure 3.19, where the basic SRF-PLL is operating on a grid where the voltage is polluted with: 10% 5. harmonic, 10% 7. harmonic and a 10% reduction of the phase A fundamental. A Fourier transform of the grid voltage of figure 3.19, shows that the negative sequence and harmonic disturbances are present at full amplitude in the extracted grid voltage. Furthermore, the extracted phase angle is clearly distorted. A solution to this problem through adaptive filtering, is provided in following section.

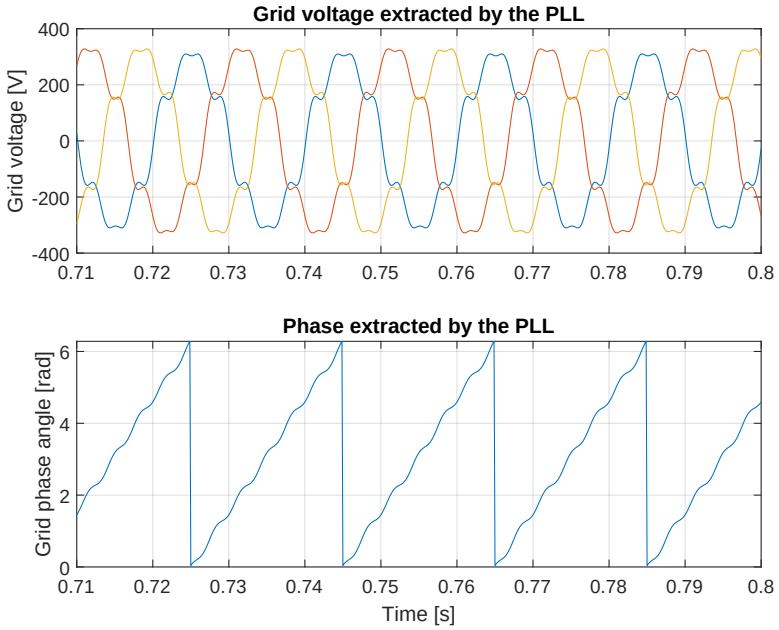

Figure 3.19: Basic PLL operating in a grid with low order harmonics and negative sequence voltage.

DSOGI PSC SRF-PLL

This section aims to explain the adaptive filtering method, that is utilized in the Double Second Order Generalized Positive Sequence Calculator SRF-PLL, and finally to show simulations of the performance of the DSOGI PSC SRF-PLL under non-ideal grid conditions.

In the scientific literature, there exist a number of different methods to improve characteristics of the PLL under distorted grid conditions. Most of them are based on adaptive filtering. The strength of adaptive filtering/adaptive noise cancelling, is that the filter algorithm is capable of automatically adjusting its own parameters during operation, and the design is virtually independent of the signal type [18]. The basic principle of noise cancellation through adaptive filtering is shown in figure 3.20. 's' is the signal of interest, 'n_0' is noise uncorrelated to 's', n_1 is noise correlated to n_0. If 'AF (Adaptive filter)' minimizes the power of the signal 'z', the noise term 'n_0' is removed through cancellation. This can be shown with some statistic manipulation [20], assuming that:

$$z = s + n_0 - y \tag{3.25}$$

Squaring on both sides, and then taking the expected value:

$$E[z^2] = E[s^2] + E[(n_0 - y)^2] + 2E[s(n_0 - y)] \tag{3.26}$$

Realizing that 's' is uncorrelated with both 'n_0' and 'y', and the signals are stationary and have zero mean values, the last term disapppears. When the filter minimizes 'z' through

manipulating 'y':

$$minE[z^2] = E[s^2] + minE[(n_0 - y)^2] \tag{3.27}$$

So, the filter output 'y' is equal to the noise 'n_0' and the 'z' is equal to the signal of interest 's'.

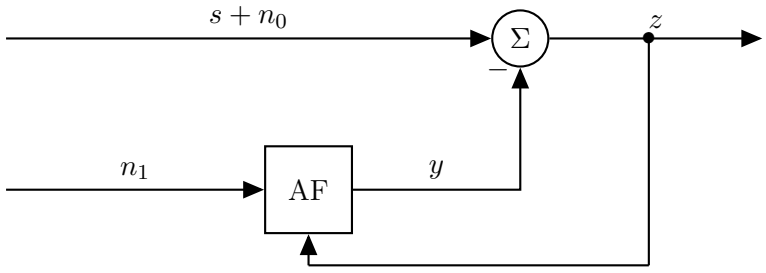

Figure 3.20: Principle of active noise cancelling.

Second Order Generalized Integrator (SOGI)

A common and efficient way to implement an adaptive filter for synchronization in power systems [21], is by using the SOGI in the forward path, which is displayed in figure 3.21.

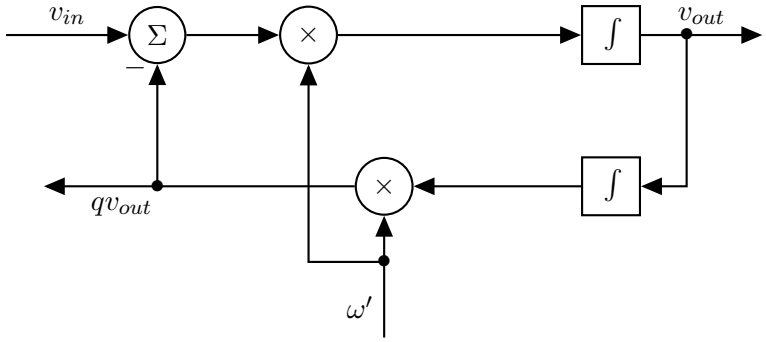

Figure 3.21: SOGI open loop

The SOGI provides infinite gain, at only the frequency ω' which is fed into the SOGI. This frequency response is visualized in figure 3.22. The transfer function is equation 3.28 [18].

$$\frac{v_{out}}{v_{in}} = \frac{\omega' s}{s^2 + \omega'^2} \tag{3.28}$$

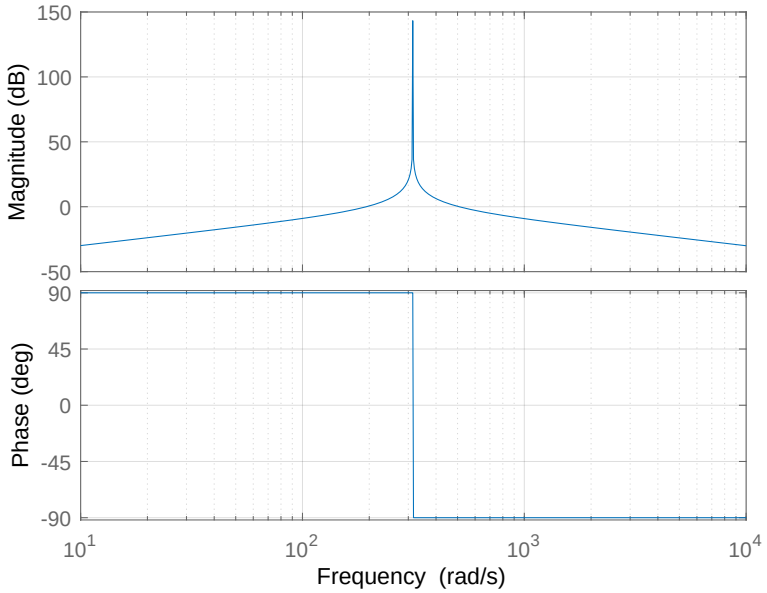

Figure 3.22: Frequency plot of SOGI from equation 3.28, where $\omega' = 2\pi 50$

A complete adaptive bandpass filter is obtained on figure 3.24, by closing the loop around the SOGI (figure 3.21) and inserting a gain 'k' in the forward path. The transfer function for the adaptive bandpass filter is equation 3.29 [18] and the frequency plot is shown on figure 3.23.

$$\frac{v_{out}}{v_{in}} = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \tag{3.29}$$

The bandwidth of the filter (figure 3.24) is solely dependent on k, while the center frequency is ω'.

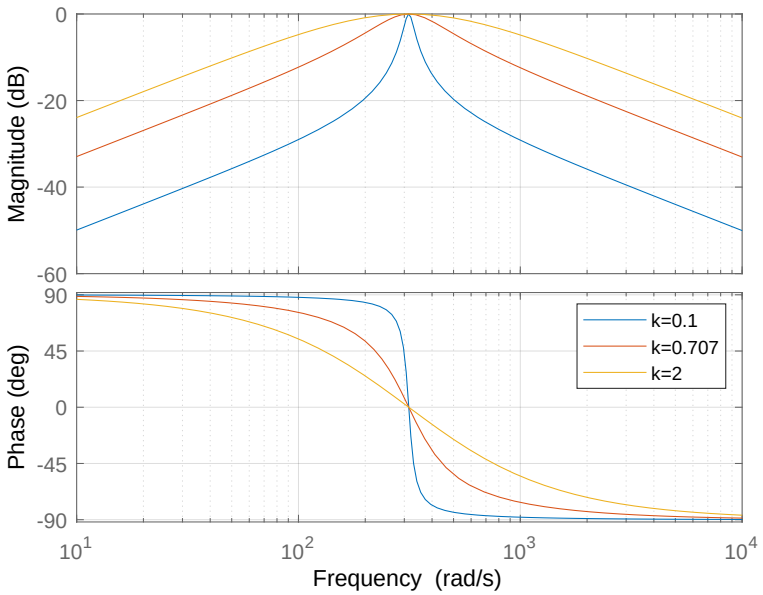

Figure 3.23: Frequency plot of SOGI from equation 3.29, where $\omega' = 2\pi 50$, with diferent values of k.

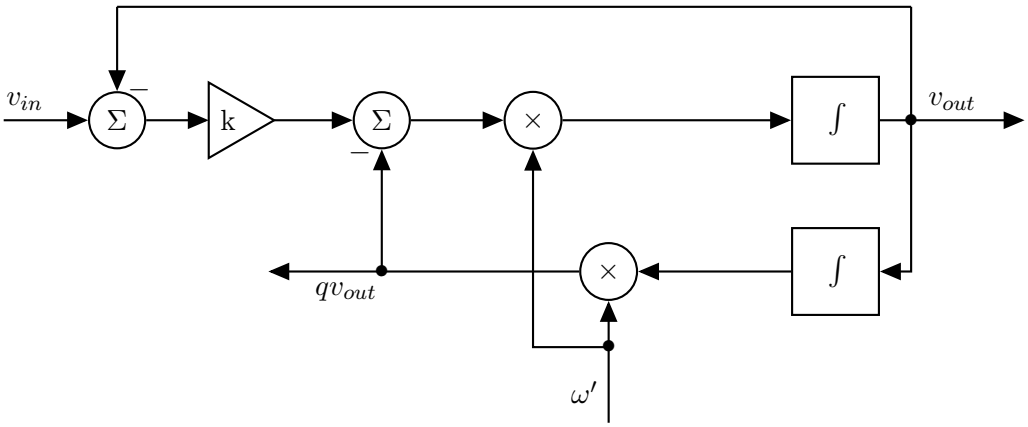

Figure 3.24: SOGI closed loop

Full PLL topology including the PSC

A convenient feature of the SOGI, is that it generates at 90° displaced version of the signal v_{out}, which is qv_{out}. This signal is useful for extraction of the positive sequence component, as the positive sequence component of a signal in the $\alpha\beta$-domain can be calculated from equation 3.30 [22].

$$\mathbf{v}^{+}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & -1 \end{bmatrix} \mathbf{v}_{\alpha\beta} \tag{3.30}$$

Where $q = e^{-j\frac{\pi}{2}}$.

The implementation of equation 3.30 is the (PSC) positive sequence calculator of the PLL.

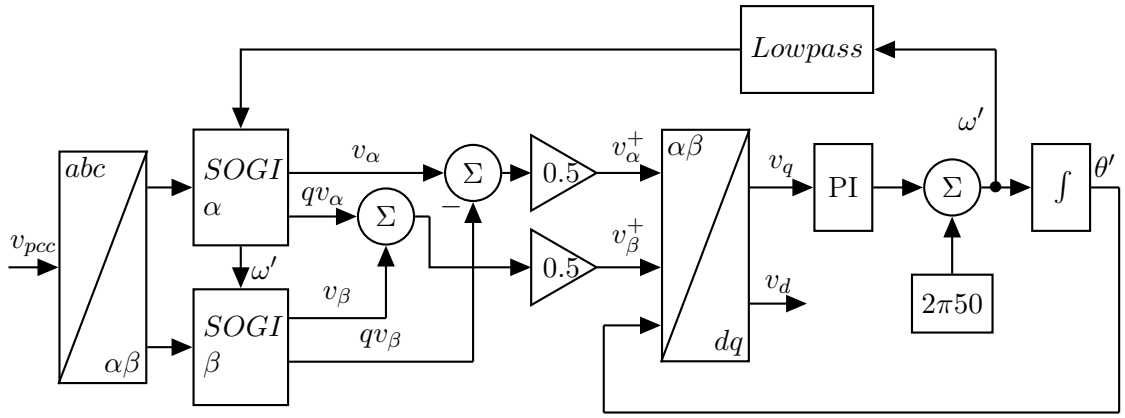

Figure 3.25: DSOGI PSC SRF-PLL

The complete PLL system is shown in figure 3.25. The system is composed of the following elements from left:

- **Adaptive bandpass filter (DSOGI)**: A SOGI (3.24) for the α-component of v_{pcc} and a SOGI for the β-component of v_{pcc}.

- **PSC**: Implementation of equation 3.30 through summations and gains.

- **SRF-PLL**: The basic SRF-PLL from figure 3.19.

A first order low-pass filter with a bandwidth of 20 Hz, is inserted into the feedback path of ω', as stability issues were arising during transients, in simulation and experiments.

The distorted grid scenario from figure 3.19 is repeated, where the grid is superimposed with 10% 5. harmonic, 10% 7. harmonic and 10% reduction of phase a fundamental. With the adaptive filtering and PSC added, the extracted voltage and phase should purely contain the positive sequence of the fundamental with no harmonics. The positive sequence of the fundamental grid voltage, when there is a 10% reduction in phase a amplitude, has an amplitude of 314 V.

Figure 3.26 shows the results from the PLL operating on the distorted grid. As intented, the extracted voltage is perfectly balanced 3-phase voltage with an amplitude of 314 V and no harmonic distortion. Furthermore, the phase signal is an ideal sawtooth with no oscillations.

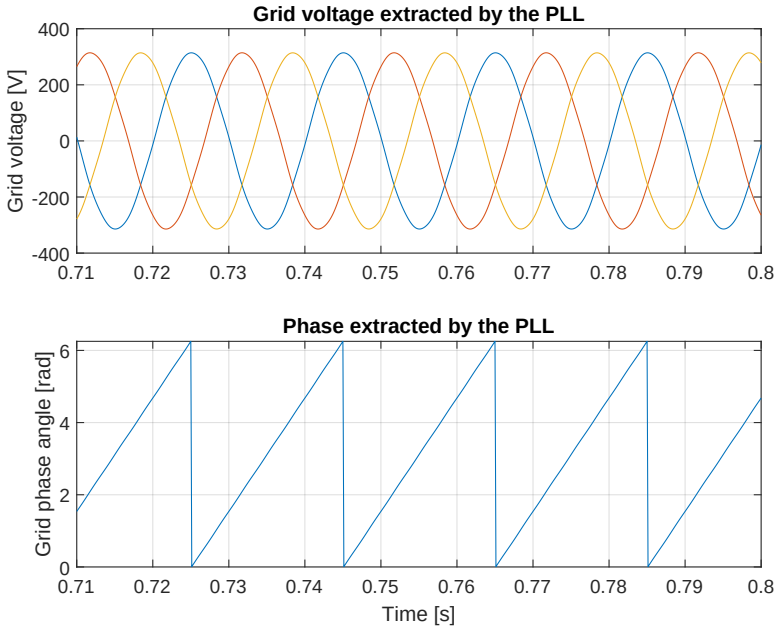

Figure 3.26: Voltage and phase extracted from distorted grid by the DSOGI PSC SRF-PLL.

3.2.3 Converter Output Filter and Current Control

Filter considerations

The appearance of high frequency harmonics in the converter output can quickly deteriorate and pollute the grid. In order to mitigate this problem, a filter is required to act as interface between inverter and grid. Among the most used filters are the L filter and LCL filter.

In practice, a simple L filter would require a high inductance value, as a first order filter only provides 20 dB/decade among other reasons. This translates to a bulky, heavy and expensive physical inductor. Using an LCL filter, that provides an attenuation of 60 dB/decade, does generally allow for much lower inductance values [23]. In this project an LCL filter is used with the following parameters:

$L_1 = 1.8$ [mH] - inductor on inverter side

$L_2 = 2$ [mH] - inductor on grid side

$C = 4.7$ [µF] - capacitor

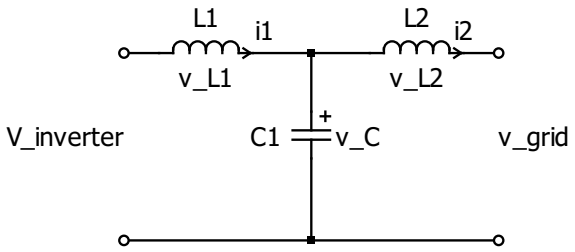

Figure 3.27: LCL filter schematic.

The transfer function for the filter can be obtained by performing basic Kirchhoff's laws analysis on figure 3.27 as such:

$$v_{inverter} - v_{L_1} - v_{L_2} - v_{grid} = 0 \tag{3.31}$$

$$v_{inverter} - v_{L_1} - v_C = 0 \tag{3.32}$$

$$v_C - v_{L_2} - v_{grid} = 0 \tag{3.33}$$

$$i_1 - i_2 - i_C = 0 \tag{3.34}$$

By decoupling the grid voltage (setting $v_{grid} = 0$), substituting $v_{L_1} = L_1 \cdot \frac{di_1}{dt}$, $v_{L_2} = L_2 \cdot \frac{di_2}{dt}$ and $i_C = C \cdot \frac{dv_c}{dt}$, performing equation reduction and transforming to Laplace domain, the following transfer function is obtained:

$$\frac{i_2(s)}{v_{inverter}(s)} = \frac{1}{C \cdot L_1 \cdot L_2 \cdot s^3 + (L_1 + L_2) \cdot s} \tag{3.35}$$

The positioning of an inductor near a capacitor usually results in resonance issues that need to be dealt with in order to ensure proper operation of the filter. This resonance happens as the collapsing magnetic field of the inductor generates an electric current in its windings which charges the capacitor; following this, the capacitor then provides electric current which builds back the magnetic field in the inductor, leading to a loop. In practice, this means that at the resonance frequency, the circuit shows theoretically zero impedance, which can cause over-currents.

As seen in the open loop Bode diagram for an LCL filter from figure 3.28, the resonance happens at 2385 [Hz], based on the following formula $f_{res} = \sqrt{\frac{L_1+L_2}{L_1 \cdot L_2 \cdot C}} \cdot \frac{1}{2 \cdot \pi}$.[24]

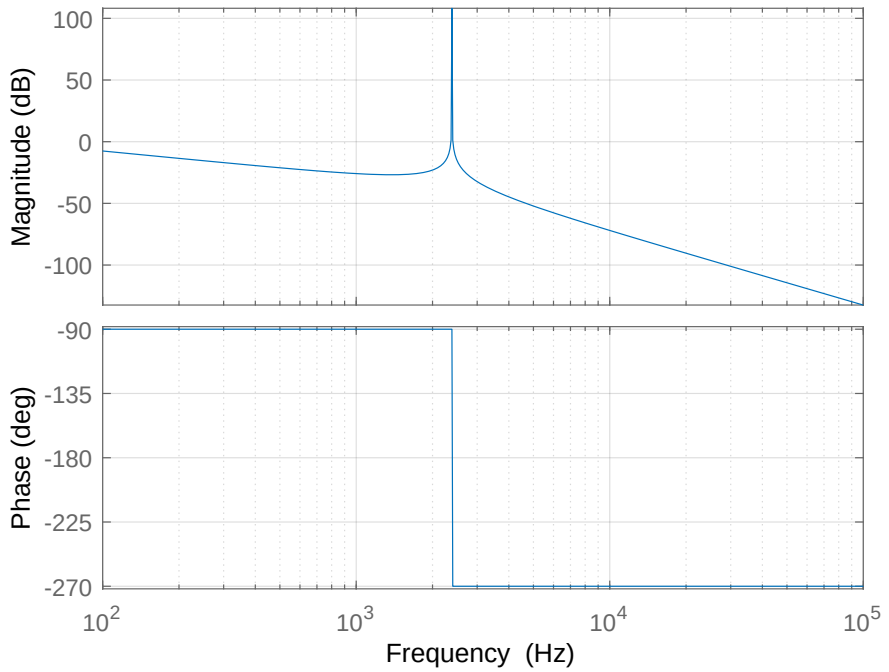

Figure 3.28: Bode diagram for LCL filter.

In order to eliminate this resonance, ideally, multiple control strategies have been developed and discussed in [18], [24] which vary from performing active or passive damping in the circuit, to using either proportional-resonant controllers or notch filter, each with its own benefits and trade-offs. In this project however, perfect control of the LCL filter is not the main aim, therefore a simpler method is implemented to ensure basic proper functionality. In this method, PI controllers will be used; the cutoff frequency of these controllers will be chosen as to not interfere with the LCL's resonance frequency. As a consequence, the LCL filter could be treated as a simple L filter which significantly reduces the complexity of controlling it, where $L = L_1 + L_2$. For more accurate representation, the parasitics of the inductors is also accounted for ($R = r_{L1} + r_{L2}$) and R is approximated to $R = 0.01[\Omega]$.

Therefore, eliminating the capacitor from figure 3.27 the following transfer function can be obtained from the resulting two-port circuit:

$$\frac{i_2}{v_{inverter}} = \frac{1}{L \cdot s + R} \tag{3.36}$$

which can be written as a first order system (3.37), which simplifies the control system analysis.

$$\frac{i_2}{v_{inverter}} = \frac{1}{R} \cdot (\frac{1}{\tau \cdot s + 1}) \tag{3.37}$$

where $\tau = \frac{L}{R}$ and $\frac{1}{R}$ is a constant gain.

The L filter behaves as a low pass filter, as shown in 3.29, with the cutoff frequency at $\frac{R}{L} \cdot 2\pi = 0.41$Hz but with a gain of $\frac{1}{R} = 100$ voltage-ratio, which equals to 40 dB.

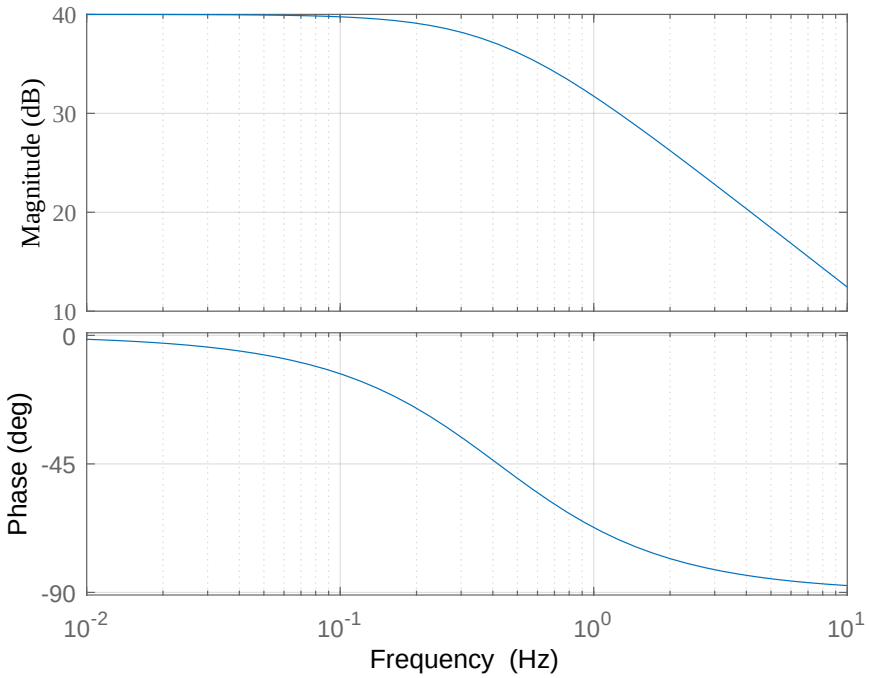

Figure 3.29: Bode diagram for L filter.

It needs to be noted though, that in order for this approximation to work, the controller bandwidth must be carefully chosen to be far enough from the resonance frequency as to be able to dampen the LCL resonance after it, but high enough to let the 7^{th} order harmonics at 350 [Hz] pass, as it will be part of the applications tackled later on this project.

Current control

Having made the above-mentioned approximations, the control strategy will be elaborated in this section.

The control objectives for the closed loop current control are as follows:

- Stability with a steady state error within maximum of 2%.
- Maximum overshoot of 10%.
- Ensuring a good controller bandwidth that would not interfere with the resonance of the LC filter nor would it dampen the 7^{th} harmonic. In this case the chosen cutoff frequency is 500 Hz.

The objective of the current control strategy is to derive a linear transfer function with inverter voltage as input and grid injected current as the output.To this end, having figure

3.30 as starting point, the following equation derivation is performed:

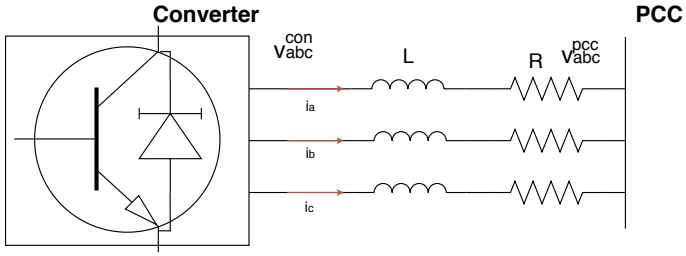

Figure 3.30: Converter - PCC connection with LR filter.

By using Kirchhoff' voltage law,

$$\begin{bmatrix} v_a^{con} \\ v_b^{con} \\ v_c^{con} \end{bmatrix} - \begin{bmatrix} v_a^{pcc} \\ v_b^{pcc} \\ v_c^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.38}$$

By applying the inverse Park tranformation,

$$\left[T_{dq0}^{-1}\right] \begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \left[T_{dq0}^{-1}\right] \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \left[T_{dq0}^{-1}\right] \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \left(\left[T_{dq0}^{-1}\right] \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \right) \tag{3.39}$$

where $[T_{dq0}^{-1}] = \begin{bmatrix} cos(\theta) & -sin(\theta) & 1 \\ cos\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ cos\left(\theta + \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix}$

and represents the inverse of $[T_{dq0}]$ from equation 3.17.

Performing more calculations and keeping the voltage difference isolated the equation 3.40 is obtained.

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \omega \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \begin{bmatrix} -i_q \\ i_d \\ i_0 \end{bmatrix} \tag{3.40}$$

For better understanding it is worth reminding that the derivative terms can be expanded as,

$$\frac{d}{dt}\left(\left[T_{dq0}^{-1}\right] \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \right) = [T_{dq0}^{-1}] \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \left(\frac{d}{dt}[T_{dq0}^{-1}] \right) \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{3.41}$$

and

$$\left(\frac{d}{dt}[T_{dq0}^{-1}] \right) \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \omega \cdot [T_{dq0}^{-1}] \begin{bmatrix} -i_q \\ i_d \\ i_0 \end{bmatrix} \tag{3.42}$$

and a detailed mathematical derivation of these two equations as well as equation 3.40 can be found in appendix E.

The system is assumed balanced therefore, the 0 component can be safely ignored, and thus, from equation 3.40 the two components (d and q) can be written in s-domain as:

$$\begin{aligned} v_d^{con} &= i_d \cdot (R + Ls) + v_d^{pcc} - \omega \cdot L \cdot i_q \\ v_q^{con} &= i_q \cdot (R + Ls) + v_q^{pcc} + \omega \cdot L \cdot i_d \end{aligned} \tag{3.43}$$

where $\omega L i_{qd}$ are the decoupling terms and v^{pcc} are the feed-forward terms, which will be added after the PI controller so non-linearity problems in the control scheme can be avoided. This means that the controller will be tuned only for $\frac{1}{R+Ls}$ - the LR filter transfer function from 3.36.

An important observation that can be made is that the control for d-axes is similar to the control for q-axis as the PI depends only on the L and R which are constant values. Therefore the LR transfer function has one pole at $-\frac{R}{L}$. A simple control solution here is to cancel it using the modulus optimum approach. Modulus optimum technique aims at achieving a closed loop transfer function that is constant on value 1 between 0 frequency and a limit frequency (ω_c). The L filter transfer function

$$G_p(s) = \frac{1}{L \cdot s + R} = \frac{1}{R} \cdot \frac{1}{\tau s + 1} \tag{3.44}$$

and the PI transfer function is

$$G_{PI}(s) = \frac{k_p \cdot s + k_i}{s} = k_i \cdot \frac{\frac{k_p}{k_i} \cdot s + 1}{s} \tag{3.45}$$

For pole cancellation it can be noticed that $k_p = \tau \cdot k_i$ and, from a purely mathematical perspective k_i would equal R; however at this point it is important to take into account the maximum controller bandwidth that can be used. Having said this, the control parameters, from an analytical point of view, are $k_i = \omega_c \cdot R$ and $k_p = \omega_c \cdot L$ with $\omega_c = 2\pi \cdot f_c$. As explained earlier, for this project, ω_c has been chosen for a $f_c = 500Hz$ therefore $\omega_c = 2\pi \cdot 500\ rad/s$; this way the controller bandwidth will not dampen the 7^{th} harmonic, which is desired for later applications; more explanations regarding the harmonics will be discussed in the **Harmonic Compensation** section.

Figure 3.31 shows a block diagram representation of the analytical model used to tune the PI controller. However, figure 3.32 shows the full block diagram for equations 3.43, including the adding of decoupling and feed-forward terms.

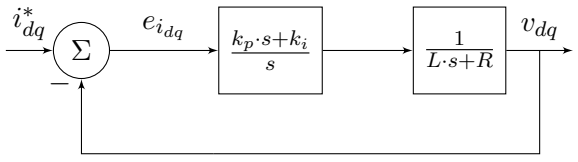

Figure 3.31: Simplified current control block diagram.

The closed loop equation characterising the block diagram in figure 3.31 is:

$$G_{closedloop} = \frac{G_p \cdot G_{PI}}{1 + G_p \cdot G_{PI}} = \frac{k_p s + k_i}{s^2 L + s(R + k_p) + k_i} \tag{3.46}$$

and will be used in the mathematical analysis for the closed loop step response in order to compare it with the simulated result and validate the dq control procedure.

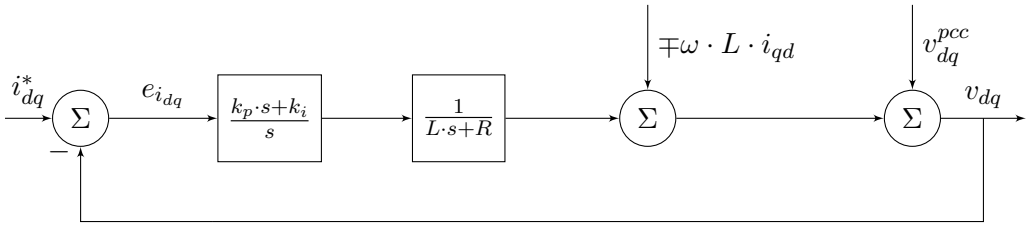

Figure 3.32: Detailed current control block diagram.

In order to discretize the control loop, discrete integrator blocks are used in the PI controller system.

Figure 3.33 shows the open loop frequency response for the LR filter approximation and the PI controller and how they interact with each other. It can be seen that the PI compensates the filter, turning the whole system to behave like an integrator with the phase fixed at -90° and constant slope of -20 dB/dec.

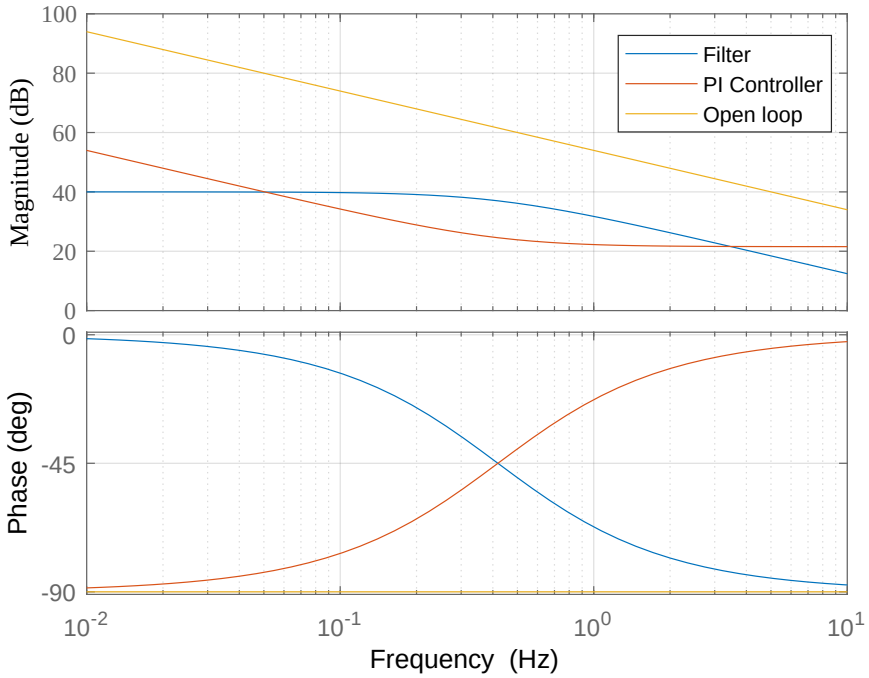

Figure 3.33: Bode diagram for the L filter and PI controller.

In order to validate the control strategy from a theoretical point of view, a step response is applied both to the closed loop transfer function (seen in equation 3.46) and the Simulink simulation in which a PLECS model of grid connected converter is controlled using the

dq scheme described so far. Figure 3.34 shows the results of this: both from an analytical perspective as well as resulting from the simulation, the step response's overshoot is within the maximum of 10% range, system is stable within a 2% steady state error and the parameter - $k_p = 11.94$ and $k_i = 31.42$ which are obtained through the analysis procedure described in this section.

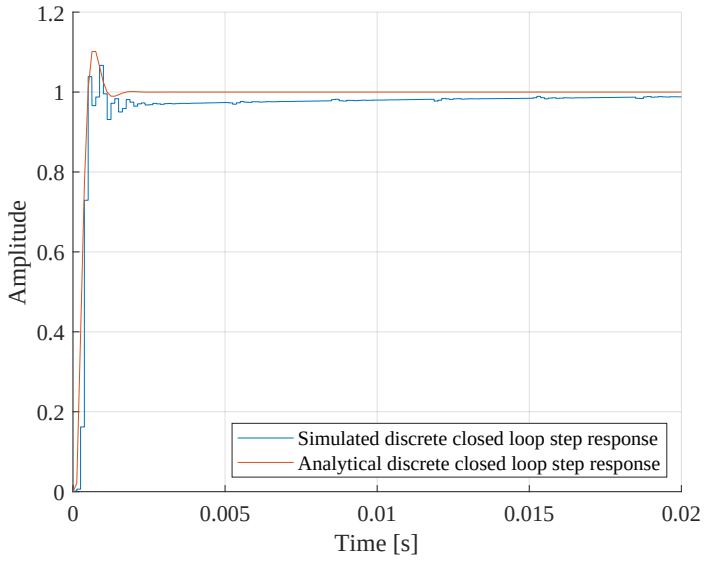

Figure 3.34: Closed loop step response for PI controlled grid injected d-component current.

The step response for the simulation is conducted for a change in step from 0 to 8 A in d current component and graphically represented as a normalized function, to fit the mathematical step response. It is worth mentioning that the simulated discrete step response follows the reference step even more precisely as the simulation continues, but visualising the whole time frame would be too cumbersome to follow on the same graph.

3.3 Harmonic Compensation

In ideal applications, grid currents are treated as three perfectly sinusoidal waveforms, phased out by 120° of each other. In reality however, the grid current is anything but perfectly sinusoidal. Various non-linear loads that are connected to the grid - such as rectifiers, variable frequency drives etc - inject into the grid currents with frequencies that are integer multiple of the fundamental frequency which add up and distort the desired sinusoidal profile. For this project the grid fundamental frequency is 50 [Hz].

In order to distinguish between the harmonics and the fundamental waveform, a distorted signal can be decomposed into the fundamental signal and each individual existing harmonic, using Fourier analysis as described by the following equation:

$$i(t) = I_{avg} + \sum_{k=1}^{\infty} I_k \sin(k\omega_0 t + \theta_k) \tag{3.47}$$

where I_{avg} is the average, I_k is the peak magnitude of each k-th harmonic, ω_0 is the fundamental frequency and θ_k is the phase angle of each harmonic.

Figure 3.35 shows an example of how harmonics behave and affect the fundamentals. The bottom most graph represents how current can actually look in the grid, once the 5^{th} and 7^{th} harmonics have been added over the fundamental frequency. This figure is just an example and it is worth pointing out that normally, one can find more types of harmonics in a grid.

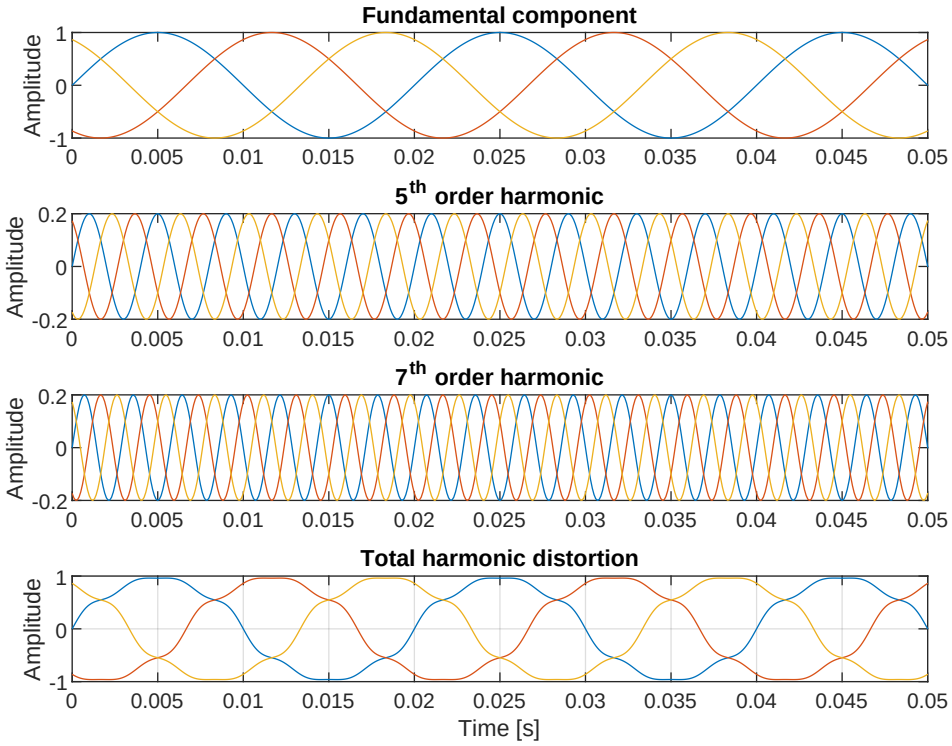

Figure 3.35: Visualisation of harmonics affecting the fundamental frequency.

By distorting the currents, harmonics can greatly affect the supplied power quality which results in significant lowering the lifetime of consumer devices, raising heating problems and increasing up the end user's final costs. Due to this, mitigating harmonics is of paramount importance and has been a major focus for engineers and manufacturers.

As discussed in section 3.2.3, the current controllers will dampen any frequency higher than the cut-off frequency of $f_c = 500[Hz]$. This means that harmonics higher than f_c will be negated and ideally not affect the system.

Before proceeding with the compensation strategy, certain consideration about these harmonics have to be made in order to understand the following rationals.

3.3.1 Even Order Harmonics

As mentioned previously, harmonics happen at integer multiple of the fundamental frequency, as such: 2^{nd} harmonic at 100 Hz, 3^{rd} harmonic at 150 Hz, 4^{th} harmonic at 200 Hz, 5^{th} harmonic at 250 Hz etc.

Most of the power electronic loads draw current from the grid via a full-bridge rectifier with a capacitor connected at its output, in parallel with the load. Due to this type of rectifiers, the drawn current presents what is known as half-wave symmetry. In order to have half-wave symmetry, a periodic function must stay the same after being shifted by half a period and inverted as shown by $f(t) = -f(t \pm \frac{T}{2})$ and in figure F.1 from Appendix F. This property translates to even-order harmonics being nullified. A more detailed mathematical explanation for this can be found in Appendix F.

For the purpose of this project, this property allows for neglecting the need of even order harmonic compensation and as such it will not be tackled.

3.3.2 3^{rd} Harmonic and Multiples of 3

Assuming a symmetrical, balanced, non-linear, 3-phase load, draws current containing the third harmonic which can be mathematically described as:

$$i_{a3} = I_3 \cdot \sin 3 \cdot \omega t \tag{3.48}$$

$$i_{b3} = I_3 \cdot \sin 3(\omega t - \frac{2\pi}{3}) = I_3 \cdot \sin(3\omega t - 2\pi) \tag{3.49}$$

$$i_{c3} = I_3 \cdot \sin 3(\omega t + \frac{2\pi}{3}) = I_3 \cdot \sin(3\omega t + 2\pi) \tag{3.50}$$

and thus $i_{a3} = i_{b3} = i_{c3}$. This shows that the 3^{rd} order harmonics is present on the 0-sequence component.

It can be seen that the three currents are in phase. As mentioned in section 2.1, the primary side of the transformer has a delta connection (no neutral wire to conduct the added phase currents), therefore $i_{a3} + i_{b3} + i_{c3} = 0$. This means that the 3^{rd} order harmonic currents cancel each other and stay trapped in the three wires connection, not being injected in the grid.

The same rational applies for all multiple of three harmonics, thus, including the 9^{th} order harmonic. As a conclusion, this project will not focus on 3^{rd} order or multiple of three harmonics compensation, since they do not represent a major problem.

3.3.3 5^{th} Harmonic

Figure 3.36 shows the distortion produced by 20% 5^{th} order harmonic on top of the fundamental frequency.

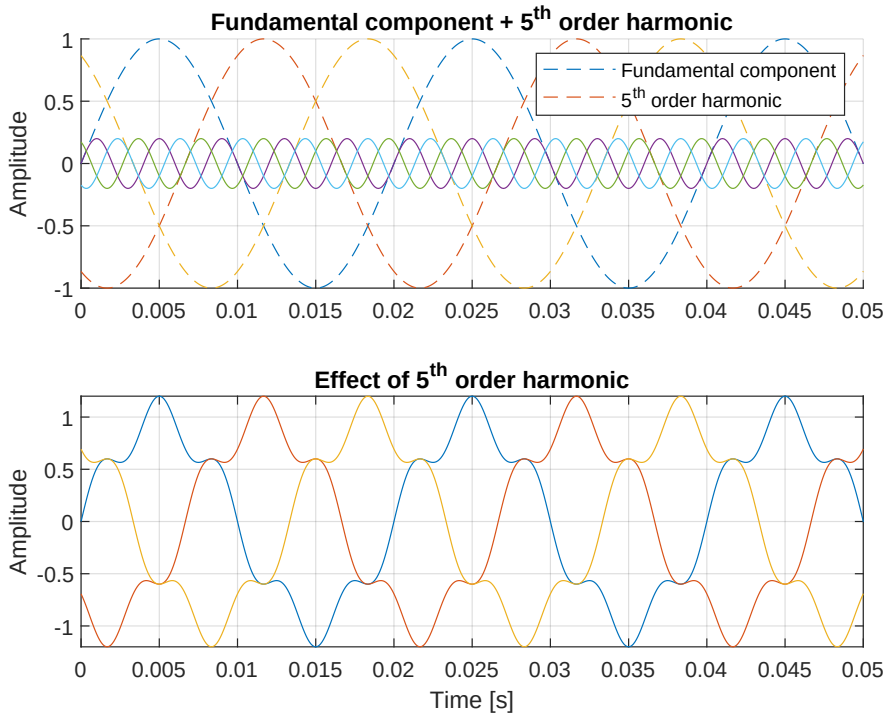

Figure 3.36: 5^{th} harmonic distortion in a 3-phased current.

Mathematically, the 5^{th} order harmonic can be expressed as:

$$i_{a5} = I_5 \cdot \sin 5 \cdot \omega t \tag{3.51}$$

$$i_{b5} = I_5 \cdot \sin 5(\omega t - \frac{2\pi}{3}) = I_5 \cdot \sin(5\omega t + \frac{2\pi}{3}) \tag{3.52}$$

$$i_{c5} = I_5 \cdot \sin 5(\omega t + \frac{2\pi}{3}) = I_5 \cdot \sin(5\omega t - \frac{2\pi}{3}) \tag{3.53}$$

It can be noticed that the 5^{th} order harmonic distorts the current following the negative sequence, as the corresponding phases rotate opposite to the fundamental component. In practice, this distortion usually produces significant torque problems.

3.3.4 7^{th} Harmonic

Figure 3.37 shows the distortion produced by 20% 7^{th} order harmonic on top of the fundamental frequency.

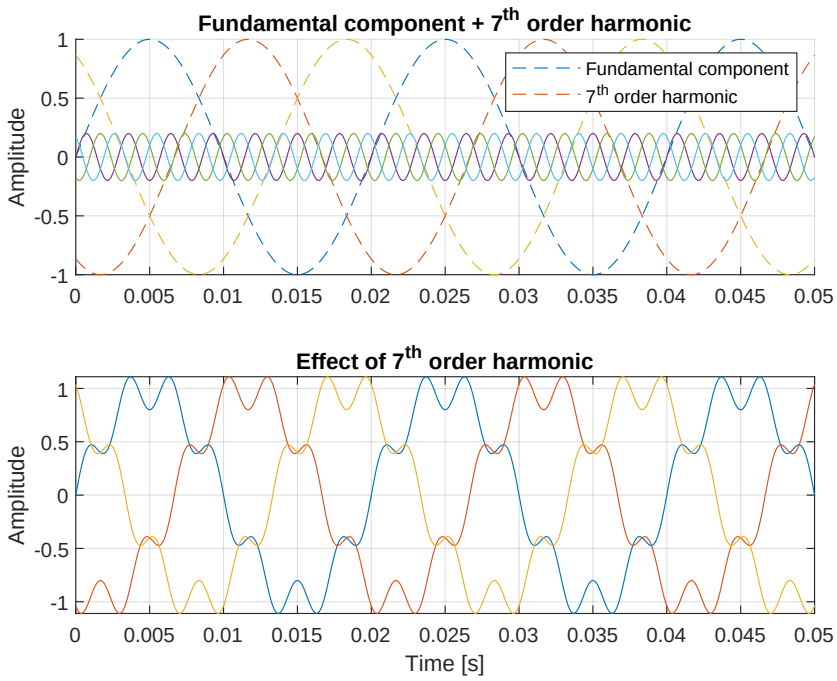

Figure 3.37: 7^{th} harmonic distortion in a 3-phased current.

Mathematically, the 7^{th} order harmonic can be expressed as:

$$i_{a7} = I_7 \cdot \sin 7 \cdot \omega t \tag{3.54}$$

$$i_{b7} = I_7 \cdot \sin 7(\omega t - \frac{2\pi}{3}) = I_7 \cdot \sin(7\omega t - \frac{2\pi}{3}) \tag{3.55}$$

$$i_{c7} = I_7 \cdot \sin 7(\omega t + \frac{2\pi}{3}) = I_7 \cdot \sin(7\omega t + \frac{2\pi}{3}) \tag{3.56}$$

Unlike the 5^{th}, the 7^{th} harmonic follows the fundamental component and rotates with the positive sequence currents. Positive sequence harmonics are commonly associated with increase in temperature, resulting in overheating problems.

Moving forward, the aim is to compensate only for the 5^{th} and 7^{th} harmonics.

The compensation method, as described in [18], implies speeding up the error between reference and measured $\alpha\beta$ currents, using $dq0$ transformation, in order to reach the desired harmonic frequency. For this, the same θ provided by the PLL is used. Once this is achieved, the resulting dq components are controlled to 0 using a free integrator with manually adjusted gain. A free integrator is enough in this case, as the P component for steady state stability is inherited from the current controller via the measured currents.

The detailed control scheme can be seen in figure 3.38

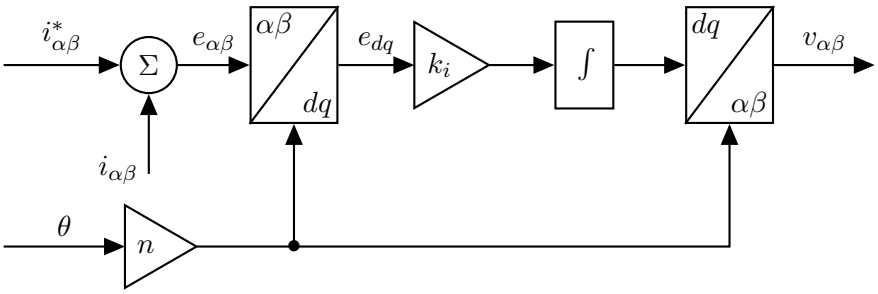

Figure 3.38: Block diagram for harmonic compensation implementation.

where, $i^*_{\alpha\beta}$ is the reference current in $\alpha\beta$, $i_{\alpha\beta}$, the measured $\alpha\beta$ current, k_i is the integrator gain, and will have different manually tuned values for each of the harmonics and n represents the order of the harmonic and is used to increase the signal frequency to match the expected harmonic. As showed in section 3.3.3, the 5^{th} harmonic exists on the negative current sequence, therefore, in this case the n gain will also feature a " $-$ " sign to account for the reversed rotation taking place. Having said this, for this project's purpose, $n \in \{-5, 7\}$. After each compensation, the output signal will be added to the output of the current control loop described in section 3.2.3.

This simulations are used to prove the compensation strategy is working. As the harmonics are also manually created, the exact harmonic values are not relevant. The parameters for the simulation are:

- $i^*_d = 8A$ and $i^*_q = 0A$ - reference dq currents;

- 15% distortion will be applied for each type of harmonic;

- The current control strategy is tuned with $k_p = 11.94$ and $k_i = 31.42$.

Figures 3.39, 3.42 and 3.45 show the compensation strategy taking place. Top plots show the desired sinusoidal shaped current while the bottom ones present an overlap of the distorted signal, polluted with harmonics and the same signal after the previously described control scheme is turned on and properly tuned.

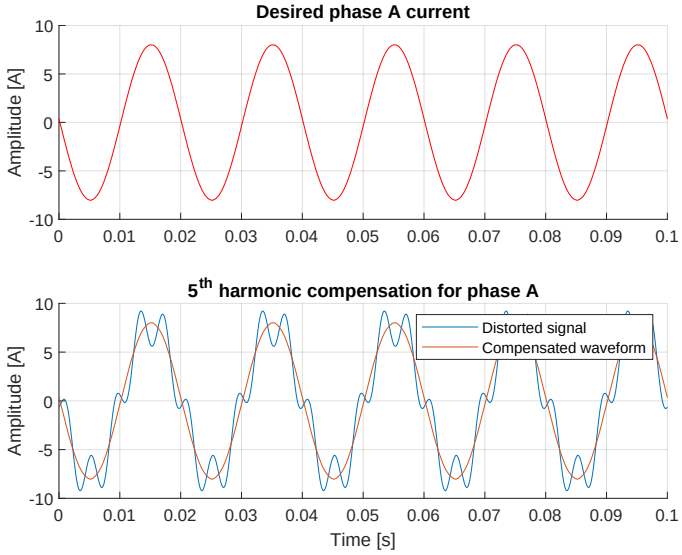

Figure 3.39: 5^{th} harmonic compensation in phase A of the grid.

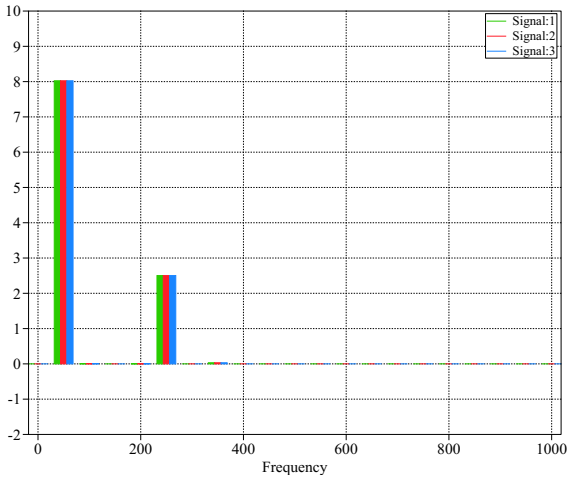

Figure 3.40: 5^{th} order harmonic Fourier spectrum of 3-phased grid current before harmonic compensation

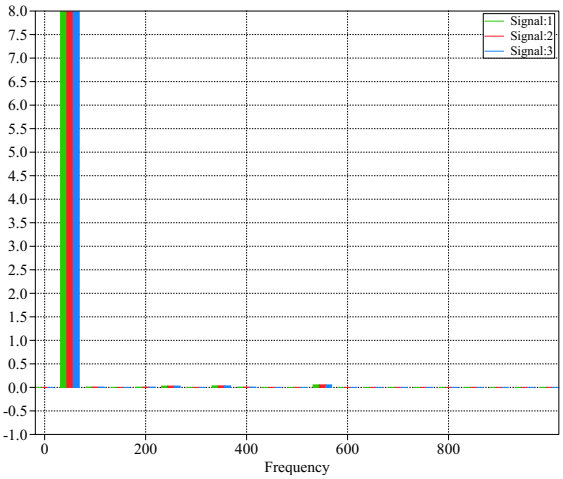

Figure 3.41: 5^{th} order harmonic Fourier spectrum of 3-phased grid current after harmonic compensation

Figures (3.40, 3.41) and (3.43, 3.44) show the respective Fourier spectrum for the grid current under 5^{th} and 7^{th} order harmonics, before and after the compensation.

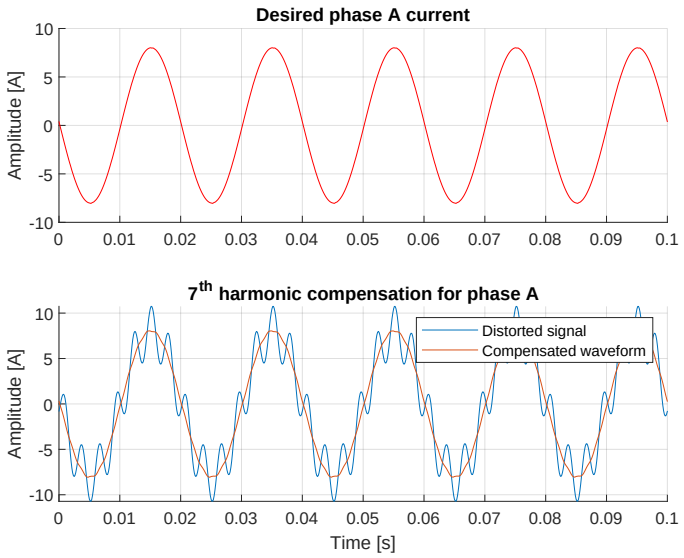

Figure 3.42: 7^{th} harmonic compensation in phase A of the grid.

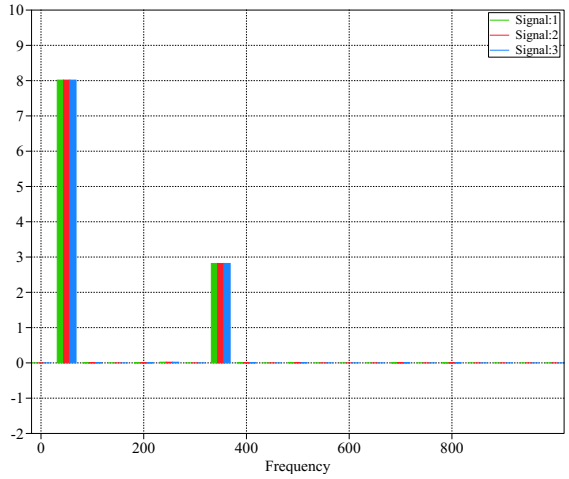

Figure 3.43: 7^{th} order harmonic Fourier spectrum of 3-phased grid current before harmonic compensation

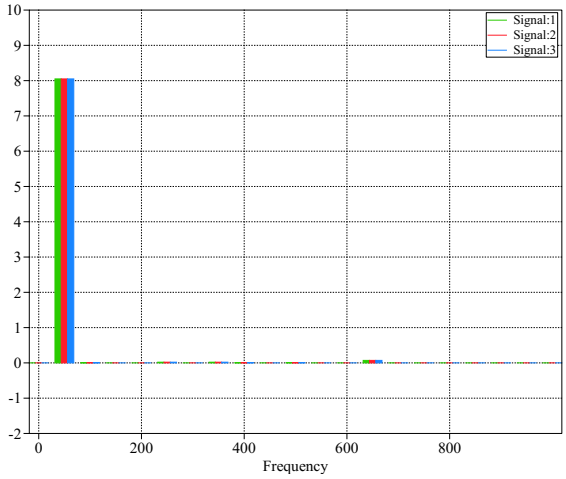

Figure 3.44: 7^{th} order harmonic Fourier spectrum of 3-phased grid current after harmonic compensation

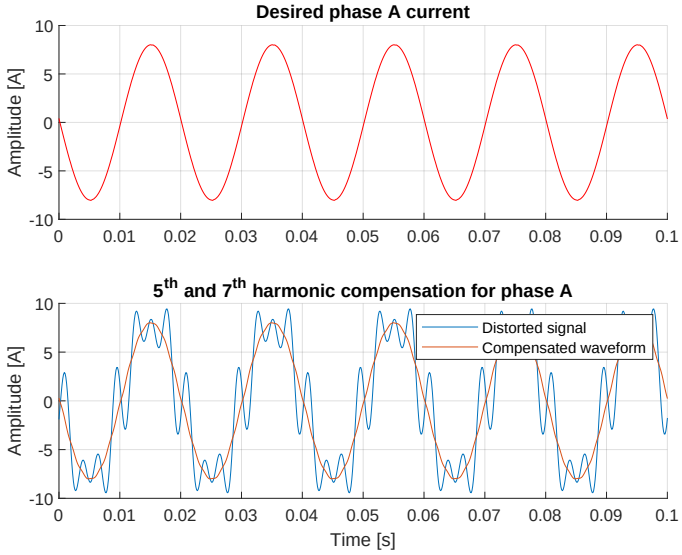

Figure 3.45: 5^{th} and 7^{th} harmonic compensation in phase A of the grid.

3.4 Reactive Power Compensation

Besides the harmonic compensation another aspect can be added to the grid connected converter for the purpose of supporting grid stability. Reactive power can be used to affect the voltage supplied from the grid, in order to maintain the stated grid requirements. By absorbing or injecting reactive power into the grid the amplitude of the grid voltage will vary, hence the reactive power compensation is also known as voltage support.

3.4.1 Purpose

The main purpose of reactive power is voltage regulation. Usually grid codes demand no more than $\pm 10\%$ variation in the nominal voltage amplitude provided[25]. Violating the grid codes might lead to malfunction of equipment connected to the grid or even outage, hence why it is necessary to preserve the grid codes stated.

If the grid is heavily loaded the voltage starts to drop. The load slows down the synchronous generators connected to the grid, i.e the frequency drops. Since the voltage generated from the generators is proportional to the frequency the voltage starts to drop. The voltage drop can be compensated by increasing the capacitive behaviour of the system. By increasing the reactive power the current will start to lead the voltage, which in turn will increase the voltage. On the other hand, a light loaded grid can give rise to a voltage, which can be lowered by decreasing the reactive power with an inductive behaviour.

By increasing the reactive power the RMS current will rise, which increases the active power loss of the system. Additionally the reactive power provided limits the amount of active power accessible. The amount of reactive power provided to the grid can be limited by putting restrictions on the power factor, which is a quality measure of the power. Grid

operators have different criteria to fulfill dependent on the configuration connected to grid. A common practice is to allow a power factor of 0.95 or above [25]. The desired power factor is dictated by the power factor set point, figure 3.46 show a power factor set point at 0.95. The axes combine two pieces of information for visualization purposes....

The shaded area is the operating area, which indicates the required reactive power supply for different active power levels. Figure 3.46 is based on power generating plants up to 125 kW and voltage level $\leq$ 1 kV, hence is the generator sign convention applied in this figure.

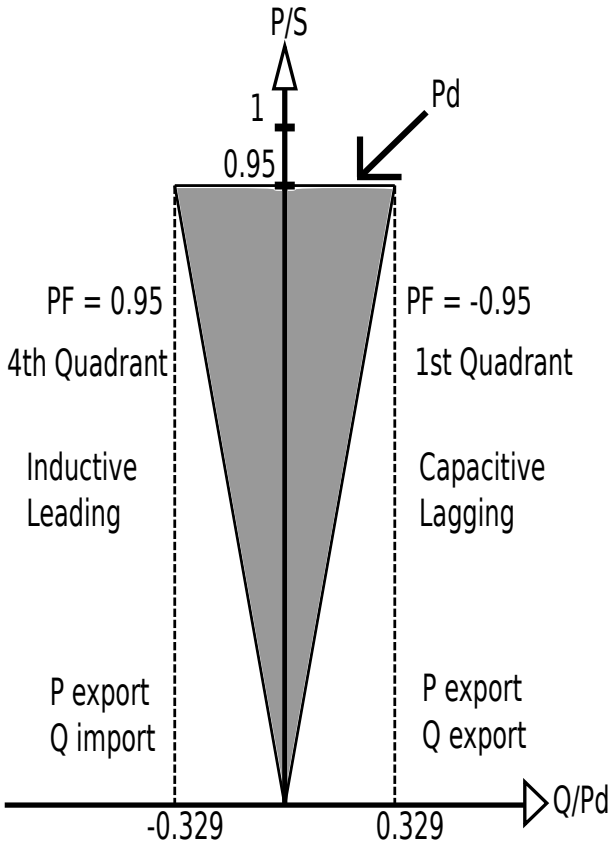

Figure 3.46: Reactive power requirements for different active power levels [25]

Pd is the maximum active power possible to supply while also supplying nominal reactive power. Moreover, Figure 3.46 is illustrating a specified power factor set point at 0.95. That can vary dependent on the demand for voltage support. The demand for voltage support is dependent on the grid characterisation and is a function of several factors such as location, generator output and load. The short circuit power level is measure of the strength of the grid at a particular point. A weak grid is more likely to have bigger voltage variations compared to a strong grid.

The reactive power is changed by adjusting the q component current reference, while the active power is controlled by the corresponding d component. Several method can be applied for voltage support, which all differ in advantages and disadvantages. The focus for this project is on the ΔU - Q compensation, which now will be presented.

3.4.2 ΔU - Q Compensation

Tracking of the voltage deviation compared to the voltage set point is one of the strategies to perform the reactive power and grid voltage control[26]. The reactive power is generated using reverse droop control, which is defined as given in Equation 3.57.[27]

$$Q^* = \frac{1}{n_r}(U^* - U_g) = k_Q(U^* - U_g) \tag{3.57}$$

where U_g is the amplitude of the grid side voltage, U^* is the amplitude of the set point value, Q^* is the reactive power reference, n_r is the reverse droop parameter and k_Q is the inverse of n_r. The reverse droop parameter is defined from the maximum allowable voltage deviation, ΔU, and maximum reactive power, Q_{max} as shown in Equation 3.58.[27]

$$n_r = \frac{\Delta U_{dev}}{Q_{max}} \tag{3.58}$$

The nominal voltage amplitude in RMS is 230V, which with ±10% variation gives a maximum allowable voltage deviation of 10%. Since the active power is restricted to 4kW, which is equal to 1315kVAr of reactive power with power factor limitation of 0.95. Hence, the reverse droop parameter is equal to 0.0076, which inverse value corresponds to 132. The characteristics of droop control are shown in Figure 3.47.

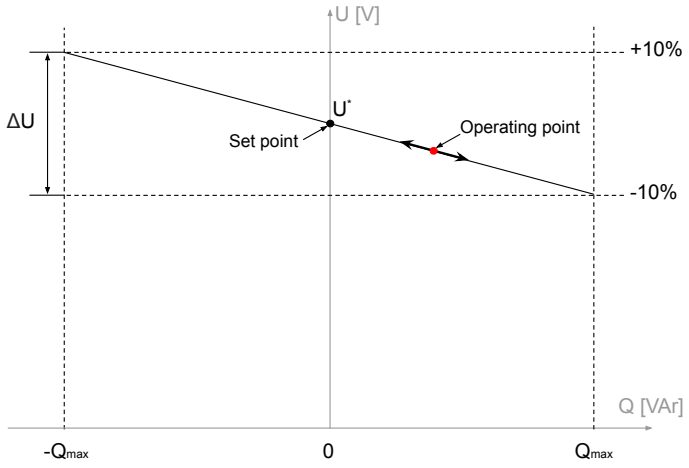

Figure 3.47: Droop control Characteristics.

An outer control loop is added to control the active and reactive power. The power loop provides the corresponding current reference for the inner current control loop. Hence, the reactive power reference is attained from the reverse droop control, while the active power reference depends on the connected device.

3.4.3 Simulations

The simulations will be done in order to show the advantages and disadvantages of the reactive power compensation. The RMS voltage and current will be recorded, along with the reactive power. For all simulations is the nominal active power of the converter injected into the grid, which is 4kW.

Two different grid conditions will be made. One where the grid is weakened in order to pass the limit of the grid codes. Another grid configuration is made for the purpose of matching the grid in experimental results obtained in the laboratory. The grid parameters are presented in table 3.2. Moreover, each simulation will contain tests with no reactive

	Weak grid	Lab grid
R_{grid}	5 Ω	1.05 Ω
L_{grid}	22mH	2.1mH

Table 3.2: Simulated grid parameters

power compensation, one with reactive power compensation and one test with the reactive power only limited by the power factor. Q_{max} is calculated according to Equation 3.59.

$$Q_{max} = P \cdot \tan\Big(\arccos(PF)\Big) \tag{3.59}$$

Q_{max} will be similar in all cases, since the active power is 4kW and the power factor is 0.95. Using equation 3.59 calculates Q_{max} to 1315 Var.

Weak grid

Firstly the grid is weakened for the purpose of violating the restriction from the grid codes, namely the ±10% voltage deviation. Figure 3.48 shows the RMS voltage with and without compensation and with Q_{max}. The dashed line indicates the limit of grid code at +10% of the base voltage, which is 230V. Doing this test 4kW was injected into the grid, hence the rise in the RMS voltage.

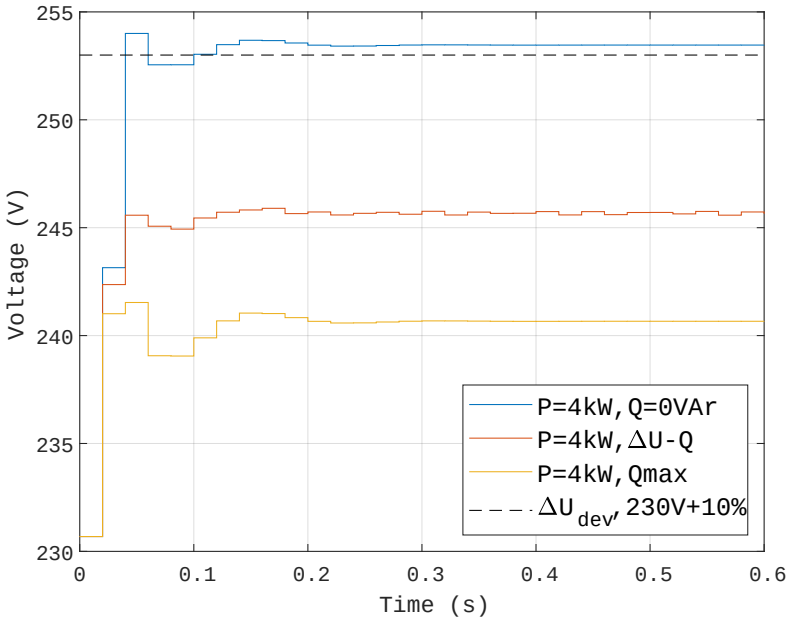

Figure 3.48: RMS voltage with 4kW active power weak grid injection with and without compensation and with Q_{max}

The compensation is based on the reversed droop parameter n_r and Q_{max} is found by decreasing n_r until Q^* reaches Q_{max} according to Equation 3.59.

As can be seen, the simulation done without compensation increases the voltage to above the demanded grid code at 253V. When the compensation is implemented the voltage is reduced to now being within the limit stated by the grid code. Obviously the voltage decreases even further when Q_{max} is implemented. However the RMS current increases as can be seen in Figure 3.49.

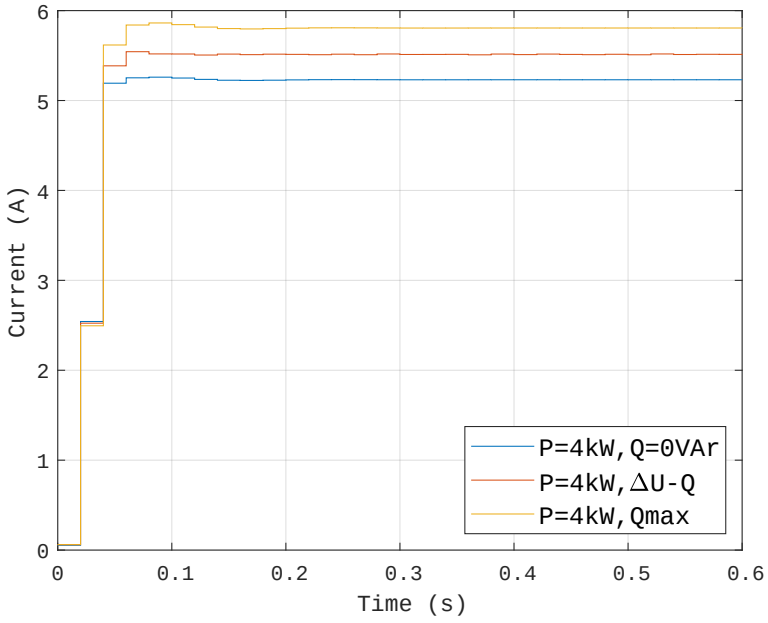

Figure 3.49: RMS current with 4kW active power weak grid injection with and without compensation and with Q_{max}

The compensation works as a compromise between the increase in the current and decrease in voltage. Figure 3.50 shows the corresponding reactive power levels from Figure 3.48 and 3.49

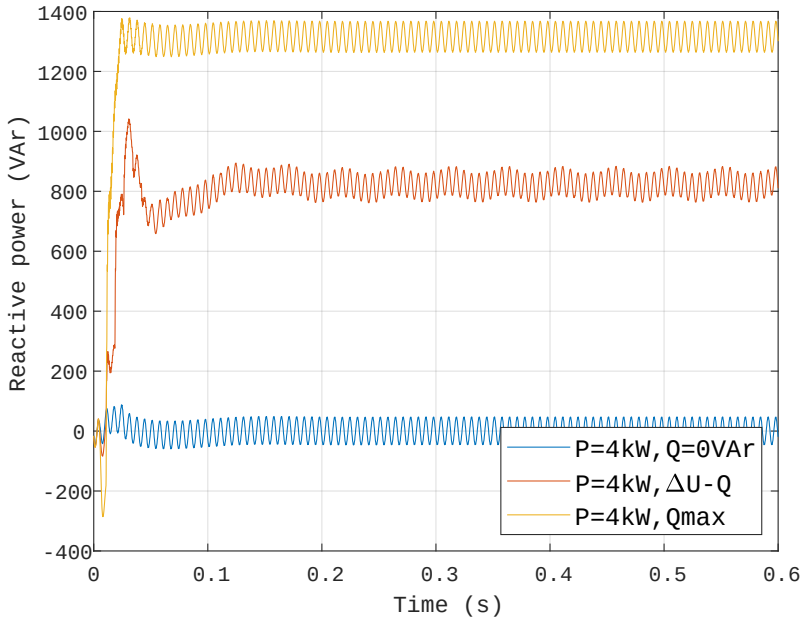

Figure 3.50: Reactive power with 4kW active power weak grid injection with and without compensation and with Q_{max}

Now simulations will be made trying to match the grid in the laboratory.

Lab grid

Table 3.2 indicates that the parameters found to test the lab grid are significantly smaller compared to the weak grid. In other words these grid parameters are less sensitive to change in voltage and current. Figure 3.51 is tested in the same manner as Figure 3.48.

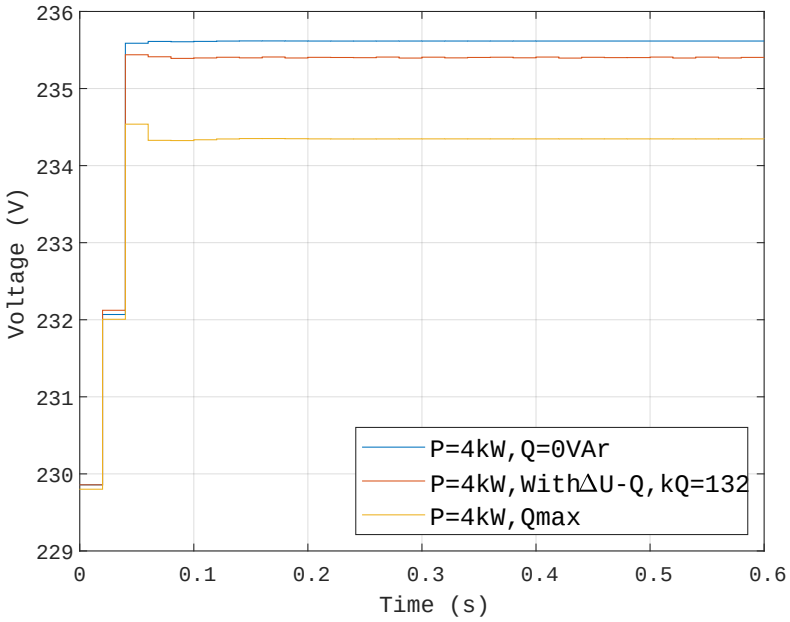

Figure 3.51: RMS voltage with 4kW active power strong grid injection with and without compensation and with Q_{max}

First of all, the voltage stays within the grid codes even without the compensation and Q_{max}. The amount of active power the converter can inject into the grid is not enough to push the voltage above the limit. However, the intention is to visualise that the compensation works. The voltage decreases when the compensation is activated, which is as expected. Figure 3.52 shows the corresponding current

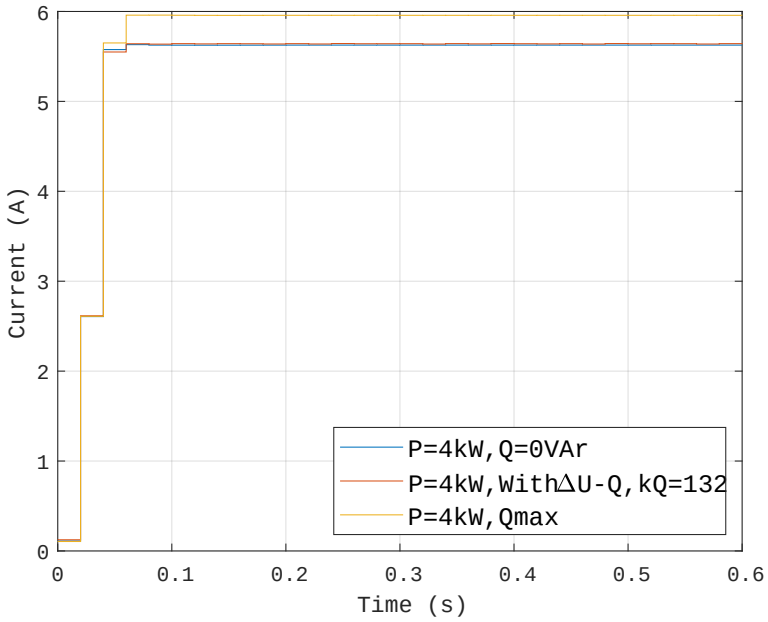

Figure 3.52: RMS current with 4kW active power strong grid injection with and without compensation and with Q_{max}

It can be seen the compensation is barely increasing the current, which also confirms that the compensation is not really effective. Q_{max} is both increasing the voltage and current. Figure 3.53 shows the reactive power injection for all three cases.

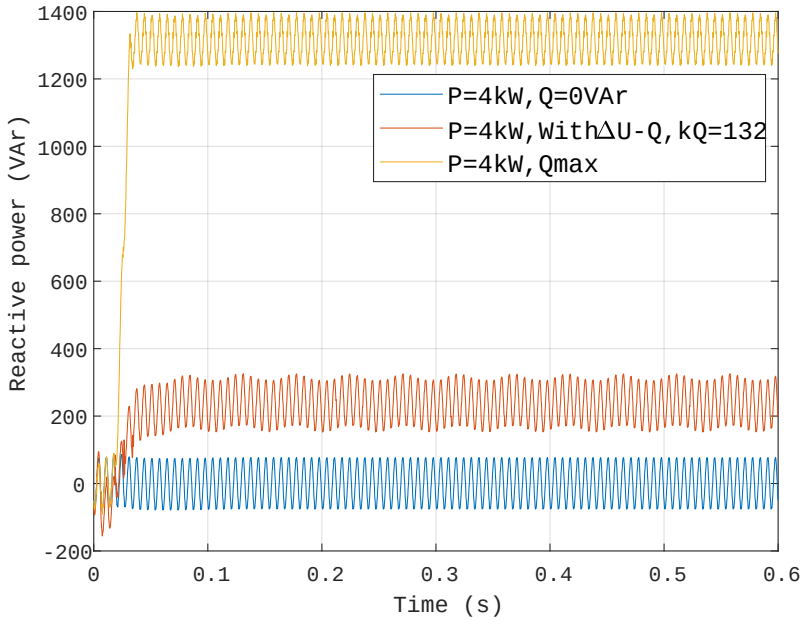

Figure 3.53: Reactive power with 4kW active power strong grid injection with and without compensation and with Q_{max}

As calculated from Equation 3.59, Q_{max} goes to 1315 VAr.

It has been proven the reactive power compensation works as intended. However, the grid available for the laboratory setup, the size of converter is not able to violate the grid codes of ±10% in voltage amplitude. Hence a weaker grid was simulated in order to pass these limits and see if the reactive power compensation pushes the voltage back with the operating range. Now the experimental results conducted in this project be presented.

Experimental Results 4

4.1 PLECS RT Box

As mentioned in Section 2.3, the PLECS RT box is used to mimic the actual grid connection as an intermediate stage between the simulation and grid connected converter. To validate the implemented control the dq-reference step response of the current is taken in the RT Box prior to moving to the physical setup.

The step response is captured from 3 to 6A and then normalized for both the d- and q-components as shown in Figure 4.1 and 4.2.

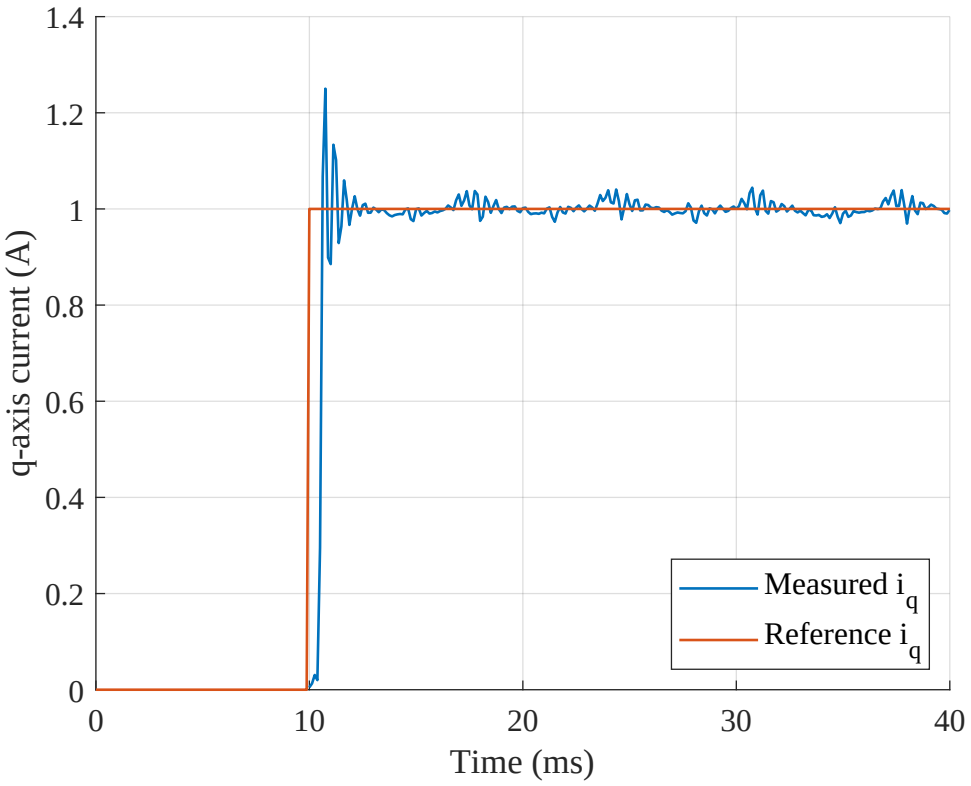

Figure 4.1: Step response of d-axis current in the PLECS RT Box.

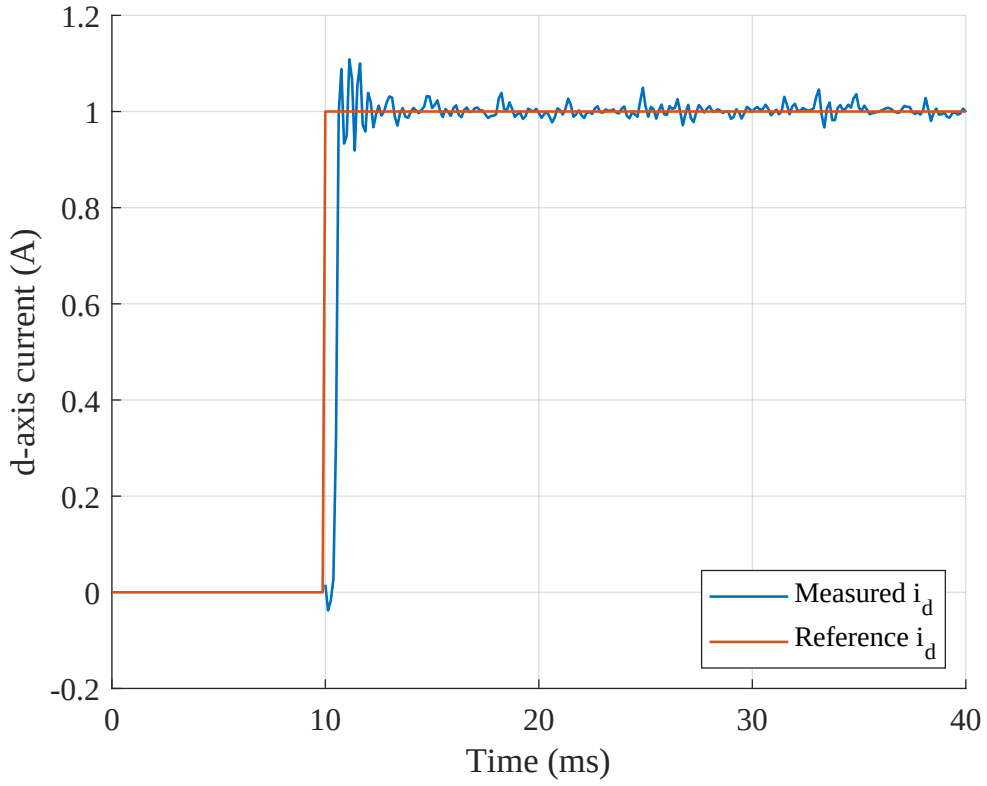

Figure 4.2: Step response of q-axis current in the PLECS RT Box.

4.2 Phase-Locked Loop

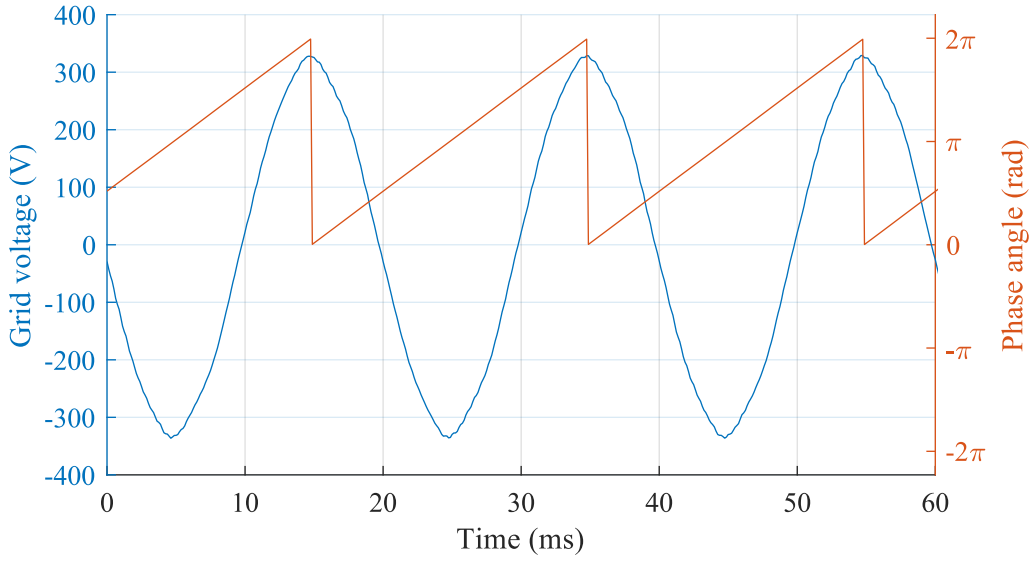

Figure 4.3: Measured phase A grid voltage and phase angle obtained through the PLL.

4.3 Current Controllers

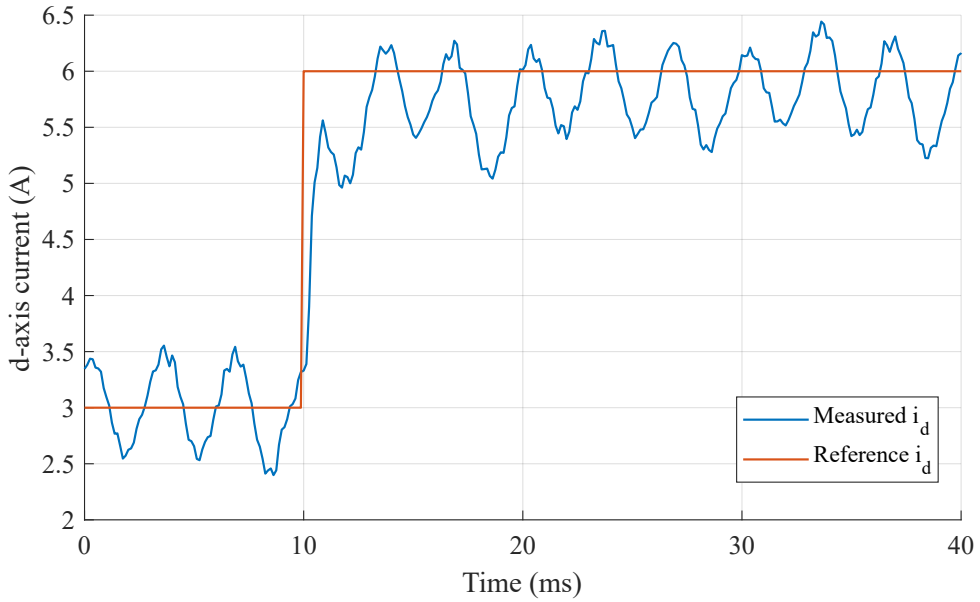

Figure 4.4: Step response of d-axis current without harmonic compensation.

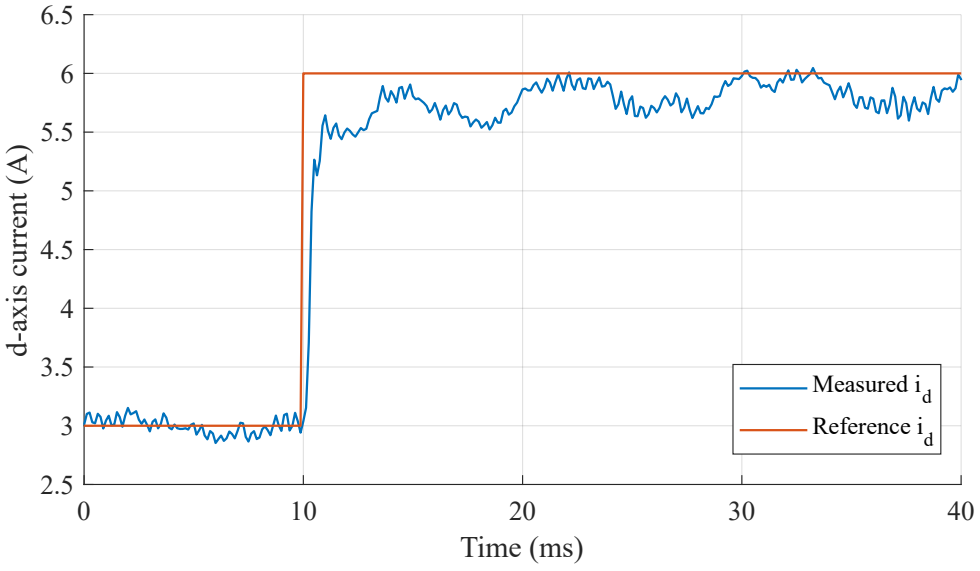

Figure 4.5: Step response of d-axis current compensating for 5th and 7th harmonics.

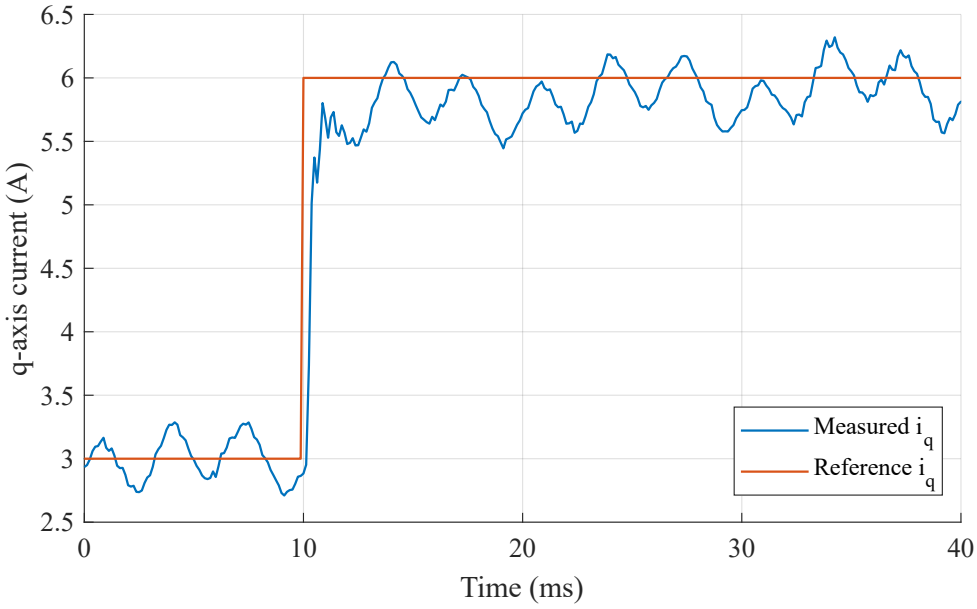

Figure 4.6: Step response of q-axis current without harmonic compensation.

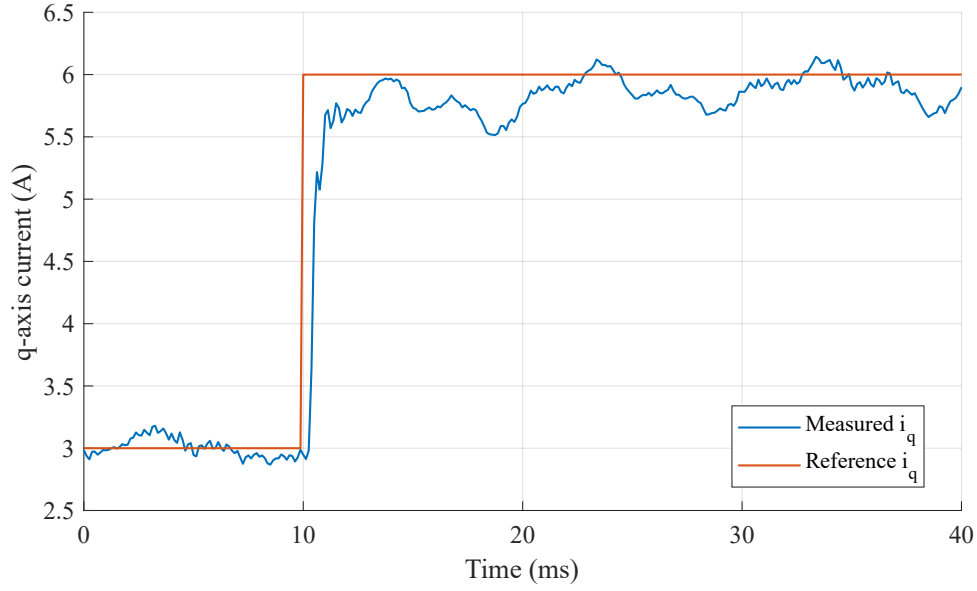

Figure 4.7: Step response of q-axis current compensating for 5th and 7th harmonics.

4.4 Harmonic Compensation

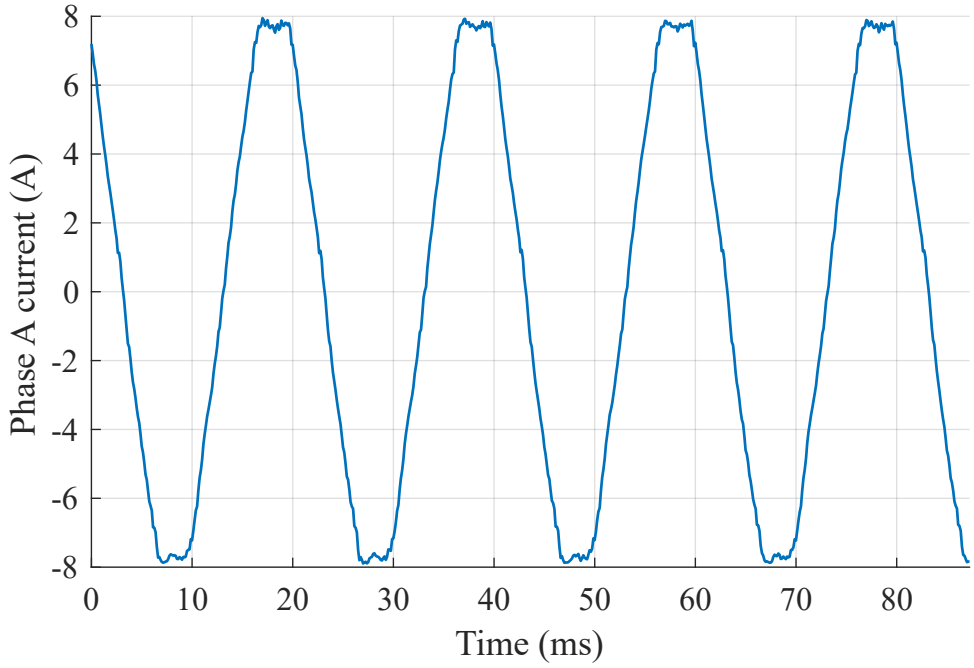

Figure 4.8: Phase A current without harmonic compensation.

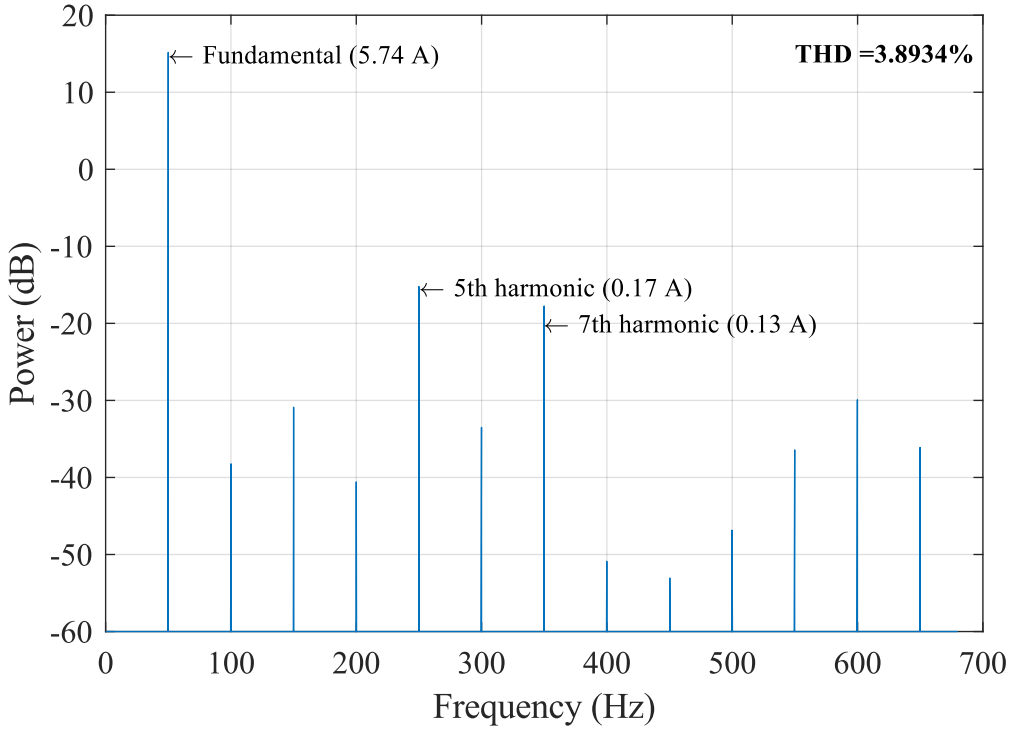

Figure 4.9: Harmonic spectrum of phase A current without harmonic compensation.

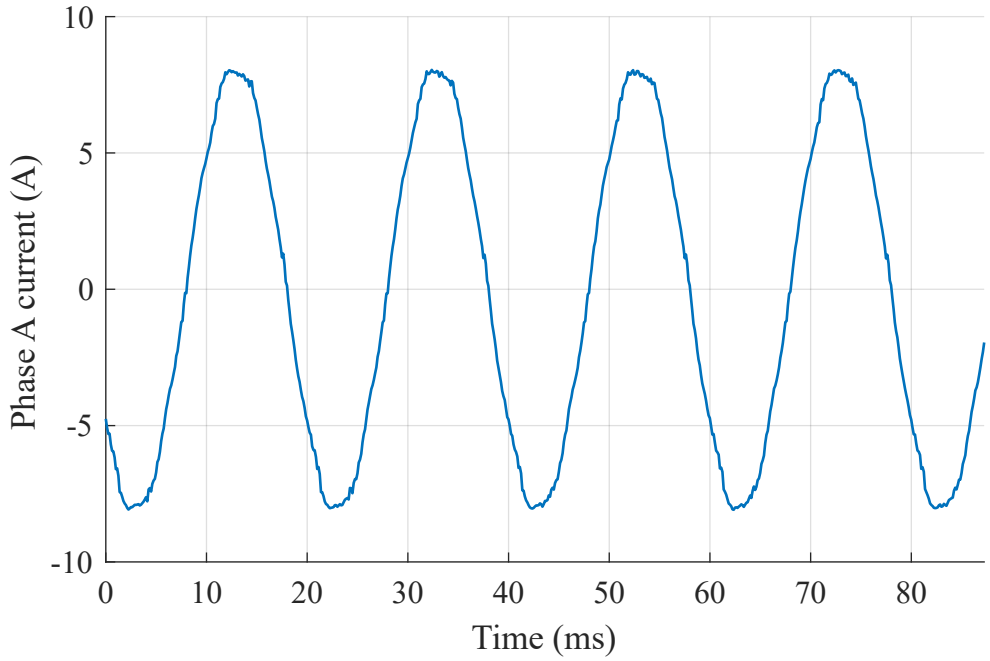

Figure 4.10: Phase A current compensating for the 5th harmonic.

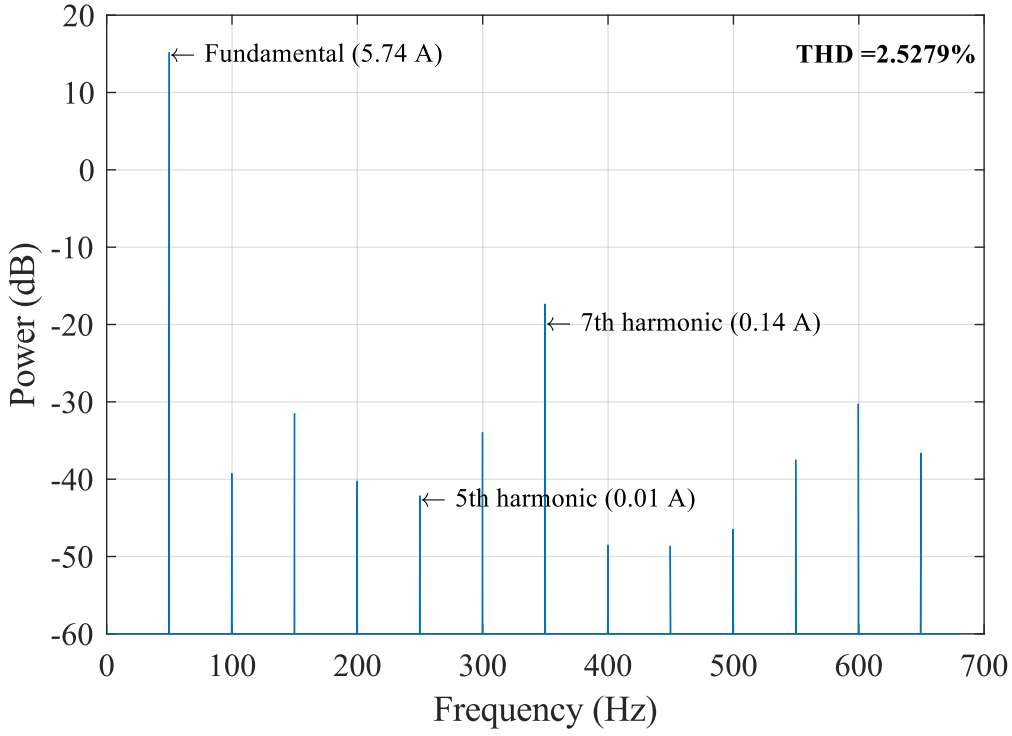

Figure 4.11: Harmonic spectrum of phase A current compensating for the 5th harmonic.

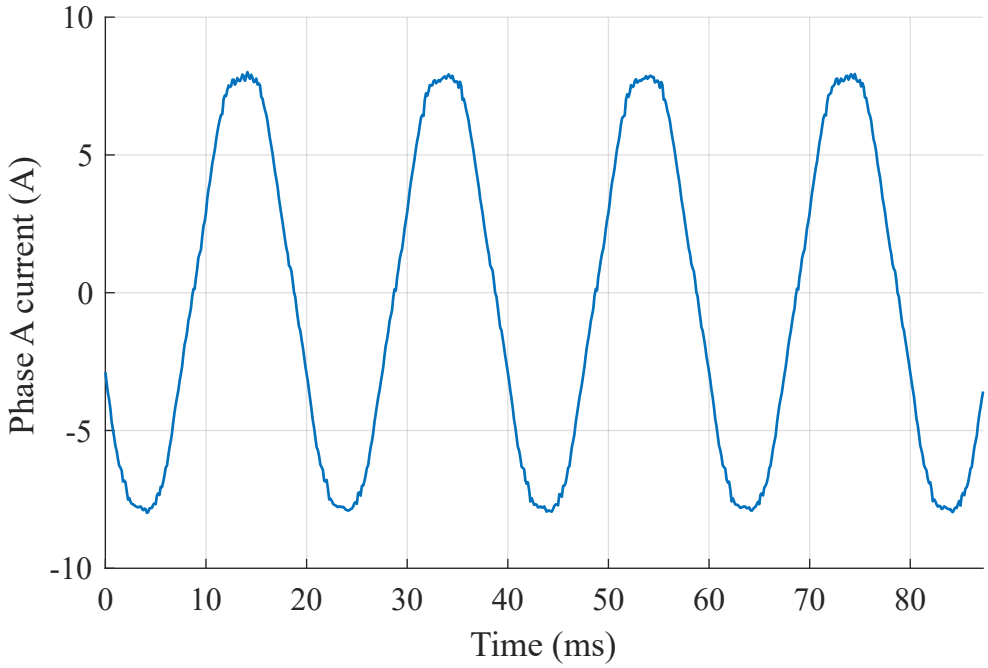

Figure 4.12: Phase A current compensating for the 7th harmonic.

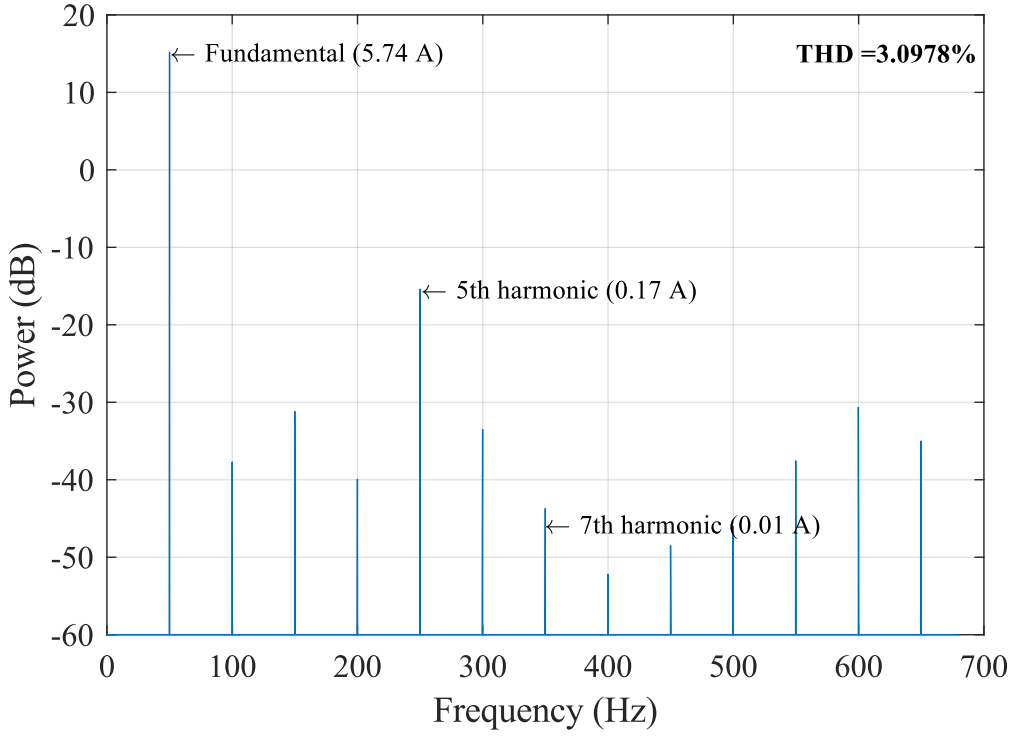

Figure 4.13: Harmonic spectrum of phase A current compensating for the 7th harmonic.

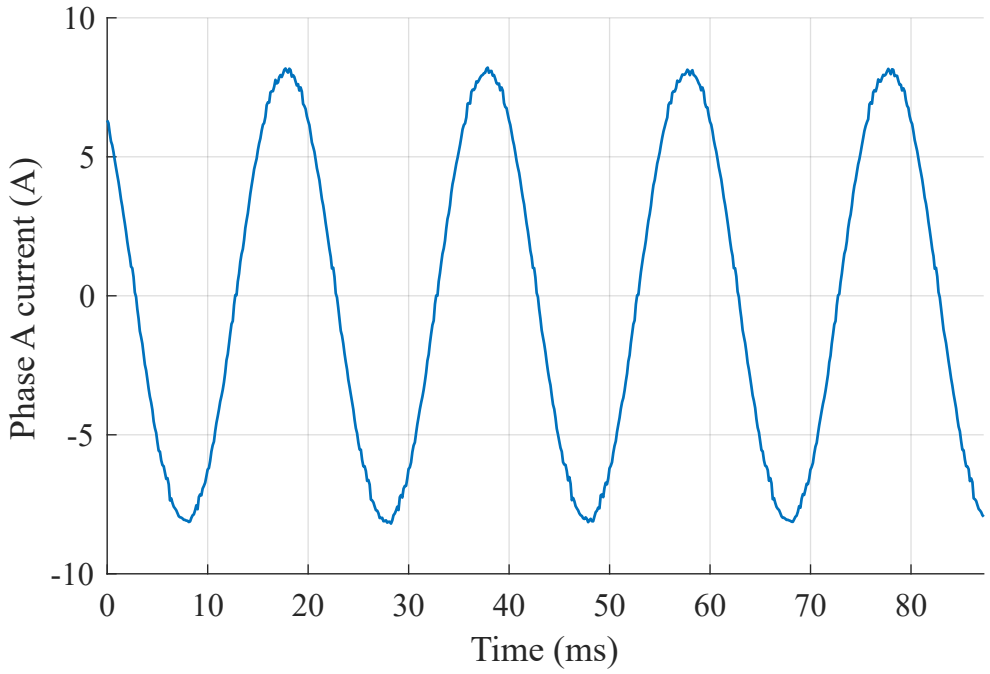

Figure 4.14: Phase A current compensating for both the 5th and 7th harmonics.

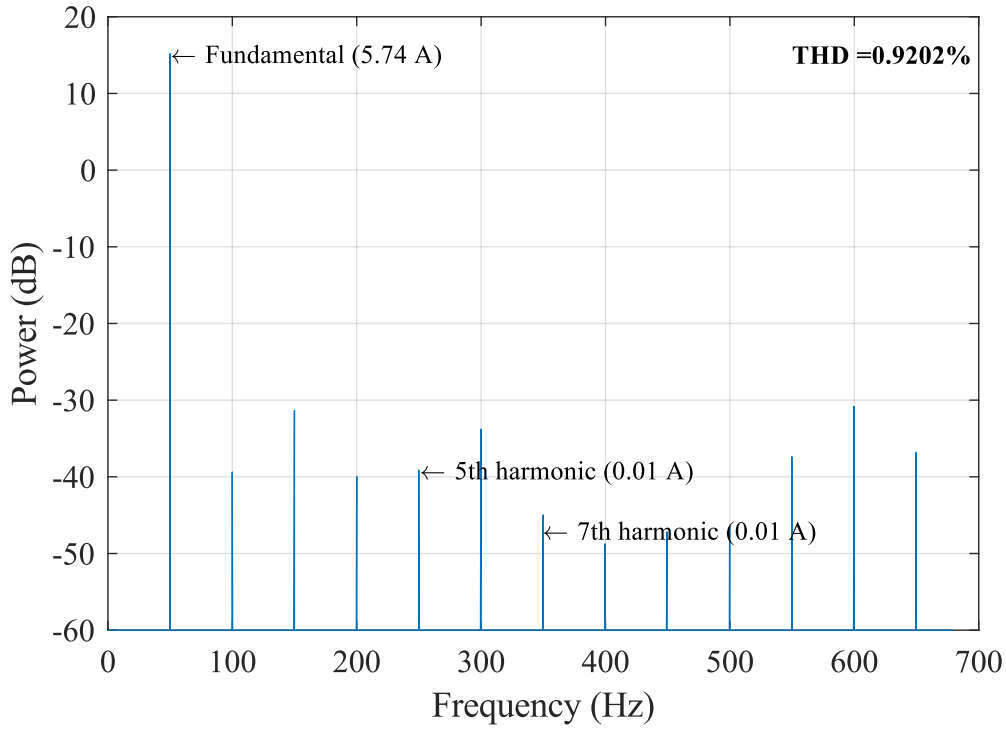

Figure 4.15: Harmonic spectrum of phase A current compensating for both the 5th and 7th harmonics.

4.5 Reactive Power Compensation

The experimental tests for the reactive power compensation were done in order to confirm the theory and simulations done in section 3.4. The converter applied for the experiment had a nominal power of 4kW. The size of the converter is not able to affect the grid with voltage deviations up to ±10%. Thus is the goal for these experiments to show the reactive power compensation is performing as expected, by decreasing the grid voltage. The base value, grid RMS voltage, recorded for all experiments is 233.05V.

Due to the strength of the grid four tests are conducted. One with reactive power compensation, one without compensation and two where the maximum amount of reactive power is injected or absorbed according to Equation 3.59.

Firstly a test was carried out without compensation. 4 kW was injected into the grid and the voltage and current waveforms was recorded. Phase A is visualized in Figure 4.16.

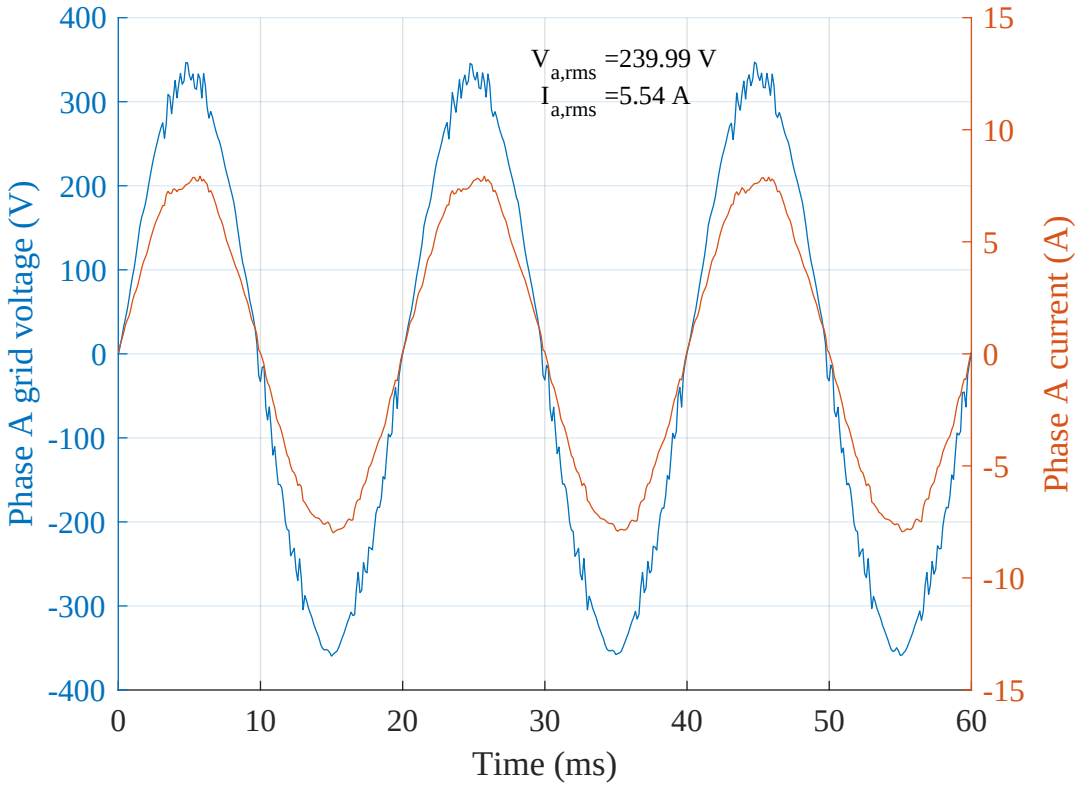

Figure 4.16: Phase A voltage and current for $P = 4\,kW$ and $Q = 0$.

The current and voltage are in phase, since the reactive power equal zero. The RMS voltage increases with approximately 7V, since the converter injects the power into the grid, the voltage rises.

The same experiment was carried out in Figure 4.17. However, now the reactive power

compensation was introduced. The reverse droop parameter n_r was calculated by Equation 3.58, in order to calculate the reactive power reference, Q^*, using Equation 3.57. Figure 4.17 show the outcome of reactive power compensation.

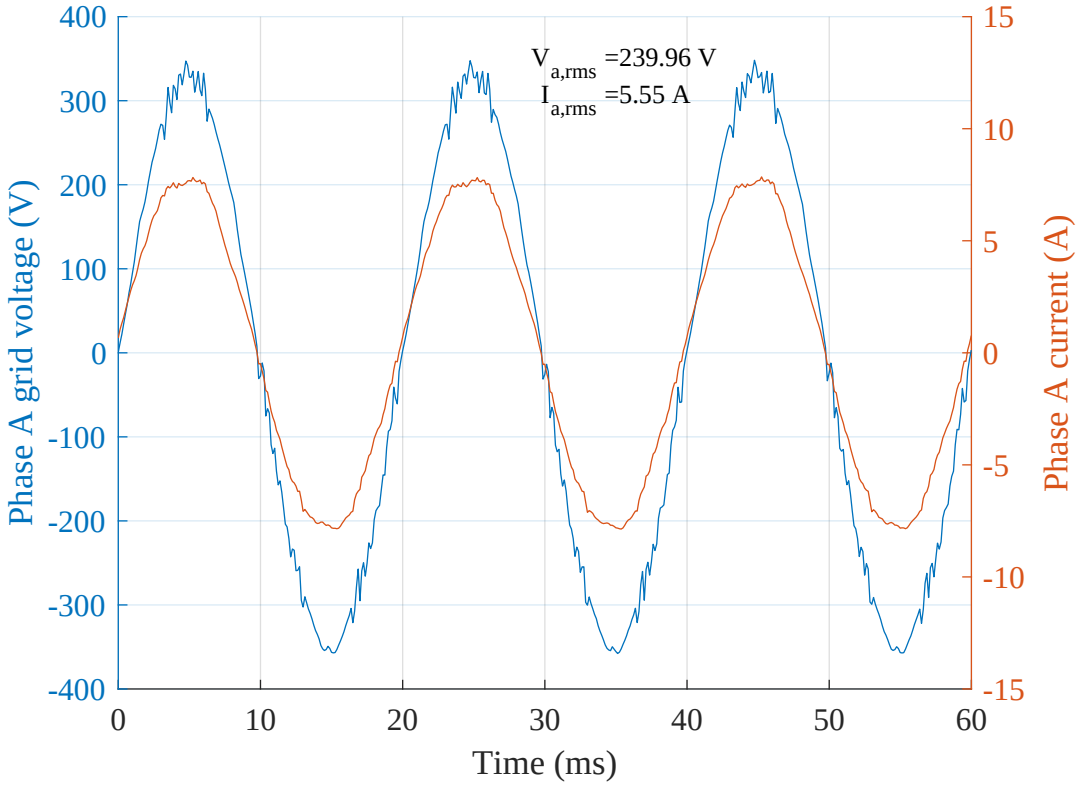

Figure 4.17: Phase A voltage and current for $P = 4\,kW$ and $Q = 1.315 kVAr$.

Compared to Figure 4.16 the voltage has decreased, while the RMS current has increased. However the compensation affect is negligible due to the strength of the grid.

Due to the minor decrease from the compensation two last test was conducted where the maximum amount of reactive power was injected and absorbed from the grid. The limitation was set accordingly to Equation 3.59. For an input of 4kW and 0.95 power factor, Q_{max} is equal to 1.315 $kVAr$. The test results are shown in Figure 4.18 and 4.19

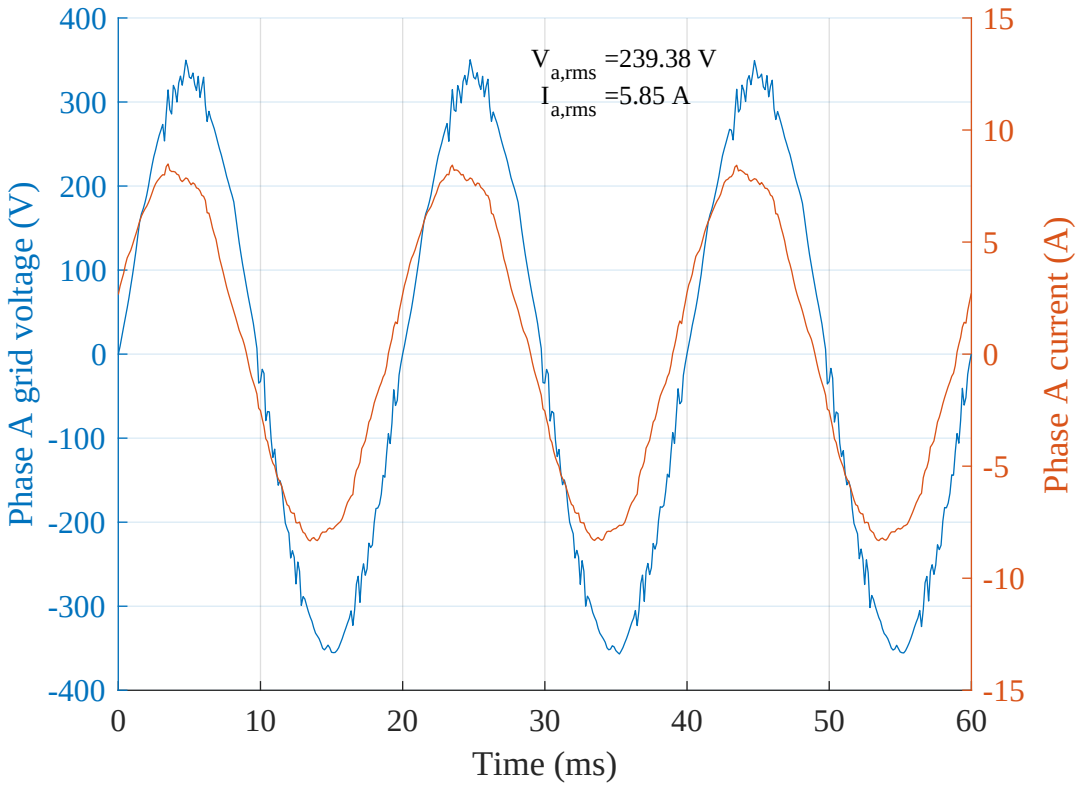

Figure 4.18: Phase A voltage and current for $P = 4\,kW$ and $Q = 1.315 kVAr$. Q injected into the grid

Figure 4.18 show the current leading the voltage, which indicate the converter is provides reactive power to the grid. Figure 4.19 indicates the reverse of Figure 4.18. The current now lag the voltage, which means the converter absorbs reactive power from the grid. As seen the outcome is a further increase in the RMS voltage.

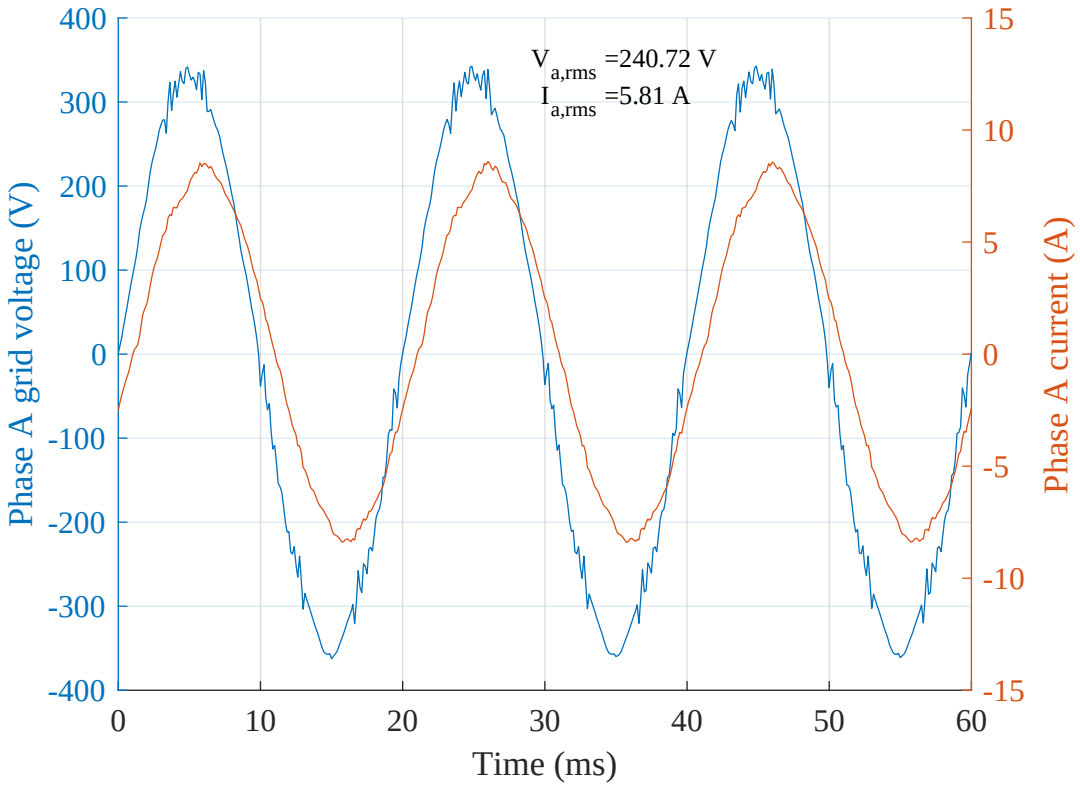

Figure 4.19: Phase A voltage and current for $P = 4\,kW$ and $Q = -1.315 kVAr$. Q absorbed from the grid

With the experimental results done the discussion for this project will take place.

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State Space Modelling A

The appendix presents the necessary state space definitions to obtain a state space model of the proposed three switch converter.

State space modelling describes linear time-invariant (LTI) dynamic system in a matrix form using differential and algebraic equations. It is a powerful method that allows repackaging of high order differential equations into first order differential equations. A continuous LTI form of state space modelling is given in Equations A.1 and A.2. [28]

$$\dot{\mathbf{x}}(t) = \mathbf{A} \cdot \mathbf{x}(t) + \mathbf{B} \cdot \mathbf{u}(t) \tag{A.1}$$

$$\mathbf{y}(t) = \mathbf{C} \cdot \mathbf{x}(t) + \mathbf{D} \cdot \mathbf{u}(t) \tag{A.2}$$

Considering nth order system with a number of inputs r and a number of outputs p, the equations consist of:

x - (n x 1) state vector
A - (n x n) system matrix
B - (n x r) input matrix
u - (r x 1) input vector (vector composed of the system input function)
y - (p x 1) output vector (vector composed of the defined outputs)
C - (p x n) output matrix
D - (p x r) matrix representing the direct coupling between the input and output

The derivative $\dot{\mathbf{x}}(t)$ describes how the state vector changes as a function of state vector $\mathbf{x}(t)$ and input vector $\mathbf{u}(t)$. The matrices **A**, **B**, **C** and **D** are linear combinations of state and input vectors.

When using a state-space model to simulate a physical system, the goal is then to find the rate of change of the state vector, $\dot{\mathbf{x}}(\mathbf{t})$. By updating the state values according to the obtained derivatives, the model can be run iteratively to reflect the behavior of the modelled system during a given time. Thus, the solution of the state equations can be analytically derived. The first step is to restate equation A.1 using its Laplace transform:

$$\mathcal{L}\{\dot{\mathbf{x}}(t)\} = \mathcal{L}\{\mathbf{A} \cdot \mathbf{x}(t) + \mathbf{B} \cdot \mathbf{u}(t)\} \tag{A.3}$$

$$s\mathbf{X}(s) - \mathbf{x}(0) = \mathbf{A}\mathbf{X}(s) + \mathbf{B}\mathbf{U}(s) \tag{A.4}$$

$$\mathbf{X}(s) = \frac{\mathbf{x}(0)}{s - \mathbf{A}} + \frac{\mathbf{B}\mathbf{U}(s)}{s - \mathbf{A}} \tag{A.5}$$

The inverse Laplace transform of $\mathbf{X}(s)$ can then be found in terms of inputs and initial

state values. For the initial value term this transform is straightforward:

$$\mathcal{L}^{-1}\Big\{\frac{\mathbf{x}(0)}{s-\mathbf{A}}\Big\} = \mathbf{x}(0)\mathcal{L}^{-1}\Big\{\frac{1}{s-\mathbf{A}}\Big\} = \mathbf{X}(0)e^{\mathbf{A}t} \tag{A.6}$$

For the input term, the inverse Laplace transform can be derived as such:

$$\mathcal{L}^{-1}\{F(s)G(s)\} = \int_0^t f(t-\tau)g(\tau)d\tau;\ F(s) = \frac{\mathbf{B}}{s-\mathbf{A}},\ G(s) = \mathbf{U}(s) \tag{A.7}$$

$$\mathcal{L}^{-1}\Big\{\frac{\mathbf{B}\mathbf{U}(s)}{s-\mathbf{A}}\Big\} = \int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{A.8}$$

Therefore, the general solution to a set of linear state-space equations can be found to be:

$$\mathbf{x}(t) = \mathcal{L}^{-1}\{\mathbf{X}(s)\} = e^{\mathbf{A}t}\mathbf{x}(0) + e^{\mathbf{A}t}\int_0^t e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{A.9}$$

The state-space system of equations described in equations A.1 and A.2, the solution of which has been described above, is a continuous time system. For most practical purposes, however, it is common to discretize state-space models, simplifying the calculation of the changes of state values for every sampling instant. This is the approach used in discrete MPC schemes, such as the one presented in [1]. It is also by using discretization that Matlab/Simulink and PLECS obtain numeric solutions to state-space models when running fixed time step simulations. A discrete state-space model can be defined as:

$$\mathbf{x}((k+1)T) = \mathbf{G}(T)\mathbf{x}(kT) + \mathbf{H}(T)\mathbf{u}(kT) \tag{A.10}$$

$$\mathbf{y}(kT) = \mathbf{C}\mathbf{x}(kT) + \mathbf{D}\mathbf{u}(kT) \tag{A.11}$$

Where k is an integer value denoting the sampling instant and T is the sampling time, which will be assumed to be constant. According to this definition, the coefficient matrices $G(T)$ and $H(T)$ are both time invariant, having constant values for any particular sampling interval size. The first step to discretize the model is performed by obtaining the state equations for the sampling instants k and $k+1$, based on equation A.9. Thus:

$$\mathbf{x}((k+1)T) = e^{\mathbf{A}(k+1)T}\mathbf{x}(0) + e^{\mathbf{A}(k+1)T}\int_0^{(k+1)T} e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{A.12}$$

$$\mathbf{x}(kT) = e^{\mathbf{A}kT}\mathbf{x}(0) + e^{\mathbf{A}kT}\int_0^{kT} e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{A.13}$$

We want to find an expression for $\mathbf{x}((k+1)T)$ that does not depend on initial state values, but only on the previous sampling instant states $\mathbf{x}(kT)$. To do so, all terms of equation A.13 can be multiplied by $e^{\mathbf{A}T}$ and the equation can be solved for $e^{\mathbf{A}(k+1)T}\mathbf{x}(0)$, then substituting this term into equation A.12. This procedure then becomes:

$$e^{\mathbf{A}(k+1)T}\mathbf{x}(0) = e^{\mathbf{A}T}\mathbf{x}(kT) - e^{\mathbf{A}(k+1)T}\int_0^{kT} e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{A.14}$$

$$\mathbf{x}((k+1)T) = e^{\mathbf{A}T}\mathbf{x}(kT) + e^{\mathbf{A}(k+1)T}\left[\int_0^{(k+1)T} e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau - \int_0^{kT} e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau\right] \tag{A.15}$$

$$\mathbf{x}((k+1)T) = e^{\mathbf{A}T}\mathbf{x}(kT) + e^{\mathbf{A}(k+1)T}\int_{kT}^{(k+1)T} e^{-\mathbf{A}\tau}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{A.16}$$

As both $\mathbf{B}$ and $\mathbf{u}(kT)$ are by definition constant within a sampling interval, they can be taken out of the integral. For the next step, the term $e^{\mathbf{A}(k+1)T}$ will be taken inside the interval. Therefore, the expression becomes:

$$\mathbf{x}((k+1)T) = e^{\mathbf{A}T}\mathbf{x}(kT) + \Big[\int_{kT}^{(k+1)T} e^{\mathbf{A}[(k+1)T-\tau]}d\tau\Big]\mathbf{B}\mathbf{u}(kT),\ \tau \in [kT, (k+1)T] \quad \text{(A.17)}$$

To simplify the evaluation of the integral, let us define a new variable $\lambda = (k+1)T - \tau$, $d\lambda = -d\tau$. The integration range for λ then goes from T to 0 τ ranges from kT to $(k+1)T$. Taking into consideration the sign change associated to the $d\lambda$ term (inverting the integration interval), we now have:

$$\mathbf{x}((k+1)T) = e^{\mathbf{A}T}\mathbf{x}(kT) + \Big[\int_{0}^{T} e^{\mathbf{A}\lambda}d\lambda\Big]\mathbf{B}\mathbf{u}(kT),\ \lambda \in [0, kT] \quad \text{(A.18)}$$

And this equation has the exact same form as A.10. Therefore, the discrete state-space coefficient matrices are defined as:

$$\mathbf{G}(T) = e^{\mathbf{A}T} \quad \text{(A.19)}$$

$$\mathbf{H}(T) = \Big[\int_{0}^{T} e^{\mathbf{A}\lambda}d\lambda\Big]\mathbf{B} \quad \text{(A.20)}$$

Assuming that the matrix $\mathbf{A}$ is invertible, the integral in the expression for $\mathbf{H}(T)$ can easily be solved, by using the fact that:

$$\int \mathbf{A}e^{\mathbf{A}T}dt = e^{\mathbf{A}T} \quad \text{(A.21)}$$

Therefore:

$$\mathbf{H}(T) = \mathbf{A}^{-1}\Big[\int_{0}^{T} \mathbf{A}e^{\mathbf{A}\lambda}d\lambda\Big]\mathbf{B} = \mathbf{A}^{-1}(e^{\mathbf{A}T} - \mathbf{I})\mathbf{B} \quad \text{(A.22)}$$

With the calculated values of the coefficient matrices $\mathbf{G}(T)$ and $\mathbf{H}(T)$, equation A.10 can be directly used to update the values of the states of a model at any given time, provided that the values of both states and inputs are known for the previous sampling step.

Ćuk Converter B

The appendix presents the derived state space model for the Ćuk converter shown in Figure B.1. The Ćuk converter has a switch with two possible states, where two modes in Figure B.2 and B.3 are obtained. The circuit analysis techniques such as Kirchhoff's Current Law (KCL), Kirchhoff's Voltage Law (KVL), voltage dividers and current dividers are used to obtain the state space matrices for each state.

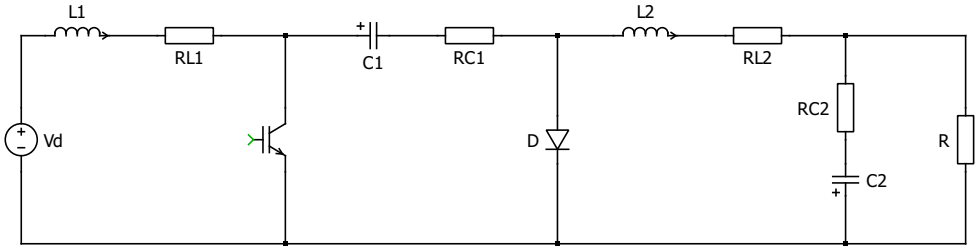


Figure B.1: Ćuk converter schematic.

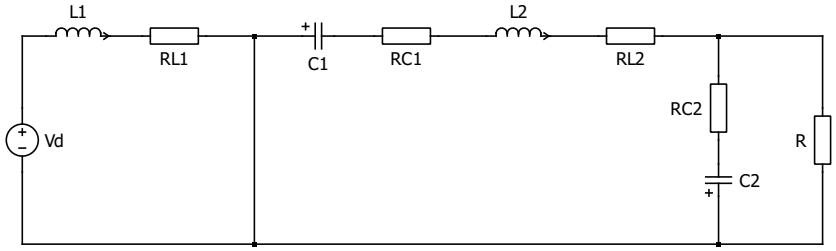


Figure B.2: Ćuk converter schematic, where the switch is conducting (ON mode).

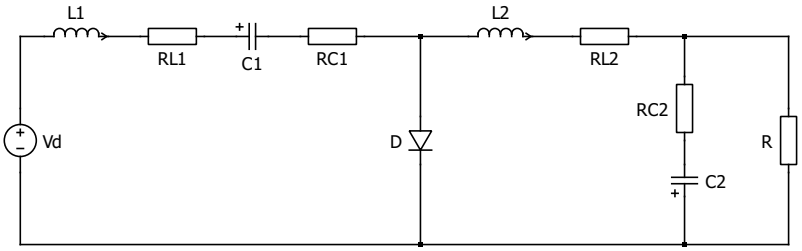


Figure B.3: Ćuk converter schematic, where the switch is not conducting (OFF mode).

The Ćuk converter have four passive storage components, which are chosen as the states of the state space model as defined in Equation B.1. The V_{dc} is defined as an input, $u = V_{dc}$

and V_{out} is defined as an output, $y = V_{out}$.

$$\mathbf{x} = \begin{bmatrix} i_{L1} & i_{L2} & v_{C1} & v_{C2} \end{bmatrix}^T \tag{B.1}$$

The derivatives of the inductor currents and capacitor voltages are found using KVL and KCL, respectively. The state derivatives in ON mode are found in Equations B.2, B.3, B.4 and B.5.

$$\frac{di_{L1}}{dt} = \frac{V_{dc}}{L_1} - \frac{r_{L1} \cdot i_{L1}}{L_1} \tag{B.2}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1}}{L_2} - \frac{(r_{C1} + r_{L2}) \cdot i_{L1}}{L_2} - \frac{R}{(R + r_{C2})L_2} V_{C2} \tag{B.3}$$

$$\frac{dv_{C1}}{dt} = -\frac{i_{L2}}{C_1} \tag{B.4}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{V_{C2}}{(R + r_{C2})L_2} \tag{B.5}$$

The state derivatives in OFF mode are found in Equations B.2, B.3, B.4 and B.5.

$$\frac{di_{L1}}{dt} = \frac{V_{dc}}{L_1} - \frac{(r_{L1} + r_{C1}) \cdot i_{L1}}{L_1} - \frac{V_{C1}}{L_1} \tag{B.6}$$

$$\frac{di_{L2}}{dt} = -\frac{r_{L2} \cdot i_{L2}}{L_2} - \frac{R}{(R + r_{C2})L_2} V_{C2} \tag{B.7}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} \tag{B.8}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{V_{C2}}{(R + r_{C2})L_2} \tag{B.9}$$

The system matrix, A, and input matrix, B, are defined for both ON and OFF modes in Equation B.10, B.11 and B.12.

$$\mathbf{A}_{ON} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{r_{C1}+r_{L2}}{L_2} & \frac{1}{L_2} & -\frac{R}{(R+r_{C2})L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{(R+r_{C2})C_2} \end{bmatrix} \tag{B.10}$$

$$\mathbf{A}_{OFF} = \begin{bmatrix} -\frac{r_{L1}+r_{C1}}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{r_{L2}}{L_2} & 0 & -\frac{R}{(R+r_{C2})L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{(R+r_{C2})C_2} \end{bmatrix} \tag{B.11}$$

$$\mathbf{B} = \mathbf{B}_{ON} = \mathbf{B}_{OFF} = \begin{bmatrix} \frac{1}{L1} & 0 & 0 & 0 \end{bmatrix}^T \tag{B.12}$$

The output matrix C is described as a linear combination of the state V_{C2} in Equation B.13.

$$\mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & \frac{R}{R+r_{L2}} \end{bmatrix} \tag{B.13}$$

The system matrices A_{ON} and A_{OFF} for ON and OFF modes can be combined into one as shown in Equation B.14 using state space averaging as a function of duty cycle of the switch.

$$\mathbf{A} = \begin{bmatrix} -D\frac{r_{L1}}{L_1} - (1-D)\frac{r_{L1}+r_{C1}}{L_1} & 0 & -(1-D)\frac{1}{L_1} & 0 \\ 0 & -\frac{r_{L2}}{L_2} - D\frac{r_{C1}}{L_2} & D\frac{1}{L_2} & -\frac{R}{(R+r_{C2})L_2} \\ (1-D)\frac{1}{C_1} & -D\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{(R+r_{C2})C_2} \end{bmatrix} \tag{B.14}$$

Equation B.14 is then reduced to the matrix shown in Equation B.15.

$$\mathbf{A} = \begin{bmatrix} -\frac{r_{L1}+(1-D)r_{C1}}{L_1} & 0 & \frac{D-1}{L_1} & 0 \\ 0 & -\frac{r_{L2}+D\cdot r_{C1}}{L_2} & \frac{D}{L_2} & -\frac{R}{(R+r_{C2})L_2} \\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{(R+r_{C2})C_2} \end{bmatrix} \tag{B.15}$$

The model derived by Ćuk in his PhD thesis [14], which does not include component parasitics, has the following state coefficient matrices (rearranging to match the order of our state vector):

$$\mathbf{A}_{ON,ideal} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \tag{B.16}$$

$$\mathbf{A}_{OFF,ideal} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \tag{B.17}$$

These matrices, shown in page 199 of Ćuk's thesis, match the ones shown in equations B.10 and B.11 once the values of all parasitic resistances are set to 0. This validates the accuracy of our modelling.

Reduced Two Switch Converter

C

The appendix presents the derived state space model for the reduced two switch converter shown in Figure C.1. Each switch of the two switch converter has two possible states, where four modes in Figure C.2 are obtained. The state space matrices are obtained using KCL and KVL..

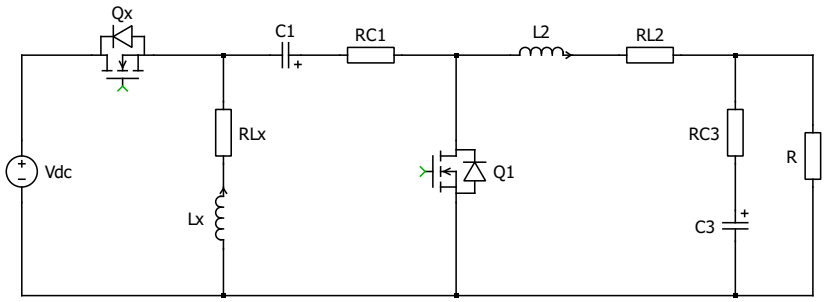
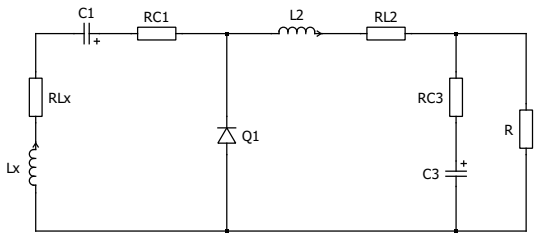
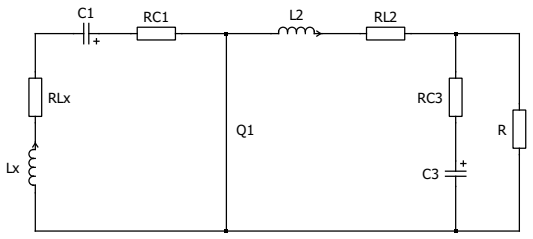


Figure C.1: Two switch converter schematic.

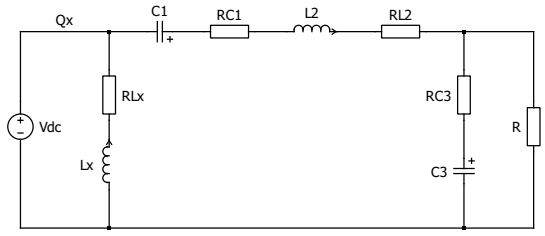
The two switch converter has four passive storage components like the Ćuk converter, which are also chosen as the states of the state space model as defined in Equation XXX.



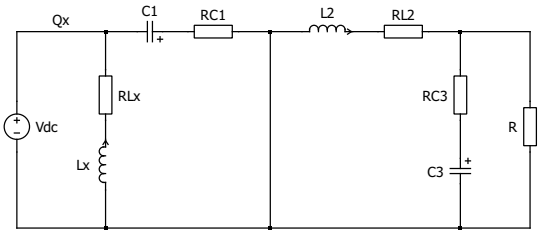
(a) Mode 1



(b) Mode 2



(c) Mode 3



(d) Mode 4

Figure C.2: Two switch converter modes

The V_{dc} is defined as an input, $u = V_{dc}$ and V_{out} is defined as an output, $y = V_{out}$.

$$\mathbf{x} = \begin{bmatrix} i_{Lx} & i_{L2} & v_{C1} & v_{C3} \end{bmatrix}^T \tag{C.1}$$

Similarly, as with Ćuk converter in Appendix B the state derivatives are obtained using KVL and KCL. The state space averaged system and input matrices, A and B, are given in Equations C.2 and C.3.

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{(1-Q_x}{C_1} & -\frac{Q_x(1-Q_1)}{C_1} \\ 0 & -\frac{1}{RC_2} & 0 & \frac{1}{C_2} \\ \frac{(Q_x-1)Q_1}{L_x} - \frac{(1-Q_x)(1-Q_1)}{L_x+L_1} & \frac{(1-Q_x)(1-Q_1)}{L_x+L_1} & 0 & 0 \\ \frac{Q_x(1-Q_1)}{L_1} - \frac{(1-Q_x)(1-Q_1)}{L_x+L_1} & \frac{Q_x+(1-Q_x)Q_1}{L_1} - \frac{(1-Q_x)(1-Q_1)}{L_x+L_1} & 0 & 0 \end{bmatrix} \tag{C.2}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 & \frac{Q_x}{L_x} & \frac{Q_x(1-Q_1)}{L_1} \end{bmatrix}^T \tag{C.3}$$

The output matrix, C, is given in Equation C.4.

$$\mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}^T \tag{C.4}$$

The Proposed Three Switch Converter

D

The appendix presents the derived state space model for the proposed three switch converter topology shown in Figure D.1. Each switch of the converter has two possible states, which corresponds to eight possible modes shown in Figure D.2, D.3, D.4, D.5, D.6, D.7, D.8 and D.9. The state space matrices are obtained using KCL and KVL.

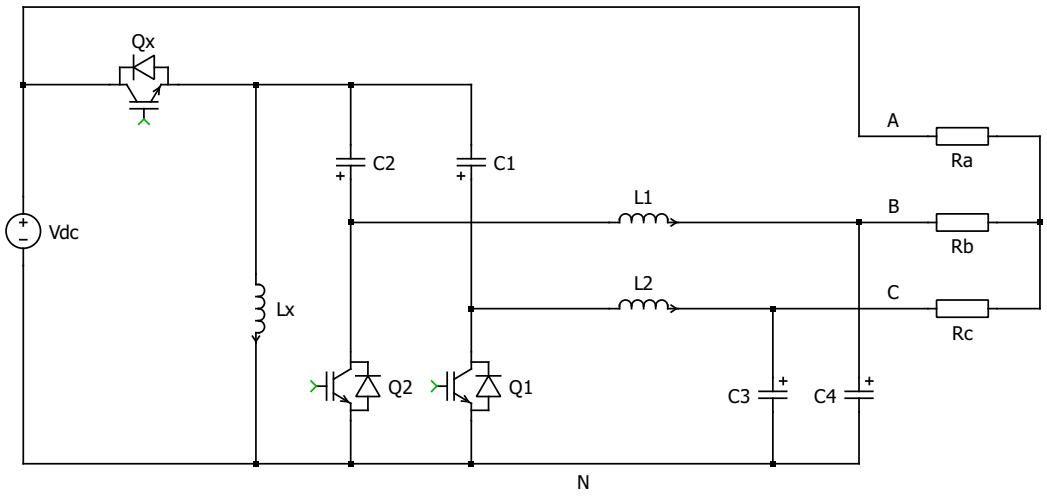


Figure D.1: Three switch converter schematic.

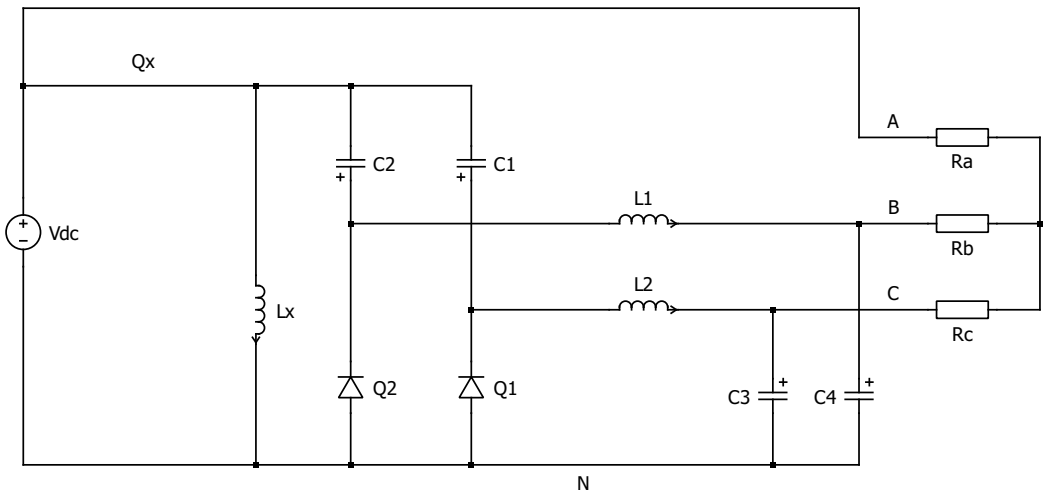


Figure D.2: Three switch converter schematic, where the switch is conducting in Mode 1.

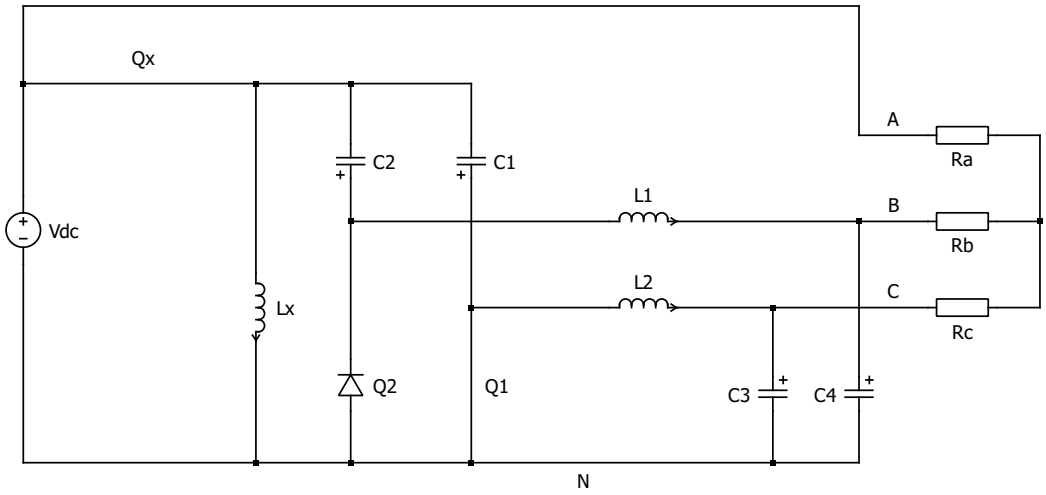


Figure D.3: Three switch converter schematic, where the switch is conducting in Mode 2.

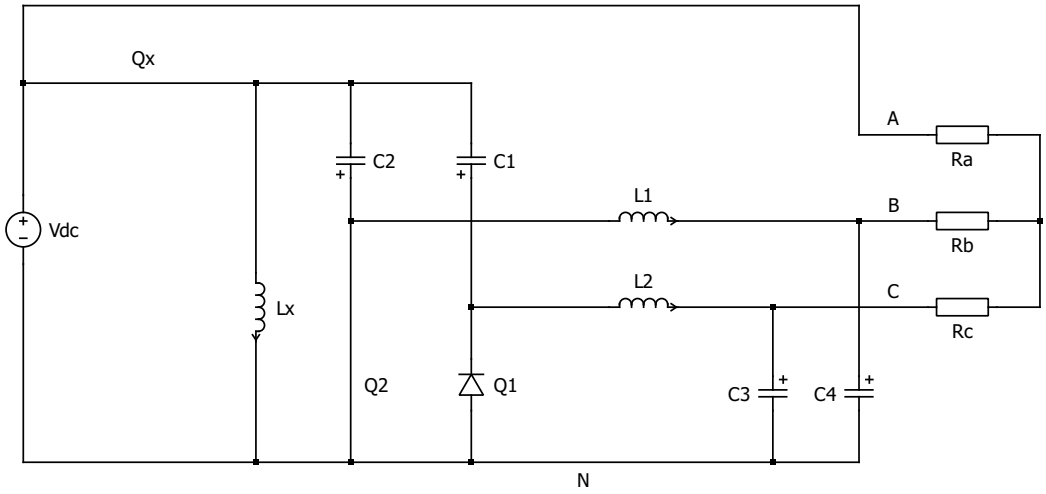


Figure D.4: Three switch converter schematic, where the switch is conducting in Mode 3.

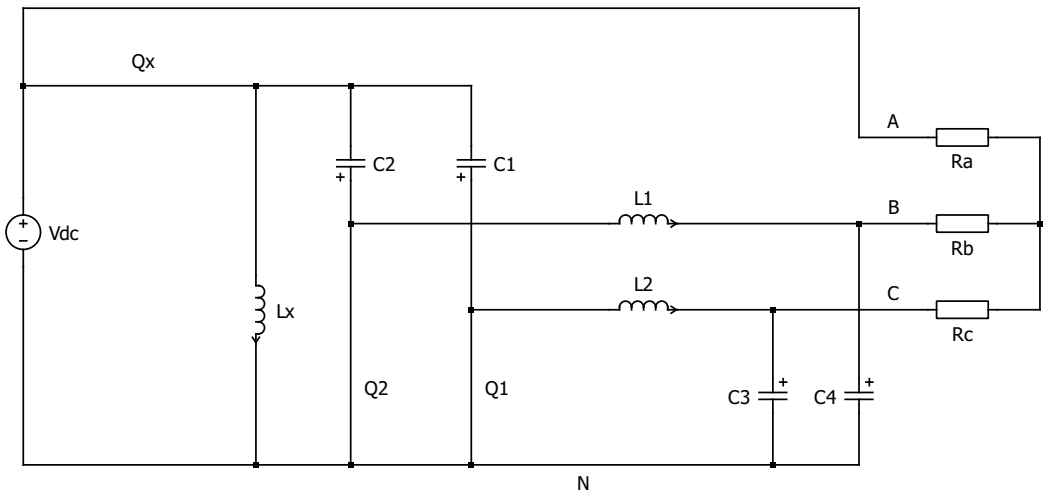


Figure D.5: Three switch converter schematic, where the switch is conducting in Mode 4.

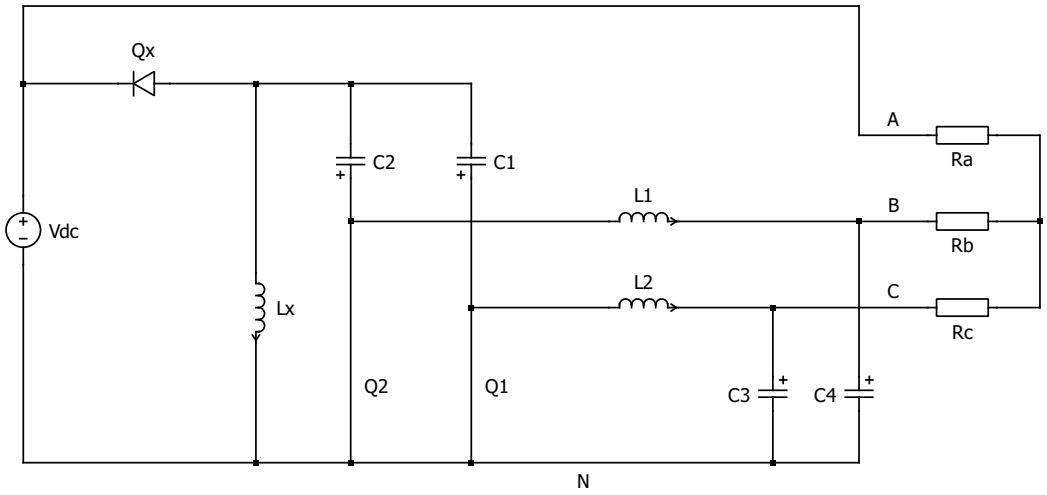


Figure D.6: Three switch converter schematic, where the switch is conducting in Mode 5.

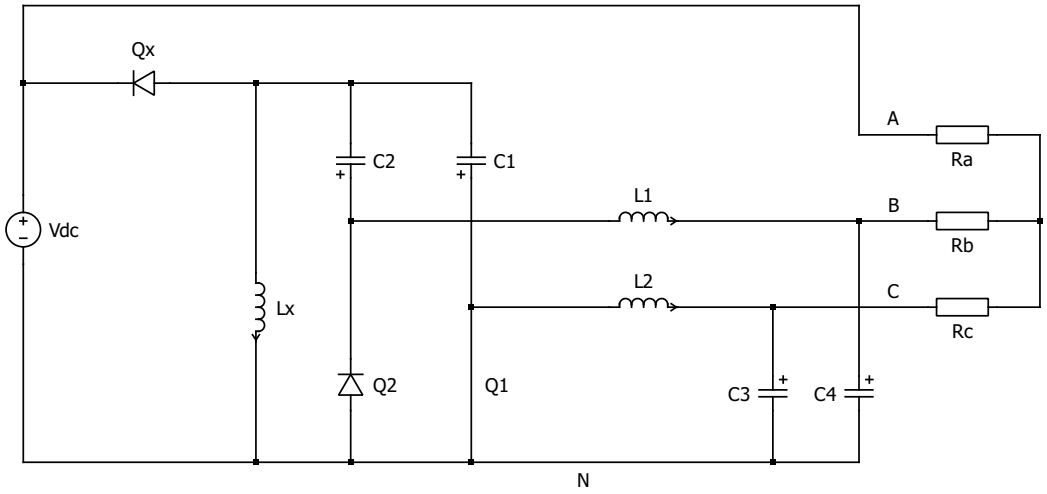


Figure D.7: Three switch converter schematic, where the switch is conducting in Mode 6.

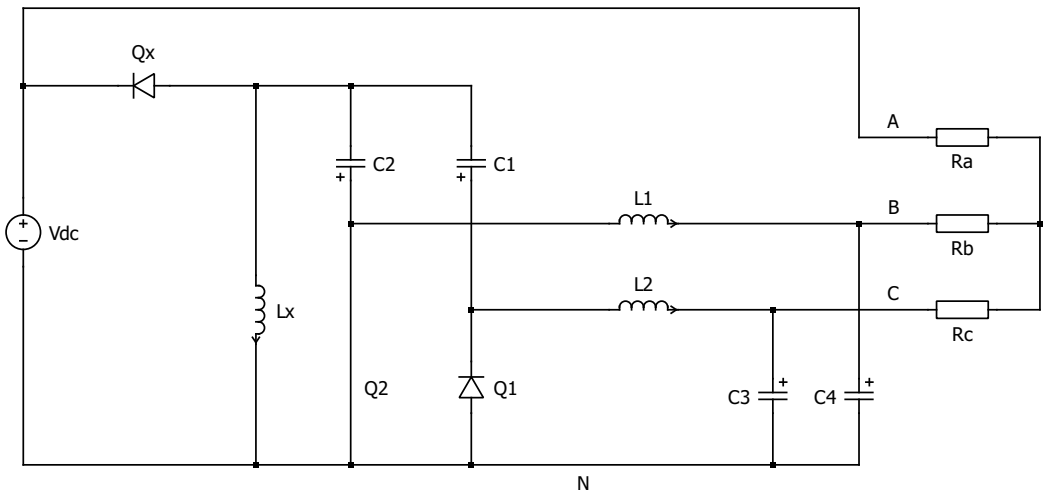


Figure D.8: Three switch converter schematic, where the switch is conducting in Mode 7.

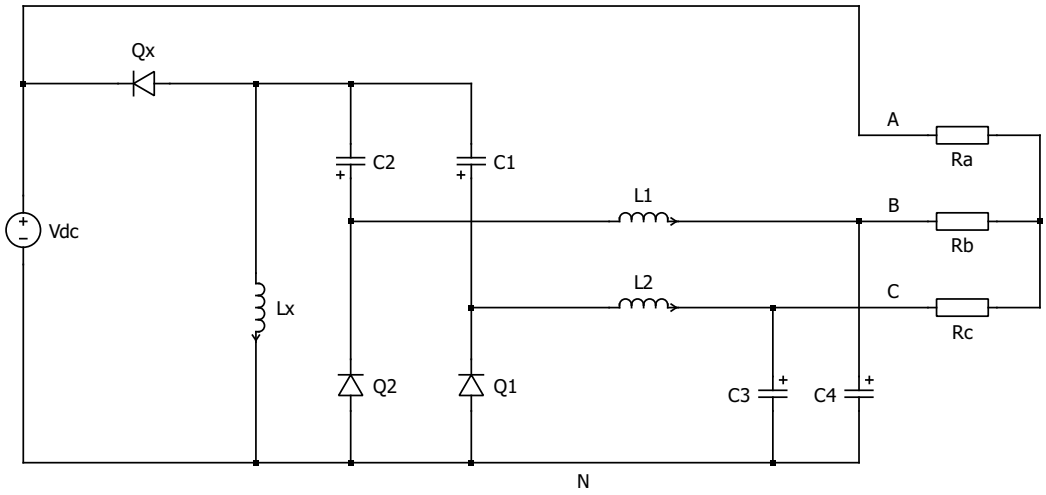


Figure D.9: Three switch converter schematic, where the switch is conducting in Mode 8.

The three switch converter has seven passive storage components that are chosen as the states for the state space model. The states are shown in Equation D.1. The V_{dc} is defined as an input, $u = V_{dc}$, and phase-to-phase voltages V_{AB}, V_{BC} and V_{CA} are defined as an output as shown in Equation D.2.

$$\mathbf{x} = \begin{bmatrix} i_{Lx} & i_{L1} & i_{L2} & v_{C1} & v_{C2} & v_{C3} & v_{C4} \end{bmatrix}^T \tag{D.1}$$

$$\mathbf{y} = \begin{bmatrix} V_{AB} & V_{BC} & V_{CA} \end{bmatrix}^T \tag{D.2}$$

The state derivatives are obtained using KVL and KCL as with the Ćuk and the two switch converters. The state space averaged system and input matrices, **A** and **B**, are given in Equations D.3 and D.4. The output and coupling matrices, **C** and **D**, are given in Equation D.5 and D.6.

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{Q_1(1-Q_x)(2-Q_2)}{2C_1} & \frac{(1-Q_x)Q_1(1-Q_2)}{C_1} & -\frac{(1-Q_1}{C_1} \\ 0 & 0 & 0 & 0 & \frac{Q_2(1-Q_x)(2-Q_1)}{2C_2} & -\frac{(1-Q_2}{C_2} & \frac{(1-Q_x)(1-Q_1)Q_2}{C_2} \\ 0 & 0 & -\frac{1}{RC_3} & 0 & 0 & 0 & \frac{1}{C_3} \\ 0 & 0 & 0 & -\frac{1}{RC_4} & 0 & \frac{1}{C_4} & 0 \\ \frac{(Q_x-1)Q_1}{L_x} & \frac{(Q_x-1)(1-Q_1)Q_2}{L_x} & 0 & 0 & 0 & 0 & 0 \\ -\frac{(1-Q_x)Q_1(1-Q_2)}{L_1} & \frac{Q_x(1-Q_2)+(1-Q_x)Q_1(1-Q_2)}{L_1} & 0 & -\frac{1}{L_1} & 0 & 0 & 0 \\ \frac{Q_x(1-Q_1)+(1-Q_x)(1-Q_1)Q_2}{L_2} & -\frac{(1-Q_x)(1-Q_1)Q_2}{L_2} & -\frac{1}{L_2} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{D.3}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{Q_x}{L_x} & \frac{Q_x(1-Q_2}{L_1} & \frac{Q_x(1-Q_1)}{L_2} \end{bmatrix}^T \tag{D.4}$$

$$\mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{D.5}$$

$$\mathbf{D} = \begin{bmatrix} 1 & 0 & -1 \end{bmatrix} \tag{D.6}$$

dq0 Derivation E

The appendix presents the step by step derivation process for the equations in section 3.2.3 and it will pick up from 3.39:

$$\begin{bmatrix} T_{dq0}^{-1} \end{bmatrix} \begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} T_{dq0}^{-1} \end{bmatrix} \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} T_{dq0}^{-1} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \left(\begin{bmatrix} T_{dq0}^{-1} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \right) \tag{E.1}$$

In order to have only v_{dq} on the left side, the whole equation is left-multiplied with $[T_{dq0}]$.

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} T_{dq0} \end{bmatrix} \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} T_{dq0}^{-1} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} T_{dq0} \end{bmatrix} \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \left(\begin{bmatrix} T_{dq0}^{-1} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \right) \tag{E.2}$$

By applying $\frac{d}{dt}$ to

$$\begin{bmatrix} T_{dq0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{E.3}$$

and remembering the chain derivation rule: $[f(g(x))]' = f'(g(x)) \cdot g'(x)$ where f(x) and g(x) are two differentiable functions. In this case it is worth remembering that $\frac{d\theta}{dt} = \omega$ and f(x) would be the *cos* or *sin* functions, while $g(x) = \theta$. Thus,

$$\frac{d}{dt} \begin{bmatrix} T_{dq0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} -\omega\cos(\theta) & -\omega\cos(\theta - \frac{2\pi}{3}) & -\omega\cos(\theta + \frac{2\pi}{3}) \\ -\omega\sin(\theta) & -\omega\sin(\theta - \frac{2\pi}{3}) & -\omega\sin(\theta + \frac{2\pi}{3}) \\ 0 & 0 & 0 \end{bmatrix} \tag{E.4}$$

$$\frac{d}{dt} \begin{bmatrix} T_{dq0} \end{bmatrix} = \frac{2}{3}(-\omega) \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ 0 & 0 & 0 \end{bmatrix} \tag{E.5}$$

$$\frac{d}{dt} \begin{bmatrix} T_{dq0} \end{bmatrix} = (-\omega) \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} T_{dq0} \end{bmatrix} \tag{E.6}$$

$$\frac{d}{dt}\left[T_{dq0}\right] = \omega \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \left[T_{dq0}\right] \tag{E.7}$$

Therefore,

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt}\left(\left[T_{dq0}^{-1}\right] \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \right) \tag{E.8}$$

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt}\left(\left[T_{dq0}\right] \right) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt}\left(\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \right) \left[T_{dq0}\right] \tag{E.9}$$

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt}\left(\left[T_{dq0}\right] \right) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{E.10}$$

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \omega \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \left[T_{dq0}\right] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{E.11}$$

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \omega \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{E.12}$$

$$\begin{bmatrix} v_d^{con} \\ v_q^{con} \\ v_0^{con} \end{bmatrix} - \begin{bmatrix} v_d^{pcc} \\ v_q^{pcc} \\ v_0^{pcc} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \omega \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \begin{bmatrix} -i_q \\ i_d \\ i_0 \end{bmatrix} \tag{E.13}$$

From E.13, the two equations for v_{dq} can be extracted as shown in equation 3.43.

Half-Wave Symmetry in Even Order Harmonics

F

Before explaining the effects of half-wave symmetry, it is worth remembering the basics of Fourier analysis and the Fourier coefficients.

According to Fourier, a periodic function can be represented by an infinite sum of cosine and sine functions that are related harmonically. Equation 3.47 can be expanded to its rectangular form:

$$i(t) = a_v + \sum_{k=1}^{\infty} \Big(a_k \cos(k\omega_0 t) + b_k \sin(k\omega_0 t) \Big) \tag{F.1}$$

with ω_0 representing the fundamental frequency and a_v, a_k and b_k being the Fourier coefficients defined as:

$$a_v = \frac{1}{T} \int_{t_0}^{t_0+T} i(t)dt \tag{F.2}$$

$$a_k = \frac{2}{T} \int_{t_0}^{t_0+T} i(t) \cos(k\omega_0 t)dt \tag{F.3}$$

$$b_k = \frac{2}{T} \int_{t_0}^{t_0+T} i(t) \sin(k\omega_0 t)dt \tag{F.4}$$

Having said this, a function having half-wave symmetry, has the following property:

$$f(t) = -f(t \pm \frac{T}{2}) \tag{F.5}$$

visualised in figure F.1, where it can be seen that moving the sine by half a period and then inverting it yields the exact same function as the original. Thus $a_v = 0$ because the average value of a sinusoidal function over one period is 0.

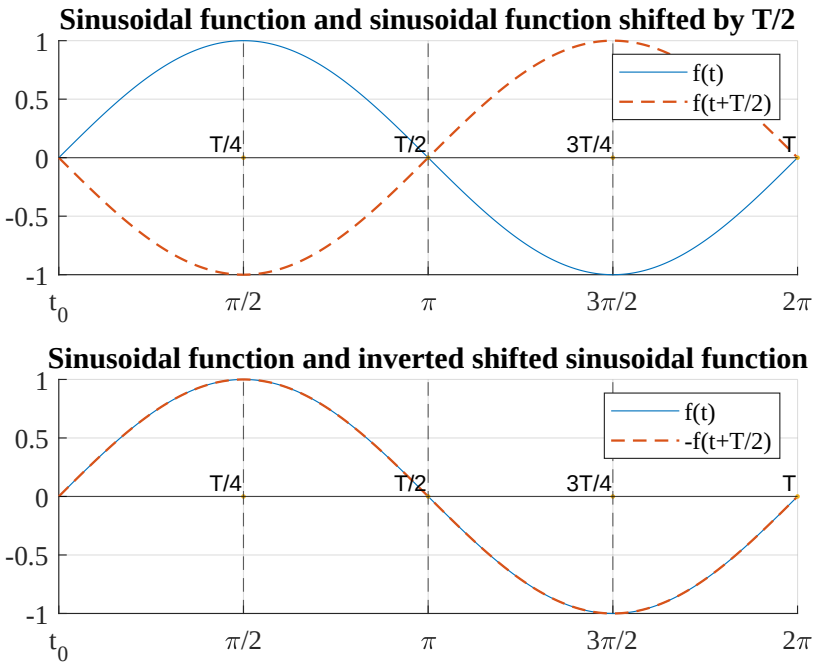


Figure F.1: Visualisation of the half-wave symmetry property for a sinusoidal function with T=2π.

For a_k when $k \in \{2, 4, 6, 8...\}$:

$$a_k = \frac{2}{T} \int_{t_0}^{t_0+T} i(t) \cos(k\omega_0 t) dt \tag{F.6}$$

$$a_k = \frac{2}{T} \Big[\int_{t_0}^{t_0+\frac{T}{2}} i(t) \cos(k\omega_0 t) dt + \int_{t_0+\frac{T}{2}}^{t_0+T} i(t) \cos(k\omega_0 t) dt \Big] \tag{F.7}$$

For ease of calculation, equation F.7 can be written as $a_k = \frac{2}{T}[A_1 + A_2]$ and A_2 will be analyzed further on, after making the substitution $\tau = t - \frac{T}{2}$:

$$A_2 = \int_{t_0}^{t_0+\frac{T}{2}} i(\tau + \frac{T}{2}) \cos(k\omega_0(\tau + \frac{T}{2})) d\tau \tag{F.8}$$

Accounting for equation F.5:

$$A_2 = -\int_{t_0}^{t_0+\frac{T}{2}} i(\tau) \cos(k\omega_0(\tau + \frac{T}{2})) d\tau \tag{F.9}$$

$\cos(k\omega_0(\tau + \frac{T}{2})) = \cos(k\omega_0\tau + k\pi)$ can be simplified using the trigonometric identity

$$\cos(a \pm b) = \cos(a)\cos(b) \mp \sin(a)\sin(b) \tag{F.10}$$

Therefore

$$\cos(k\omega_0\tau + k\pi) = \cos(k\omega_0\tau)\cos(k\pi) - \sin(k\omega_0\tau)\sin(k\pi) \tag{F.11}$$

Since $\cos(k\pi) = (-1)^k$ and $\sin(k\pi) = 0$, equation F.11 can be simplified further to

$$\cos(k\omega_0\tau + k\pi) = (-1)^k\cos(k\omega_0\tau) - 0 \tag{F.12}$$

Thus

$$A_2 = -(-1)^k \int_{t_0}^{t_0+\frac{T}{2}} i(\tau)cos(k\omega_0\tau)d\tau \tag{F.13}$$

Moving back to a_k:

$$a_k = \frac{2}{T}(1-(-1)^k) \int_{t_0}^{t_0+\frac{T}{2}} i(t)cos(k\omega_0 t)dt \tag{F.14}$$

For any k being an even number, $(1-(-1)^k) = 0$, therefore $a_k = 0$.

A similar rational can be performed for b_k, yielding $b_k = 0$.

Having said this, for k being any even number, equation F.1 becomes $i(t) = 0$ and as such, even harmonics would not be present.