Model Predictive Control of Power Converters for Robust and Fast Operation of AC Microgrids

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***Abstract*—This paper proposes the application of a finite control set model predictive control (FCS-MPC) strategy in standalone ac microgrids (MGs). AC MGs are usually built from two or more voltage source converters (VSCs) which have the capability of regulating the voltage at the point of common coupling, while sharing the load power at the same time. Those functionalities are conventionally achieved by hierarchical linear control loops. However, they present severe limitations in terms of slow transient response and high sensitivity to parameter variations. This paper aims to mitigate these problems by first introducing an improvement of the FCS-MPC strategy for a single VSC that is based on explicit tracking of derivative of the voltage reference trajectory. Using only a single step prediction horizon, the proposed strategy exhibits very low computational expense, but provides steady-state performance comparable to carrier-based sinusoidal PWM, while its transient response and robustness to parameter variation is far superior to hierarchical linear control. These benefits are exploited in a general ac MG setting where a methodology for paralleling multiple FCS-MPC regulated VSCs is described. Such an MG is characterized by rapid transient response, inherent stability in all operating conditions, and fully decentralized operation of individual VSCs. These findings have been validated through comprehensive simulation and experimental verification.**

***Index Terms*—AC microgrid (MG), finite control set (FCS), model predictive control (MPC), voltage source converter (VSC).**

I. Introduction

MICROGRIDS (MGs) are one of the key technologies that will enable high penetration of renewable energy sources (RES) in future power systems [1]. By locally aggregating multiple RES with distributed energy storage and adaptive loads, they can achieve much higher flexibility than individual resources. In this context, MGs can be used to provide different types of ancillary services to the overhead alternating-current (ac) system such as peak load shaving, load shifting, and voltage support [2], [3]. On the other hand, in case of outage or low power quality of utility mains, they can seamlessly disconnect and continue to supply the loads with high quality power in the standalone mode.

Among different MG types, ac and direct current (dc) MGs can be distinguished. Although dc MGs present more attractive characteristics from the efficiency and control simplicity point of view, vast majority of conventional loads require ac power supply [4], [5]. Therefore, it is usually necessary to establish an ac MG architecture at the end of the overall energy conversion chain. Such an architecture, as well its control functionalities are enabled by the flexible interlinked voltage source converters (VSCs), which serve as interfaces between the ac and dc parts of the MG, local generation, energy storage systems (ESSs), flexible loads, and the overhead power system [6].

Several VSCs are typically connected in parallel to form an ac MG. This is done for several reasons. For instance, paralleled operation provides redundancy and high reliability which is often required in mission critical applications. Moreover, in some cases it is more economically feasible to distribute the high power load to several VSCs and then use power devices with lower current ratings or even adapt the number of online VSCs to maximize the system efficiency.

In any case, it is highly desirable to realize the paralleled VSC operation in a decentralized fashion, i.e., without the use of any external communication. In this context, a droop control strategy and its variants are the most commonly deployed [7]–[13]. They are normally implemented as the outer control loops which generate a voltage reference that is fed to the corresponding VSC's inner control. Inner control typically comprises the virtual impedance and voltage regulation loop [12]. Virtual impedance is used to fix the output impedance value and hence to decouple the control of active and reactive powers [14], while voltage regulation comes down to regulating the voltage at the VSC's output LC filter according to the imposed reference.

The conventional way of realizing overall VSC control structure in MGs is through hierarchically organized linear loops and a pulse width modulator (PWM) [11], [12], [15], [16]. However, although widely accepted in practice, this method suffers from several practical limitations. First, it is inherently slow since every outer loop is designed with approximately an order of magnitude smaller bandwidth compared to the inner one [17]. While this kind of design is needed in order to operate all the loops independent from each other, it also results in a sluggish transient response. Moreover, tuning of control parameters requires careful consideration as they have a profound effect on the stability properties of the overall system [18]. Finally, vast majority of publications assume a common sampling of all converters by default. In order to achieve this condition in practice, multiple VSCs need to be synchronized and essentially regulated as a single converter, which is in obvious conflict with the desire to have a decentralized control system [19].

Manuscript received March 28, 2017; revised July 20, 2017; accepted August 22, 2017. Date of publication August 24, 2017; date of current version March 5, 2018. Recommended for publication by associate editor B. P. McGrath.

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Digital Object Identifier 10.1109/TPEL.2017.2744986

In clear contrast to linear control, finite control set model predictive control (FCS-MPC) is based on a fundamentally different principle. Instead of designing independent loop for every controlled variable and then cascading them together, it uses a discrete model of the VSC with associated filter to predict its future behavior for all possible control inputs, and consequently applying the one that is expected to minimize some preprogrammed cost function (CF) at the future sampling step [20]. Such a CF is most commonly based on a square of Euclidean distance between the controlled variable and the reference signal [21]. Due to its robustness, excellent transient characteristics and easiness to include nonlinearities, constraints and additional control objectives, the FCS-MPC principle has emerged as an attractive alternative for the control of power converters and was recently successfully applied to a wide range of power electronics based areas such as current control of grid connected converters and active power filters, as well as torque control of electrical drives [22]–[29].

However, most power electronics systems to which the FCS-MPC was applied so far comprised of a strong electromotive force (EMF) lying behind the first-order inductive filter. On the contrary, there is no strong EMF in standalone MGs, while the filters are commonly of second-order LC type. In this case, there exist dynamic coupling between the filter state variables and an Euclidean distance-based CF provides relatively poor steady-state performance as it does not take into account these coupled dynamics [30], [31]. One possible approach to circumvent this issue is deployment of longer prediction horizons [32]. However, this not only results in significant increase of computational expense, but it also requires highly accurate model of the system for proper functioning. While it should be noted that the mitigation of high computational expense has been recently proposed using sphere decoding algorithms, this approach is limited to linear systems [33], [34]. Besides, such algorithms are fairly complicated to implement in practice, and give only marginal improvements for two-level VSCs if a proper CF is used.

This paper proposes the usage of a single step prediction horizon FCS-MPC as an alternative to solve control challenges of both a single VSC and multiple paralleled VSC in the ac MG environment. Focusing in particular on standalone ac MG operation, this paper provides following key contributions to the field:

1) Modification of conventional FCS-MPC algorithm for voltage regulation of a single standalone VSC with LC filter which explicitly takes into account dynamic coupling between state variables, thereby improving the steady-state performance, while maintaining fast transient response.
2) Connection of multiple FCS-MPC regulated VSCs into fully decentralized (no common synchronization signal) ac MG resulting in much faster transient response and improved robustness to control parameter variations compared to state-of-the art linear cascaded loops.

The paper is organized as follows. In Section II, the structure of the ac MG is described. Section III provides a detailed model of the two-level VSC with associated LC filter and discusses the discretization aspects, which are necessary for the implementation of the FCS-MPC. The operating principle of the conventional FCS-MPC method applied to voltage regulation of a standalone VSC with LC filter is discussed in Section IV, where its performance limitations are also qualitatively explained. Based on those findings, a modified algorithm that can overcome the identified limitations is proposed. In Section V, the methodology of creating an ac MG from multiple FCS-MPC regulated VSCs is described. Comprehensive simulation results are provided in Section VI, while the experimental verification is given in Section VII. Finally, Section VIII gives the conclusion.

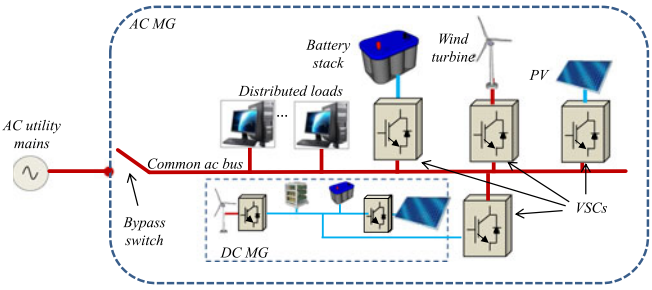

Fig. 1. Diagram of a VSC enabled ac MG.

II. System Description

Fig. 1 shows an exemplary ac MG. It comprises several distributed generators, which are interfaced to the common ac bus through VSCs. Such an MG can in general also be connected to utility mains and be able to seamlessly transfer between grid connected and standalone modes. However, the main focus of this paper is standalone operation.

With regards to the functionalities of VSCs as main MG building blocks, they can be divided into three main categories, namely grid-forming, grid-feeding, and grid-supporting VSCs [35]. The latter category plays a key role when two or more VSCs are connected in parallel. In that case, their voltage amplitudes and frequencies need to be adapted online according to the loading conditions in order to ensure the proper power sharing among different modules. It is interesting to notice that droop control methodology, as presented in [7]–[13], essentially corresponds to a grid-supporting VSC.

Droop control operates at the highest level of primary control. Hence, it relies on the voltage regulation capability of control layers below. This whole structure is conventionally implemented using linear cascaded loops. Such loops are designed independently from each other, which means that each outer one needs to have an order of magnitude lower bandwidth compared to the one below [11]. As a result, traditional MG hierarchical control suffers from very slow transient response. Motivated by this limitation, this paper proposes a new control structure for an ac MG which embodies the attractive transient capabilities of the FCS-MPC together with decentralized features of droop methodology.

In that sense, first the modification of state-of-the art FCS-MPC is proposed to improve the VSC voltage tracking

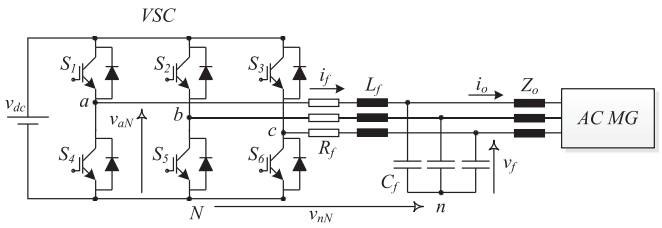

Fig. 2. Two-level three-phase VSC feeding an output LC filter which is connected to an ac MG through a line with an impedance Z_o.

performance. This results both in reduced voltage THD when a single VSC is operated alone, but also in an improved power sharing when operated together with other VSCs in a MG. The resulting VSC is then integrated into an ac MG, which is characterized by fast and robust performance, and fully decentralized operation in the sense that it does not require any kind of common synchronization signal.

Next section provides the modeling background for the VSC, which is necessary for the implementation of FCS-MPC and integration into the overall MG framework.

III. VSC Modeling and Discretization

As its name suggests, an MPC strategy relies on the model of the system to predict how the possible control actions would affect its response. Consequently, the action that is expected to minimize a certain CF is applied and the process is sequentially repeated.

In order to achieve a good control performance when deploying such a methodology to a VSC, proper models of both the converter and filter are needed. In particular, two-level three-phase VSC shown in Fig. 2 is the most basic and commonly used converter topology in ac MGs. It can be seen from the figure that an LC filter, which attenuates the switching harmonics is connected at the output of VSC terminals.

The respective VSC will be modeled here using a stationary $\alpha\beta$ orthogonal reference frame. Since balanced conditions are assumed, zero sequence components are neglected in this particular model. To that end, all generic three-phase voltages v and currents i, given in a-b-c can be transformed into corresponding $\alpha\beta$ frame by applying an amplitude invariant Clarke transformation $\bar{\mathbf{T}}$:

$$\begin{aligned} \bar{v} &= v_\alpha + jv_\beta = \bar{\mathbf{T}}\,[v_a v_b v_c]' \\ \bar{i} &= i_\alpha + ji_\beta = \bar{\mathbf{T}}\,[i_a i_b i_c]' \end{aligned} \tag{1}$$

where

$$\bar{\mathbf{T}} = \frac{1}{3}\left[\, 1 e^{j\frac{2}{3}\pi} e^{j\frac{4}{3}\pi}\,\right]. \tag{2}$$

A. Converter Model

The switch configuration of the VSC shown in Fig. 2 is fully defined by the three gating signals S_a, S_b, and S_c. Each one of them can take two possible values, i.e., 1 or 0, as follows:

TABLE I
Switch Configurations and Complex Voltage Vectors Used in Two-Level Three-Phase VSC

S_a	S_b	S_c	Voltage vector $\bar{v}_i$
0	0	0	$\bar{v}_0 = 0$
1	0	0	$\bar{v}_1 = \frac{2}{3} v_{\text{dc}}$
1	1	0	$\bar{v}_2 = \frac{1}{3} v_{\text{dc}} + j\frac{\sqrt{3}}{3} v_{\text{dc}}$
0	1	0	$\bar{v}_3 = -\frac{1}{3} v_{\text{dc}} + j\frac{\sqrt{3}}{3} v_{\text{dc}}$
0	1	1	$\bar{v}_4 = -\frac{2}{3} v_{\text{dc}}$
0	0	1	$\bar{v}_5 = -\frac{1}{3} v_{\text{dc}} - j\frac{\sqrt{3}}{3} v_{\text{dc}}$
1	0	1	$\bar{v}_6 = \frac{1}{3} v_{\text{dc}} - j\frac{\sqrt{3}}{3} v_{\text{dc}}$
1	1	1	$\bar{v}_7 = 0$

$$S_a = \begin{cases} 1, \text{ if } S_1 \text{ is ON and } S_4 \text{ is OFF} \\ 0, \text{ if } S_1 \text{ is OFF and } S_4 \text{ is ON} \end{cases} \tag{3}$$

$$S_b = \begin{cases} 1, \text{ if } S_2 \text{ is ON and } S_5 \text{ is OFF} \\ 0, \text{ if } S_2 \text{ is OFF and } S_5 \text{ is ON} \end{cases} \tag{4}$$

$$S_c = \begin{cases} 1, \text{ if } S_3 \text{ is ON and } S_6 \text{ is OFF} \\ 0, \text{ if } S_3 \text{ is OFF and } S_6 \text{ is ON.} \end{cases} \tag{5}$$

Therefore, the overall converter can be in eight (2^3) possible switch configurations. Voltages of inverter legs with respect to the point N are then calculated by multiplying the dc link voltage with the state of the respective leg:

$$\begin{aligned} v_{aN} &= S_a \cdot v_{\text{dc}} \\ v_{bN} &= S_b \cdot v_{\text{dc}} \\ v_{cN} &= S_c \cdot v_{\text{dc}}. \end{aligned} \tag{6}$$

In order to obtain the effective voltages applied across each phase (i.e., from a, b, and c to the point n), common mode voltage v_{nN} needs to be subtracted from (6). Common mode voltage can simply be calculated by taking into account the Kirchhoff's voltage law:

$$v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3}. \tag{7}$$

Correspondingly, the effective phase voltage are given by

$$\begin{aligned} v_{an} &= v_{aN} - v_{nN} \\ v_{bn} &= v_{bN} - v_{nN} \\ v_{cn} &= v_{cN} - v_{nN}. \end{aligned} \tag{8}$$

By applying the complex Clarke transformation (1)–(2) to (8) for all eight possible switch configurations, the corresponding voltage input vectors $\bar{v}_i$ can be obtained in the complex $\alpha\beta$ frame, as shown in Table I.

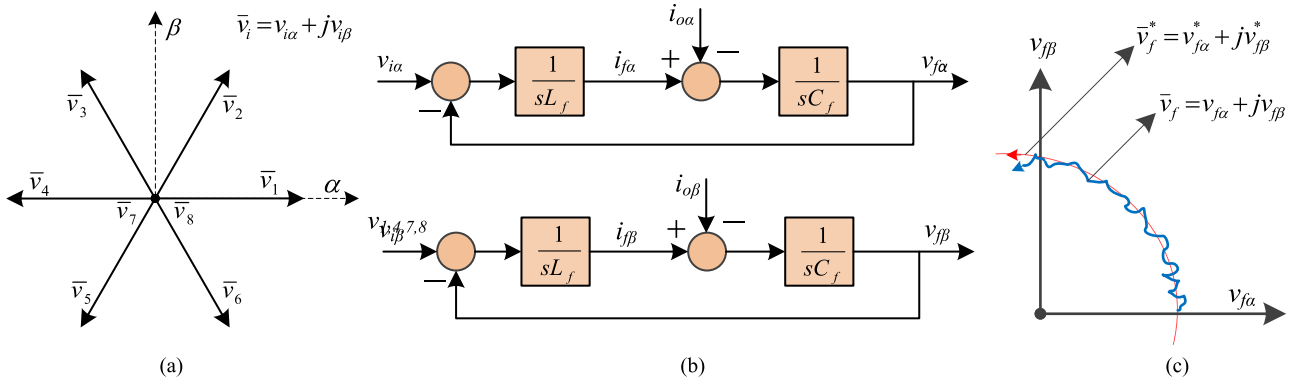

Fig. 3. Operating principle of the FCS-MPC used for voltage control of an ac bus by the two-level three-phase VSC with an LC filter. (a) Possible voltage vectors of a VSC that correspond to Table I. (b) Equivalent LC filter models in the α and β reference frames. (c) Reference voltage ($\bar{v}_f^*$) and filter capacitor voltage ($\bar{v}_f$) trajectories.

B. LC Filter

As it can be seen in Fig. 2, a three-phase LC filter is connected to the output terminals of the converter in order to suppress the switching harmonics. Each leg of the filter comprises an inductor with inductance L_f and series resistance R_f, and a capacitor with capacitance C_f. Inductor current i_f which flows through the L_f and capacitor voltage v_f across the C_f are the state variables of this second-order system. By assuming that the parameter values are equal in all three legs, the dynamics in the complex $\alpha\beta$ can be described as:

$$L_f \frac{d\bar{i}_f}{dt} = \bar{v}_i - \bar{v}_f - R_f \bar{i}_f \tag{9}$$

where $\bar{v}_i$ is one of the possible voltage vectors given in Table I. On the other hand, the dynamic behavior of the voltage across the filter capacitor is defined by the following:

$$C_f \frac{d\bar{v}_f}{dt} = \bar{i}_f - \bar{i}_o \tag{10}$$

where $\bar{i}_o$ is the output current. It should be noted that this current can be either measured or estimated [30]. In this paper, direct measurement is deployed.

For convenience, (9), (10) can be expressed in the state-space form as

$$\frac{d}{dt}\begin{bmatrix} \bar{i}_f \\ \bar{v}_f \end{bmatrix} = \mathbf{A}\begin{bmatrix} \bar{i}_f \\ \bar{v}_f \end{bmatrix} + \mathbf{B}\begin{bmatrix} \bar{v}_i \\ \bar{i}_o \end{bmatrix} \tag{11}$$

where

$$\mathbf{A} = \begin{bmatrix} -\frac{R_f}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix} \tag{12}$$

and

$$\mathbf{B} = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{C_f} \end{bmatrix}. \tag{13}$$

The equations above fully define the continuous state-space model of an LC filter which takes the voltage vector $\bar{v}_i$ and output current $\bar{i}_o$ as inputs.

C. Discrete Time-Domain Model of the LC Filter

In order to make practical use of the model developed in previous section, it needs to be prepared for the implementation in digital control system by deploying an appropriate discretization. Out of different discretization methods, zero-order hold (ZOH) provides the exact matching between the continuous- and discrete-time systems at sampling instants for staircase inputs [36]. Assuming a constant dc link voltage v_{dc}, the power converter under study indeed has staircase inputs which are defined by the eight $\bar{v}_i$ values given in Table I. The ZOH discretization method can be expressed as

$$\begin{bmatrix} \bar{i}_f(k+1) \\ \bar{v}_f(k+1) \end{bmatrix} = \mathbf{A_d}\begin{bmatrix} \bar{i}_f(k) \\ \bar{v}_f(k) \end{bmatrix} + \mathbf{B_d}\begin{bmatrix} \bar{v}_i(k) \\ \bar{i}_o(k) \end{bmatrix} \tag{14}$$

with

$$\mathbf{A_d} = e^{\mathbf{A}T_s} \tag{15}$$

and

$$\mathbf{B_d} = \int_0^{T_s} e^{\mathbf{A}\tau}\mathbf{B}d\tau \tag{16}$$

where T_s is the sampling time. These equations will be used for the prediction step of the FCS-MPC controller, as discussed in the following section.

IV. Finite Control Set MPC for Voltage Regulation of an AC Bus

An illustration of the unified model of the VSC and an LC filter is presented in Fig. 3. Fig. 3(a) shows eight possible voltage vectors $\bar{v}_i$ that a two-level VSC can generate in the $\alpha\beta$ stationary reference frame. Each of these vectors comprises a specific set of voltage values, $v_{i\alpha}$ and $v_{i\beta}$, which are applied as inputs to the corresponding LC filter models, as shown in Fig. 3(b). Outputs of the respective two models, $v_{f\alpha}$ and $v_{f\beta}$, finally define the propagation of the filter capacitor voltage trajectory $\bar{v}_f$. Consequently, the main control objective is to successively select the

voltage input vectors $\bar{v}_i$ in such a way that $\bar{v}_f$ tracks the reference voltage trajectory $\bar{v}_f^*$ with minimal error, as depicted in Fig. 3(c). An FCS-MPC principle designed to achieve this goal with respect to secondary control objectives as well is described in the following section.

A. Operating Principle

FCS-MPC algorithms are normally implemented in digital control platforms and they are characterized by synchronized switching and sampling instants [37]. The basic operation principle of the algorithm is as follows. At the beginning of every sampling instant, new measurements of $\bar{v}_f$, $\bar{i}_f$, and $\bar{i}_o$ are received. These measurements define the starting point from which the algorithm predicts the future trajectories of state variables $\bar{v}_f$ and $\bar{i}_f$ according to (14), for every possible voltage vector. Each of those predicted values are then evaluated with a predesigned CF, and a vector that corresponds to the minimal value of CF is applied to the VSC.

It should be noted that in practical applications there exist a computational delay which requires compensation. This can be done by adding an additional step to the algorithm described above. This issue is discussed in more details in Section VII-B.

B. Cost Function

Design of a CF is the cornerstone of the FCS-MPC methodology. A CF that covers a prediction horizon of N time steps and, apart from voltage regulation, also simultaneously keeps track of several other objectives can be formulated as follows:

$$g_{\text{gen}} = \sum_{i=k}^{k+N-1} \left(\|\bar{v}_{fe}(i)\|_2^2 + h_{\text{lim}}(i) + \lambda_u \text{sw}^2(i) \right) \tag{17}$$

where $\bar{v}_{fe}(i)$ is the predicted tracking error, $h_{\text{lim}}(i)$ imposes the current constraint, while $\text{sw}^2(i)$ penalizes the switching effort which can be controlled by the associated weighting factor λ_u. These terms are defined as follows:

$$\bar{v}_{fe}(i) = \bar{v}_f^*(i) - \bar{v}_f(i) \tag{18}$$

$$h_{\text{lim}}(i) = \begin{cases} 0, \text{ if } |\bar{i}_f(i)| \leq i_{\max} \\ \infty, \text{ if } |\bar{i}_f(i)| > i_{\max} \end{cases} \tag{19}$$

and

$$\text{sw}(i) = \sum |u(i) - u(i-1)|. \tag{20}$$

Later in this section, a variation of (17), based only on Euclidean distance, is qualitatively analyzed and improved CF is proposed accordingly. Before that, a delay compensation which is needed in practical FCS-MPC applications is discussed.

C. Conventional FCS-MPC Algorithm

In [30], the conventional Euclidean distance-based CF in the $\alpha\beta$ frame was used:

$$g_{\text{con}} = \left(v_{f\alpha}^* - v_{f\alpha}\right)^2 + \left(v_{f\beta}^* - v_{f\beta}\right)^2. \tag{21}$$

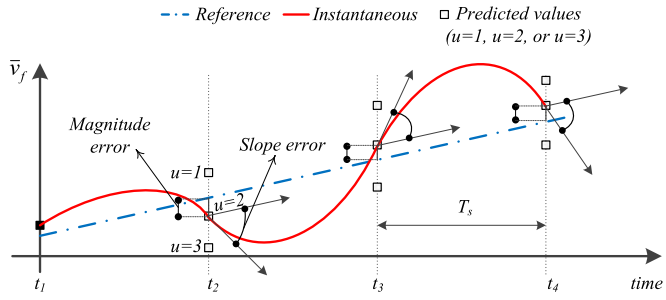

Fig. 4. Voltage tracking problems with the conventional FCS-MPC scheme.

The CF stated above is simply a generalized case of (17) with $N = 1$, and no secondary objectives. It aims to minimize the Euclidean distance at every sampling instant.

Although this may result in satisfactory performance for first order systems, coupling between the state variables makes it somewhat unsuitable for second order ones. The reason is that the controlled variable in first-order systems (i.e., converter side inductor current in the L filter) can be directly regulated by the control input, allowing an instantaneous change of its derivative at a particular sampling instant. On the contrary, capacitor voltage in the second-order LC filter configuration can only be regulated indirectly through the inductor current. As respective current cannot change instantaneously its value, the capacitor voltage correspondingly cannot change its derivative instantaneously.

Therefore, by involving exclusively the capacitor voltage error in the CF, as in (21), no respect is given to its derivative. The result is that the minimal magnitude error will often be achieved at a cost of having voltage trajectory pointing significantly away from the reference trajectory. This causes intractable voltage deviations in intersampling periods which often lead to unfavorable starting points at future time instants, ultimately resulting in high total harmonic distortion (THD) in the measured voltage signal.

This phenomenon is illustrated in Fig. 4, where the exemplary propagation of capacitor voltage is shown. It can be seen from the figure that, although the transition from the initial time step t_1 to step t_2 with control input $u = 2$ leads to the smallest error at the sampling instance t_2, it also results in a significant deviation of voltage trajectory heading from the reference heading. Therefore, the capacitor voltage will continue to decrease rapidly regardless of the input applied at time instant t_2, resulting in a large oscillations around the reference and consequently a large THD.

D. Proposed Modification of the FCS MPC Algorithm for Improving the Voltage Tracking Performance

In order to improve the VSC's capacitor voltage quality compared to conventional FCS-MPC strategy in [30] and [31], while circumventing practical application problems associated with multistep prediction horizon methods reported in [32], a new FCS-MPC strategy is proposed here.

As discussed in the previous section, inability to control the derivative of capacitor voltage is a fundamental cause of high

THD using the conventional scheme. Therefore, the ideal regulator should simultaneously track both the voltage reference and its derivative. In the following, these two signals are analyzed and treated as two separate references. The voltage reference can be written as

$$\bar{v}_f^*(t) = \overbrace{V_{\text{ref}}\sin(\omega_{\text{ref}}t)}^{v_{f\alpha}^*(t)} + j\overbrace{V_{\text{ref}}\cos(\omega_{\text{ref}}t)}^{v_{f\beta}^*(t)} \tag{22}$$

where V_{ref} and ω_{ref} are the voltage amplitude and angular frequency ($\omega_{\text{ref}} = 2\pi f_{\text{ref}}$) of the reference signal, respectively, while t is the time signal. By taking a time derivative of (22), the voltage derivative reference is obtained:

$$\frac{d\bar{v}_f^*(t)}{dt} = \overbrace{\omega_{\text{ref}}V_{\text{ref}}\cos(\omega_{\text{ref}}t)}^{\omega_{\text{ref}}v_{f\beta}^*(t)} - j\overbrace{\omega_{\text{ref}}V_{\text{ref}}\sin(\omega_{\text{ref}}t)}^{\omega_{\text{ref}}v_{f\alpha}^*(t)}. \tag{23}$$

Tracking of $v_f^*(t)$ is already accomplished by the CF presented in (22). Therefore, what remains is to expand it so that $\frac{d\bar{v}_f(t)}{dt}$ can also track $\frac{d\bar{v}_f^*(t)}{dt}$. In order to do that, prediction of the capacitor voltage derivative is needed, which can be obtained from predicted currents $\bar{i}_f$ and measured currents $\bar{i}_o$:

$$\frac{d\bar{v}_f(t)}{dt} = \overbrace{\frac{i_{f\alpha}(t) - i_{o\alpha}(t)}{C_f}}^{\frac{dv_{f\alpha}(t)}{dt}} + j\overbrace{\frac{(i_{f\beta}(t) - i_{o\beta}(t))}{C_f}}^{\frac{dv_{f\beta}(t)}{dt}}. \tag{24}$$

It can be readily observed that the voltage derivative trajectory will be well tracked if the respective differences between the first and second terms from (23) and (24) are minimized. This objective can be explicitly formulated as follows:

$$g_{\text{der}} = \left(C_f\omega_{\text{ref}}v_{f\beta}^* - i_{f\alpha} + i_{o\alpha}\right)^2 + \left(C_f\omega_{\text{ref}}v_{f\alpha}^* + i_{f\beta} - i_{o\beta}\right)^2. \tag{25}$$

The term g_{der} can now simply be added to the conventional CF in (21) and its effect can be controlled by the weight λ_d. It is important to notice that no additional current sensors are required in order to implement g_{der}, compared to conventional CF. In particular, six current sensors (i_{fa}, i_{fb}, i_{fc}, i_{oa}, i_{ob}, i_{oc}) and three voltage sensors (v_{fa}, v_{fb}, v_{fc}) are used in both cases. Complete version of the proposed CF is as follows:

$$g_p = g_{\text{con}} + \lambda_d g_{\text{der}} + h_{\text{lim}} + \lambda_u \text{sw}^2. \tag{26}$$

VSCs with such a voltage regulation capability can now be integrated into the ac MG environment, as it will be described in the next section.

V. Building an AC MG From Multiple FCS-MPC Regulated VSCs

The single line diagram representing two VSCs connected to a common ac bus through generic power lines ($Z_{oi} = R_{oi} + jX_{oi}$) is shown in Fig. 5. Equivalent diagram is also applicable for the case with more VSCs. In order to design the control strategy for them, the principle of active and reactive power exchange between one VSC and a common ac bus first needs to be understood.

Power exchange is essentially defined by the impedance of the line connecting the two, where equations that describe these

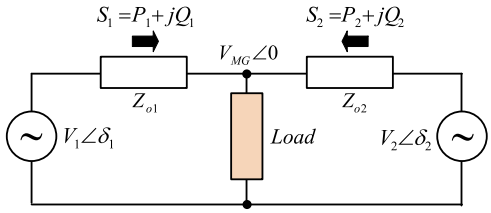

Fig. 5. Two VSCs connected to a common ac MG bus with a load through complex impedances $Z_{oi} = R_{oi} + jX_{oi}$.

relationships are as follows [35]:

$$P_i = \frac{V_i}{R_{oi}^2 + X_{oi}^2}\left[R_{oi}(V_i - V_{MG}\cos\delta_i) + X_{oi}V_{MG}\sin\delta_i\right] \tag{27}$$

$$Q_i = \frac{V_i}{R_{oi}^2 + X_{oi}^2}\left[-R_{oi}V_{MG}\sin\delta_i + X_{oi}(V_i - V_{MG}\cos\delta_i)\right] \tag{28}$$

where V_i and V_{MG} are the amplitudes of the VSC and the bus voltage, respectively, while δ_i are the corresponding power angles.

It can be seen from (27), (28) that active and reactive power exchange depends on both V_i and δ_i, and hence they cannot be controlled independently by those variables. A widely accepted solution to this issue is to enforce the effective output impedance seen by the VSC to become purely resistive or inductive via control efforts. In the literature, this is commonly referred to as the virtual impedance concept [14].

A. Virtual Impedance Loop

Although the output impedance can be easily shaped to become either resistive or inductive using the virtual impedance concept, it is arguably better to make it resistive [13]. Since resistive virtual impedance does not change with frequency, the whole frequency range is automatically covered with a single feedback loop. This makes it particularly suitable for power sharing of nonlinear loads and during transient conditions. Moreover, resistive virtual impedance is known to add damping to the system, and is hence favorable from the MG stability perspective.

Resistive virtual impedance loop is implemented as follows:

$$\bar{v}_f^* = \bar{v}_{ref} - R_v\bar{i}_o \tag{29}$$

where R_v is the resistive virtual impedance, $\bar{v}_f^*$ is the filter capacitor voltage reference to be fed into (26), while $\bar{v}_{\text{ref}}$ is the voltage reference provided by the outer droop control, which is elaborated in the next section.

Under the condition that R_v is set high enough so that the output impedance becomes dominantly resistive, and taking a reasonable practical assumption of small angle δ_i between the voltage vectors at VSC and MG ends, it can be stated that $X_{oi} \approx 0$, $\sin\delta_i \approx \delta_i$, and $\cos\delta_i \approx 1$ in (27) and (28). This leads

to the following set of equations:

$$P_i = \frac{V_i}{R_{oi}}\left(V_i - V_{MG}\right) \tag{30}$$

$$Q_i = -\frac{V_i V_{MG}}{R_{oi}}\delta_i. \tag{31}$$

It is now easy to observe that the exchange of active power in such a system can be controlled by the amplitude difference $\Delta V = V_i - V_{MG}$, whereas the reactive power can be regulated by manipulating the power angle δ_i.

B. Droop Control Strategy

Bearing in mind (30), (31), droop control is correspondingly designed

$$V_{\text{ref}} = V_{\text{nom}} - k_p P_{\text{cal}} \tag{32}$$

$$\omega_{\text{ref}} = \omega_{\text{nom}} + k_q Q_{\text{cal}} \tag{33}$$

where V_{ref} and ω_{ref} are the reference voltage amplitude and frequency used to synthesize $\bar{v}_{\text{ref}}$, which is fed to the virtual impedance loop (29), while V_{nom} and ω_{nom} are nominal voltage amplitude and frequency, respectively.

Droop coefficients, k_p and k_q, determine the slope of the droop curves and correspondingly, voltage drops and frequency boosts for given operating conditions. Such coefficients are normally designed in proportion to the power rating of VSCs. Finally, P_{cal} and Q_{cal} are instantaneous active and reactive powers, which can be calculated as

$$P_{\text{cal}} = v_{f\alpha} i_{o\alpha} + v_{f\beta} i_{o\beta} \tag{34}$$

$$Q_{\text{cal}} = v_{f\beta} i_{o\alpha} - v_{f\alpha} i_{o\beta}. \tag{35}$$

Before the application to (32), (33), powers calculated in (34), (35) need to be processed through low-pass filters with bandwidth approximately an order of magnitude lower than underlying loops when cascaded linear control is used [11]. This leads to very slow response during load transients (e.g., see in [11, Fig. 15]). On the contrary, essentially no filtering is needed if inner control is resolved by the FCS-MPC. This is because its speed is only limited by the sampling time T_s, but also due to a fact that oscillations in P_{cal} and Q_{cal} get nullified by the droop coefficients, k_p and k_q. Therefore, interaction between outer and inner loops is no longer an issue, while the oscillations present in P_{cal} and Q_{cal} will generally have negligible influence on calculation of V_{ref} and ω_{ref}. On the other hand, when droop coefficients are set in a way that the respective influence is not negligible, filters of much higher bandwidth compared to the conventional case can be deployed. All this allows several orders of magnitude faster response compared to conventional methods. It should be noted that such a structure also allows the possibility to implement secondary control with much higher bandwidth compared to state-of-the-art methods [38]. However, secondary control is out of the scope of this paper and is not analyzed here.

Control strategy described in (32) and (33) is in the literature commonly referred to as the conventional droop control [9], [10], [13]. While its main advantage is a fact that it is fully decentralized, it also has several practical limitations. For instance, in order to achieve accurate power sharing, output impedances of all connected VSCs need to be the same. Moreover, voltage drops which come as a consequence of load currents and droop settings are unavoidable when such control is employed. To that end, certain modifications which rely on measuring the load voltage have been proposed to avoid these problems [10], [13]. However, such techniques usually require additional communication hardware and are hence difficult to implement in more complex MG configurations. On the other hand, the advantages of using FCS-MPC regulated VSC can be demonstrated regardless of the particular variant of the droop strategy. Therefore, conventional droop control is deployed in this paper for the proof of concept.

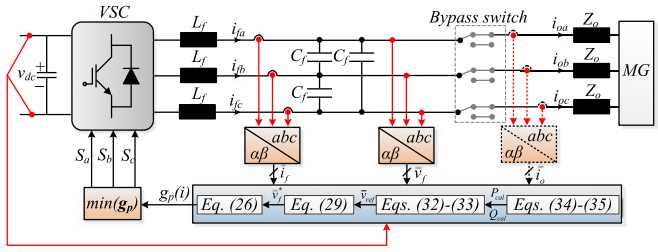

Fig. 6. FCS-MPC scheme for VSCs used in ac MG.

Fig. 6 shows systematic implementation procedure of all the control structures for the VSC suitable for ac MG integration. It can be seen that the voltage reference generated by droop controller and virtual impedance loop is simply fed to the FCS-MPC algorithm, which is proposed in the previous sections. In the following section, simulation results for both a single standalone FCS-MPC regulated VSC, and paralleled operation of multiple VSCs controlled by a control strategy described here are presented.

C. Extension of the Concept to Grid-Connected AC MG

While the methodology proposed in this paper is specifically designed and tested using IEC standard for standalone systems, it can be extended to grid-connected MGs as well. Namely, when power converters are connected in parallel, their main objective is to regulate the voltage at the point of common coupling (PCC), while sharing the power at the same time. Therefore, connecting the respective PCC to the grid is conceptually similar as connecting a single FCS-MPC regulated VSC to the grid through additional L filter. In fact, such connection has been discussed in some recent publications (see, e.g., [37]).

It should be noted, however, that grid connected systems use other standards and have different performance objectives compared to standalone applications. The focus in those applications is on shaping the grid side current on the outer L of the overall LCL filter, which is generally more problematic than regulating the voltage on the LC filter [37]. In this sense, low harmonic distortion of the grid-side current, and provision of grid ancillary services are some important requirements normally not needed in standalone applications. Due to wide harmonic spectrum produced by FCS-MPC, it is also somewhat challenging

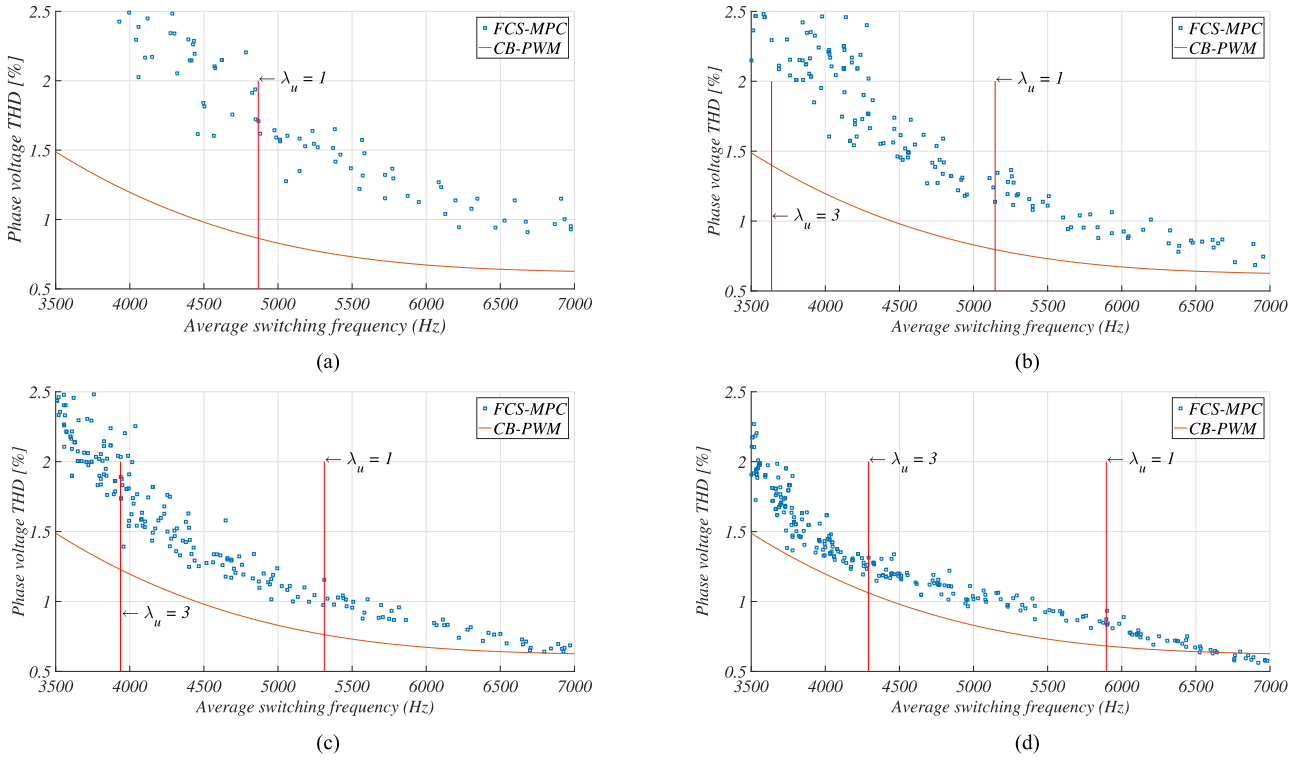

Fig. 7. Influence of weight settings λ_d and λ_u from (26) on the average switching frequency and resulting voltage THD. (a) THD versus switching frequency for $\lambda_d = 0$. This corresponds to conventional strategy with added switching penalization. (b) THD versus switching frequency for $\lambda_d = 0.1$. (c) THD versus switching frequency for $\lambda_d = 0.2$. (d) THD versus switching frequency for $\lambda_d = 0.5$.

TABLE II
PARAMETERS OF THE TEST SYSTEM (SEE FIG. 6)

DC link voltage	$v_{\text{dc}} = 520$ V
Sampling time	$T_s = 25\ \mu$s
LC-filter	$L_f = 2.4$ mH, $C_f = 25\ \mu$F
Linear load	$R_l = 33\ \Omega$
Nonlinear load (diode rectifier)	$R_n = 70\ \Omega$, $C_n = 1100\ \mu$F
Nominal voltage	$V_{\text{nom}} = 200$ V, $f_{\text{nom}} = 50$ Hz
Droop coefficients	$k_p = 0.001$ V/W, $k_q = 0.001$ rad/sVar
Line impedance	$R_{oi} = 0.1\ \Omega$, $L_{oi} = 2.4$ mH
Virtual resistance	$R_v = 2\ \Omega$

to guarantee the THD of the grid side current, especially under line inductance variations. For all these reasons, research about grid-connected MGs regulated by FCS-MPC deserves careful and individualized attention, where detailed investigation should be carried out from somewhat different angle than in the case of standalone MGs.

VI. SIMULATION RESULTS

Proposed FCS-MPC-based control strategy has been verified in MATLAB/Simulink simulation environment and experimentally. Extensive simulations have been done for both a single VSC and two VSCs in parallel, while experimental validations have been done on a single VSC prototype. Nominal simulation parameters have been chosen to be identical to those in an experimental platform, as given in Table II.

It should be noted that analytical methodology for filter design procedure in FCS-MPC regulated power converters is an open research topic for which an accepted solution is still not found [21]. Therefore, the parameters of the test setup were selected to be similar as other comparable systems reported in the literature (e.g., [30], [39]–[42]) in order to easily benchmark the proposed control methodology.

Several sets of simulations have been carried out. First, steady-state simulations for a single VSC have been done to verify the performance of proposed modification of the conventional FCS-MPC algorithm under both sinusoidal and harmonic voltage references. Then, the transient performance of the VSC has been tested with respect to the IEC 62040 standard for standalone UPS systems. Further, robustness study of the proposed algorithm to uncertainty of the system's parameters has been done using large number of simulations with different parameter sets. Finally, two VSCs regulated with proposed FCS-MPC algorithm have been connected into an ac MG structure using droop control methodology and respective power sharing properties have been verified.

A. Steady-State Analysis

Fig. 7 shows the relationship between the phase voltage THD and average switching frequency of a single VSC regulated by (26) for different weight settings λ_d and λ_u.

In all simulations, two fundamental cycles (0.04 s) of the capacitor voltage sampled at 1 μs were processed using a Fast Fourier Transform (FFT) algorithm available in MATLAB

library to identify individual harmonic amplitudes. No windowing functions were used. The THD was then calculated for harmonics up to 400. In some standards, it is recommended to include up to 40th harmonic. However, when power converter is regulated by the FCS-MPC, it produces a wide frequency harmonic spectrum at the output, unless specific measures are taken [21]. In this case, accounting for only 40 harmonics, would give somewhat different results than accounting for up to 400.

Following equation has been used to calculate the average switching frequency:

$$f_{\text{av}} = \frac{\sum_{i=1}^{N} \text{sw}(i)}{3 \cdot N \cdot T_s} \tag{36}$$

with N being the total number of time instants for which the calculation is done. Here, N was chosen to be 800 as it corresponds to one fundamental period under $T_s = 25\ \mu$s. Results are obtained from a large number of simulations that have been carried by sweeping the λ_d parameter from 0 to 1 with a step of 0.1, and by sweeping the λ_u parameter from 0 to 7 with a step of 0.02. Only four values of λ_d have been shown here because the general improvement could be readily observed for those values, while further increase of the respective parameter beyond $\lambda_d = 0.5$ did not result in further performance improvement. In each of those four figures, also a THD versus switching frequency has been plotted for a carrier-based (CB) sinusoidal PWM to serve as a benchmark.

It can be clearly seen from those figures that proposed FCS-MPC algorithm improves the steady-state performance compared to conventional FCS-MPC and achieves only slightly worse characteristics than CB-PWM even though only a single step prediction horizon was used. Finally, in Fig. 8, two exemplary waveforms are shown which demonstrate the capability of tracking harmonic voltages. In particular, 5th, 7th, and 11th harmonic voltage references, each having an amplitude of 5 V, are imposed on top of 200 V fundamental voltage reference. Considerably better tracking can be observed with the proposed method.

B. Transient Analysis

Transient performance of the proposed algorithm has been tested with respect to IEC 62040 standard. Based on conclusions drawn from carrying a large number of simulations for FCS-MPC settings, $\lambda_d = 0.5$ and $\lambda_u = 1$ have been chosen for this investigation. These particular settings allow a voltage THD lower than 1% and average switching frequency around 6 kHz, as also indicated in Fig. 7(d). Two simulations have been carried out under these settings. Fig. 9 shows the voltage deviation from the reference when a step change in linear load is applied. Fig. 10 shows the operation under nonlinear load conditions. It can be seen that the IEC 62040 standard for the most critical loads is respected in both scenarios by a large margin with transient response being several orders of magnitude faster than state-of-the-art linear control methods. For instance, dynamic response of proposed method from Fig. 9 can be compared to the one achieved by hierarchical control (see [39, Fig. 18]) or to the one achieved by internal-model-based control (see [40, Fig. 32]).

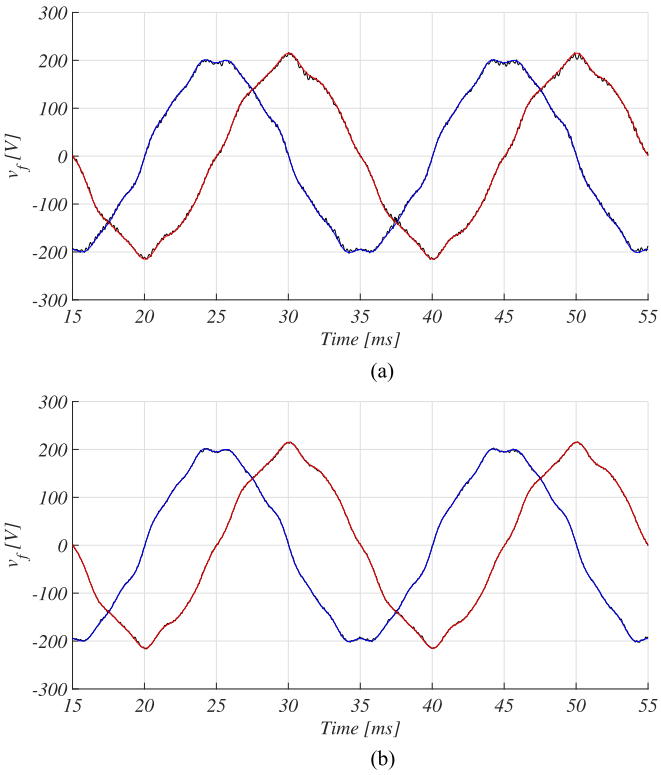

Fig. 8. Comparison of tracking performance when 5th, 7th, and 11th harmonic voltages of 5 V are imposed on top of 200 V fundamental voltage reference. (a) Capability of tracking harmonic voltages using a conventional FCS-MPC algorithm stated in (21). (b) Capability of tracking harmonic voltages using a proposed FCS-MPC algorithm stated in (26).

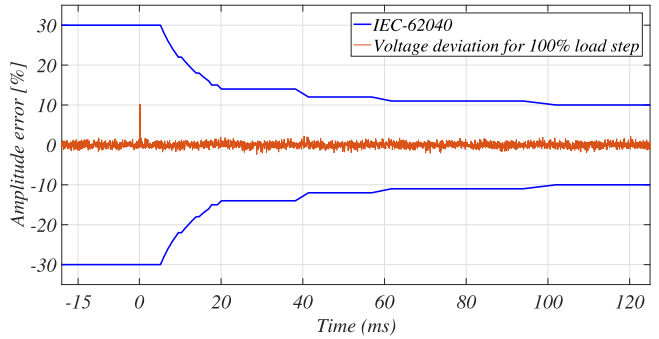

Fig. 9. Dynamic characteristics according to the IEC 62040 standard (for the most critical and sensitive loads) with 100% step change of linear load (open circuit to $R_{\text{load}} = 20\,\Omega$). Values $\lambda_d = 0.5$ and $\lambda_u = 1$ have been used.

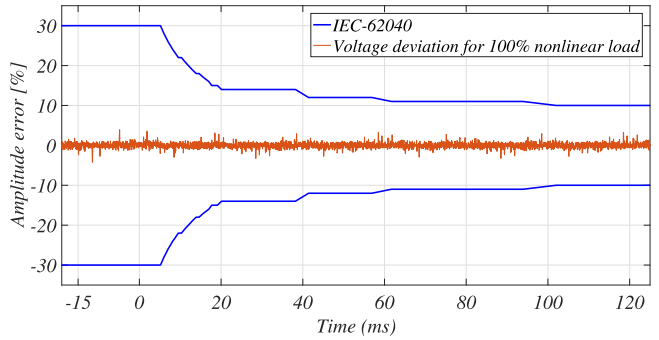

Fig. 10. Dynamic characteristics according to the IEC 62040 standard (for the most critical and sensitive loads) with 100% nonlinear load ($R_{\text{load}} = 30\,\Omega$ and $L_{\text{load}} = 0.084$ mH). Values $\lambda_d = 0.5$ and $\lambda_u = 1$ have been used.

C. Robustness to Model Parameter Variation

Here, the robustness of the proposed algorithm to model parameter variations is investigated. In order to do that, the behavior of the system is first tested in simulation for a large number of different L_f and C_f settings, while the parameters of the physical part of the simulation are kept fixed according to Table II. With this approach, a clear picture about the robustness of the controller can be obtained, where the behavior of the system for some key parameter sets can be easily verified experimentally, as it will be shown in the next section.

In particular, L_f was varied in the model from 0.4 to 10 mH in step of 0.1 mH, whereas C_f from 4 to 70 μF in step of 1 μF. For each combination of L_f and C_f parameters, an individual discrete model of the system is created as described in Section III, and one simulation was run. To this end, 6500 simulations have been executed in total, where both the THD and the amplitude error of fundamental harmonic were captured. The results are shown in Fig. 11. In particular, Fig. 11(a) shows the variation of THD of the output capacitor voltage, Fig 11(b) shows the variation of magnitude of fundamental harmonics from the reference, while Fig. 11(c) shows simply a summation of those two metrics to indicate the best L_f and C_f settings in general.

By observing the respective figures above, some interesting features of the algorithm can be observed:

1) Algorithm is extremely robust to parameter uncertainty—stability is not lost even under high mismatch between the parameters used by the algorithm and those existing in the physical system. This characteristic cannot be achieved using conventional control techniques. For instance, other controllers always identify fairly conservative bounds for permissible parameter variations to ensure stability (e.g., see [41] for repetitive control, [42] for combined deadbeat and linear matrix inequality-based control, or [39] for hierarchical linear control).
2) Fundamental harmonic tracking is somewhat more sensitive to inductance variation, while THD of the output voltage has similar sensitivity to inductance and capacitance variation.
3) Algorithm behaves better (lower combined THD and amplitude error) when it uses somewhat lower filter parameter values than in the physical system [see Fig. 11(c)]. In particular, setting the value $L_f = 2.2$ mH and $C_f = 11$ μF in the algorithm, results in slightly better performance than setting $L_f = 2.4$ mH, and $C_f = 25$ F, which corresponds to the real physical parameters. Nevertheless, excellent performance can be observed for a wide range of parameter variations around the optimal point, so precise setting is not of crucial importance.

The analytical observations given above are also confirmed by experimental results for several key sets of L_f and C_f values used by the internal model. The experimental tests are elaborated in more detail the next section.

D. MG Operation

As a proof of concept, power sharing properties for two VSCs connected in parallel using the strategy explained in Section V

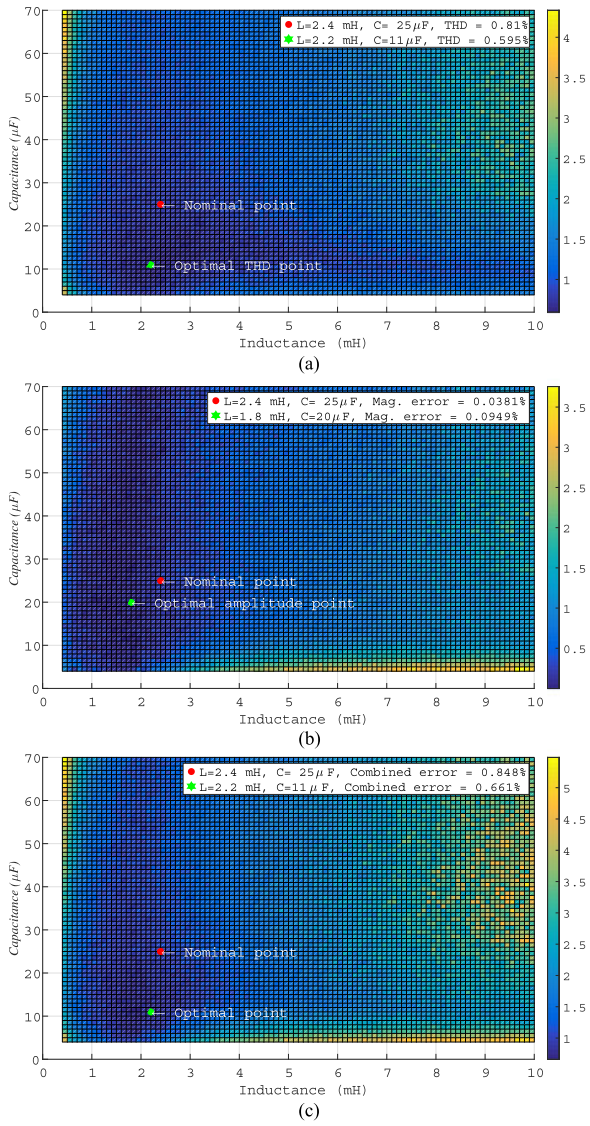

Fig. 11. Effects of changing the parameters in the internal model used by the FCS-MPC algorithm on the performance of the system. In each plot, the simulations using nominal L_f and C_f settings, and those resulting in best performance are indicated too. (a) Effect of changing the parameters on the THD of the output voltage. (b) Effect of changing the parameters on the amplitude error of the fundamental harmonic of the output voltage. (c) Effect of changing the parameters on the combined THD and amplitude error of the fundamental harmonic of the output voltage.

have been tested for the linear load. The respective droop and virtual impedance settings are shown in Table II. It should be noted that λ_u in one of the VSCs has been purposely set to 0.97 so that the two VSCs generate slightly different phase voltages on filter capacitors. This essentially emulates the real-world conditions where the voltages of two or more VSCs are not synchronized with each other. In addition, the VSCs were physically separated. For that reason, an inductance L_{oi} has been connected after the LC filter of each converter in order to reduce the circulating currents.

It is important to notice that addition of L_{oi} changes the configuration of the filter of each VSC from LC to LCL. However, due to overall control structure, the L_{oi} portion of the filter is

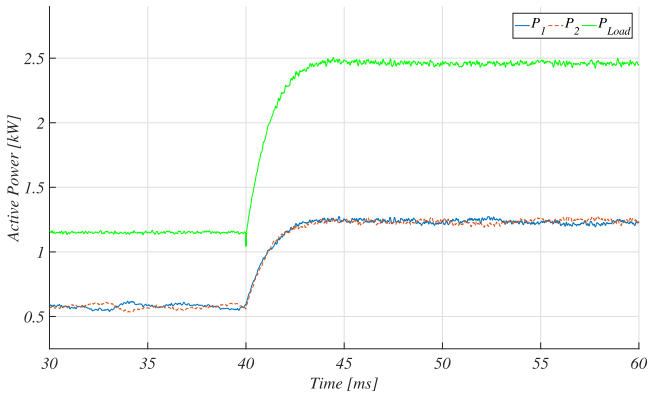

Fig. 12. Active power sharing performance with two VSCs connected in parallel.

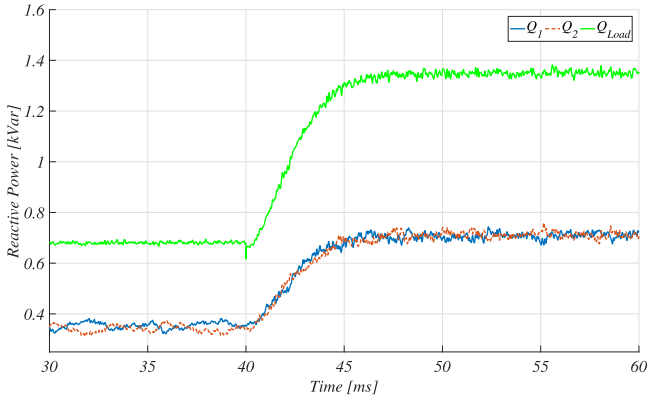

Fig. 13. Reactive power sharing performance with two VSCs connected in parallel.

decoupled from the inner LC part. Namely, as the FCS-MPC controller only regulates the voltage on the LC part of the filter, the algorithm sees the current flowing through the L_{oi} only as the load current. As it has been shown earlier in the paper, the controller is extremely robust and has high dynamic performance, so it is able to precisely regulate the voltage on the LC part. In this sense, there is effectively no difference between this configuration and feeding a standalone RL load. Therefore, the value of L_{oi} has a negligible influence on dynamics of the system here.

Nonetheless, harmonic voltage distortion at the LC part of each VSC cannot be avoided. When more VSCs are connected in parallel, these distortions produce circulating currents among them. Therefore, control of circulating current should be the main criteria in selecting the inductance value. In particular, L_{oi} = 2.4 mH was chosen empirically, as it was shown to result in acceptable level of circulating current between the inverters.

Using those settings, a combined resistive and inductive load step has been applied at the common ac bus at t = 40 ms. Figs. 12 and 13 demonstrate rapid active and reactive power sharing capability following a load change and also the ability to maintain a good power sharing accuracy in the steady state. It is important to notice that the ability to share the power during transient period is much more accurate compared to, e.g., [11, Fig. 15] which uses hierarchical linear control methodology. It should also be highlighted, that the power oscillations are kept relatively low due to good steady-state performance resulting from the proposed CF stated in (26), but also due to L_{oi}.

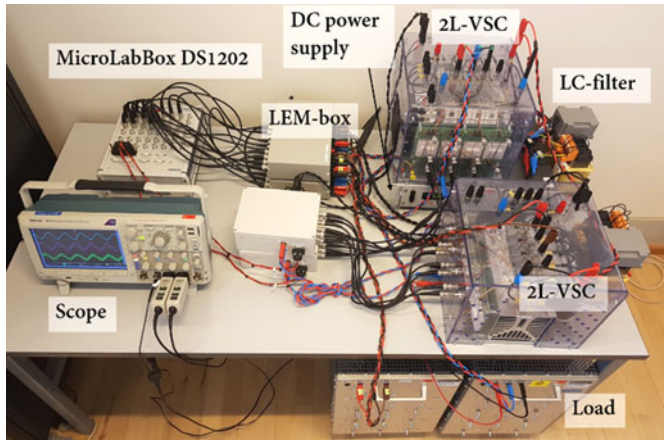

Fig. 14. Photo of the experimental setup.

VII. Experimental Verification

The proposed control algorithm was verified experimentally, where an 18-kW-rated test system, shown in Fig. 14, was built for that purpose. The power stage comprises a Delta Elektronika SM 600-10 dc power supply, two Semikron two-level three-phase VSCs, a linear load, and a nonlinear load. The test setup corresponds to the one presented in Fig. 6, with parameters given in Table II. Three sets of tests are carried out. First, Section VII-A verifies steady state and transient performances with nominal system settings when feeding linear and nonlinear loads. Second, in Section VII-B, it is explained how to compensate the computational delay in the software, where the phase voltages are shown for the cases before and after the compensation. Finally, in Section VII-C, the effects of model parameter uncertainty on the performance of the system are tested to validate the results shown in Fig. 11(c).

A. Evaluation of Proposed CF Under Nominal Settings

For the nominal settings of the model parameters, three sets of tests have been carried out. Each one of them for two settings of weight coefficient corresponding to either a conventional ($\lambda_d = 0$), or proposed ($\lambda_d = 0.5$) control strategy. First test was done to evaluate the steady-state performance when feeding a linear load R_l = 33 Ω. Measured line-to-line capacitor voltages for conventional and proposed strategy are shown in Fig. 15(a) and (b), respectively.

Second test evaluates the performance of the algorithm during abrupt load connection for both strategies. Measured values of v_{fcb} and i_{oa} are shown in Fig. 15(c) and (d). Finally, the steady-state performance when feeding a nonlinear load (diode rectifier with parallel connection of C_n and R_n with values given in Table II) is presented in Fig. 15(e) and (f). Fundamental voltage amplitude and THD calculations are reported within the

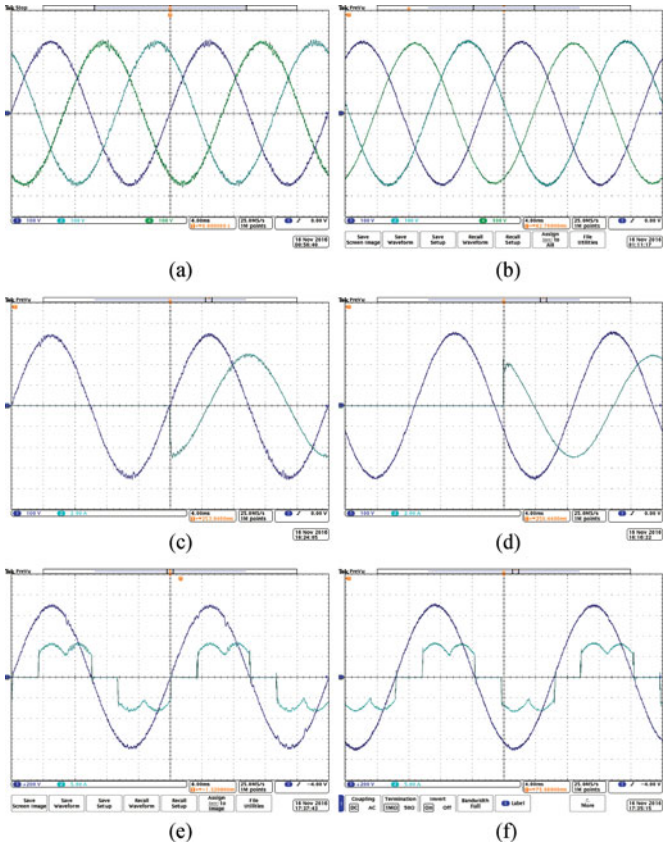

Fig. 15. Experimental validation of proposed control strategy. (a) Conventional strategy. Fundamental voltage amplitude: 342.5 V (1.13% error), Voltage THD: 2.16%. (b) Proposed strategy. Fundamental voltage amplitude: 345.6 V (0.23% error), Voltage THD: 1.10 %. (c) Linear load connection instance (33 Ω) for conventional strategy. v_{fcb} and i_{oa} are shown. (d) Linear load connection instance (33 Ω) for proposed strategy. v_{fcb} and i_{oa} are shown. (e) Conventional strategy when supplying a nonlinear load (diode rectifier with parameters in Table II). v_{fcb} and i_a are shown. Fundamental voltage amplitude: 341.9 V (1.3% error), Voltage THD: 2.31%. (f) Proposed strategy when supplying a nonlinear load (diode rectifier with parameters in Table II). v_{fcb} and i_a are shown. Fundamental voltage amplitude: 345.3 V (0.32% error), Voltage THD: 1.22%.

figure captions which reveal superior performance of proposed method with approximately 50% reduction in THD and 1% better fundamental voltage tracking performance (around 3.5 V in line–line voltages).

B. Effect of Computational Delay and Its Compensation

In practical implementation of the FCS-MPC algorithm, digital hardware requires a certain processing time to execute the code. Therefore, the optimal voltage vector $\bar{v}_i$ becomes available in between the two sampling/switching periods, which means that it can only be applied with T_s delay. This delay needs to be compensated for proper functioning of the algorithm. In particular, a delay compensation elaborated in [43] is the one most commonly used for this purpose. For completeness of this paper, the basic principle of this method is summarized below:

1) The fresh measurements of the signals $\bar{i}_f$, $\bar{v}_f$, $\bar{i}_o$ are obtained.
2) The model in (14) is used to predict how those variables will propagate according to currently active voltage vector. This step provides the expected set of variables after the T_s delay.
3) Variables calculated from (2) are used again in the model (14) to predict how those variables will further propagate for all possible actuations $\bar{v}_i$.
4) Finally, all the predictions from (3) are evaluated in the CF, where the actuation with minimal cost is applied.

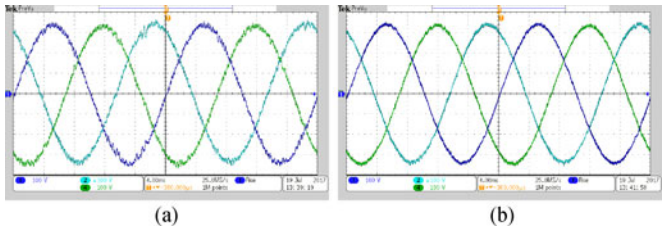

Fig. 16. Phase voltages, before and after compensating the computational delay. (a) Phase voltages without compensating the T_s delay. (b) Phase voltages after compensating the T_s delay.

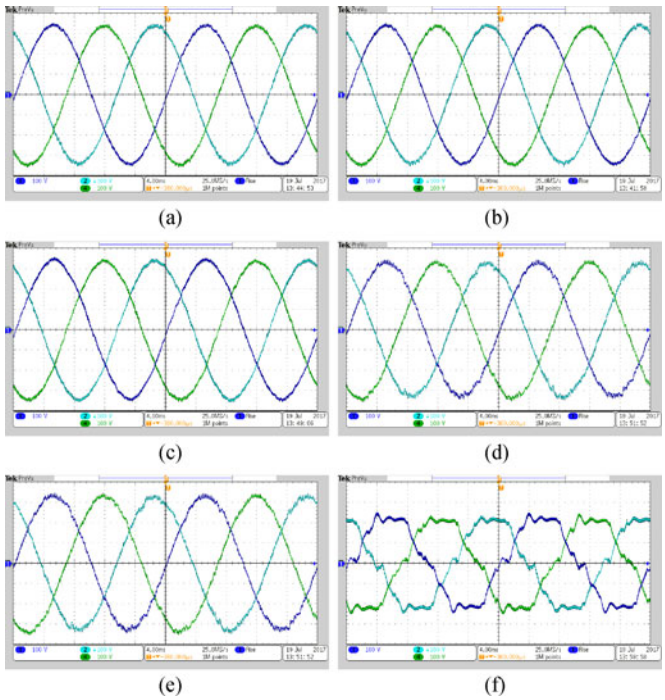

Fig. 17. Experimental results for validation of model parameter uncertainty. (a) L_f and C_f are set to nominal values from Table II. (b) L_f and C_f are set to 2.2 mH and 11 μF, respectively. This values correspond to optimal point from Fig. 11(c), (c) L_f and C_f are set to 2 mH and 70 μF, respectively. (d) L_f and C_f are set to 10 mH and 15 μF, respectively. (e) L_f and C_f are set to 10 mH and 70 μF, respectively. (f) L_f and C_f are set to 1 mH and 4 μF, respectively.

Fig. 16 compares the two cases, i.e., when delay is not compensated to situation when it is. In particular, Fig. 16(a), a noticeable distortion in the output voltage can be seen for the first case. On the other hand, significant reduction in THD can be observed in (b), where delay compensation technique is applied.

C. Model Parameter Uncertainty

Here, the model parameter uncertainty is experimentally validated. In particular, Fig. 17 shows results for six different sets of settings of L_f and C_f in the model.

It can be seen that experimental results are consistent with the simulation results from Fig. 11(c). Again, it is observed that the control algorithm is very robust against parameter uncertainties. It remains stable under high parameter mismatch (e.g., when L_f and C_f are chosen as approximately six times smaller and four times bigger than in reality, respectively). It should be noted, however, that the performance of point where $L_f = 0.4$ mH and $C_f = 4$ μF is somewhat worse in experimental setup than predicted in simulations. This could be attributed to imperfect switching procedures and dead time effects which cannot be handled by the algorithm under the extreme parameter mismatch.

On the other hand, for somewhat smaller, but still considerable parameter mismatch the performance of the algorithm remains reasonably good, as predicted by simulation results. Finally, when setting the parameters corresponding to point nominal or optimal parameters, the best performance can be observed.

VIII. Conclusion

In this paper, a finite control set model predictive control strategy for power electronics converters that form an ac MG is presented. First, a simple and intuitive modification of the conventional FCS-MPC for a two-level three-phase VSC with an output LC filter which allows explicit tracking of the derivative of the capacitor voltage trajectory was proposed. This modification allows significant improvement of the converter's voltage tracking performance compared to the reference case for both linear and nonlinear loads, while still relying only on one step prediction. In this respect, the steady-state performance of the system becomes comparable with the CB-PWM, but with much faster dynamic performance and significantly improved robustness compared to conventional methods. When VSCs are connected together in an ac MG using a droop control strategy, they demonstrate a rapid and accurate power sharing performance in both transient and steady-state conditions. All the findings of the paper have been also verified experimentally on a dual inverter test-setup.

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