Project Report

ARM Simulator

25th October 2017

Manish Mahalwal 2016054
Raj Kamal Yadav 2016076
Rahul Patwardhan 2016075

ARM Simulator

Design and implement the function simulator in Java for subset of ARM instructions discussed in class

LANGUAGE: Java.

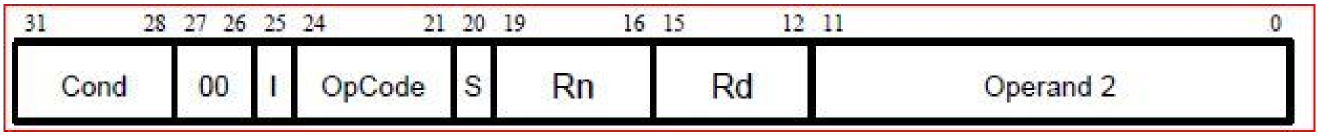
IMPLEMENTATION:

Memory is implemented as a HashMap of pair of strings where the key is address and the value is of type Instruction.

Register is implemented as an array representing the 16 GPR registers.
Including Stack pointer at 13, Program counter at 15.
CPSR flags Z (zero) and N (negative)
Stack pointer is initialised to 21504
PC is initialized 4096.
All other registers are zero.

ARM conditions instructions

Code	**Suffix**	**Flags**	**Meaning**
0000	**EQ**	**Z =1**	**set equal**
0001	**NE**	**Z =0**	**not equal**
0100	**MI**	**N =1**	**negative**
0101	**PL**	**N=0**	**positive or zero**
1110	**AL**	**(ignored)**	**always**



OPCODES:

0000 = AND

Rd= Op1 and Op2

0010 = SUB

Rd= Op1 - Op2

0100 = ADD

Rd= Op1 + Op2

1010 = CMP

set condition bits on Op1 - Op2

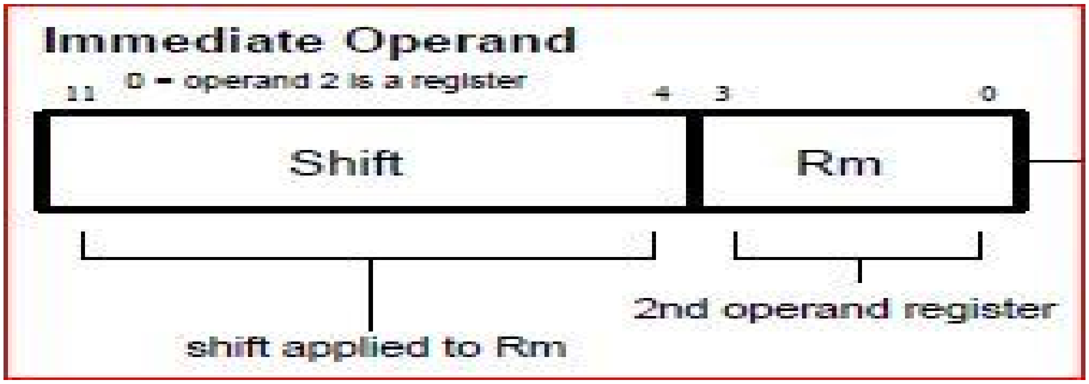
1100 = ORR

Rd= Op1 | Op2

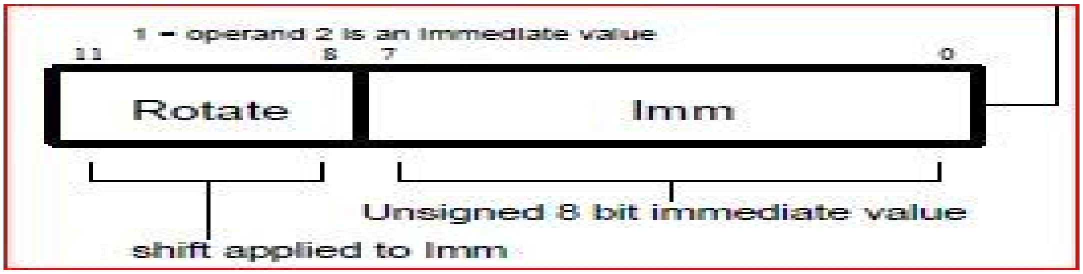
1101 = MOV

Rd= Op2

When bit 25 in the instruction word is 0 the operand 2 field is of this type.

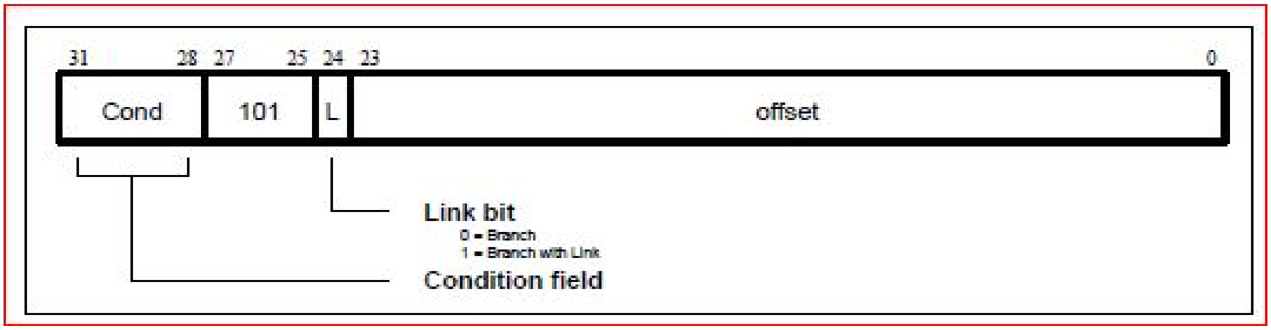


When bit 25 in the instruction word is 1 the operand 2 field is of this type.

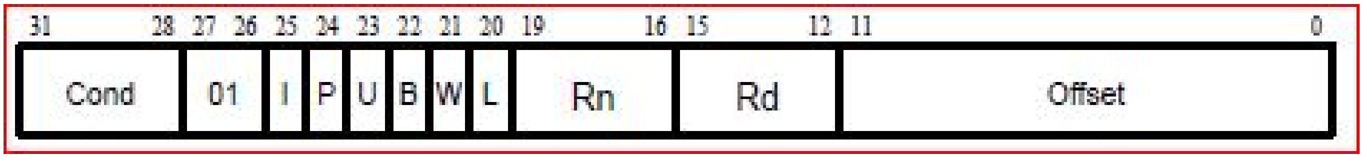

1 = operand 2 is an immediate value
11
8
7
0
Rotate
Imm
Unsigned 8 bit immediate value
shift applied to Imm

BRANCH TYPE INSTRUCTIONS:

This type of instruction word contains a signed 2's complement 24 bit offset. The instruction word is sign extended to 32 bits, by adding 8 zero bits and added to the PC.



LOAD AND STORE INSTRUCTIONS



This instruction is executed only when the condition bits are true.
The load/store instructions are used to load or store single bytes or words of data. The memory address used in the transfer is calculated by adding an offset to or subtracting an offset from a base register.
The result of this calculation may be written back into the base register if auto-indexing is required.

CITATION:

ARM7TDMI-S Data Sheet
ARM DDI 0084D