

8.10 TIMING DIAGRAMS FOR 8085 INSTRUCTION

The instructions of 8085 are one, two or three byte instructions. The timing diagram of each instruction is combination of opcode fetch cycle, memory read cycle, memory write cycle, I/O read cycle, I/O write cycle and INTA cycle. The first machine cycle in each instruction is opcode fetch cycle of length 4T or 6T states. The number of machine cycles required for each instruction depends up on type of instruction, and availability of operand i.e. in memory or registers.

After fetching the instruction it requires additional machine cycles if the operand is available in memory. The minimum number of machine cycles or T states required for one, two or three byte instruction is given in table 8.5.

Table 8.5.

Type of Instruction	Minimum		Additional		Total	
	Machine Cycles	T states	Machine Cycles	T states	Machine Cycles	T states
One Byte	1 (OF)	4/6	Operand Availability	Operand Availability		
For example MOV A, B MOV A, M	1 (OF) 1 (OF)	4 4	- 1 (MR)	- 3	1 2	4 7
Two Byte	1 + 1 (OF) (OPF/MR)	4/6 + 3	Operand Availability	Operand Availability		
For example MVI A, 02 MVI M, 02	1 + 1 (OF) (OPF/MR) 1 + 1 (OF) (OPF/MR)	4 + 3 4 + 3	- 1 (MW)	- 3	2 2	7 10
Three Byte	1 + 1 + 1 (OF) (OPF/MR) (OPF/MR)	4/6 + 3 + 3	Operand Availability	Operand Availability		
For example LX14, 7000 STA 7000	1 + 1 + 1 (OF) (OPF/MR) (OPF/MR) 1 + 1 + 1 (OF) (OPF/MR) (OPF/MR)	4 + 3 + 3 4 + 3 + 3	- 1 (MW)	- 3	3 4	10 13

TIMING DIAGRAMS

8.10.1 MOV r₁, r₂

This instruction copy the content of r₂ register to r₁ register.

$$(r_1) \leftarrow (r_2)$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
One byte	1 (OF)	4	-	-	1	4

Only opcode fetch machine cycle is required to fetch and execute this instruction. Assume that the instruction is stored at memory location 7000H.

7000 Opcode of MOV r₁, r₂ Opcode fetch

The timing diagram is shown in fig. 8.12.

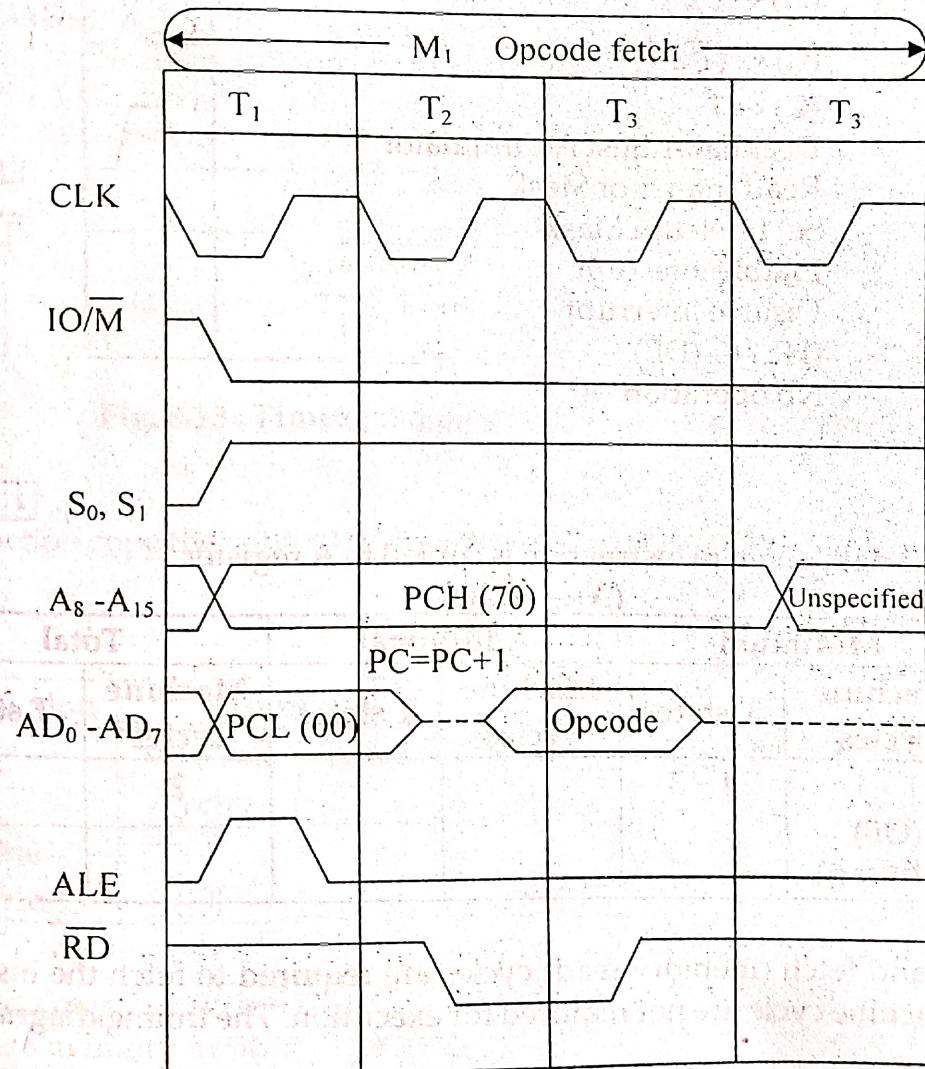


Fig. 8.12 : Timing diagram MOV r₁, r₂ instruction

The timing diagram for following instruction is same as fig. 8.12. These instruction are one byte instruction and doesnot require T5 and T6 states. No additional machines cycles are not required for execution.

8.10.2 MVI A, data :

The 8-bit immediate data given in instruction is copied to A register

$(A) \leftarrow (\text{Data})$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
Two Byte	1 + 1 (OF) (OPF/MR)	4 + 3	-	-	2	7

Opcode fetch and operand fetch (memory read) cycles are required to fetch the instruction from memory. Additional machine cycle are not required for execution. The timing diagram is shown in fig. 8.13.

Assume that instruction is stored from memory location from 7000H.

For example : MVI A, 25

7000 3E (Opcode) Opcode Fetch

7001 25 (Data) Operand Fetch or Memory Read

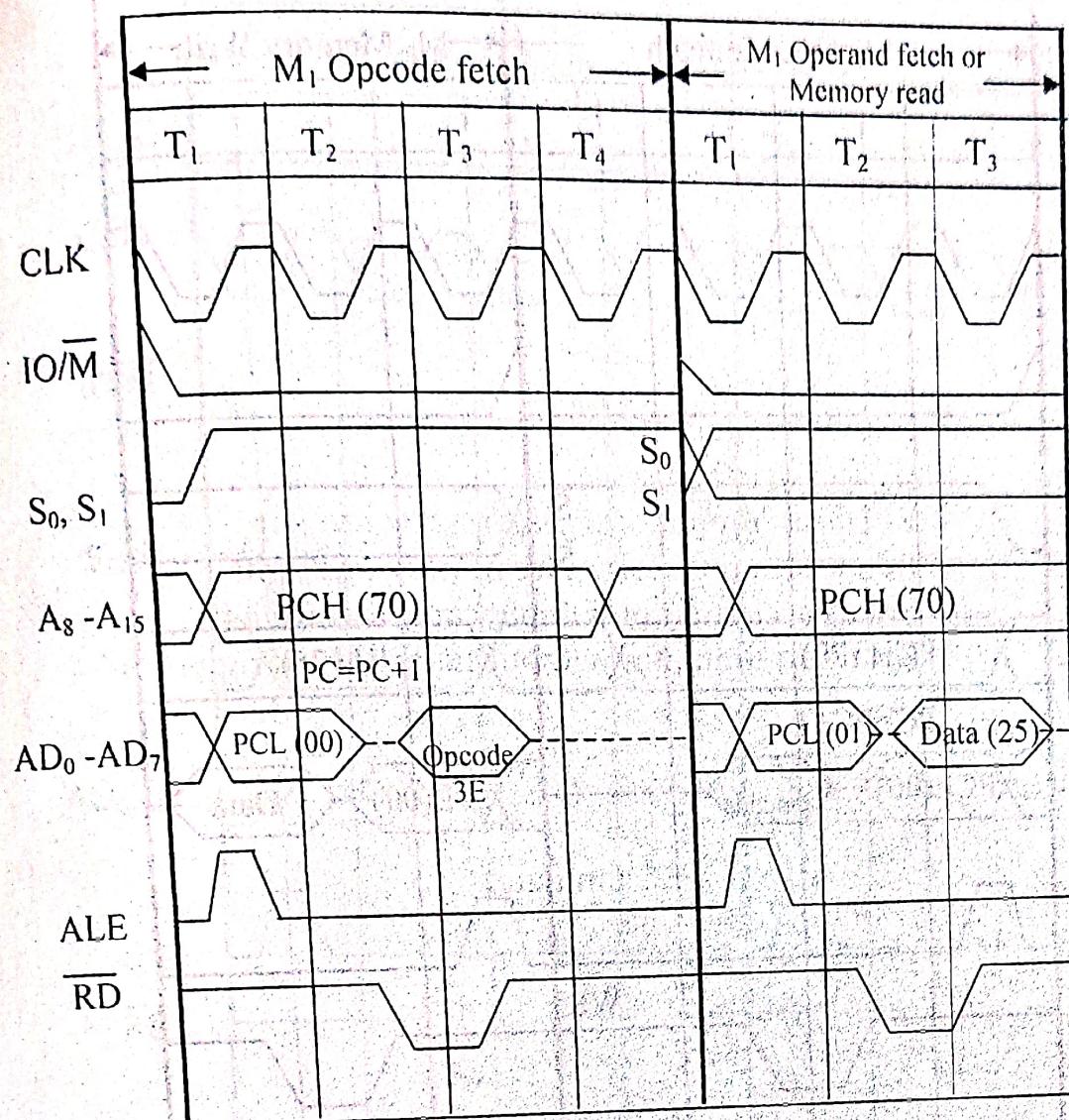


Fig. 8.13 : Timing diagram for MVI A, data instruction

8.10.3 MOV M, r

This instruction copy the content of register r to memory location addressed by HL pair

$$[[\text{HL}]] \leftarrow (\text{r})$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
One Byte	1 (OF)	4	1 (MW)	3	2	7

Opcodes for this instruction are 7E and 7F. The timing diagram is shown in fig. 8.14. Assume that instruction is stored from memory location from 7000H.

For Example : MOV M, A

Assume HL = 7500
7000 Opcode (7E) Opcode Fetch
7500 Data Memory Write

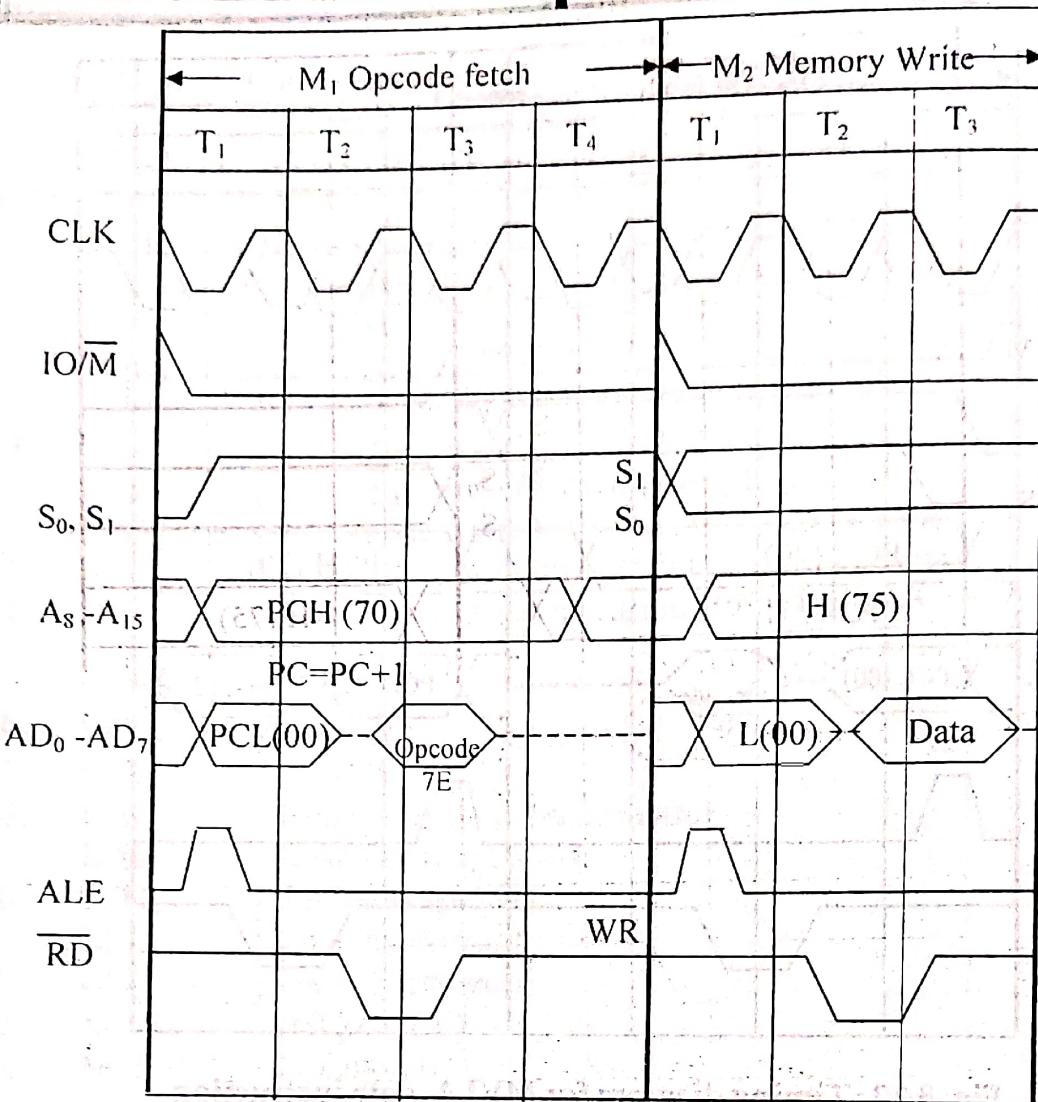


Fig. 8.14 : Timing diagram for MOV M, r instruction

8.10.4 MOV r, M

This instruction copy the content of memory location addressed by the HL pair to register r.

$$(r) \leftarrow [(HL)]$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
One Byte	1 (OF)	4	1 (MR)	3	2	7

Opcodes fetch and memory read cycles are required. Additional machine cycle is required to copy the content of memory location to register. The timing diagram is shown in fig. 8.15. Assume that instruction is stored from memory location from 7000H.

For Example : MOV A, M

Assume HL = 7500

7000	Opcode (77)	Opcode Fetch
7500	Data	Memory Read

TIMING

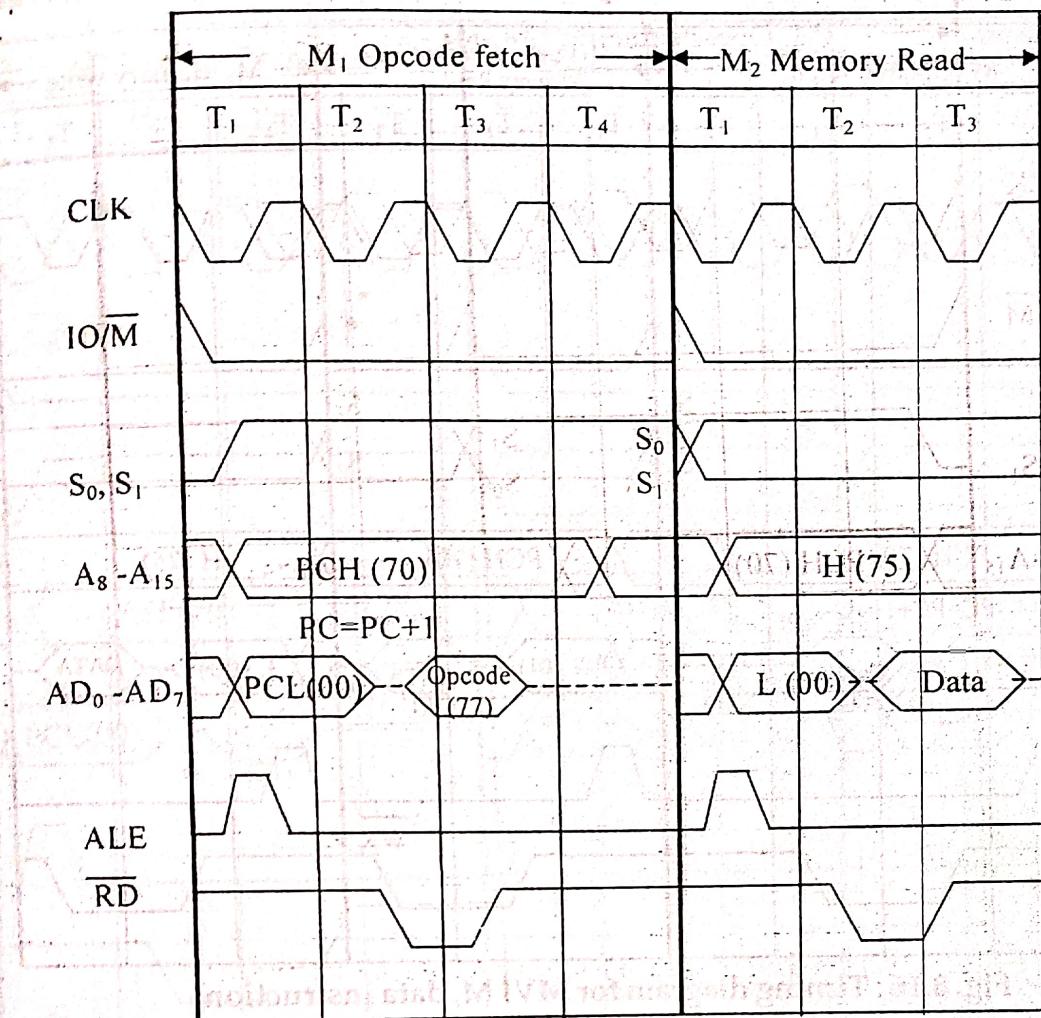


Fig. 8.15 : Timing diagram for MOV r, M Instruction.

8.10.5 MVI M, data

This instruction copy the data given in instruction to memory location addressed by the HL pair.

$$[(HL)] \leftarrow [(Data)]$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
Two byte	1 + 1 (OF) (OPF/MR)	4 + 3	1 (MW)	3	3	10

The two machine cycle i.e. opcode fetch and operand fetch (memory read) cycles are required to fetch instruction from memory. Additional machine cycle is required to copy the data to memory location. The timing diagram is shown in fig. 8.16.

Assume that instruction is stored from memory location from 7000H.

For example : MVI M, 55

Assume HL = 7500

7000	Opcode (36)	Opcode Fetch
7001	55	Operand Fetch/ Memory Read
7500	Data	Memory Write

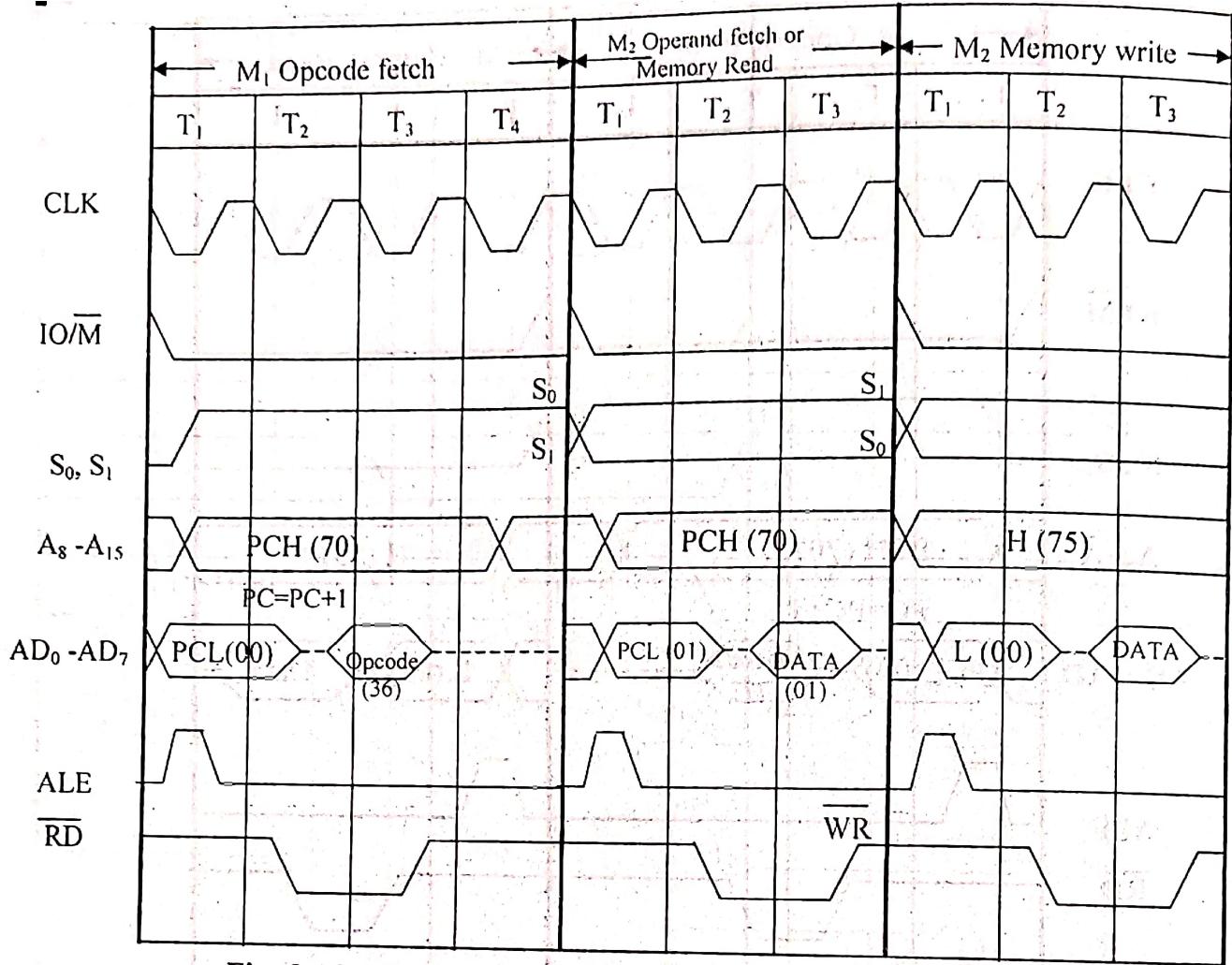


Fig. 8.16 : Timing diagram for MVI M, data instruction

8.10.6 LXI rp, data 16

The 16 bit data specified in the instruction is copied to rp.

$$(rp) \leftarrow \text{Data 16}$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
Three Byte	1 + 1 + 1 (OF) (OPF/MR) (OPF/MR)	4 + 3 + 3	-	-	3	10

The three machine cycles are required to fetch instruction from memory. Additional machine cycle is not required for execution. The timing diagram is shown in fig. 8.17. Assume that instruction is stored from memory location 7000H.

For example : LXI H, 7500

- 7000 opcode (21)
- 7001 low order data (00)
- 7002 high order data (75)

Opcode Fetch
Operand Fetch/ Memory Read
Operand Fetch/ Memory Read

TIMING DIAGRAM

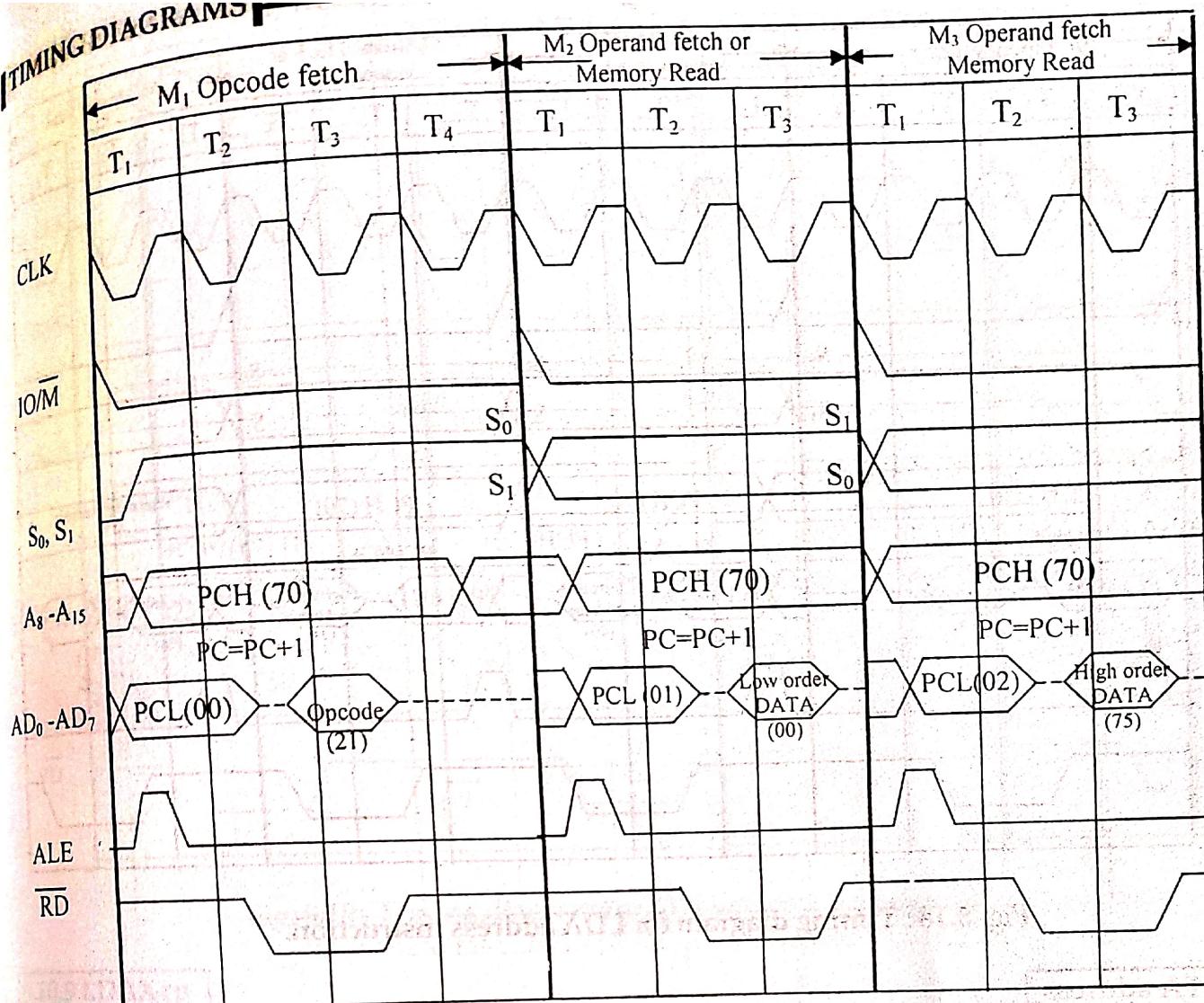


Fig. 8.17: Timing diagram for LXI rp, data 16

8.10.7 LDA address

This instruction loads the content of memory location whose address is specified in instruction to A register.

(A) \leftarrow (address)

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
Three Byte	1 + 1 + 1 (OF) (OPF/MR) (OPF/MR)	4 + 3 + 3	1 (MR)	3	4	13

The three machine cycles are required to fetch instruction from memory. Additional machine cycle is required to load content of memory to A register. The timing diagram is shown in fig. 8.18. Assume that instruction is stored from memory location 7000H.

For example : LDA 7500

- | | | |
|------|----------------------|----------------------------|
| 7000 | Opcode | Opcode Fetch |
| 7001 | Lower order address | Operand Fetch/ Memory Read |
| 7002 | Higher order address | Operand Fetch/ Memory Read |
| 7500 | Data | Memory Read. |

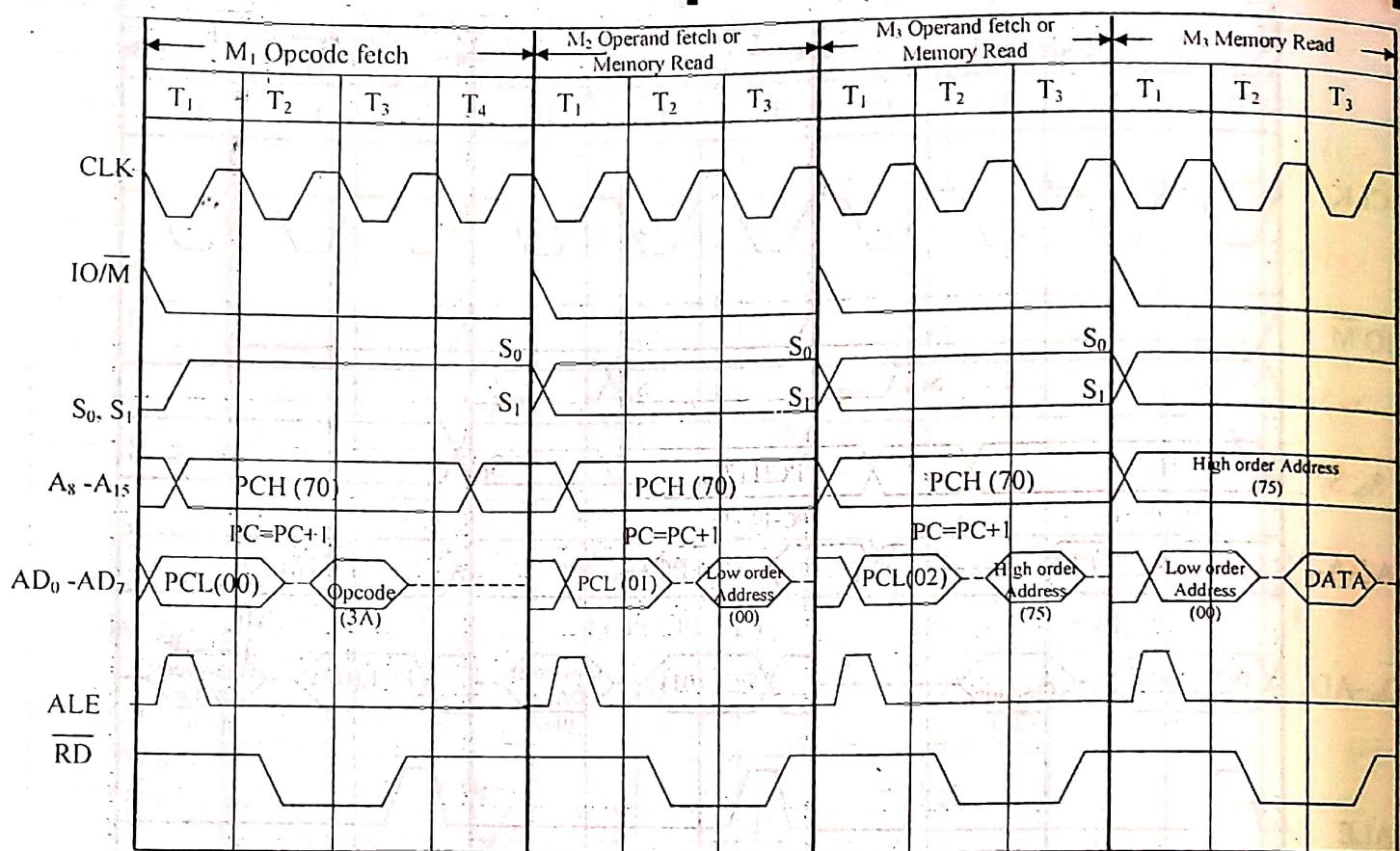


Fig. 8.18 : Timing diagram for LDA address instruction.

8.10.8 STA address

This instruction stores the content of A register to memory location whose address is specified in instruction.

(Address) \leftarrow (A)

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
Three Byte	1 + 1 + 1 (OF) (OPF/MR) (OPF/MR)	4 + 3 + 3	1 (MW)	3	4	13

The three machine cycles are required to fetch instruction from memory. Additional machine cycle is required to store the content of A register to memory. The timing diagram is shown in fig. 8.19. Assume that instruction is stored from memory location 7000H.

For example : STA 8000

7000 Opcode (32)

7001 Lower order address

7002 Higher order address

8000 Data

Opcode Fetch

Operand Fetch/ Memory Read

Operand Fetch/ Memory Read

Memory Write.

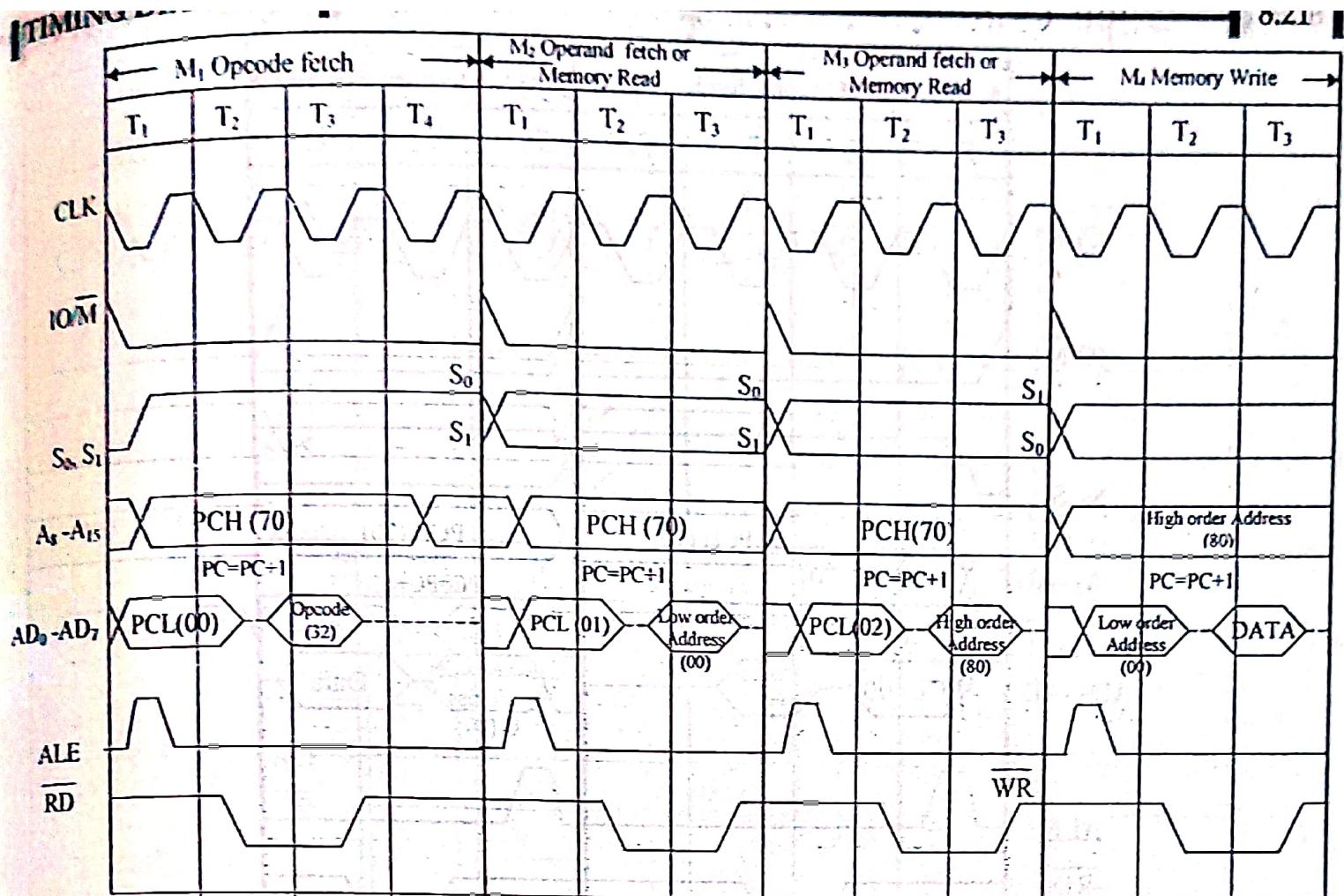


Fig. 8.19: Timing diagram for STA address instruction.

8.10.9 LDAX rp

This instruction transfers the content of memory location addressed by register pair rp to accumulator.

$$(A) \leftarrow [rp]$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
One Byte (OF)	1	4	1	3	2	7

Only one machine cycle is required to fetch instruction from memory. Additional machine cycle is required to load data from memory to accumulator. The timing diagram is shown in fig. 8.20. Assume that instruction is stored from memory location 7000H.

For Example : LDAX B

Assume BC = 7500

7000	opcode (0A)	Opcodes Fetch
7500	Data	Memory Read

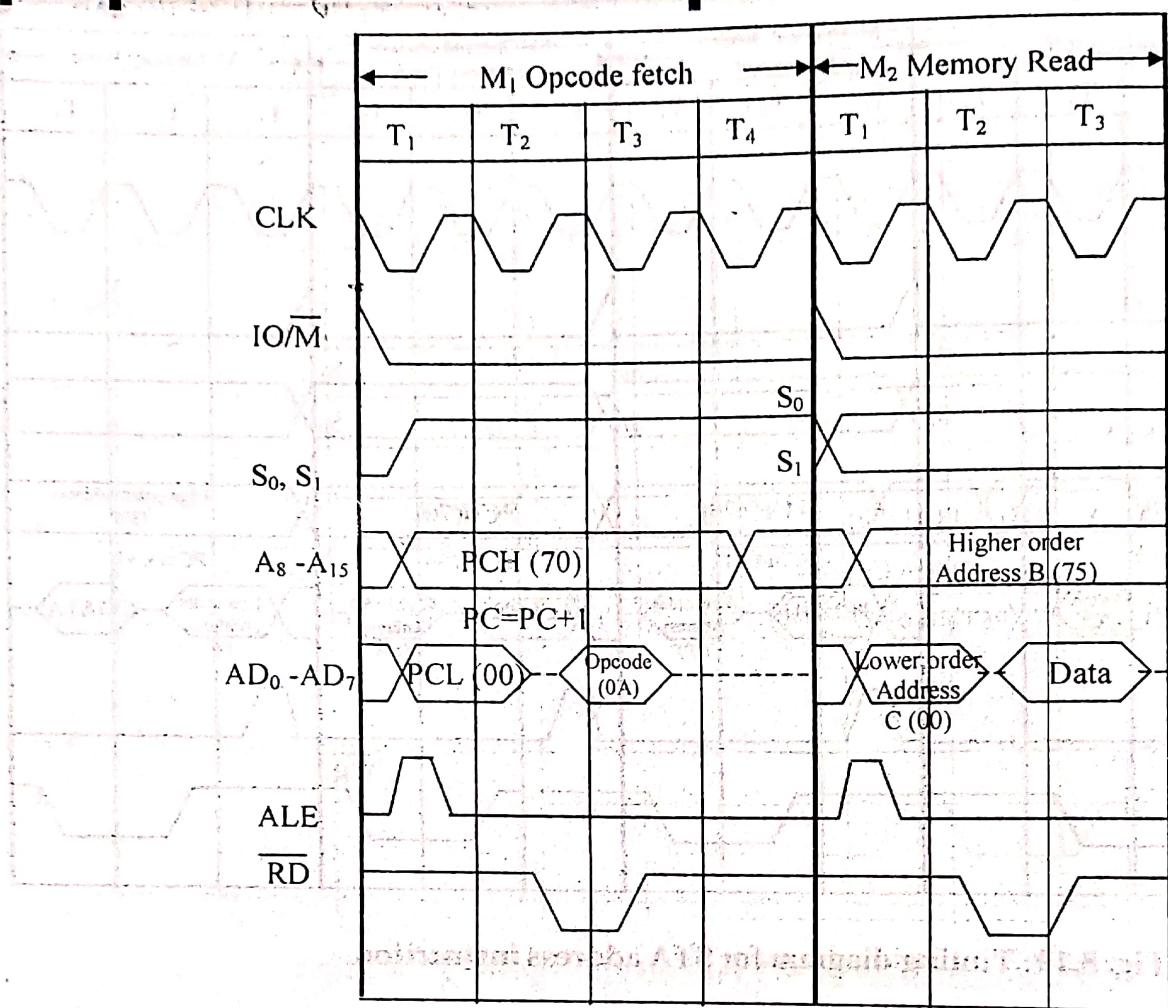


Fig. 8.20: Timing diagram for LADX rp Instruction.

8.10.10 STAX rp

This instruction stores the contents of accumulator to memory location addressed by register pair rp.

$[(rp)] \leftarrow (A)$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
One Byte (OF)	1	4	1	3	2	7
(MW)						

One machine cycle is required to fetch instruction from memory. Additional machine cycle is required to store the content of accumulator to memory. The timing diagram is shown in fig. 8.21. Assume that instruction is stored from memory location 7000H.

For Example : STAX D

Assume DE = 8000

7000	opcode (12)	Opcodes Fetch
8000	Data	Memory Write

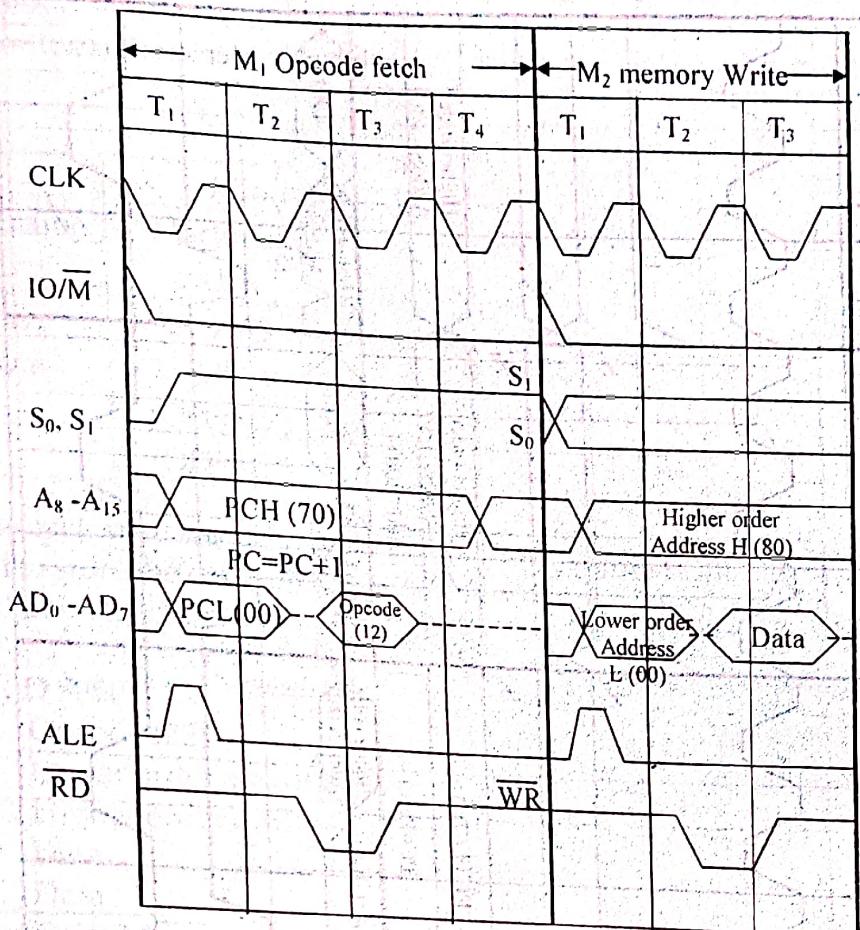


Fig. 8.21: Timing diagram for STAX rp Instruction.

8.10.11 LHLD address

This instruction load the content of memory location to HL pair.

$$\begin{aligned} (L) &\leftarrow (\text{Address}) \\ (H) &\leftarrow (\text{Address} + 1) \end{aligned}$$

Instruction	Minimum		Additional		Total	
	Machine cycles	T states	Machine cycles	T states	Machine cycles	T states
Three byte	1 + 1 + 1 (OF) (OPF/MR) (OPF/MR)	4 + 3 + 3	1 + 1 (MR) (MR)	3 + 3	5	16

Three machine cycles are required to fetch instruction from memory. Two additional machine cycles are required to load the content of memory location to HL pair. The timing diagram is shown in fig. 8.22. Assume that instruction is stored from memory location 7000H.

For example : LHLD 8050

7000	Opcode (2A)	Opcode Fetch
7001	Lower order address (50)	Operand Fetch/ Memory Read
7002	Higher order address (80)	Operand Fetch/ Memory Read
8050	Data	Memory Read.
8051	Data	Memory Read.

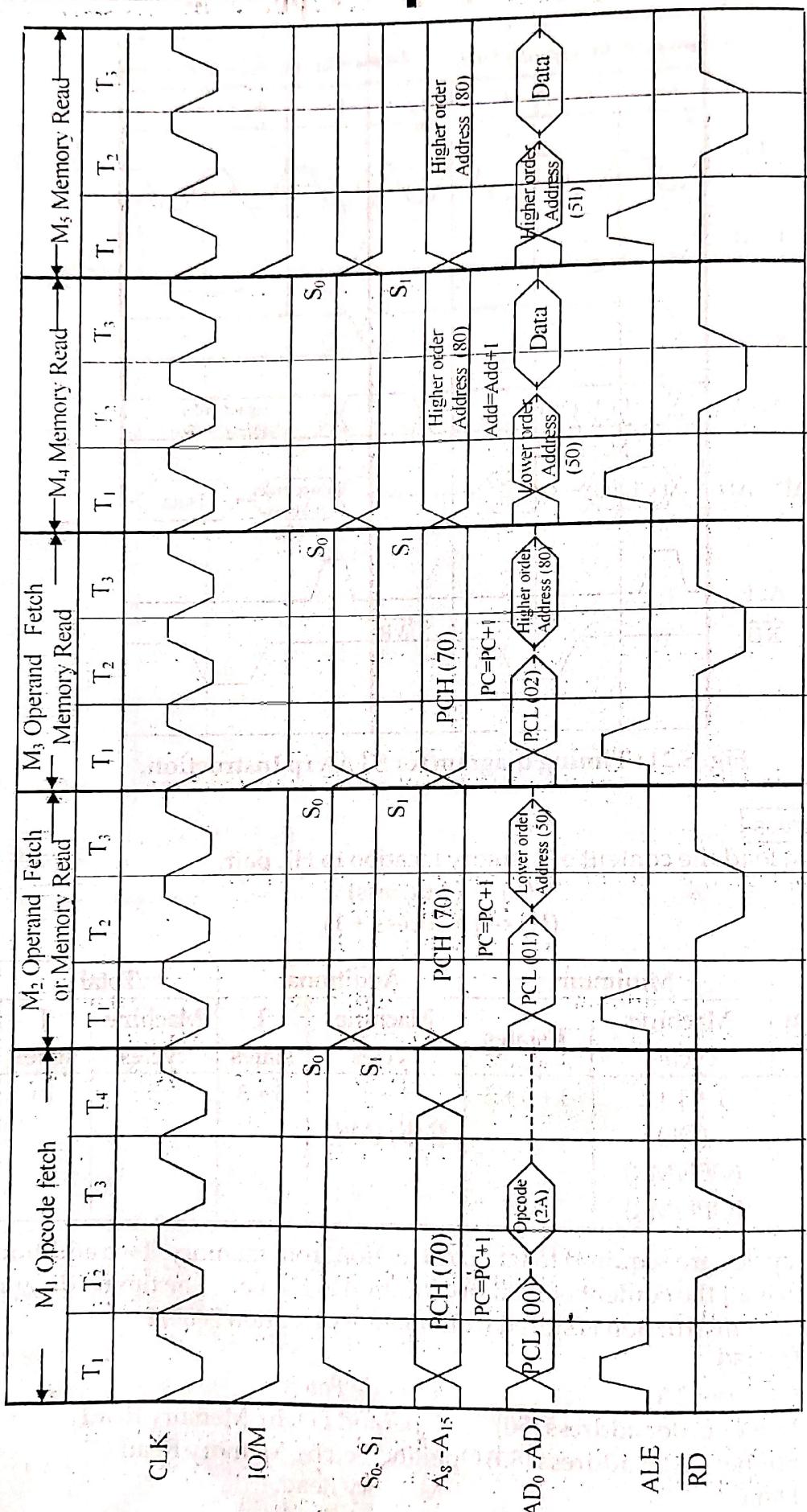


Fig. 8.22 : Timing diagram for LHLD address instruction.