

## # 8255 (Programmable Peripheral Interface)

- The 8255 is a multipoint device, useful for interfacing peripheral devices.
- It has three 8-bit ports, namely Port A, Port B, & Port C.
- Port C further divided into two 4-bit ports : Port C Upper & Port C Lower.
- Therefore total 4 ports are available : two 8-bit ports and two 4-bit ports.
- Each port can be programmed either as an input port or output port.

PA3 ↔ 1	40 ↔ PA4
PA2 ↔ 2	39 ↔ PA5
PA1 ↔ 3	38 ↔ PA6
PA0 ↔ 4	37 ↔ PA7
RD → 5	36 ← WR
CS → 6	25 ← Reset
GND → 7	34 ↔ D0
A1 → 8	33 ↔ D1
A0 → 9	32 ↔ D2
PC7 ↔ 10	31 ↔ D3
PC6 ↔ 11	30 ↔ D4
PC5 ↔ 12	29 ↔ D5
PC4 ↔ 13	28 ↔ D6
PC0 ↔ 14	27 ↔ D7
PC1 ↔ 15	26 ← Vcc
PC2 ↔ 16	25 ↔ PB7
PC3 ↔ 17	24 ↔ PB6
PB0 ↔ 18	23 ↔ PB5
PB1 ↔ 19	22 ↔ PB4
PB2 ↔ 20	21 ↔ PB3

8255

- It is a 40 pin I.C., operates on 5V supply.
- PA0 - PA7 : 8 pins of port A.
- PB0 - PB7 : 8 pins of port B

PC<sub>0</sub> - PC<sub>3</sub> : 4 pins of Port C Lower

PC<sub>4</sub> - PC<sub>7</sub> : 4 pins of Port C Upper

→  $\overline{CS}$  (Chip Select)

The low status of signal enables communication between the CPU and 8255.

→  $\overline{RD}$  (Read)

When  $\overline{RD}$  goes low, it allows CPU to read data from the input port of 8255.

→  $\overline{WR}$  (Write)

When  $\overline{WR}$  goes low, it allows CPU to write data to the output port of 8255.

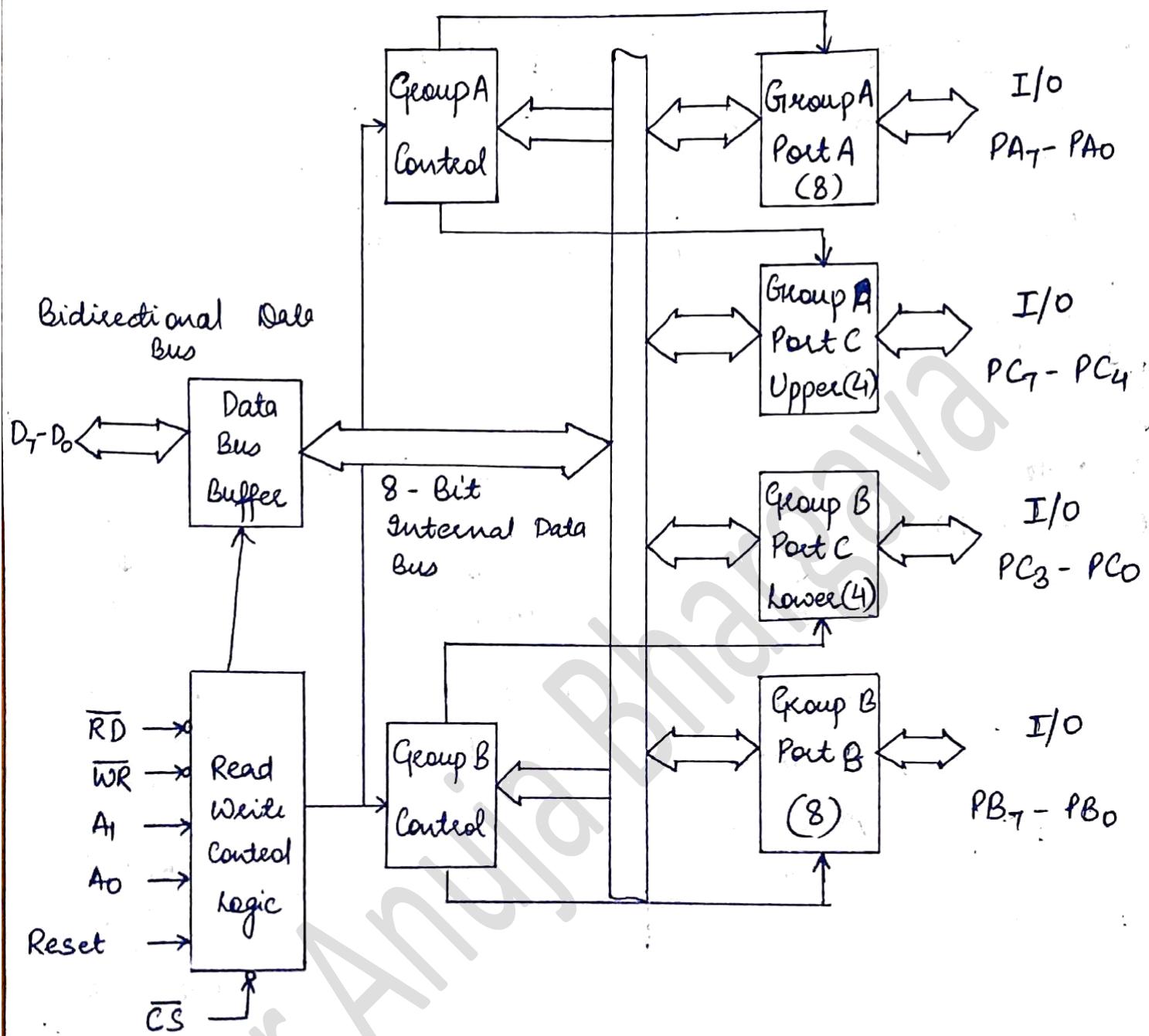
→ A<sub>0</sub> & A<sub>1</sub>

The selection of input port and control word register is done using A<sub>0</sub> and A<sub>1</sub>.

	A <sub>1</sub>	A <sub>0</sub>	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$
Port A → Data Bus 0	0	0	0	1	0
Port B → Data Bus 0	1	0	0	1	0
Port C → Data Bus 1	0	0	0	1	0
Data Bus → Port A 0	0	1	1	0	0
Data Bus → Port B 0	1	1	1	0	0
Data Bus → Port C 1	0	1	1	0	0
Data Bus → CWR 1	1	1	1	0	0

# # Block Diagram of 8255 :- (Architecture)

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→ The block diagram shows two 8-bit ports (A & B), two 4-bit ports ( $C_U$  &  $C_L$ ), data bus buffer and control logic.

→ The control section has six lines  
 $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{CS}$ ,  $A_0$ ,  $A_1$  (explained in PN Diagram)

Reset: It is active high signal, it clears the control register and sets all ports in input mode.

Architecture of 8255 consist of three sections.

### (1) Data Bus Buffer

- 3-state bi-directional, 8-bit buffer.
- It is used to interface the 8255 to the system bus.
- Based on input, data is transmitted or received.
- Here, control word or status information is also transferred.

### (2) Read / Write Control Logic

- The function of this block is to manage all of the internal & external transfer of both data & control or status word.

### (3) Group A & B Control

- The signals from CPU and send the command to individual control block.
- Group A send the control signal to Port A & Port C Upper.
- Group B send the control signal to Port B & Port C Lower.

Port A → It can be programmed by Mode 0, Mode 1, Mode 2

Port B → It can be programmed by mode 0 & mode 1.

Port C → It is splitted into two parts : C<sub>U</sub> & C<sub>L</sub>.

→ It can be programmed by Bit Set / Reset Operation

Control Word Register:-

Control Word

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
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Bit No. 0 : Used for Port C Lower

for Input port the bit is set to 1.

for Output port the bit is set to 0.

Bit No. 1 : Used for Port B.

for Input Port the bit is set to 1.

for Output Port the bit is set to 0.

Bit NO. 2 : Used for selection of Mode for Port B.

for Mode 0, the bit is set to 0.

for Mode 1, the bit is set to 1.

Bit NO. 3 : Used for Port C Upper.

for Input Port, the bit is set to 1.

for Output Port, the bit is set to 0.

Bit NO. 4 : Used for Port A.

for Input Port, the bit is set to 1.

for Output Port, the bit is set to 0.

Bit No. 5 & 6: These bits are to define operating mode of the Port A.

Mode of Port A                      Bit 6                      Bit 5

Mode 0                              0                              0

Mode 1                              0                              1

Mode 2                              1                              0 or 1

Bit No. 7: It is set to 1, for Simple Input / Output Mode.

It is set to 0, for BSR Mode.

~~Simple~~

## Modes of 8255 :-

- ① Simple Input Output Mode.
- ② Bit Set / Reset Mode.

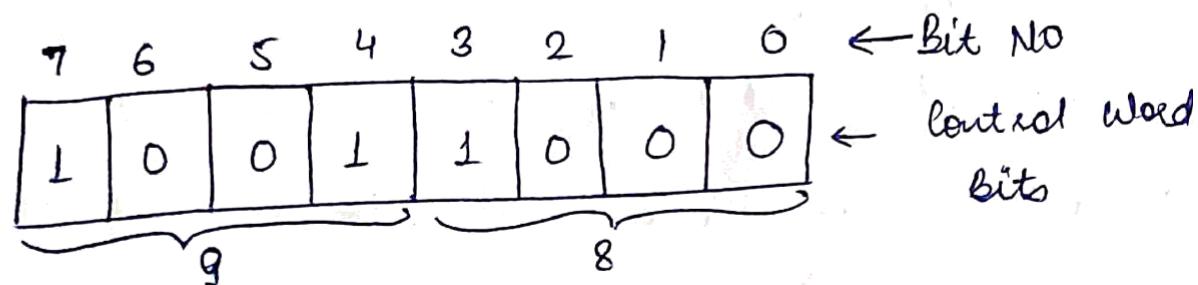
### Simple I/O Mode

- In this mode port A & B are used as two simple 8-bit I/O ports and port C as two 4-bit ports.
- The Control Word Format for Simple Input Output Mode is as shown above.

Eg 1 Make a control word when ports of 8255 are defined as follows

- Port A as Input Output Port
- Mode of the port A - Mode 0
- Port B as Output Port
- Mode of the port B - Mode 0
- Port C upper - Input Port
- Port C lower - Output Port

Ans :



Control Word = 98 H

~~Q2~~ Form Control Word for 8255 for Mode 0 operation  
Port A - output, Port B → Output, Port C lower → output,  
Port C Upper - input.

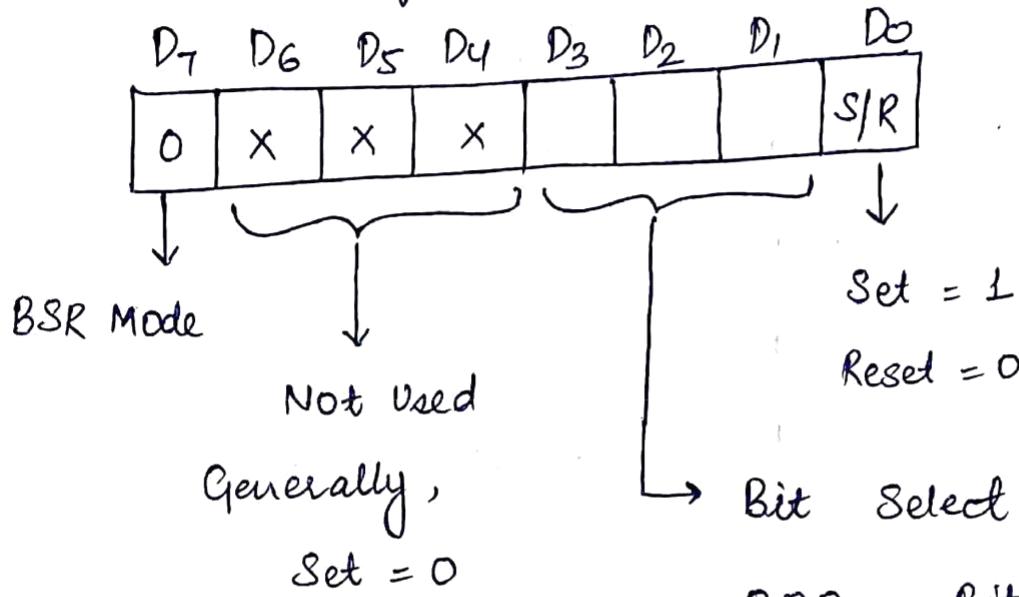
7	6	5	4	3	2	1	0	← Bit No.
1	0	0	1	0	1	a	0	0
8					8			

Control Word = 88H

# Bit Set / Reset Mode:-

- The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register.
- A control word with bit  $D_7 = 0$  is recognized as BSR control word.
- It does not alter any previously transmitted control word with bit  $D_7 = 1$ .
- Therefore, the input/output operations of port A & B are not affected by BSR control word.
- In BSR mode, individual bits of port C can be used for applications such as ON/OFF switch.

# Control Word for BSR Mode



000 Bit 0

001 Bit 1

010 Bit 2

011 Bit 3

100 Bit 4

101 Bit 5

110 Bit 6

111 Bit 7

To set bit PC<sub>7</sub>      D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>  
0 0 0 0 0 1 1 1 1 = 0FH

To reset bit PC<sub>7</sub>      D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>  
0 0 0 0 0 1 1 1 0 = 0EH

To set bit PC<sub>3</sub>      D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>  
0 0 0 0 0 0 1 1 1 = 07H

To reset bit PC<sub>3</sub>      D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>  
0 0 0 0 0 0 1 1 0 = 06H

Write a BSR control word subroutine to set bits PC<sub>7</sub> & PC<sub>3</sub> and reset them after 10 ms. Assume a delay subroutine is available.

We already know that,

A <sub>1</sub>	A <sub>0</sub>	Address	Port
0	0	80 H	A
0	1	81 H	B
1	0	82 H	C
1	1	83 H	Control Register

Subroutine,

BSR MVI A, 0F H : Load byte to set PC<sub>7</sub>  
OUT 83 H

MVI A, 07 H : Load byte to set PC<sub>3</sub>  
OUT 83 H

CALL Delay : This is a 10 m-s delay.

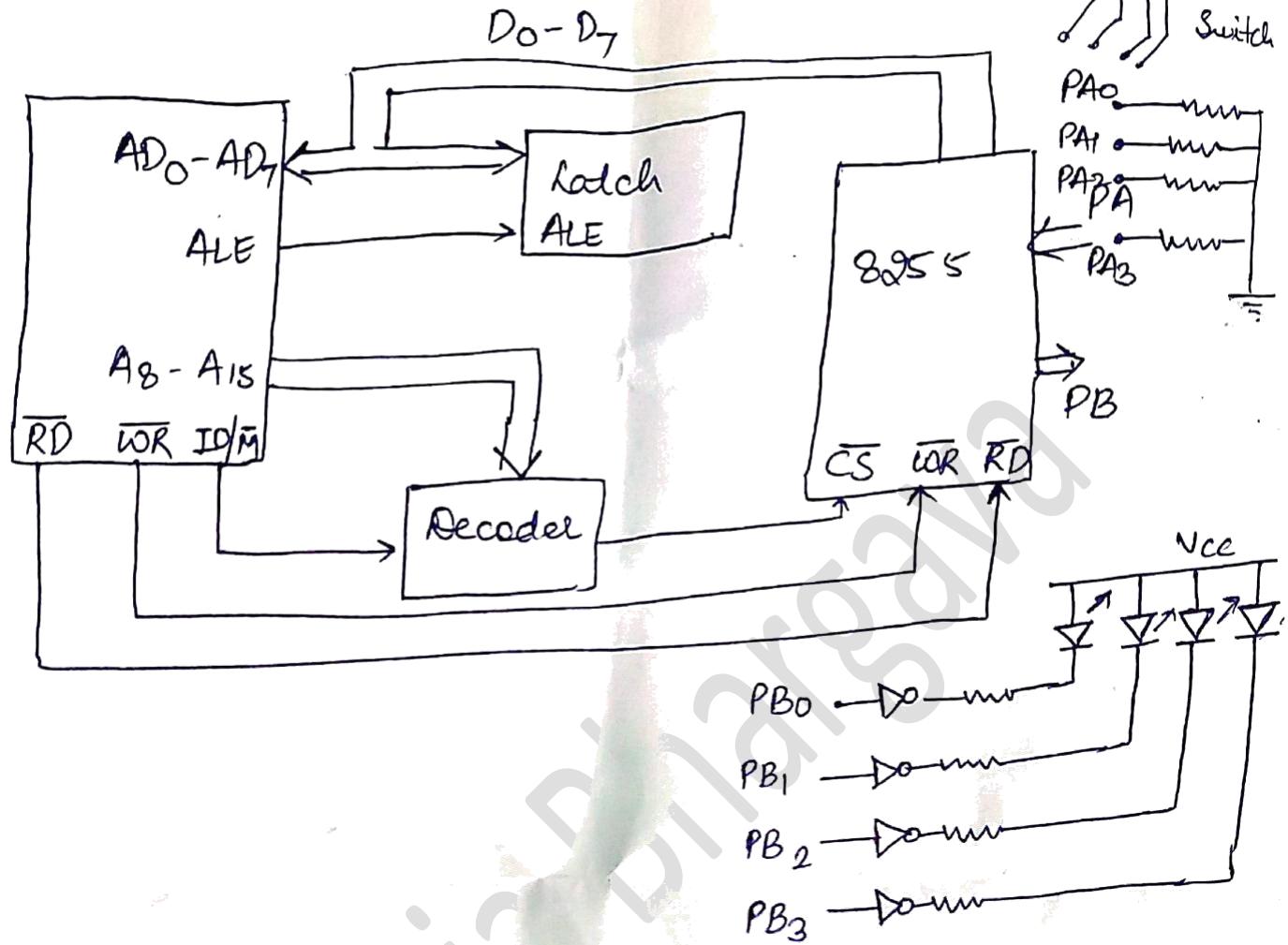
MVI A, 06 H : Load byte to reset PC<sub>3</sub>.  
OUT 83 H

MVI A, 0E H : Load byte to reset PC<sub>7</sub>.  
OUT 83 H

RET

# Interfacing Switches 4 LED's with 8085 through 8255

8255 :-



Control Word : All ports are initialized to mode 0.  
(90H)

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	0	1	0	0	0	0

Program for initializing 8255 and performing operation

MVI A, 90 H

OUT 43 H

IN 40 H

OUT 41 H