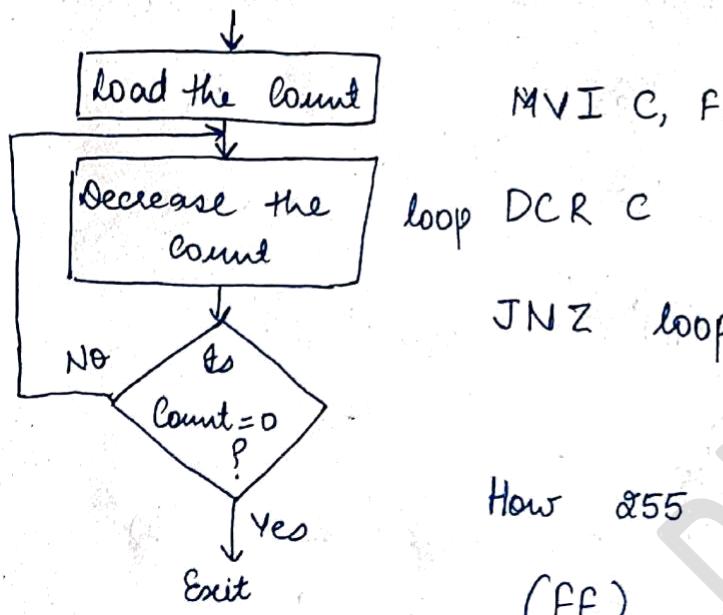


# Counters and Time Delay

- Counters are used primarily to keep track of events.
- Time delay is used to set timing between two events.

## Using One Register



How many times the States instruction is executed

1  $\times$  1

255  $\times$  255

10  $\times$  255

How 255 ?

$$\begin{aligned}
 (FF)_H &= 15 \times (16)^1 + 15 \times (16)^0 \\
 &= 255
 \end{aligned}$$

$$\begin{aligned}
 \text{Total States} &= (7 \times 1) + (4 \times 255) + (10 \times 255) \\
 &= 3577 \text{ states}
 \end{aligned}$$

Let 8085 Microprocessor  $f = 2 \text{ MHz}$

$$\therefore T = \frac{1}{f} = \frac{1}{2 \times 10^6} = 0.5 \mu\text{sec.}$$

$$\therefore \text{Delay time} = 3577 \times 0.5 \times 10^{-6}$$

$$= 1788.5 \mu\text{sec.}$$

$$= 1.78 \text{ m sec}$$

Using two register (loop with in loop)

How many times the instruction is executed

States

MVI B, 10H

1

$7 \times 1$

loop<sup>1</sup> MVI C, 78H

16

$7 \times 16$

loop<sup>2</sup> DCR C

$120 \times 16$

$4 \times 120 \times 16$

JNZ loop 2

$120 \times 16$

$10 \times 120 \times 16$

DCR B

16

$4 \times 16$

JNZ loop 1

16

$10 \times 16$

How 16?

$$\begin{aligned} (10)_{16} &= 1 \times (16)^0 + 0 \times (16)^1 \\ &= (10)_{10} \end{aligned}$$

How 120?

$$\begin{aligned} (78)_{16} &= 7 \times (16)^1 + 8 \times (16)^0 \\ &= (120)_{10} \end{aligned}$$

$$\begin{aligned} \text{Total States} &= (7 \times 1) + (7 \times 16) + (4 \times 120 \times 16) + (10 \times 120 \times 16) \\ &\quad + (4 \times 16) + (10 \times 16) \\ &= 27223 \text{ states} \end{aligned}$$

∴ Delay time =  $27223 \times 0.5$

$$= 13611.5 \mu\text{sec.}$$

Note: To give maximum delay, both registers must be loaded with maximum value i.e. FF H.

## Using Register Pair

T-State

How many lines loop  
executed

49

LXI D, FFFF H

10

1

loop DCX D

6

65535

MOV A, D

4

65535

ORA E

4

65535

JNZ loop

10

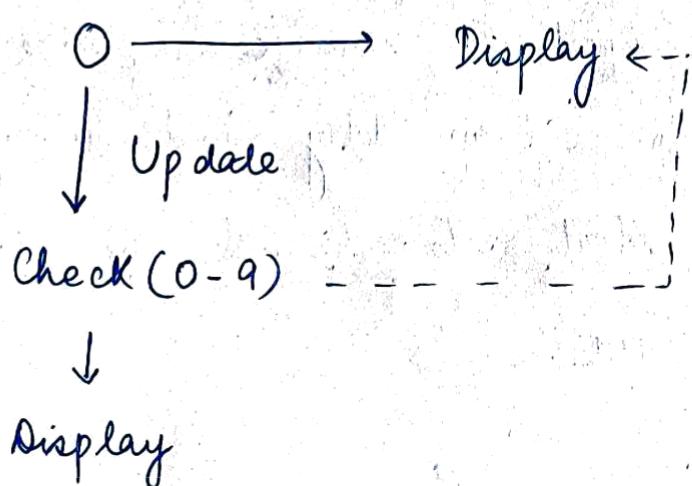
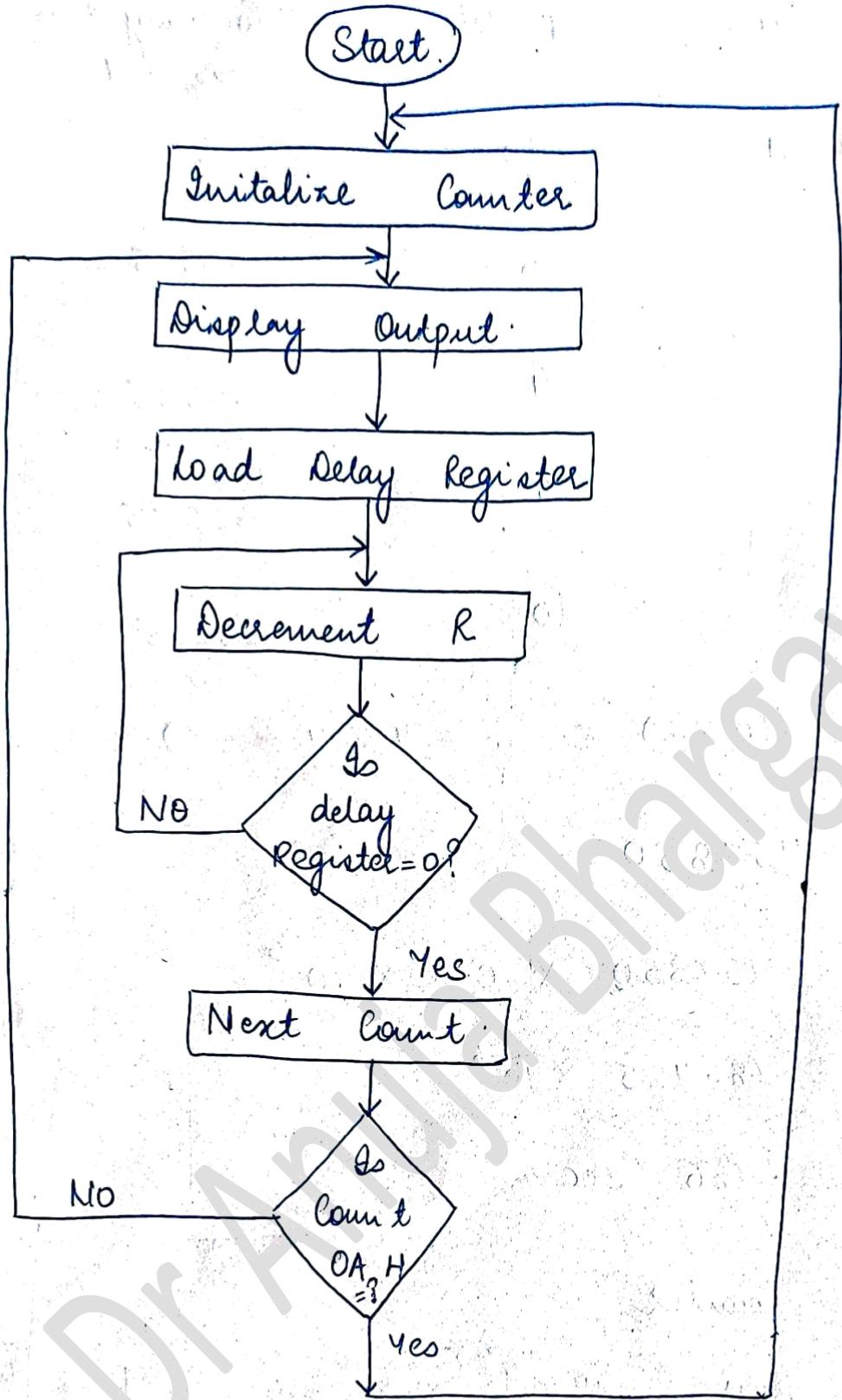
65535

$$\begin{aligned}
 \text{Total State} &= (10 \times 1) + (6 + 4 + 4 + 10) \times 65535 \\
 &= 1572850
 \end{aligned}$$

$$\begin{aligned}
 \text{Delay time} &= 1572850 \times 0.5 \times 10^{-6} \\
 &= 786.425 \times 10^{-6} \\
 &= 786 \text{ sec}
 \end{aligned}$$

## Zero to Nine Counter

WAP to count from "0" to "9" with one second of delay between each count. At the count of 9, the counter should reset itself to "0" and repeat the counter sequence continuously. Use register-pair H-L to set up delay and display each count at one of the output ports. Assume the clock freq. of the microprocessor is 1 MHz.



CPI data

[A] - data

A > data, CY = 0

A < data, CY = 1

Next MVI B, 00 H

MOV A, B (T-State)

Display OUT PORT 1 10 ✓

LXI H, Count 10 ✓ ]

loop DCX H 6 ✓ ]

MOV A, H 4 ✓ ]

ORA L 4 ✓ ]

JNZ loop 10 ✓ ]

INR B 4 ✓ ]

MOV A, B 4 ✓ ]

CPI 0A H 7 ✓ ]

JNZ Display 10 ✓ ]

JMP Next ]

Delay = Delay in loop + Delay outside the loop

$$= [24T \times (\text{Count})_{10}] + 45T$$

Given, Delay = 1 sec

$$\& f = 1 \text{ MHz} \Rightarrow T = 10^{-6} \text{ sec.}$$

$$\Rightarrow 1 = [24 \times 10^{-6} \times (\text{Count})_{10}] + 45 \times 10^{-6}$$

$$\Rightarrow (\text{Count})_{10} = 41664.79 \approx 41665$$

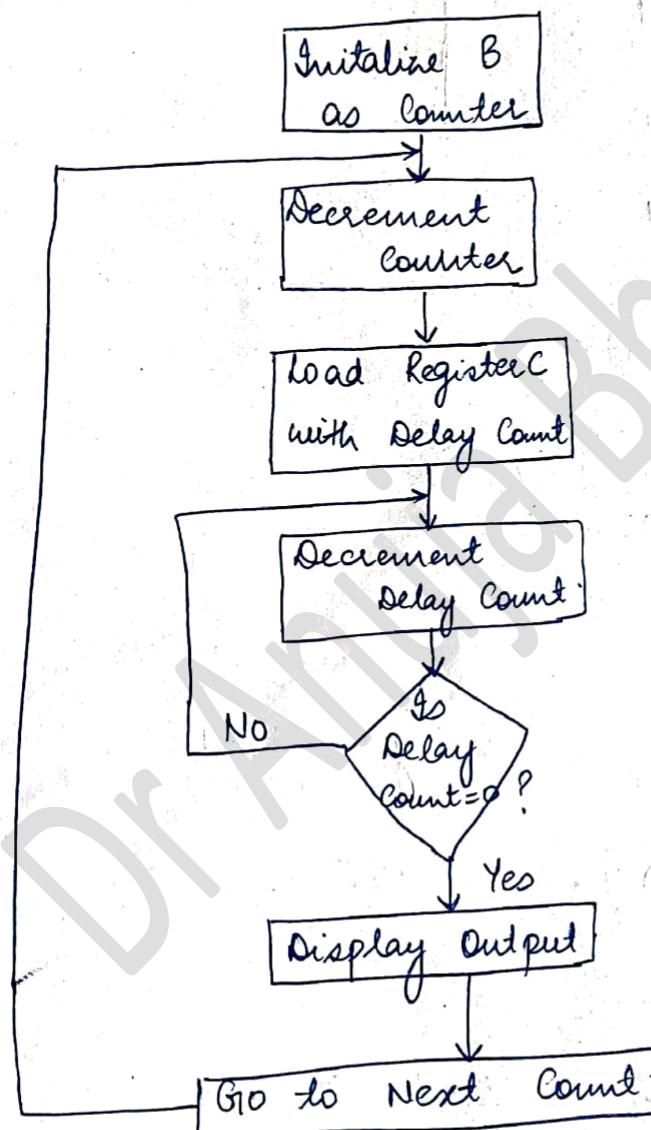
$$(\text{Count})_H = A2C1 H$$

16	41665	
16	2604	1
16	162	C
10	2	

## # Hexadecimal Counter

WAP to count continuously in hexadecimal from FF H to 00 H in a system with 0.5 μs. clock period. Use register C to set up 1 ms delay between each count and display the number at one of the output ports.

→ The problem has two parts, the first to set up a continuous down counter and the second is to design a



MVI B, 00H

Next DCR B 4T ✓

MVI C, Count 7T ✓

Delay DCR C 4T ✓

JNZ Delay 10T ✓

MOV A, B 4T ✓

OUT PORT 1 10T ✓

JMP Next 10T ✓

Delay = Delay Inside Loop + Delay Outside Loop

$$= [4T \times (\text{Count})_{10}] + 35T$$

Given, Delay = 1 ms & T = 0.5  $\mu$ s

$$\Rightarrow 1 \text{ ms} = (\text{Count})_{10} (14 \times 0.5 \times 10^{-6}) + (35 \times 0.5 \times 10^{-6})$$

$$\Rightarrow (\text{Count})_{10} = (140)_{10} = 8C H$$