8259 (Programmable Interrupt Controller) :-

- The 8259A is a programmable interrupt controller designed to work with Intel microprocessors 8085, 8086 and 8088.

- The 8259 A interrupt controller can

(1) Manage eight interrupts according to the instructions written into its control registers.

This is equivallent to providing eight interrupts request pins on the processor in place of one INTR (8085) pin.

(2) vector an interrupt request anywhere in the memory map. Since, all eight interrupts are spaced at the interval of either four or eight locations.

This eliminates the major drawback of the 8085 interrupt in which all interrupts are vectored to memory location on page 00 H.

(3) Resolve eight level of interrupts priorities in a variety of modes, such as fully Nested Mode, automatic rotation mode, and specific rotation mode.

(4) Mask each interrupt request individually.

(5) Read the status of pending interrupts, in-service

interrupt and masked interrupts.

(6) Be set up to accept either the level triggered or the edge triggered interrupt request.

(7) Be expanded to 64 priority levels by cascading additional 8259 As

(8) Be set up to work with either the 8085 Microprocessor mode or the 8086/8088 Microprocessor mode.

Block Diagram of 8259A :-

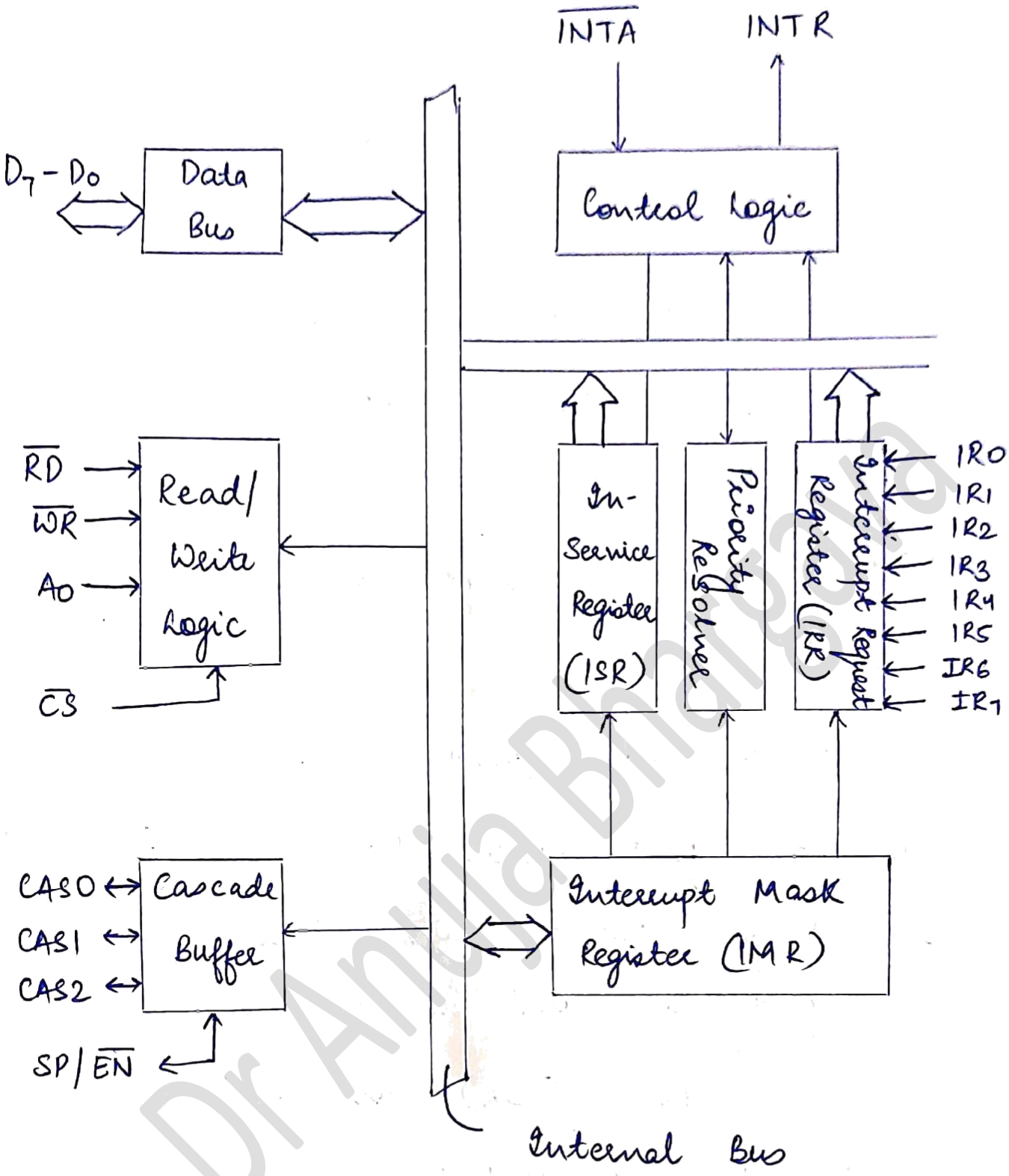
- The internal block diagram of 8259 include eight blocks : control logic, read/write logic, data bus buffer, three registers (IRR, ISR and IMR), priority resolver and cascade buffer.

- Read/Write Logic

→ This is typical read/write control logic.

→ When the address line A_0 is at logic 0, the controller is selected to write a command or read a status.

→ The chip select logic and A_0 determine the port address of the controller.



- Cascade Buffer

→ This block is used to expand the number of interrupt levels by cascading two or more 8259 A.

- **Control Logic**

→ This block has two pins : INT (Interrupt) as an output and $\overline{INTA}$ (Interrupt Acknowledge) as an input.

→ The INT is connected to the interrupt pin of the MPU. Whenever a valid interrupt is asserted, this signal goes high.

→ The $\overline{INTA}$ is the interrupt acknowledge signal from the MPU.

- **Interrupt Register and Priority Resolver**

→ The Interrupt request register (IRR) has eight input lines (IR_0 - IR_7) for interrupts. When these lines are high, the request are stored in the register.

→ The in-service register (ISR) stores all the levels that are currently being serviced

→ The Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked.

→ The Priority Resolver (PR) examines these three registers and determines whether INT should be sent to the MPU.

Pin Diagram of 8259A