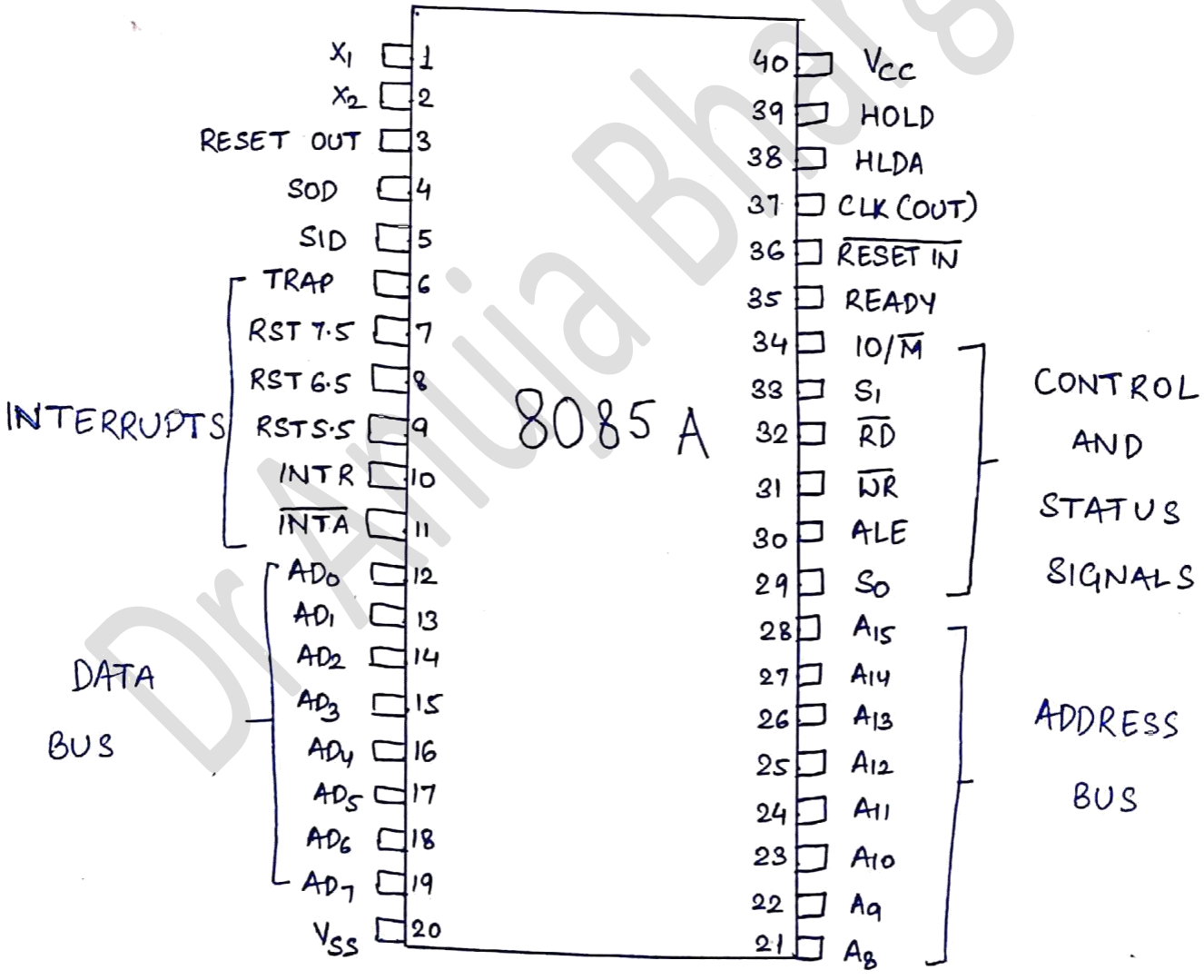
8085 Pin Diagram :-

- The 8085 A (commonly known as 8085) is an 8-bit general purpose microprocessor capable of addressing 64 K of memory.
- The device has 40 pins, require a +5V single power supply, and can operate with 3MHz single-phase clock.
- Fig shows the logic pindiagram of 8085.



• All the signals can be classified into six groups.

1) ADDRESS BUS :

→ The 8085 has signal lines (pins) that are used as address bus : however, these lines are split into two segments : $A_{15} - A_8$ and $AD_7 - AD_0$.

→ The eight signal lines $A_{15} - A_8$ are unidirectional. These lines are also known as higher - order address.

2) DATA BUS :

→ The signal lines $AD_7 - AD_0$ are bidirectional. These are used as lower order address bus and data bus.

3) CONTROL AND STATUS SIGNALS :-

→ This include following signal

a) ALE - Address latch Enable

→ If ALE = 1, i.e enable, it indicates that the bits on $AD_7 - AD_0$ are address bits.

→ If ALE = 0 ; i.e disable, it indicates that the bits on $AD_7 - AD_0$ are data.

b) $\overline{RD}$ (Read)

→ This is active low signal.

→ This signal indicates that the selected I/O or memory device is to be read and data is available on data bus.

c) $\overline{WR}$ (Write)

→ This is active low signal.

→ This signal indicates that the data on data bus are to be written into memory or I/O.

d) IO / $\overline{M}$

→ When it is high, it indicates Input - Output operation.

→ When it is low, it indicates a memory operation.

e) S_1 & S_0

→ These status signals, can identify various operations but they are rarely used in small systems

4) POWER SUPPLY & CLOCK FREQUENCY

→ V_{CC} : +5V power supply

→ V_{SS} : Ground Reference

→ X_1, X_2 : A crystal oscillator (RL or RC) is connected at these two pins. The frequency is internally divided by two, therefore to operate at 3MHz, the crystal should have 6MHz frequency.

→ CLK (OUT) : Clock Output used as clock for other devices.

5) EXTERNALLY INITIATED SIGNALS

→ INTR (Input) Interrupt Request

It is used as general purpose ~~register~~ interrupt.

→ $\overline{\text{INTA}}$ (Output) Interrupt Acknowledge

It is used to acknowledge the interrupt.

→ RST 7.5, 6.5, 5.5

These interrupts transfer the program control to specific memory location.

These have high priorities compare to INTR. interrupt.

Among these the priority order is 7.5, 6.5, 5.5.

→ TRAP (Input)

This is nonmaskable interrupt and has highest priority.

→ HOLD (Input)

This signal indicates that peripheral device such as DMA (direct memory access) is requesting the use of address and data bus.

→ HLDA (Output) Hold Acknowledge

This signal acknowledges the HOLD request.

→ READY

This signal is used to delay the microprocessor read or write cycles.

→ $\overline{\text{RESET IN}}$

When this signal is low, the program counter is set to zero.

→ RESET OUT

This signal can be used to reset other devices.

6) SERIAL I/O PORTS

SID (Serial Input Data)

SOD (Serial Output Data)

In serial transmission, data bits are sent over a single line, one bit at a time.