

TIMING DIAGRAMS

(27)

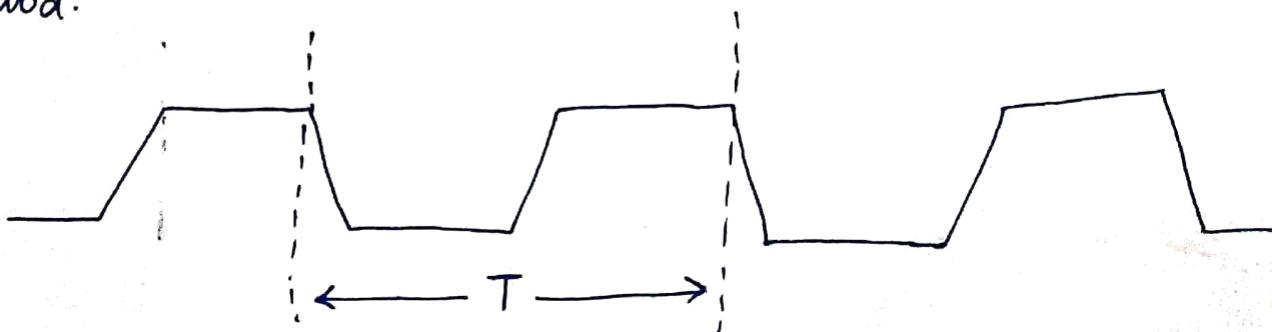
- In programming, the CPU fetches and executes instruction one by one till the HLT instruction.
- During fetch and execute operation the timing and control unit of microprocessor generates different timing and control signals i.e CLK, IO/M, S₁, S₀, ALE, RD, WR, AD₀-AD₇, A₈-A₁₅.
- These signals are issued to memory or I/O devices to perform different task. All the operations performed by the Microprocessor is in synchronization with clock pulses.
- The graphical representation of steps with respect to time i.e clock is called timing diagram.
- When any instruction is executed by microprocessor, it performs two main operation i.e. Instruction fetch & Instruction Execution

★ T-State:-

- The time between two positive and negative transitions of the clock is defined as T-State.

or

It is one subdivision of the operation performed in one clock period.

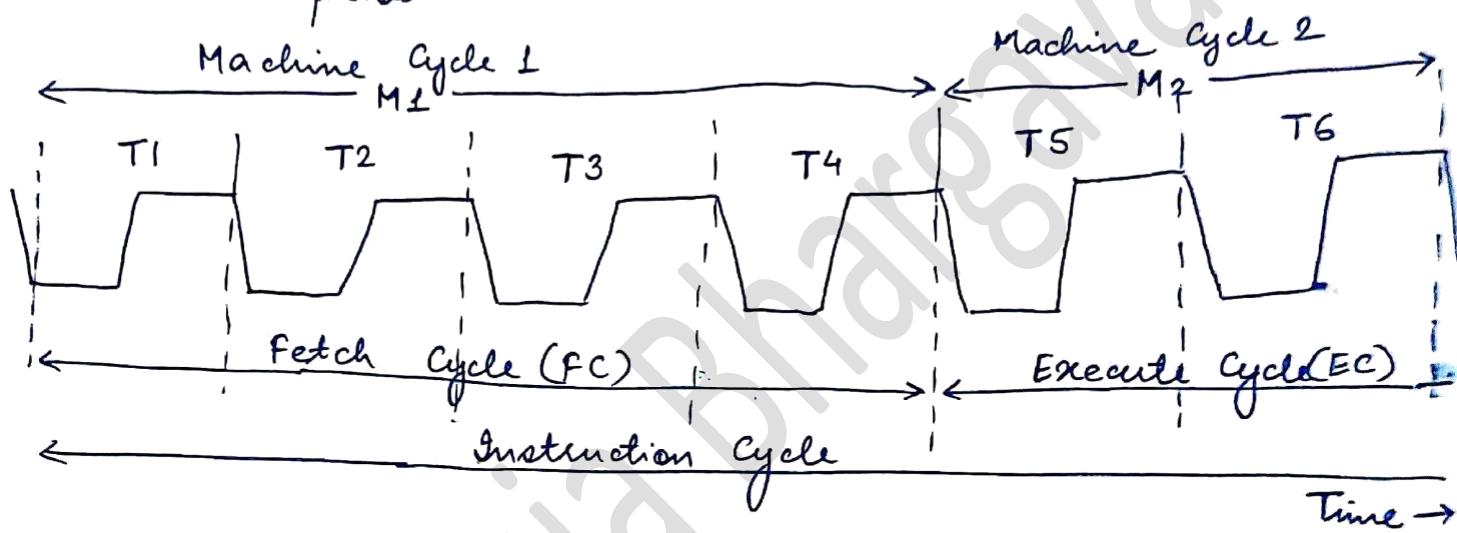


* Instruction Cycle

- It is defined as the time required to complete the execution of an instruction.
- An instruction cycle consist of fetch cycle and execute cycle.

$$IC = FC + EC$$

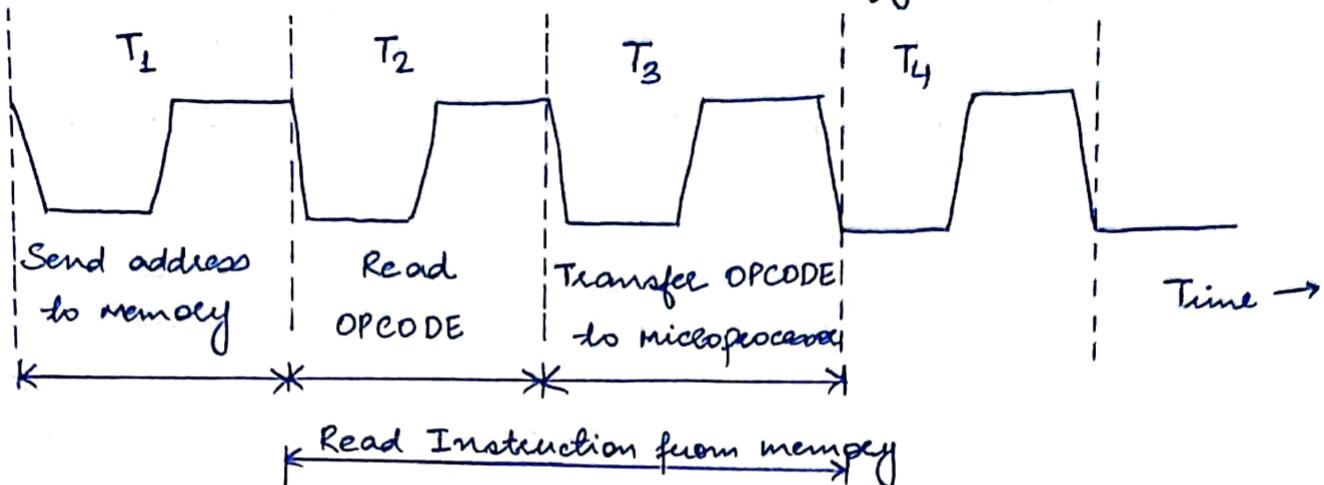
- The fetch and execute cycle are carried out in synchronization with clock pulses.



* fetch cycle

- To execute an instruction, the microprocessor first take the operation code from memory i.e opcode fetch operation.
- The fetch operation is performed in following steps
 - (i) Send instruction of next instruction to memory.
 - (ii) Receive opcode from memory.
 - (iii) Update program counter.
- Program counter keep tracks of the address of instruction to be fetched next.

- The above three steps are shown in fig.



* Execute Cycle

- After receiving the opcode from memory, microprocessor decodes the fetched opcode and then generates timing and control signals to perform a specified task.
- The total time required to do the execute operation is known as execute cycle.
- The time required for execute cycle vary from instruction to instruction.

* Comparison between fetch and execute cycle.

Fetch Cycle

1. The CPU executes this cycle to access program memory.
2. During this cycle, the CPU performs only read operation.
3. Number of cycles depends on length of instruction.
4. Program counter is incremented by 1.
5. Content of PC are placed on address bus.

Execute Cycle.

1. The CPU executes this cycle to access data memory.
2. During this cycle, the CPU performs either read or write operation.
3. Number of cycle depends on type of instruction, addressing mode.
4. Program counter is not incremented.
5. Content of SP are placed on address bus.

* Machine Cycle

- The time required by the microprocessor to complete the operation i.e. memory read / write or I/O read / write is called as machine cycle.
- The 8085 instruction consist of 1 to 5 machine cycles.
The first machine cycle of every instruction is opcode fetch cycle followed by memory read or memory write or I/O read or I/O write.

OPCODE FETCH CYCLE :-

- The first byte of any instruction is opcodes or operation code.
- The microprocessor uses this cycle to fetch opcode from memory known as opcode fetch cycle.
- In this, the microprocessor place content of program counter i.e. address of memory on address bus. The program counter is incremented by one.
- During this cycle, the microprocessor fetches opcode of current instruction into instruction register and then decodes this opcode.

Note:- The most of the 8085 microprocessor requires 4T states opcode fetch cycle except CALL, DCX, INX, PCHL, PUSH, SPHL, condition RET and RST_n instructions.

Timing & Control Signal :-

ALE :- Address latch enable

It indicates that bits on $AD_7 - AD_0$ are address bits.

\overline{RD} :- Read (Active low)

It indicates that selected I/O or memory device is to be read and data are available on data bus.

\overline{WR} :- Write (Active low)

It indicates that the data on data bus are to be written into selected memory or I/O location.

I/O/ \overline{M}

When it is high, it indicates I/O operation.

" " low ; " " memory "

S₁, S₀

To identify various operations.

CLK

This is used as system clock.

Machine Cycle	IO/M	S ₁	S ₀	Control Signal
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$

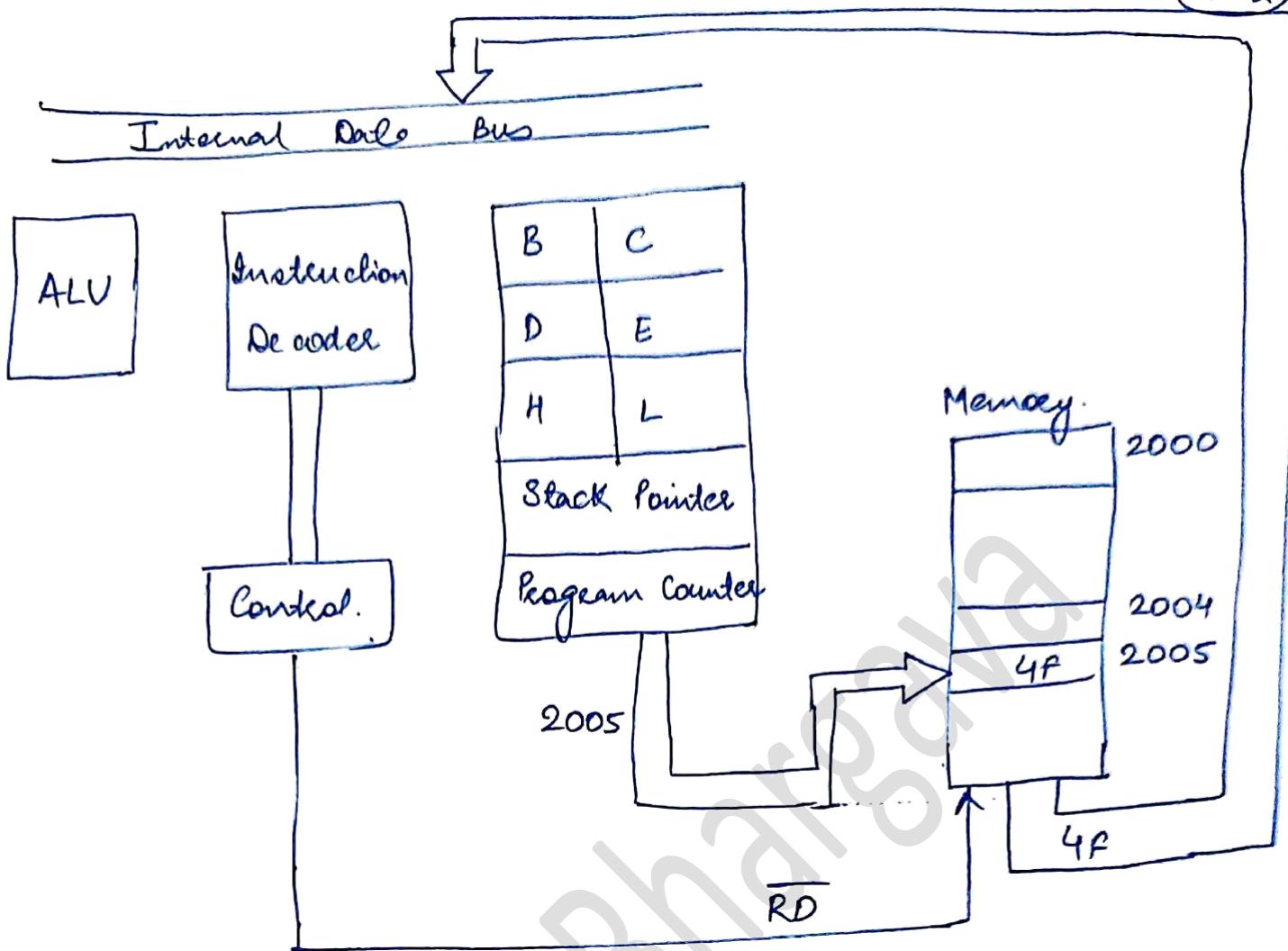
Microprocessor Communication

To understand the function of various signal of 8085, we examine the communication between microprocessor and I/O devices.

Step 1) Reading from memory or fetching the instruction.

Step 2) This can be understood by analogy of concierge.

- 1) Concierge gets the address from office, picks the van, find the street and look for house number.
- 2) Concierge rings the bell.
- 3) Somebody opens the door, and gives package by concierge.
- 4) Return back.



Step 1) CPU places the 16 bit memory address from the program counter on the address bus.

(CPU finds the street and address)

At T_1 , the higher order memory address $20H$ is placed on A_5-A_7
lower " " " " $05H$ " " A_0-A_7

ALE goes high.

$I_{0/1}$ goes low i.e. it is memory related operation
 $S_1 S_0 = 0 1$

Step 2) Control unit sends the control signal \overline{RD} to enable the memory. (Ring the bell)

At T_2 , RD signal is send out, active for two clock periods.

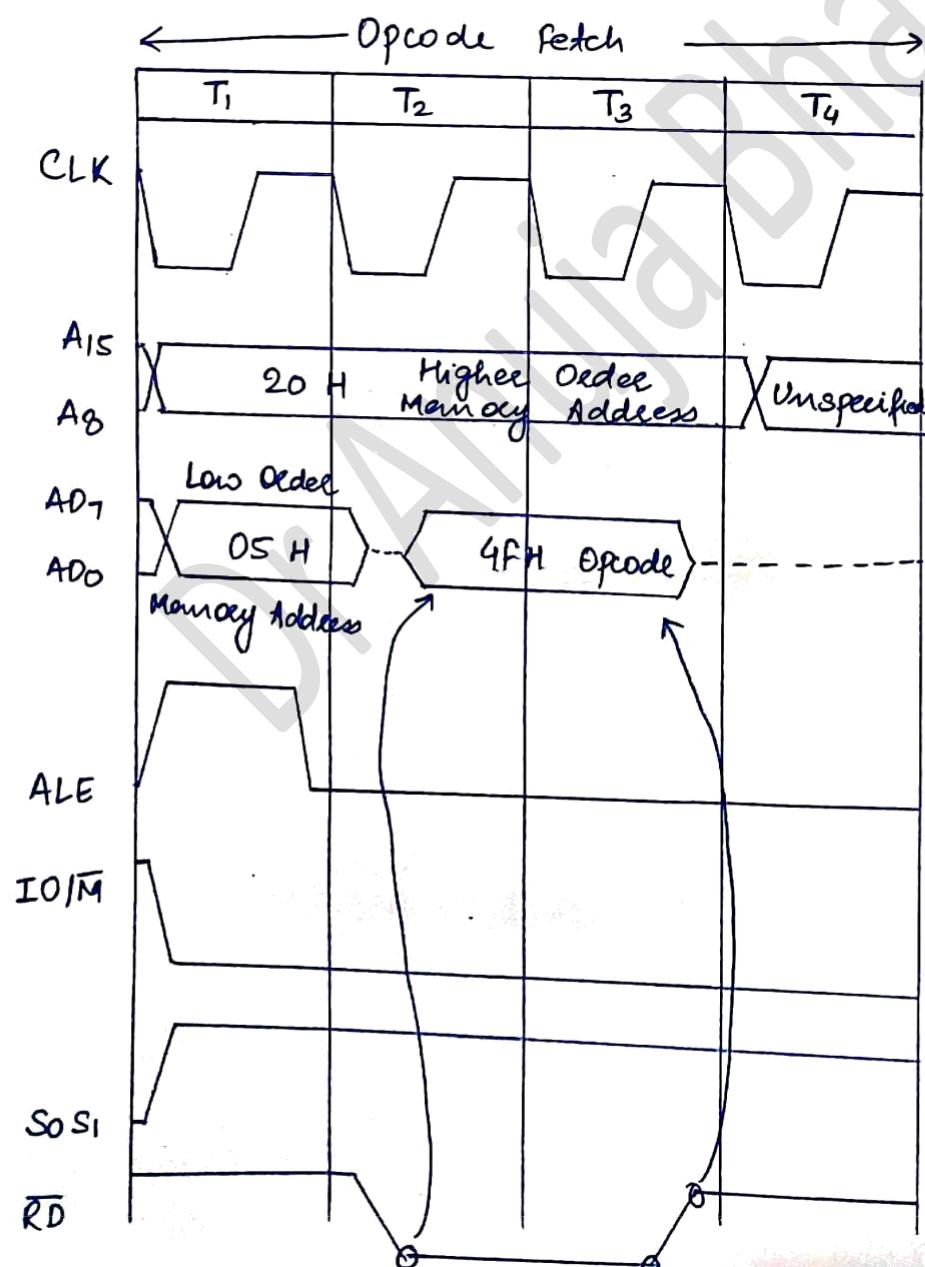
Step 3) The byte from memory location is placed on data bus.

When memory is enable, 4FH is placed on AD₇-AD₀.

The RD signal causes 4FH to be placed on AD₇-AD₀.

Step 4) The byte is placed in instruction decoder of the microprocessor and the task is carried out according to the instruction.

The 4FH is decoded, at T_4 .



Memory Read (Operand Fetch Cycle)

- The microprocessor executes this cycle to read contents from data memory. The length of cycle is 3T state.

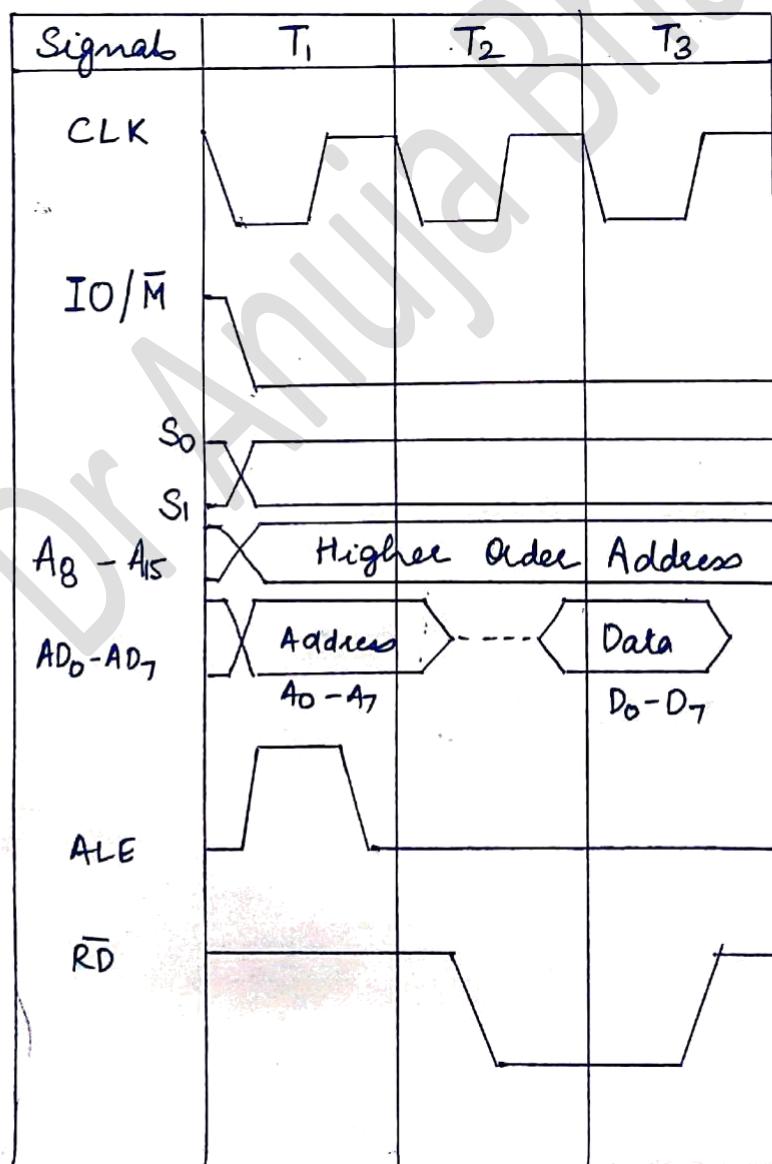
Operation

1. T₁ State:

In this state, 8085 sends $\text{IO}/\bar{M} = 0$, $S_0 = 0$ & $S_1 = 1$.

In memory read, address is from WZ or SP.

In operand fetch cycle, address is given by PC and incremented by 1. During this state, ALE is enable to enable address at $A_0 - A_7$.



2. T₂ - State

In this state, AD₀-A₇ lines will be used as D₀-D₇ i.e data lines. During this state $\overline{RD} = 0$, read is enabled and content of selected memory location will be placed on D₀-D₇.

3. T₃ - State

During this state, data from memory is transferred to microprocessor & \overline{RD} is made high. and PC is incremented by 1.

Memory Write Cycle

- The microprocessor execute this cycle to write data in memory.
- During this cycle, the content of register are placed on the address bus. Program counter is not incremented by one.
- The length of cycle is 3T state.
- Operation

1) T₁ - State :

In this state, 8085 sends IO/M = 0, S₀ = 1, S₁ = 0.

The 8085 place the content of register on address bus.

AE is enable to activate address A₀-A₇.

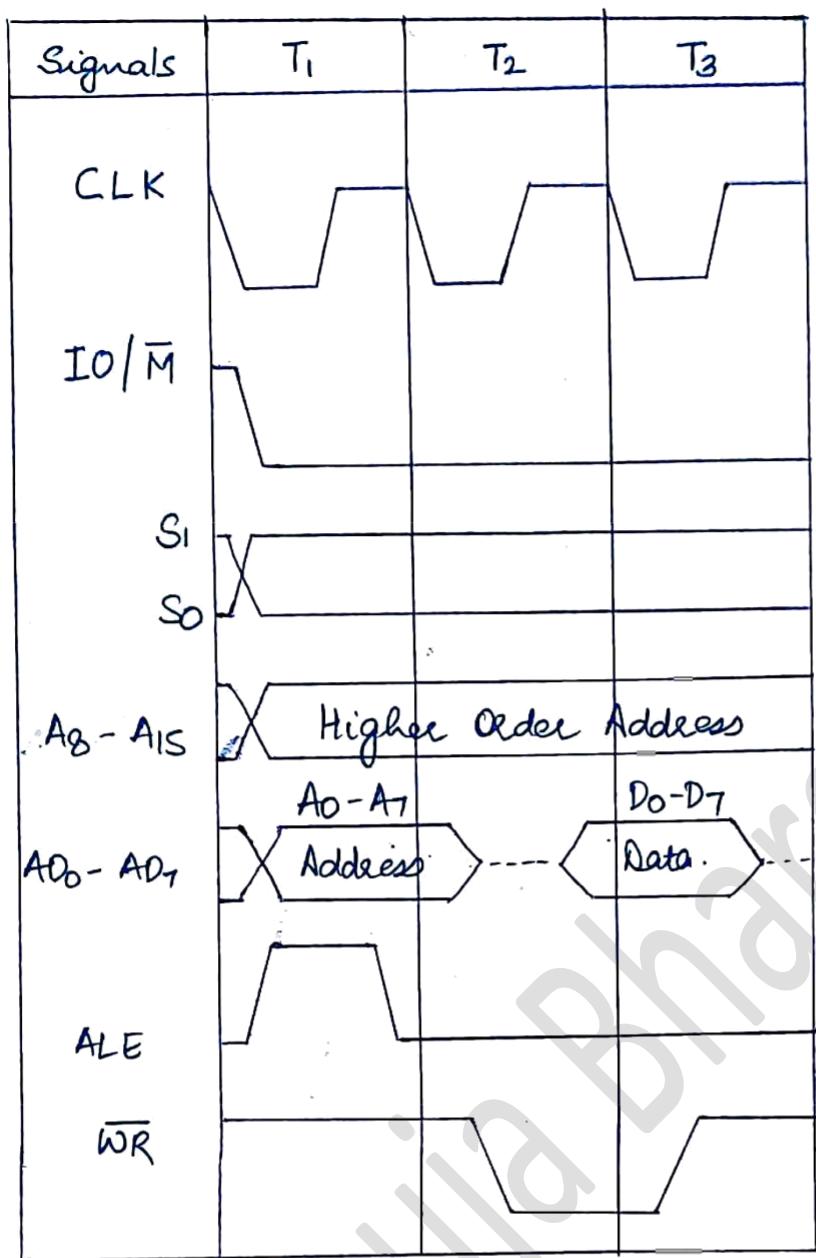
2) T₂ - State

In this state, the AD₇-AD₀ will be used as D₀-D₇ i.e data lines

During this state WR = 0, the write circuit of memory device is enabled to write and the content of data bus will be written on memory location.

3) T₃ - State

During this state, the content of data bus is stored in memory location and WR is made high.



Input / Output Read Cycle

- The microprocessor executes this cycle to read content of I/O port
- The length of the cycle is 3T states.

T_1 State :-

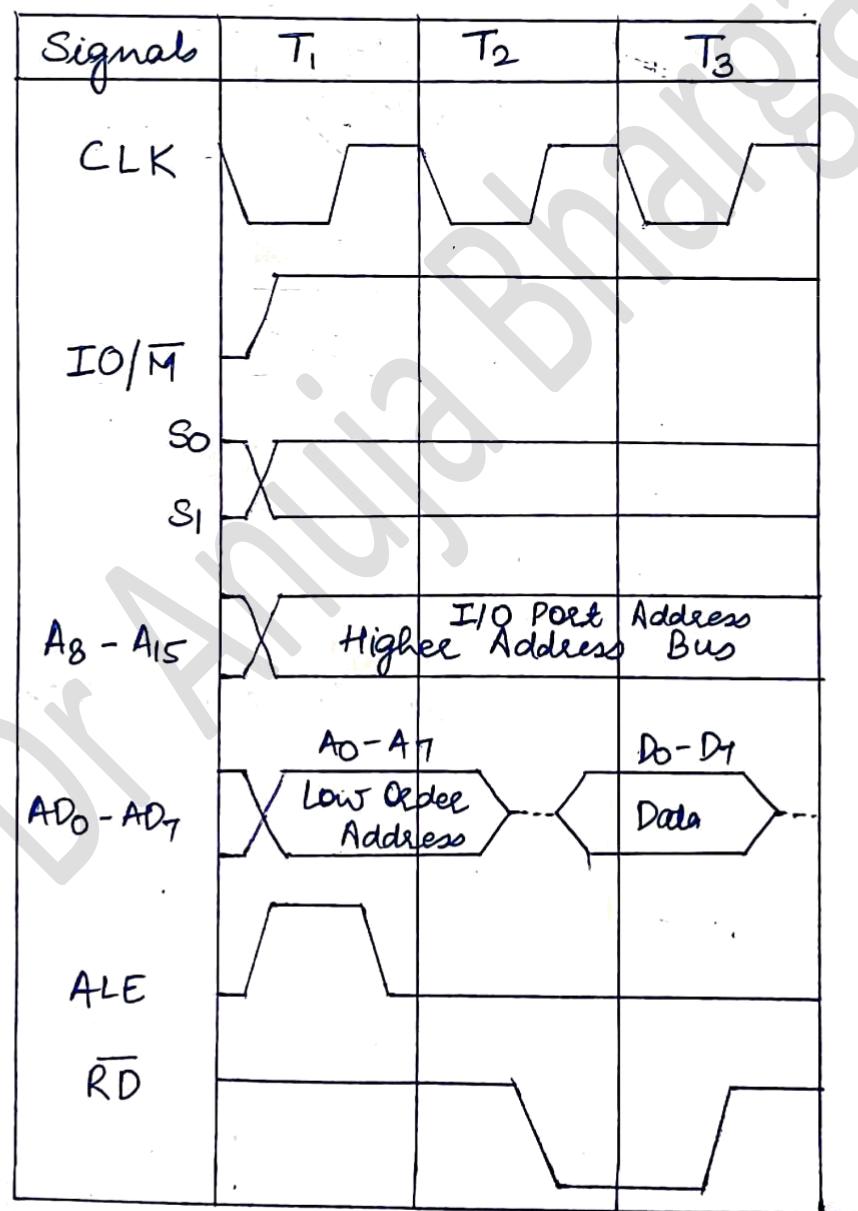
In this state, the 8085 sends signals $IO/\bar{M} = 1$, $S_0 = 0$ and $S_1 = 1$. The content is placed on address bus. During this state, the ALE pulse is activated to enable address latch $A_0 - A_7$.

T₂ State :-

In this state, the AD₀-AD₇ lines will be used as D₀-D₇ i-e data bus. During this state $\overline{RD} = 0$, the read circuit of I/O device is enable to read and the content of selected I/O port is placed on data bus.

T₃ State :-

During this state, the content of I/O port is transferred to microprocessor i-e A register. and \overline{RD} is made high.



Input / Output Write Cycle

- The microprocessor executes this cycle to write data into an I/O port.
- The length of the cycle is 3T States.

T₁ State:- In this state, the 8085 sends signals IO/M , $S_0 = 1$, $S_1 = 0$. In this cycle, the content of register is placed on address bus. The same 8 bit I/O address is placed on $A_0 - A_7$ & $A_8 - A_{15}$. During this state, the ALE is activated.

T₂ State:- In this state, $AD_0 - AD_7$ lines will be used as $D_0 - D_7$ i.e data lines. During this state $\overline{WR} = 0$, write is enabled. and content is placed on data bus.

T₃ State:- During this state the content of accumulator is written to I/O port and \overline{WR} is made high.

