

{ Process does not have any kind of memory

To communicate microprocessor to Input / Output or memory.

We need three components —

Data Bus
Address Bus
Control Bus

① Address Bus → To locate a memory address.
↓
A set of conducting wires

② Data Bus : To fetching the data from the memory location. (microproc = mem)

③ Control Bus : To control the instructions.

8085

- ↳ It is a 8 bit processor (It can handle 8 bit at a time)
- It is having 8 bit data bus.
- It has 16 bit address line. * 2^{16} - memory locations

④ RST 5.5, 6.5, 7.5, INTR
TRAP

64000

Interrupts: unwanted process.

Suppose a boy is playing a game suddenly a call notification is there so that call is an interrupt then microprocessor have 2 choices

- ① Ignore the call
- ② Respond to that call

TRAP → It has highest priority we can't avoid that Interrupt. (Non maskable)

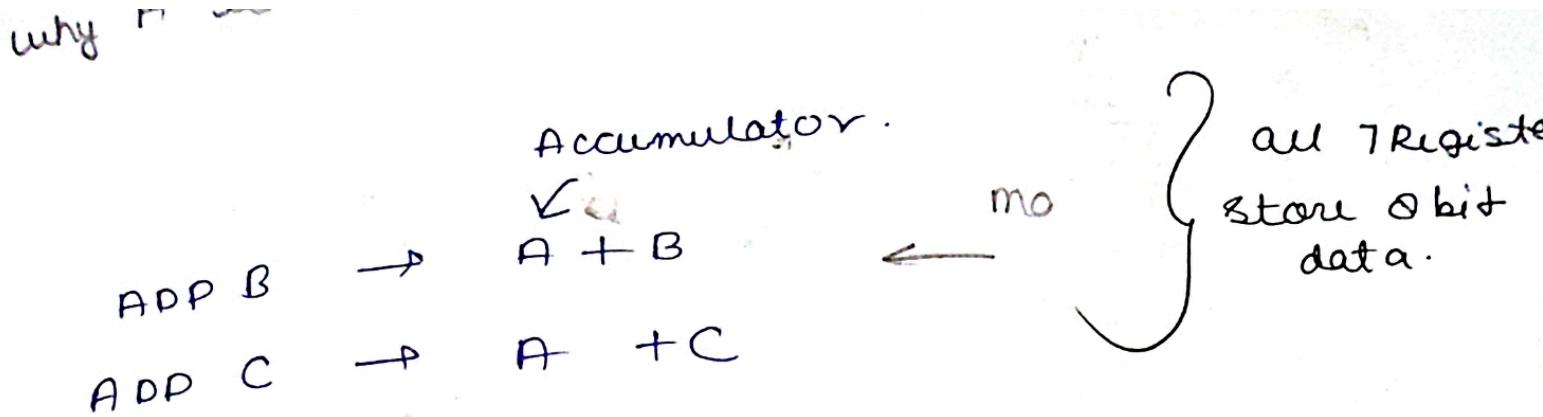
INTP → This can be avoidable. (maskable interrupt)

Processor have some Registers

7 general
purpose
Registers

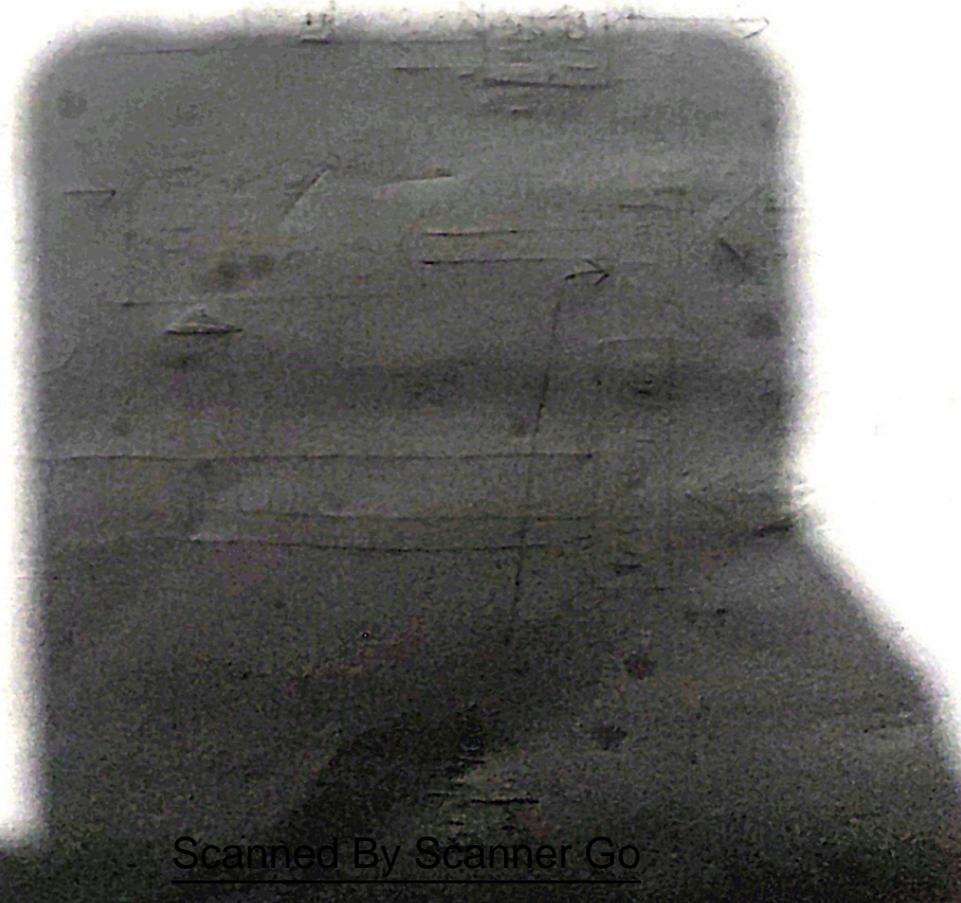
A₃ → Accumulator.
B
C
D
E
H
L

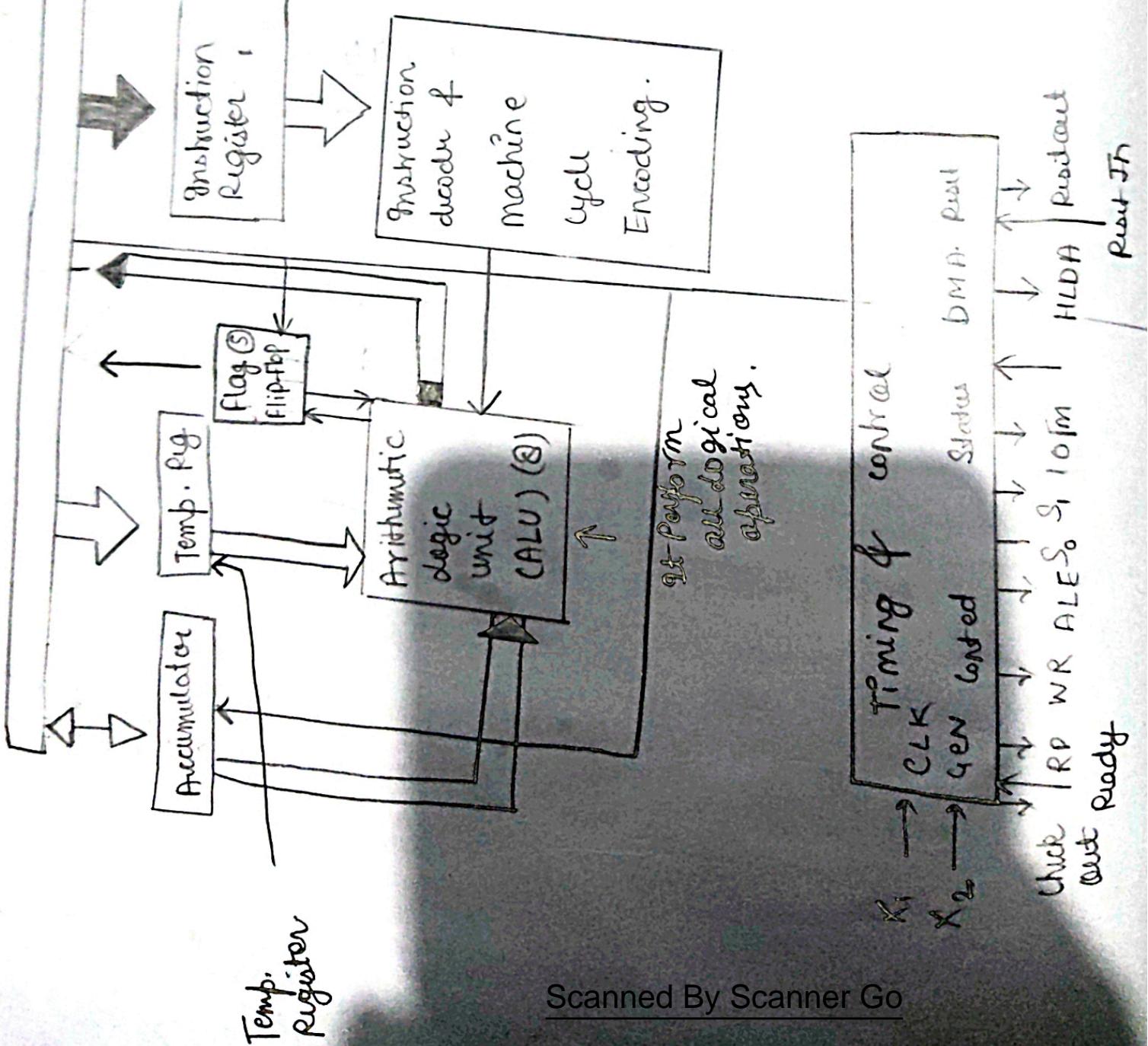
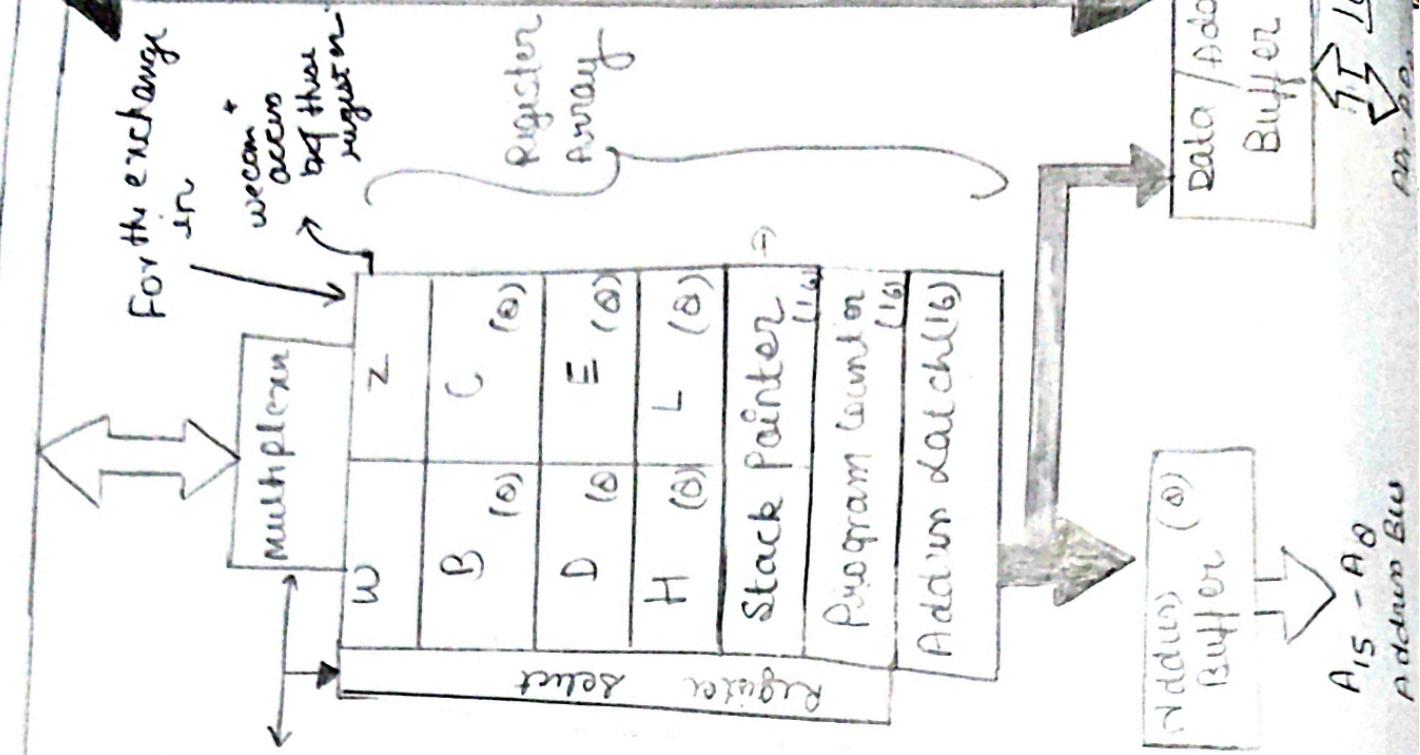
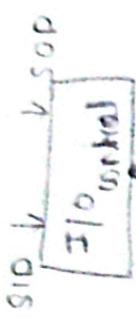
we can store
8 bit in the
Registers.



To store 16 bit data so we combine 2 Register
that means BC Pair } Register Pair
DE Pair
HL Pair }

Architecture of 8085





→
Data
Bus

B

Program counter :- It is 16 bit Register.
It holds the inc address of next instruction.

Data bus — To fetching the data.

Flag register : It store the status of the result.
Like → If it is positive Number

OR

Increment / Decrement : The result is 0
It is used to increment & decrement address.

Stack pointer → It store Address of the top stack.

Timing & control :- It is like brain which sense all the signals / It provide all types of signals. (जो काम करने की कौशल है)

Block Kab किए करेगा)

add. lines.

8085 - 2¹⁶

6500

2A
↓
0010

SID → serial input data (information give in serial)

SOP → serial out data.

④ Pinout → Reading driver peripheral value.

After processor pinouts connected

Koi unko pulse kar
rakh.]

[Processor Ko Pin Kari Rakh]

or Offer Memory

Address latch enable.

Processor baisekhiye
Kanga Ki Data Line use / or Address line.]

(Clock) Frequency match Kar raha Peripheral device
se

30 Pin HLDA → when the Processor with overloaded.

0254 → field acknowledgement →

		Function
S ₁	S ₀	
0	0	HALT
0	1	writing mode
1	0	Read
1	1	Fetch

I/O/M	S ₁	S ₀	
0	0	0	HALT
0	0	1	memory write
0	1	0	" read
0	1	1	OP code fetch
1	0	0	I/P write
1	0	1	I/O read
1	1	0	JNTA
1	1	1	

To address something
addressing mode may
be

immediate

1) direct Addressing mode
 MV B, 20 H Immediate → we are directly referring data.
 LXI D 10FF H

2) Register addressing.

MOV B A → move the content of A to B
 ADD B → A+B

3) Indirect Addressing.

LDA 1200 H

load into Accumulator.

we are referring the address.

In 8085 we have 5 addressing modes.

(4) Indirect addressing mode

MOV M,A

LDA X, C

(5) Implied.

opcode specifies the address

CMA → complement of A.

RAL → Rotate the Accumulator

immediate addressing mode.

① MVI D B, 20H → Data | It means move immediate
↓
destination add. to the data Pnto Register B.

LDX D 10FFH { d → load
X → 16 bit
I → Immediate.
load the data into
DE Pair
b/z D is only capable
to store 8 bit only.

② indirect Addressing
→ memory pointer (HL Pair)
MOV M, A { move the data of Acc
Accumulator to memory location
Pointed by HL Pair.

↓
at having the address.

LDA X C

instruction * classification

Load → From the memory
 Store → To the memory
 I → Immediate.
 X → 16 bit
 m - memory pointed by HL Pair.

- 1) Data transfer group.
- 2) Arithmetic instruction group
- 3) Logic group → Logical (AND, OR, NOR, XOR etc)
- 4) Branch group
- 5) Stack input/output group.

Date - 24 Jan.

① Data transfer group

1. i) MVI r data (8 bits)

MVI - move
 I → Immediate (it means data)

e.g. MVI B, (80)H

2) MVI m data m → memory pointer
 pointed by HL Pair.
 ↓
 HL having address.
 HL pair always having address.

3) MOV B, A → Transfer the content from A to B.

4) $MOV M, H$
 $MOV m, C$ → Transfer the content of C to the memory location pointed by HL Pair.

5) $MOV Rd, M$
 $MOV E, m$ Transfer the data pointed by HL Pair to the E Register.

6) $LXI rp(16\text{ bit})$ { L → load the data from the memory

LXI B $2030H$

immediate means data
Here 2030 is data not address.

STA → store the data of Accumulator into memory.

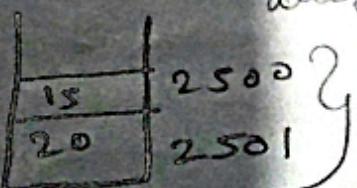
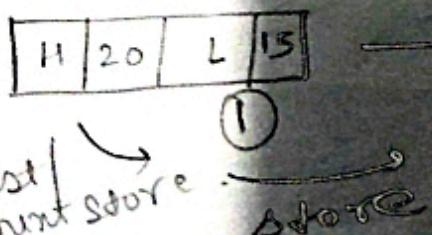
7) $ST A 2030$ → Store in Accumulator → 2030 (memory add.)

8) $LA D 2030$ → load the data of to the memory from the Accumulator.

9) $SHLD add$ { S → store the content of HL into this address location.

SHLD 2500

Last wall ka element game memory me aaga.



10) $\text{LHLD} \rightarrow$ Q
Load HL Pair Register from address 2500 .
 HL Pair Register from address 2500 .

11) $\text{STAX X} \rightarrow$ register Pair
Store X to Accumulator 16 bit.

$\text{STAX P} \rightarrow \text{DE}$
Store the Accumulator content into DE Pair.
means the address pointed by DE Pair.

12) $\text{LDAX X} \rightarrow \text{P}$. * From the memory location pointed by DE Pair to Accumulator
Load the Accumulator with the content of DE Pair.

13) XCHG . Exchange the content of $\text{HL} \leftrightarrow \text{DE}$

$$\begin{array}{l} \text{H} \leftrightarrow \text{D} \\ \text{L} \leftrightarrow \text{E} \end{array}$$

Arithmetic Group

- I) **ADD Register** → $A + B$ Result will Store in Accumulator.
- II) **ADD M** → memory pointed by HL Pair.
 $A + [M]$.
- III) **ADI data**
 $ADI, 70H$ Add 70 to Accumulator & result store in Accumulator.
- IV) **ADC r** { Add with carry
 $A \rightarrow A + r + \text{Cf} \rightarrow \text{carry}$. carry flag register.
- Eg: ADC B
 $A \rightarrow A + B + \text{carry}$.
 $A \rightarrow A + [m] + \text{carry}$.
- V) **ACI data.**
 $A \leftarrow A + 72 + \text{carry}$.



subtraction

1) $\boxed{\text{Sub}} \quad Y | 0$
 $\text{Sub} \quad B$
 $A \rightarrow A - B$

- 2) $\boxed{\text{Sub}} \quad M | 0$
 $A \rightarrow A - [m] \curvearrowright \text{gt is memory location}$
 $\text{Pointed by HL pair.}$

3) $\boxed{\text{SUI data}} | 0$ SUI 70H
 $\text{SUI} \rightarrow A - 70H$

4) $\boxed{\text{SBB}} \quad Y | 0$
 $A = A - C - \text{(y)} / \text{Br.}$

5) $\boxed{\text{SBB}} \quad M | 0$
 $A \rightarrow A - [m] / \text{Br.}$

6) $\boxed{\text{SBI}} \quad 70H | 0$
 $A \rightarrow A - 70 - \text{Br}$

(+) DAA (Decimal adjust accumulator).
BCD FORM ^{If 1 sum totaling} BCD Nos
(0-9)

If a no. is greater than 9 then we have to represent each & every number separately.

DAP

if the value of low order 4-bit. if the addition is greater than 9. then we have add to 6 in pd.

we are talking about this lower

$$\begin{array}{r}
 0011 & 1001 \\
 0001 & 0010 \\
 \hline
 0100 & 1011 \rightarrow \text{greater than } 9
 \end{array}$$

$$\begin{array}{r}
 0100 & 1011 \\
 & 0110 \\
 \hline
 01010000
 \end{array}$$

after adding 6 to lower bit
 If we get greater than 9 in Higher bit we add 6 to it

Logic graph

$$\text{XOR} \rightarrow \bar{A}B + A\bar{B}$$

A	B	
0	0	0
0	1	1
1	0	1
1	1	0

Logic * group

① $A \text{ AND } A \text{ AND } B$ \rightarrow AND Gate with A & B stored in the Accumulator.

② $A \text{ AND } M$ \rightarrow AND Gate with A & memory pointed by HL pair.

③ $A \text{ AND } \text{Data}$ \rightarrow Perform AND gate with Accumulator & Data.

④ $X \text{ RA } R$
 $X \text{ RA } B$

$A \text{ A } H$
 $2 \text{ D } H$

$$\begin{array}{r}
 1010 \quad 1010 \\
 0010 \quad 1101 \\
 \hline
 1011 \quad 0111
 \end{array}$$

$\Delta \neq H$.

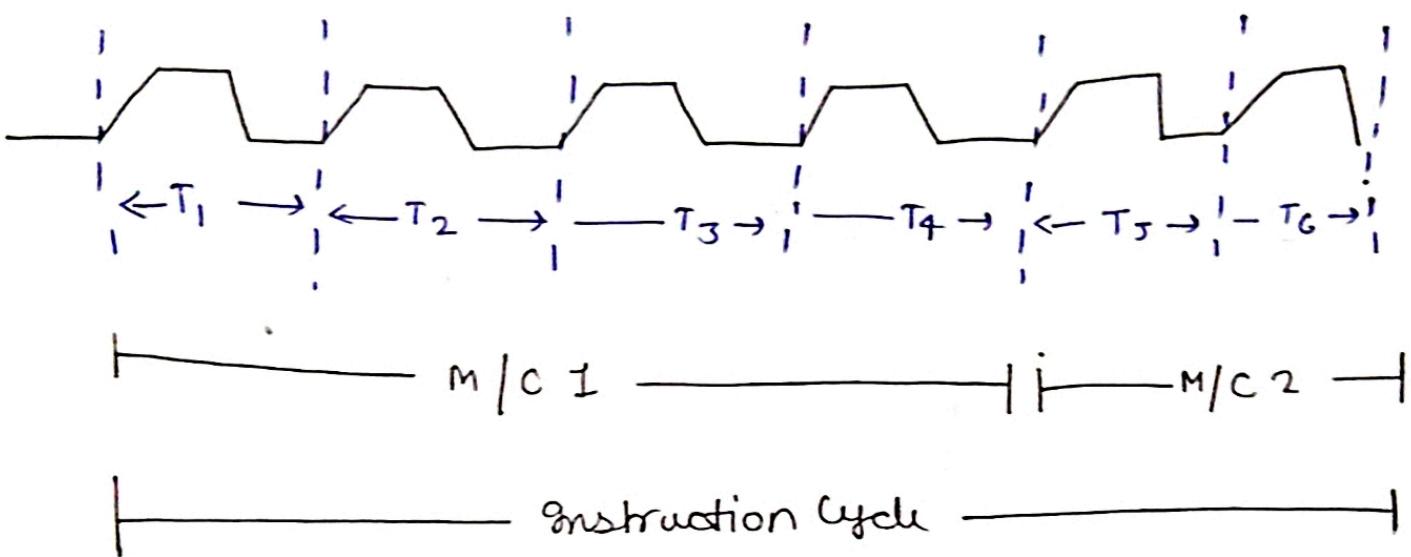
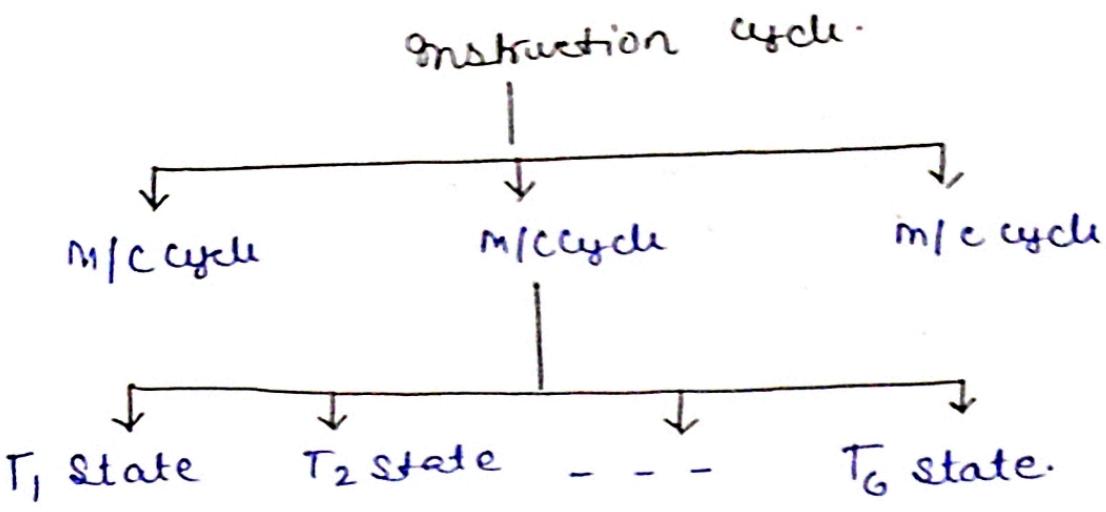
⑤ $X \text{ RA } M$

$X \text{ RA } M \rightarrow$

we perform the XOR operation with the Accumulator & M-location pointed by HL pair.

⑥ $X \text{ RI } \text{ data}$

\rightarrow In this instruction, we perform the



Opcode

Memory Read

Memory Parity

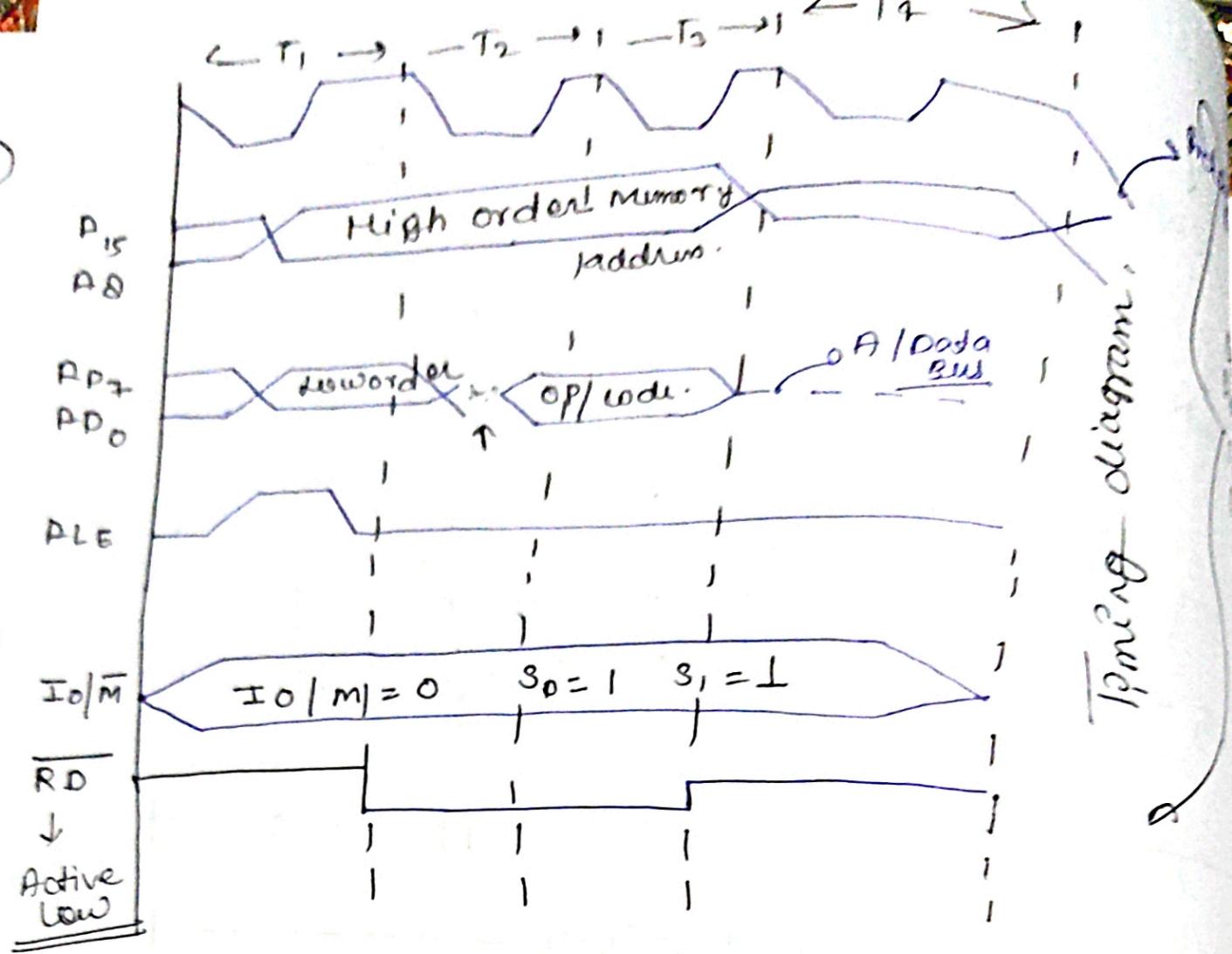
I/O Read

I/O Write

Interrupt Acknowledgment.

Bus Idle

	$I/O M$	S_1	S_0	\overline{RD}	\overline{WR}	\overline{INTF}
Opcode	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Parity	0	0	1	1	0	1
I/O Read	0	1	0	0	1	1
I/O Write	1	0	1	1	0	1
Interrupt Acknowledgment.	0	1	1	1	1	0
Bus Idle	0	0	0	1	1	1



Maximum tace state for
operation = 6 machine.

D/F⁰

Time required to execute one operation
is called instruction cycle.

Eg -

MVI A, 26H

Time required to complete one operation
→ machine cycle | No. of tace state = machine cycle.

Time Period = 0.34 sec. (microsec).

$$T = \frac{1}{3} \times 10^6$$

Kisi bhi opcode fetch karne ki tige

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