8085 Instruction Set :-

The 8085 instructions are classified into six groups

1. Data Transfer Group
2. Arithmetic Group
3. Logical Group
4. Branch Control Group
5. Stack, I/O and Machine Control Group
6. Interrupt Control Group.

(1) Data Transfer Group:

→ The instruction of this group transfer data from source to destination without changing the content of source.

→ The flag content is not affected by any instruction.

→ The instruction of this group perform various transfer as:

Data Transfer Group

Register to Register	Register to Memory	Memory to Register	Data to Register	Data to Memory
MOV r1, r2	MOV M, r	MOV r, M	MVI r, data	MVI M, data
XCHG	STA addr	LDA addr	LXI rp, data	
	SHLD addr	LHLD addr		
	STAX rp	LDAX rp		

S.NO.	Instruction	Description	No. of Bytes	Addressing Mode	Example	
					Before Execution	After Execution
1.	MOV r_1, r_2 $[r_1] \leftarrow [r_2]$	The content of register r_2 is moved to register r_1	1	Register	MOV A, B [A]= 25H [B] = 63H	 [A]= 63H [B] = 63H
2.	MOV r, M $[r] \leftarrow [[HL]]$	The content of memory whose address is in register pair rp, moved to register r.	1	Indirect	MOV A, M HL = 2500H [2500] = 75H [A] = 33H	 HL = 2500H [2500] = 75H [A] = 75H
3.	MOV M, r $[[HL]] \leftarrow r$	The content of register r is moved to memory location address by HL pair	1	Indirect	MOV M, A HL = 2500H [2500] = 75H [A] = 33H	 HL = 2500H [2500] = 33H [A] = 33H
4.	MVI r, data $[r] \leftarrow$ data	Data is moved to register r.	2	Immediate	MVI B, 53H [B] = 38H	 [B] = 53H
5.	MVI M, data $[[HL]] \leftarrow$ data	The data is moved to memory location whose address is in HL pair.	2	Immediate / Indirect	MVI M, 14H HL = 2500H [2500] = 73H	 HL = 2500H [2500] = 14H
6.	LXI rp, data 16	The 16 bit data is moved to register pair rp.	3	Immediate	LXI H, 1234H [HL] = 5678 [H] = 56 [L] = 78	 [HL] = 1234 [H] = 12 [L] = 34
7.	LDA addr [A] $\leftarrow$ addr	The content of memory location whose address is specified in instruction, is loaded into accumulator.	3	Direct	LDA 7000H [A]= 55H [7000] = 11H	 [A] = 11H [7000] = 11H

8.	STA addr [addr] ← [A]	The content of accumulator is stored in memory location whose address is specified	3	Direct	STA 7000H [A] = 55H [7000] = 11H	STA 7000H [A] = 55H [7000] = 55H
9.	LHLD addr L ← addr H ← addr+1	The content of memory location whose address is specified is loaded.	3	Direct	LHLD 7000 [7000] = 34H [7001] = 12H [L] = 55H [H] = 44H	LHLD 7000 [7000] = 34H [7001] = 12H [L] = 34H [H] = 12H
10.	SHLD addr addr ← L addr+H ← H	The content of register is stored at specified memory location.	3	Direct	SHLD 7000 [7000] = 34H [7001] = 12H [L] = 55H [H] = 44H	SHLD 7000 [7000] = 55H [7001] = 44H [L] = 55H [H] = 44H
11.	LDAX rp [A] ← [[rp]]	The content of memory location, whose address in rp, is loaded in acc.	1	Indirect	LDAX D [DE] = 5000H [5000] = 11H [A] = 22H	LDAX D [DE] = 5000H [5000] = 11H [A] = 11H
12.	STAX rp [[rp]] ← [A]	The content of accumulator is stored in memory location whose address is in rp	1	Indirect	STAX B [BC] = 7500H [7500] = 11H [A] = 22H	STAX B [BC] = 7500H [7500] = 11H [A] = 22H
13.	XCHG	Exchange the content of HL with DE pair.	1	Register	[HL] = 1234H [DE] = 5678H	[HL] = 5678H [DE] = 1234H