8085 Architecture

INTR INTA RST5.5 RST6.5 RST7.5 TRAP

Interrupt Control

Serial I/O Control — SID, SOD

Internal data bus

Accumulator (8)

Temp. Reg. (8)

Flag (5) Flip-Flop

Arithmetic Logic Unit (ALU) (8)

Instruction Register (8)

Instruction decoder & Machine Cycle Encoding

Timing & Control

X1 X2 → CLK GEN

CLK OUT

READY

Control: RD WR ALE

Status: SO S1 IO/M

DMA: HLDA HOLD

Reset: RESET OUT, RESET IN

Multiplexer

Register Array

W	Z
Temp. Reg. (8)	Temp. Reg. (8)
B (8)	C (8)
D (8)	E (8)
H (8)	L (8)
Stack Pointer (16)	
Program Counter (16)	
Address Latch (16)	

Reg. Select

Address Buffer (8) → A15 – A8 Address Bus

Data / Address Buffer (8) → AD7 – AD0 Address / Data Bus

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· Fig shows the internal architecture of 8085.

(i) ALU

→ The arithmetic / logic unit perform the computing functions; it includes the accumulator, the temporary register, the arithmetic & logic circuit and five flags.

→ The temporary register is used to hold data during arithmetic / logic operation.

→ The results are stored in accumulator and flags (flip-flops) are set or reset according to the result of the operation.

→ The flags are affected by arithmetic and logic operation in the ALU. The results are stored in accumulator.

> The description of flags are mentioned in programming Model.

eg

    BC
  + DE
  ─────
    9A

        1 1 1 1   1   ← Carry
        1 0 1 1   1 1 0 0
    +   1 1 0 1   1 1 1 0
      ─────────────────────
      1 1 D 0 1   1 0 1 0
          9   A

12 + 14 = 26
26 - 16 = 10
11 + 13 = 24
25 - 16 = 9

If MSB = 1, S = 1
Z = 0   ∵ ALE = X
AC = 0
P = 1
CY = 1

S	Z		AC		P		CY

(ii) Timing and Control Unit

→ This unit synchronizes all the microprocessor operations with the clock and generates the control signal Necessary for communication between the microprocessor and peripherals.

(III) Instruction Register and Decoder.

→ It is the part of ALU.

→ When an instruction is fetch from memory, it is loaded to the instruction register.

→ The decoder decodes the instruction and establishes the sequence of event to follow.

→ The instruction register is not programmable and cannot be accessed through any instruction.

(iv) Register Array

→ Two registers (temporary registers) W & Z are included in the register array.

→ These registers are used to hold 6-bit data during the execution of some instructions.

→ As these are used internally, they are not available to the programmer.