iCE40™ HX-Series Ultra Low-Power mobileFPGA™ Family

March 30, 2012 (1.31) **Data Sheet**

- **HX-Series - Tablet targeted series optimized for high performance**
- **Low cost package offerings**
- **80% faster than iCE65**
- **Tablet resolution HD video and imaging**
- **Proven, high-volume 40 nm, low-power CMOS technology**
- **Integrated Phase-Locked Loop (PLL)**
  - Clock multiplication/division for display, SerDes, and memory interface applications
- **Up to 533 MHz PLL Output**
- **Reprogrammable from a variety of methods and sources**
- **Flexible programmable logic and programmable interconnect fabric**
  - 8K look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **Complete iCEcube™ development system**
  - Windows® and Linux® support
  - VHDL and Verilog logic synthesis
  - Place and route software
  - Design and IP core libraries
  - Low-cost iCEman40HX development board

Figure 1: **iCE40 HX-Series Family Architectural Features**

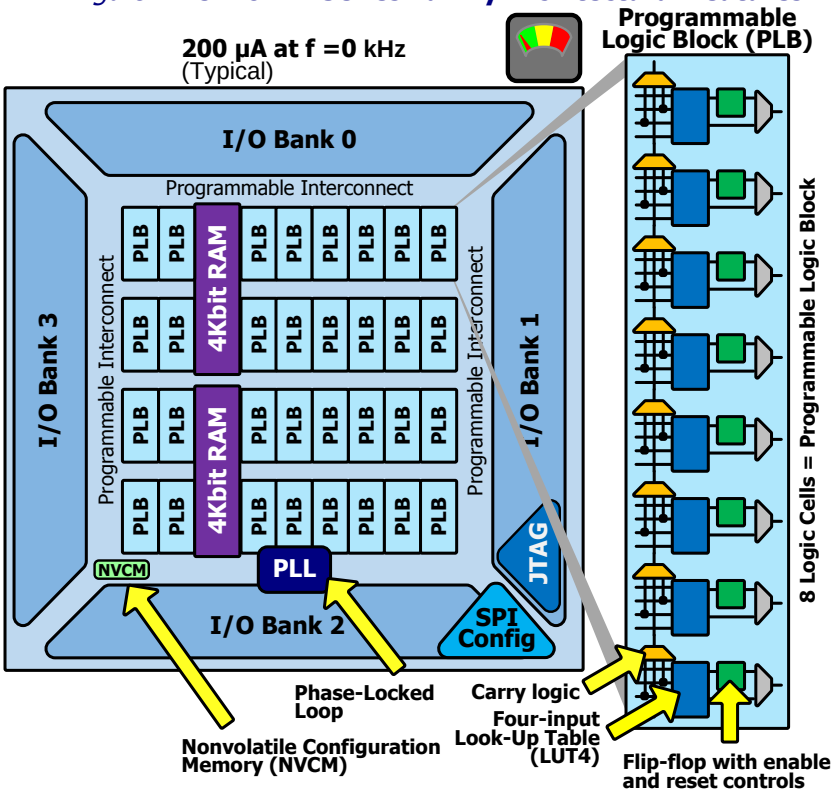


Table 1: **iCE40HX Ultra Low-Power Programmable Logic Family Summary**

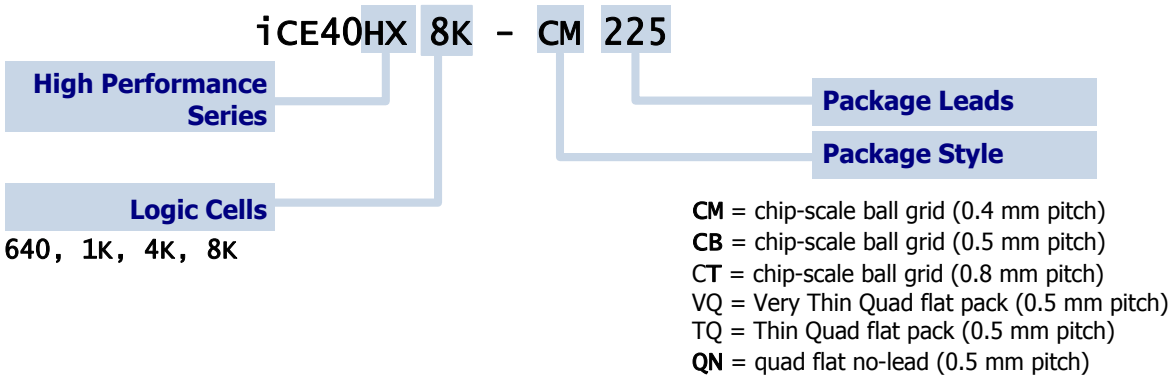
Part Number				HX640	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)				640	1,280	3,520	7,680
RAM4K Memory Blocks				8	16	20	32
RAM4K RAM bits				32K	64K	80K	128K
Phase-Locked Loops (PLLs)				1	1	2	2
Configuration bits (maximum)				120 Kb	245 Kb	533 Kb	1,057 Kb
Core Operating Power 0 KHz[1]				200 µA	267 µA	667 µA	1100 µA
Maximum Programmable I/O Pins				67	95	95	206
Maximum Differential Input Pairs				8	11	12	26
Package	**Code**	**Area mm**	**Pitch mm**	**Programmable I/O: Max I/O (LVDS)**			
225-ball BGA	CM225	7x7	0.4				178(23)
132-ball BGA	CB132	8x8	0.5		95(11)	95(12)	95(12)
284-ball BGA	CB284	12x12	0.5				
256-ball BGA	CT256	14x14	0.8				206(26)
100-pin quad flat pack	VQ100	14x14	0.5	67(8)	72(9)		

Note 1: At 1.2V VCC

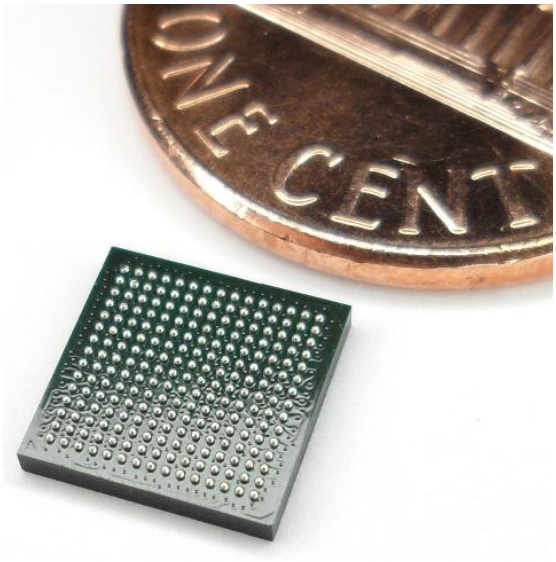
Ordering Information

Figure 2 describes the iCE40HX ordering codes for all packaged components. See the separate DiePlus data sheets when ordering die-based products. See the separate iCE40 Pinout Excel files for package and pinout specifications.

Figure 2: **iCE40HX Ordering Codes (packaged, non-die components)**



iCE40HX8K-CM225
225-ball Chip-Scale BGA Package
(7x7 mm footprint, 0.4 mm pitch)



Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, junction temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 2 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 2: **Absolute Maximum Ratings**

Symbol	Description	Minimum	Maximum	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **VCCIO_3** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, 2 and 3 plus SPI interface)	–0.5	4.00	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI** **VIN_3**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, 2 and 3 plus SPI interface)	–1.0	3.6	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)	–0.5	1.30	V
I_{OUT}	DC output current per pin	—	20	mA
T_J	Junction temperature	–55	125	°C
T_{STG}	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 3: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	High Performance, low-power	1.14	1.20	1.26	V
VPP_2V5[1]	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST[2]	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks	**LVCMOS33**	2.70	3.30	3.47	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCPLL[3]	Analog voltage supply to the Phase Locked Loop (PLL)		1.14	1.20	1.26	V
T_A	Ambient temperature		–40	—	85	°C
T_{PROG}	NVCM programming temperature		10	25	30	°C

Notes:

1. VPP_2V5 must be connected to a valid voltage, when the iCE40HX device is active.
2. VPP_FAST, used only for fast production programming, must be left floating or unconnected in application.
3. VCCPLL must be tied to VCC when PLL is not used.

I/O Characteristics

Table 4: **PIO Pin Electrical Characteristics**

Symbol	Description	Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current	V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance			6		pF
C_{GBIN}	GBIN global buffer pin input capacitance			6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration	VCCIO = 3.3V		60		kΩ
		VCCIO = 2.5V		80		kΩ
		VCCIO = 1.8V		120		kΩ
		VCCIO = 1.5V		160		kΩ
V_{HYST}	Input hysteresis	VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

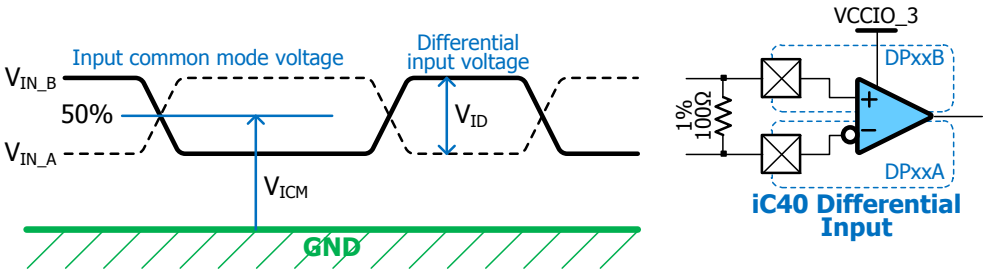
Single-ended I/O Characteristics

Table 5: **I/O Characteristics**

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	0.4	1.20	2	2

Differential Inputs

Figure 3: **Differential Input Specifications**



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

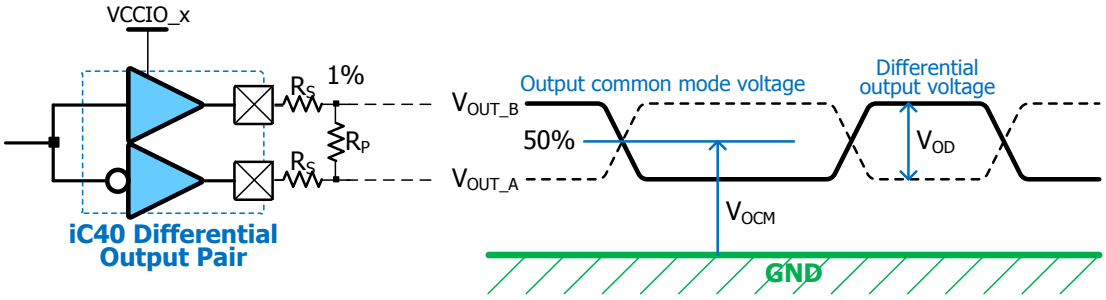
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 6: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	V_{CCIO_3} (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 4: **Differential Output Specifications**



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 7: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	V_{CCIO_x} (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	Nom	Max	R_S	R_P	Min	Nom	Max	Min	Nom	Max
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

AC Timing Guidelines

The following examples provide some guidelines of device performance. The actual performance depends on the specific application and how it is physically implemented in the iCE65P FPGA using the Lattice iCEcube2 software. The following guidelines assume typical conditions (VCC = 1.0 V or 1.2 V as specified, temperature = 25 °C). Apply derating factors using the iCEcube2 timing analyzer to adjust to other operating regimes.

Programmable Logic Block (PLB) Timing

Table 8 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 5 and Figure 6.

Figure 5 **PLB Sequential Timing Circuit**

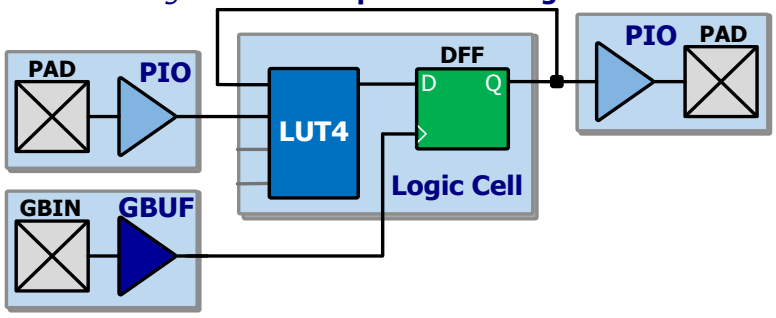


Figure 6 **PLB Combinational Timing Circuit**

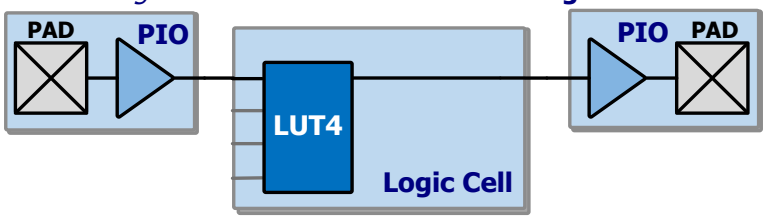


Table 8: **Typical Programmable Logic Block (PLB) Timing**

			Nominal VCC	1.2 V	
			Description	**Typ.**	**units**
Sequential Logic Paths					
F_{TOGGLE}	GBIN input	GBIN input	Flip-flop toggle frequency. DFF flip-flop output fed back to LUT4 input with 4-input XOR, clocked on same clock edge	256	MHz
t_{CKO}	DFF clock input	PIO output	Logic cell flip-flop (DFF) clock-to-output time, measured from the DFF CLK input to PIO output, including interconnect delay.	3.9	ns
t_{GBCKLC}	GBIN input	DFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the logic cell DFF flip-flop.	1.5	ns
t_{SULI}	PIO input	GBIN input	Minimum setup time on PIO input, through LUT4, to DFF flip-flop D-input before active clock edge on the GBIN input, including interconnect delay.	.67	ns
t_{HDLI}	GBIN input	PIO input	Minimum hold time on PIO input, through LUT4, to DFF flip-flop D-input after active clock edge on the GBIN input, including interconnect delay.	0	ns
Combinational Logic Paths					
t_{LUT4IN}	PIO input	LUT4 input	Asynchronous delay from PIO input pad to adjacent PLB interconnect.	1.8	ns
t_{ILO}	LUT4 input	LUT4 output	Logic cell LUT4 combinational logic propagation delay, regardless of logic complexity from input to output.	0.34	ns
t_{LUT4IN}	LUT4 output	PIO output	Asynchronous delay from adjacent PLB interconnect to PIO output pad.	3.7	ns

Programmable Input/Output (PIO) Block

Table 9 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 7 and Figure 8. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube2 development software reports timing adjustments for other I/O standards.

Figure 7: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

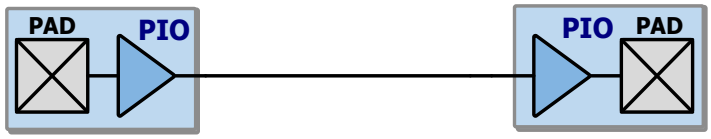


Figure 8: **Programmable I/O (PIO) Sequential Timing Circuit**

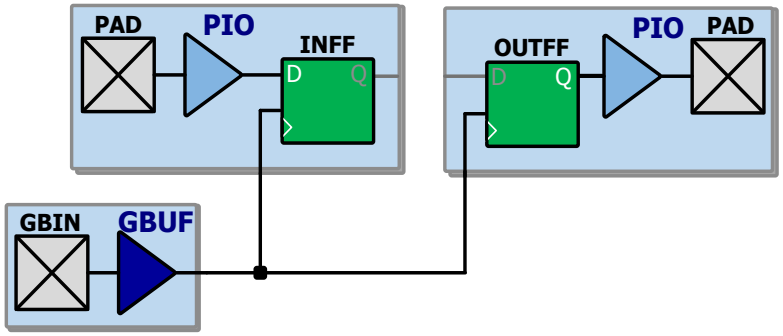


Table 9: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

			Nominal VCC	1.2 V	
			Description	**Typ.**	**units**
Synchronous Output Paths					
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	3.1	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	1.4	ns
Synchronous Input Paths					
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	1.6	ns
Pad to Pad					
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	1.8	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	3.4	ns

RAM4K Block

Table 10 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 9.

Figure 9: **RAM4K Timing Circuit**

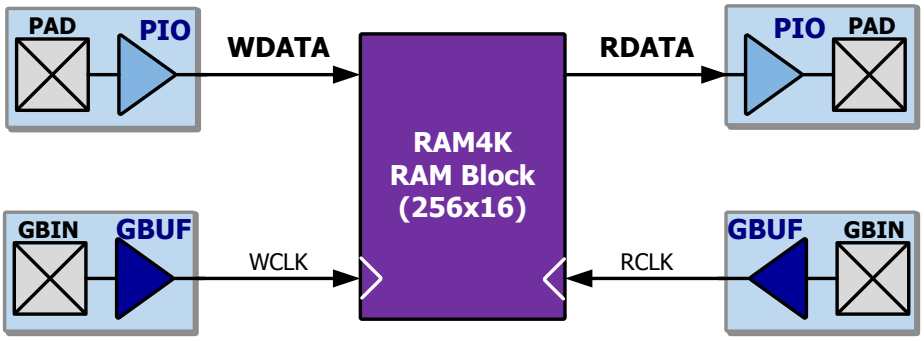


Table 10: **Typical RAM4K Block Timing**

			Nominal VCC	1.2 V	
			Description	**Typ.**	
Write Setup/Hold Time					
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.44	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	ns
Read Clock-Output-Time					
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	4.1	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	1.4	ns
Write and Read Clock Characteristics					
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.30	ns
t_{RMWCKL}			Write clock Low time	0.35	ns
t_{RMWCYC}			Write clock cycle time	0.71	ns
F_{WMAX}			Sustained write clock frequency	256	MHz

Phase-Locked Loop (PLL) Block

Table 11 provides timing information for the Phase-Locked Loop (PLL) block shown in Figure 10.

Figure 10: **Phase-Locked Loop (PLL)**

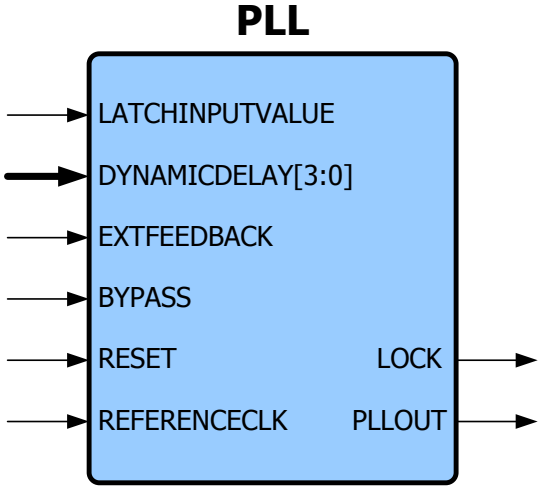


Table 11: **Phase-Locked Loop (PLL) Block Timing**

Symbol	From	To	Description	Nominal VCC 1.2 V Min.	Typical	Max.	Units
Frequency Range							
F_{REF}			Input clock frequency range	10	—	133	MHz
F_{OUT}			Output clock frequency range (cannot exceed maximum frequency supported by global buffers)	16	—	533	MHz
Duty Cycle							
PLL_{IJ}			Input duty cycle	35	—	65	%
Tw_{HI}			Input clock high time	2.5	—	—	ns
Tw_{LOW}			Input clock low time	2.5	—	—	ns
PLL_{OJ}			Output duty cycle	45	—	55	%
Fine Delay							
t_{FDTAP}			Fine delay adjustment, per tap		165		ps
PLL_{TAPS}			Fine delay adjustment settings	0	—	15	taps
PLL_{FDAM}			Maximum delay adjustment		2.5		ns
Jitter							
PLL_{IPJ}			Input clock period jitter	—	—	+/- 300	ps
PLL_{OPJ}			PLLOUT output period jitter	—	1% or ≤ 100	+/- 1.1% output period or ≥ 110	ps
Lock/Reset Time							
t_{LOCK}			PLL lock time after receive stable, monotonic REFERENCECLK input	—	—	50	µs
tw_{RST}			Minimum reset pulse width	20	—	—	ns

Notes:

1. Output jitter performance is affected by input jitter. A clean reference clock < 100ps jitter must be used to ensure best jitter performance.
2. The output jitter specification refers to the intrinsic jitter of the PLL.

Internal Configuration Oscillator Frequency

Table 12 shows the operating frequency for the iCE40's internal configuration oscillator.

Table 12: **Internal Oscillator Frequency at VCC = 1.2V**

Symbol	Oscillator Mode	Frequency (MHz)		Description
		Min.	Max.	
f_{OSCD}	**Default**	7	10	Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM.
f_{OSCL}	**Low Frequency**	21	30	Supported by most SPI serial Flash PROMs
f_{OSCH}	**High Frequency**	35	50	Supported by some high-speed SPI serial Flash PROMs
	Off	0	0	Oscillator turned off by default after configuration to save power.

Configuration Timing

Table 13 shows the maximum time to configure an iCE40HX device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 12 and the maximum configuration bitstream size from Table 1, which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

Table 13: **Typical SPI Master or NVCM Configuration Timing by Oscillator Mode**

Symbol	Description	Device	Default	Low Freq.	High Freq.	Units
$t_{CONFIGL}$	Time from when minimum Power-on Reset (POR) threshold is reached until user application starts.	iCE40HX640	53	25	11	ms
		iCE40HX1K	53	25	11	ms
		iCE40HX4K	230	110	50	ms
		iCE40HX8K	230	110	50	ms

Table 14 provides timing for the CRESET_B and CDONE pins.

Table 14: **General Configuration Timing**

Symbol	From	To	Description	All Grades		Units
				Min.	Max.	
t_{CRESET_B}	CREST_B	CREST_B	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge	200	—	ns
t_{DONE_IO}	CDONE High	PIO pins active	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated.	—	49	Clock cycles
			SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge)	Depends on SPI_SCK frequency		

Table 15 provides various timing specifications for the SPI peripheral mode interface.

Table 15: **SPI Peripheral Mode Timing**

Symbol	From	To	Description	All Grades		Units
				Min.	Max.	
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE40HX FPGA is clearing its internal configuration memory	300	—	µs
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge	12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge	12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time	20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time	20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*	40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*	1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 16 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz

Table 16: **VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	VCC	iCE40HX640 Typical	iCE40HX1K Typical	iCE40HX4K Typical	iCE40HX8K Typical	Units
I_{CC0K}	f =0	1.2V	200	267	667	1100	µA
I_{CC32K}	f ≤ 32.768 kHz	1.2V	222	297	741	1222	µA
I_{CC32M}	f = 32.0 MHz	1.2V	4	4	12	13	mA

I/O Power

Table 17 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 17: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Maximum	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		uA
I_{CCO_1}	I/O Bank 1		« 1		uA
I_{CCO_2}	I/O Bank 2		« 1		uA
I_{CCO_3}	I/O Bank 3		« 1		uA
I_{CCO_SPI}	SPI Bank		« 1		uA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE40HX Power Estimator Spreadsheet our use the power estimator built into the iCEcube2 software.

Revision History

Version	Date	Description
1.31	30-MAR-2012	Updated Table 1
1.3	22-MAR-2012	Production Release Updated Notes on Table 3: Recommended Operating Conditions Updated values in Table 4, Table 5 Table 12, Table 13 and Table 17
1.21	5-MAR-2012	Updated Figure 3 and Figure 4 to specify iCE40
1.2	13-FEB-2012	Updated company name
1.1	15-DEC-2011	Moved package specifications to iCE40 Pinout Excel files. Updated Table 1 maximum IOs.
1.01	31-OCT-2011	Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum IOs.
1.0	11-JUL-2011	Initial Release

Lattice Semiconductor Corporation
5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421
United States of America

Tel: +1 503 268 8000
Fax: +1 503 268 8347