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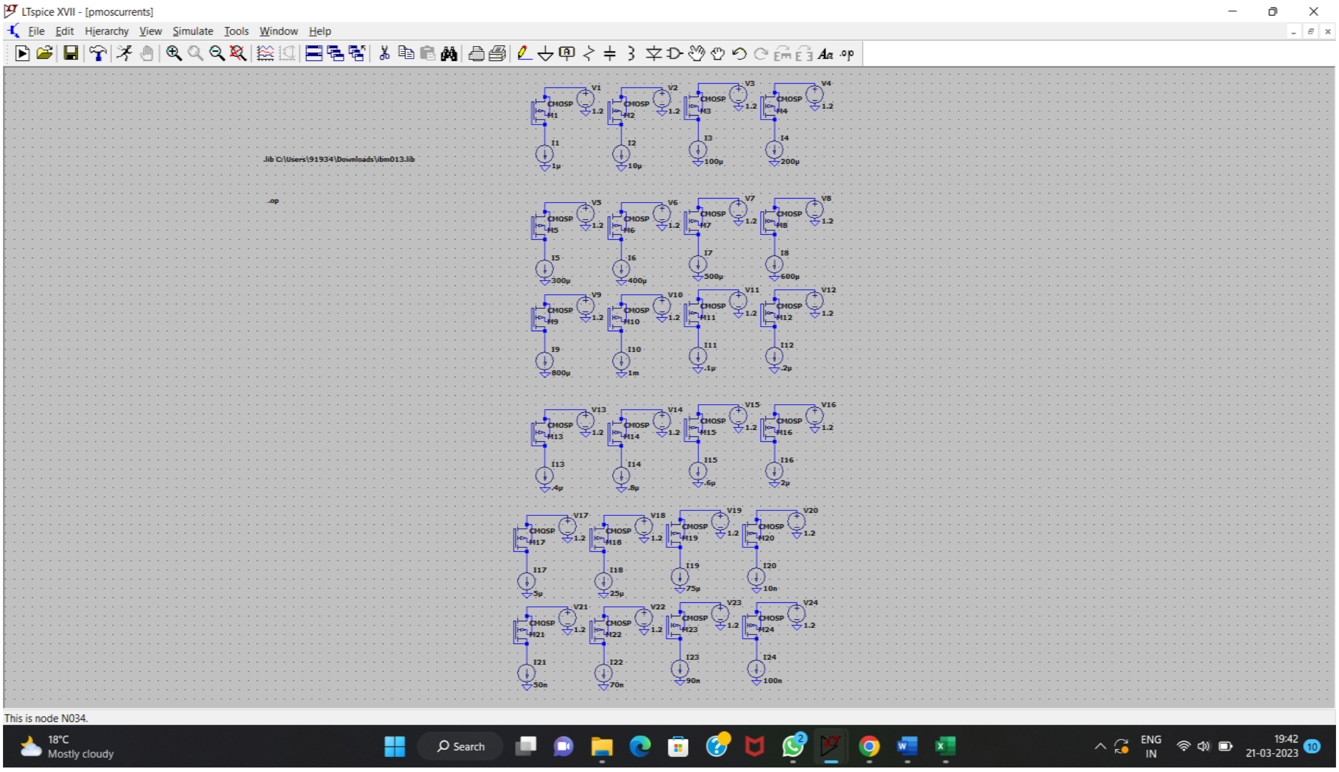
CHOICE OF TECHNOLOGY – 130 nm

INPUT STAGE -nMOS

b) Characterisation of transistors

Characterisation is done by iterative method with different biasing currents until we get desired values such as gm/gds.



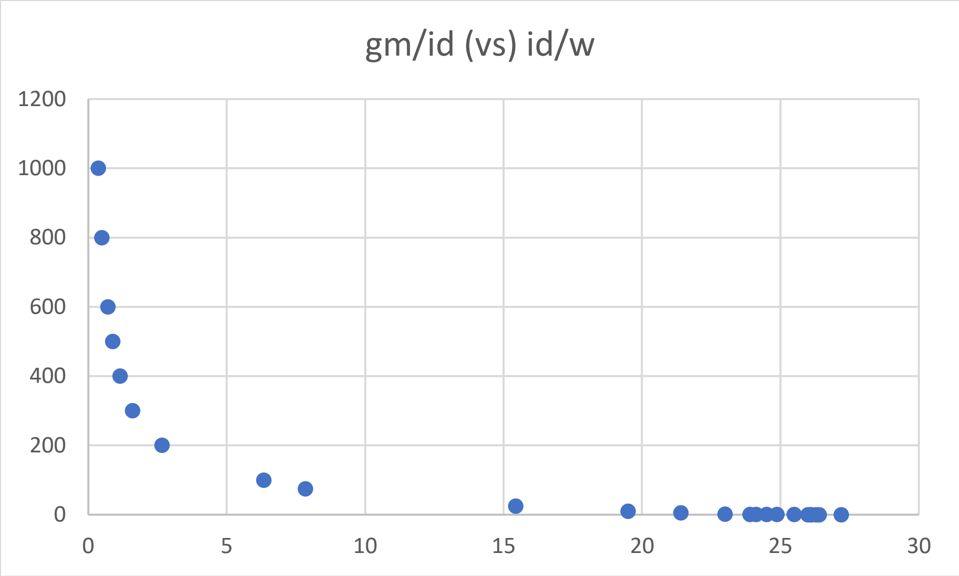
Different pmos will give values differently so choose the value which is nearby required value such as gm/gds and then change the length of selected transistor to get desired value, by this method we characterise the transistors.

Similar approach in nmos also.

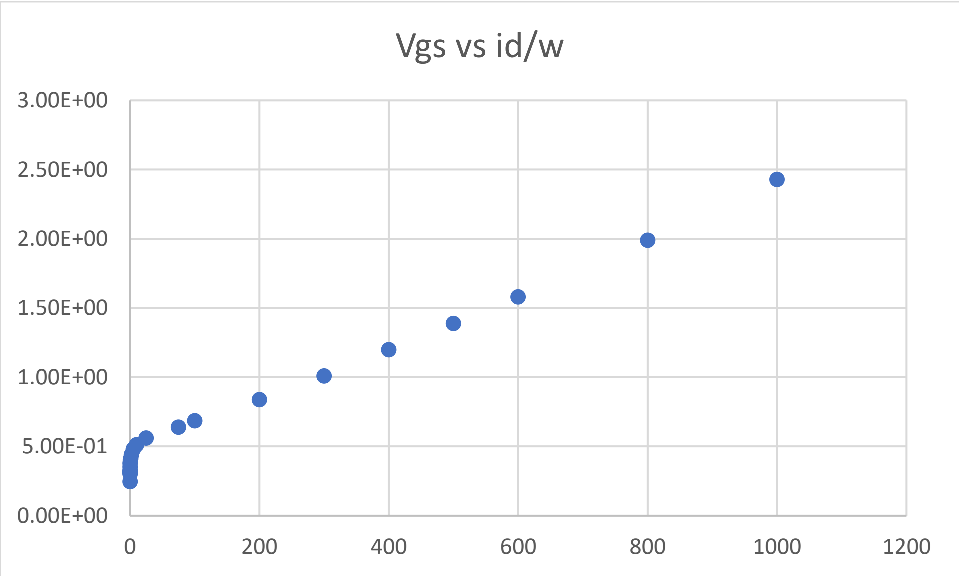
Sizes of m5 m7 and m8 are found by biasing m8 with 0.1uA and then sizing the m5 and m7 according to current that need to flow through that branch.

nMos plots for minimum length:

gm/id vs id/w

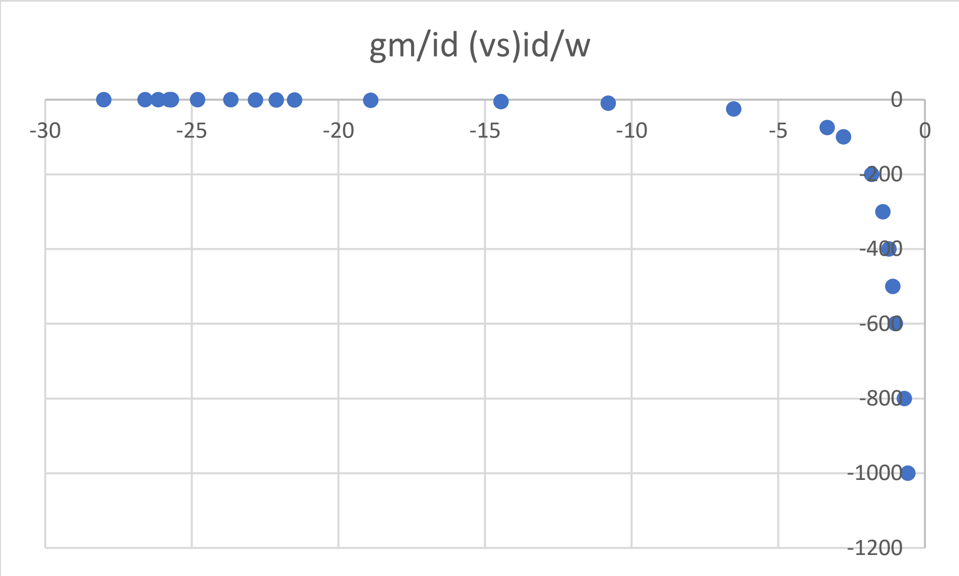


Vgs vs id/w:

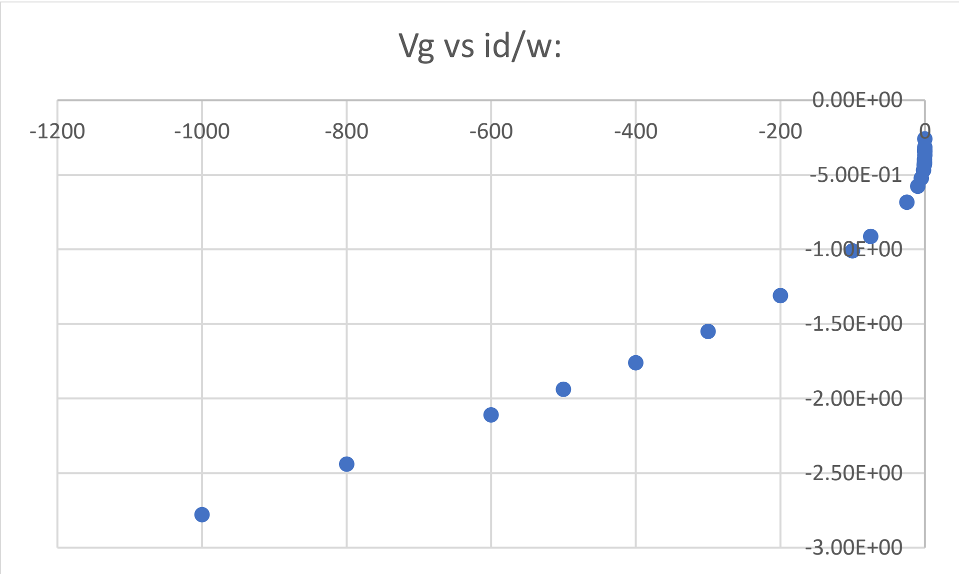


Pmos plots for minimum length:

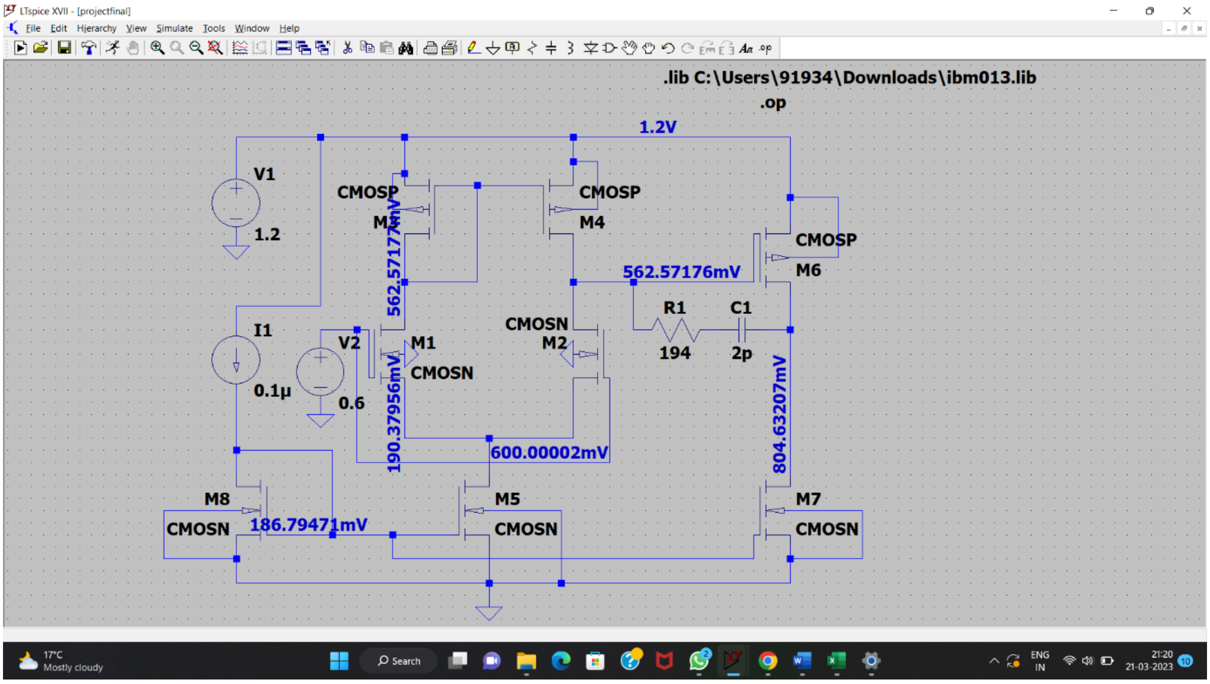
Id/w vs gm/id:



Vgs vs id/w:

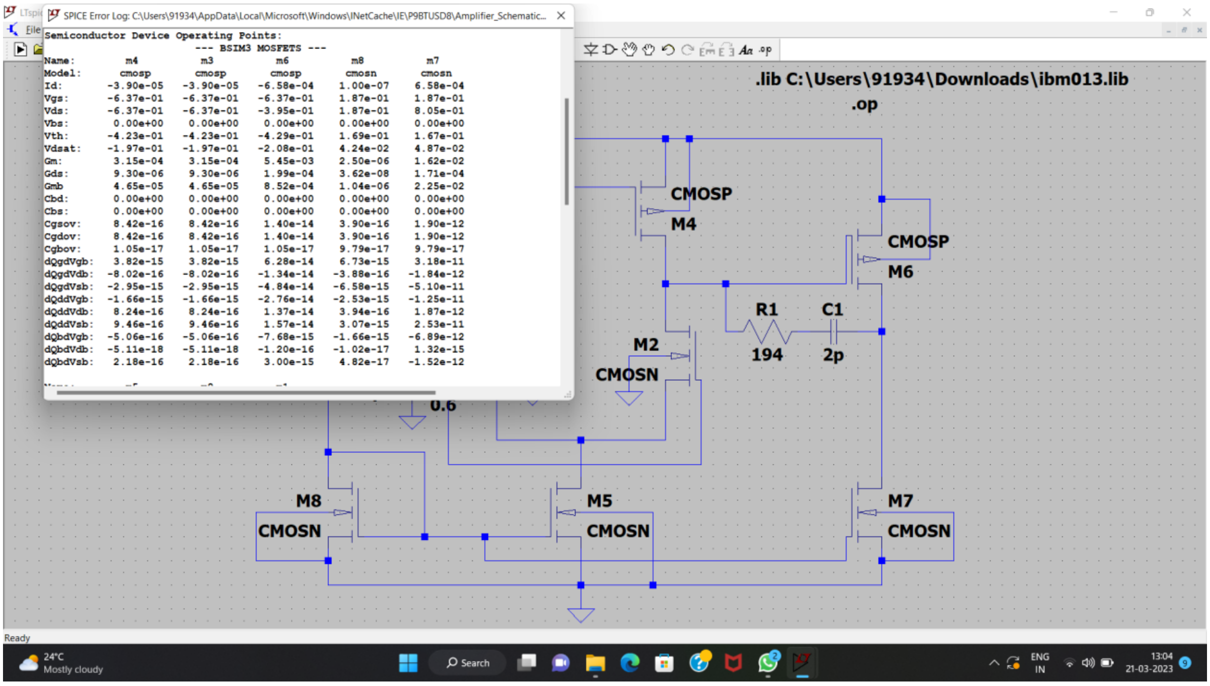


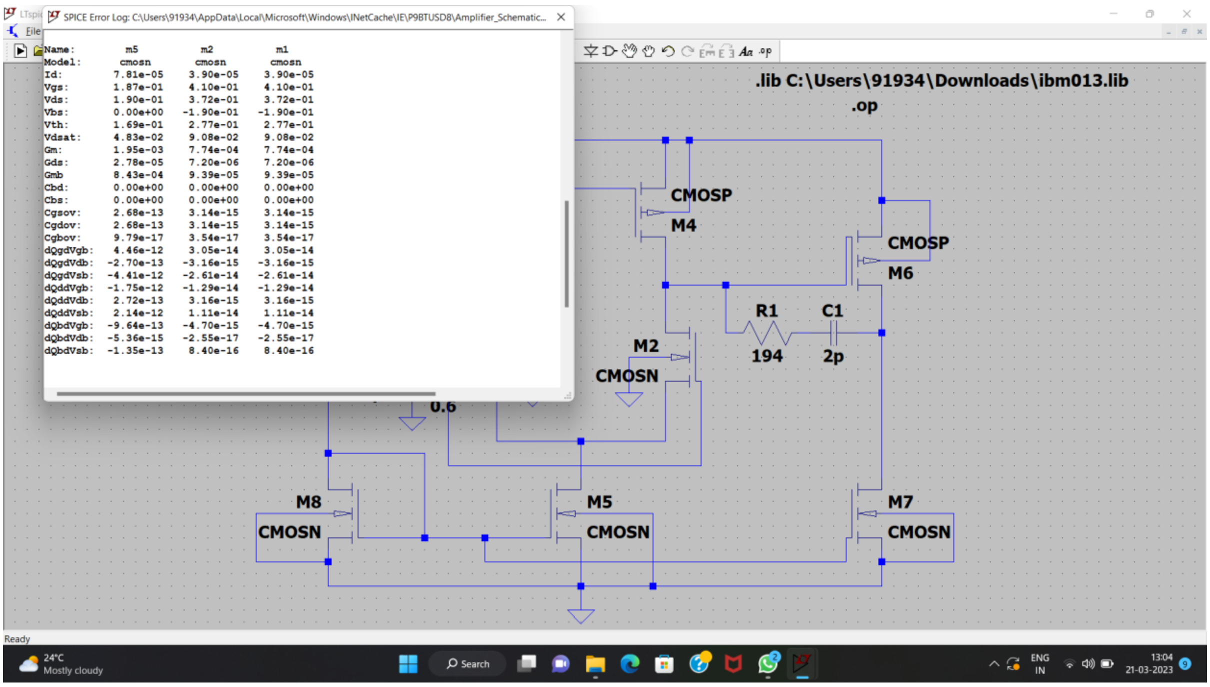
C)OTA WITH BIASING:



OTA biased with vdd and vdd/2, the required current ,width and length in each branch has computed theoretically and implemented practically, the practical values are a bit different than theoretical values so taken care by changing the dimensions of m5 and m7

DC operating Values:





Which obtain the 1)current through differential pair is 39uA

2)current through m5 is 78uA

3)current through m7 is 658 u A

The bias currents are in both simulation and theoretical are equal

D)First I imagined phase margin as 60 degrees and wu as 50Mhz and calculated all the parameters requied but I found difficulty in characterising transistor with obtained gm/gds, so I changed phase margin to 70 degrees and unity gain frequency to 60Mhz and calculated all transistors parameter as follows

I found the characteristics of nmos and pmos by taking multiple transistors with different biasing currents and simulated,out of all transistor we select one transistor which has close value of parameters which we need

By this method I found the Id and width of transistors for desired output

Dc gain (gm/gds) has obtained by iterative method by increasing length of transistor(selected from 24 transistors with different biasing current ,and obtained dc gain.

Sizes of m5 m7 and m8 are found by biasing m8 with 0.1uA and then sizing the m5 and m7 according to current that need to flow through that branch

• let $pm = 70^{\circ}$, $\omega_u = 60\text{mHz}$. $C_L = 5pf$ $R_L = 10k\Omega$

$$pm = 90 - \tan^{-1}\left(\frac{\omega_u}{p_2}\right)$$

$$70 = 90 - \tan^{-1}\left(\frac{\omega_u}{p_2}\right)$$

$$\tan^{-1}\left(\frac{\omega_u}{p_2}\right) = 20$$

$$p_2 = \frac{60 * 10^6}{\tan(20)} = 164 * 10^6 \text{ Hz}$$

we have $p_2 = \frac{Gm_2}{C_L'}$

$$Gm_2 = p_2 * C_L' \quad (C_L' \approx C_L)$$

$$Gm_2 = 164 * 10^6 * 2\pi * 5 * 10^{-12}$$

$$Gm_2 = 5152\ \mu \text{ semens}$$

from $\omega_u = \frac{Gm_1}{C_c}$

let $C_c = 2pf$ $(C_c < C_L)$

then $Gm_1 = 60 * 10^6 * 2 * 10^{-12} * 2\pi$

$$Gm_1 = 753.9 \text{ semens}$$

. let overall gain: $A = 1000$ then

$$A = \frac{Gm_1\, Gm_2}{G_1\, G_L'} \quad \left[\text{let } G_L = G_2 = 100\,\mu \text{ semens}\right]$$

$$1000 = 618240 * 10^{-12} * 2\pi$$

$$1000 = \frac{120 * 5152 * 10^{-12}}{G_1 * 2G_L} \quad (G_L = 100\mu \text{ semens})$$

$$\left[G_1 = 19.41\mu \text{ semens}\right]$$

now $\frac{G_{m1}}{G_{dsn}} = \frac{753.94}{\frac{19.41\mu}{2}} = 77.6397 = A_1$

$$A_2 = \frac{G_{m2}}{G_L'} = \frac{5152 * 10^{-6}}{2 * 100 * 10^{-6}} = 25.7$$

we observe that $(G_{m1} < G_{m2})$ and $(A_1 > A_2)$ which we need.

Finding L_n and W_n of Differential pair

- by taking multiple nmos with different current in biasing, obtained $\frac{g_m}{g_{ds}}$, the value which is closer to $\frac{g_{m1}}{g_{dsn}}$ has taken.
- now we get $L = 375n$

I_d

$$\left(\frac{G_m}{I_d}\right)_{\text{theoretical}} = \left(\frac{G_m}{I_d}\right)_{\text{simulation}}$$

$$\frac{753.94}{I_d} = \frac{9.62 * 10^{-5}}{5 * 10^{-6}}$$

$$\left[I_d = 39.184\mu A\right]$$

W_n

$$\left(I_d / \omega\right)_{\text{theorey}} = \left(I_d / \omega\right)_{\text{simulation}}$$

$$\left[\frac{5 * 10^{-6}}{1 * 10^{-6}}\right] = \left(\frac{39.18 * 10^{-6}}{W_n}\right)$$

$$\left[W_n = 7.84m\right]$$

pmos characterisation

- Similar to nmos, we follow iterative method to findout width and length of pmos

$$\left(\frac{Gdsn}{Id}\right)_{theoretical} = \frac{9.7054}{39.184} = 0.2477.$$

now by iteration findout the nearly value of $\left(\frac{Gdsn}{Id}\right)$ equal to theoretical value, to obtain that increase length.

$$\text{we got } \left(\frac{Gdsn}{Id}\right)_{simulation} = \frac{2.61\mu}{18\mu}$$

wp

$$(Id/\omega)_{simulation} = (Id/\omega)_{theory}$$

$$\left(\frac{184}{1\times10^{-6}}\right) = \left(\frac{39.184}{wp}\right)$$

$$\boxed{wp = 2.17\,um}. \quad Lp = 120\,nm.$$

- Now we need $\left(\frac{Id}{\omega}\right)_3 = (Id/\omega)_5$

$$(18.05) = (Id/\omega)_5$$

- Now by iteration with different biasing current find out gm and Id at which we get $(Id/\omega) = 18.05$.

we get $(gm/Id)_{simulation} = \frac{1.42\times10^{-4}}{1.8\times10^{-5}}$

$$(gm/Id)_{simulation} = 7.88$$

$\left(gm/Id\right)$ calculations = $\left(gm/Id\right)$-theory

$$\frac{5152\times10^{-6}}{Id} = 7.85$$

$$\left[Id = 653\ \mu A\right]$$

Now $\left(\frac{Id}{W}\right) = 18.05$

$$wp = \frac{653u}{18.05}$$

$$\left[wp = 36\ um\right]$$

<u>characterisation of m8, m5 and m7</u>

0.2uA flowing across m8 whose $w=2u$, (fixing 2u for m5, m8 & m7 lengths)

<u>m5</u>

$$\frac{0.2uA}{2u} = \frac{78.36u}{w5}$$

$$\left[(w5) = 783.6\ um\right]$$

<u>m7</u>

$$\frac{0.2u}{2u} = \frac{653u}{w7}$$

$$w7 = \left[6530\ um\right]$$

$R_1 = \frac{1}{gm_2} = 194$ ohms $\quad C_1 = C_c = 2pf.$

E)

Gm1	753.9 u siemens
Gm2	5152 u siemens
R1	194 ohms
C1	2pf
A1(gain of first stage)=Gm1/G1	38.8
A2(gain of second stage)=Gm2/Gl’	25

F)

property	M1	M2	M3	M4	M5	M6	M7	M8
Length	375n	375n	120n	120n	1u	120n	1u	1u
Width	7.8u	7.8u	2.17u	2.17u	664u	36u	4700u	1u
Biased current	39u	39u	-39u	39u	78u	658 u A	658 u A	0.1uA
vgs	.41v	.41v	-0.63v	-0.63v	.187	-0.637 v	0.187v	0.187
vds	.372 v	.372v	-0.63 v	-0.63	.19	-0.395 v	0.805v	0.187
Vth	.277 v	.227v	-.423 v	-0.423	.169	-0.429 v	0.167	0.169
Gm	774u s	774u s	315 u s	315 u s	1.95 m s	5450 u s	16200us	2.5 u s
Gds	7.2u s	7.2u s	9.3 u s	9.3 u s	27.8u s	199 u s	171u s	0.0362us

Obtained values of some transistors from simulation are given below

SPICE Error Log: C:\Users\91934\Desktop\hf project\projectfinal.log

```
Semiconductor Device Operating Points:
                        --- BSIM3 MOSFETS ---
Name:         m4          m3          m6          m8          m7
Model:      cmosp       cmosp       cmosp       cmosn       cmosn
Id:       -3.90e-05   -3.90e-05   -6.58e-04    1.00e-07    6.58e-04
Vgs:      -6.37e-01   -6.37e-01   -6.37e-01    1.87e-01    1.87e-01
Vds:      -6.37e-01   -6.37e-01   -3.95e-01    1.87e-01    8.05e-01
Vbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:      -4.23e-01   -4.23e-01   -4.29e-01    1.69e-01    1.67e-01
Vdsat:    -1.97e-01   -1.97e-01   -2.08e-01    4.24e-02    4.87e-02
Gm:        3.15e-04    3.15e-04    5.45e-03    2.50e-06    1.62e-02
Gds:       9.30e-06    9.30e-06    1.99e-04    3.62e-08    1.71e-04
Gmb        4.65e-05    4.65e-05    8.52e-04    1.04e-06    2.25e-02
Cbd:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cgsov:     8.42e-16    8.42e-16    1.40e-14    3.90e-16    1.90e-12
Cgdov:     8.42e-16    8.42e-16    1.40e-14    3.90e-16    1.90e-12
Cgbov:     1.05e-17    1.05e-17    1.05e-17    9.79e-17    9.79e-17
dQgdVgb:   3.82e-15    3.82e-15    6.28e-14    6.73e-15    3.18e-11
dQgdVdb:  -8.02e-16   -8.02e-16   -1.34e-14   -3.88e-16   -1.84e-12
dQgdVsb:  -2.95e-15   -2.95e-15   -4.84e-14   -6.58e-15   -5.10e-11
dQddVgb:  -1.66e-15   -1.66e-15   -2.76e-14   -2.53e-15   -1.25e-11
dQddVdb:   8.24e-16    8.24e-16    1.37e-14    3.94e-16    1.87e-12
dQddVsb:   9.46e-16    9.46e-16    1.57e-14    3.07e-15    2.53e-11
dQbdVgb:  -5.06e-16   -5.06e-16   -7.68e-15   -1.66e-15   -6.89e-12
dQbdVdb:  -5.11e-18   -5.11e-18   -1.20e-16   -1.02e-17    1.32e-15
dQbdVsb:   2.18e-16    2.18e-16    3.00e-15    4.82e-17   -1.52e-12
```

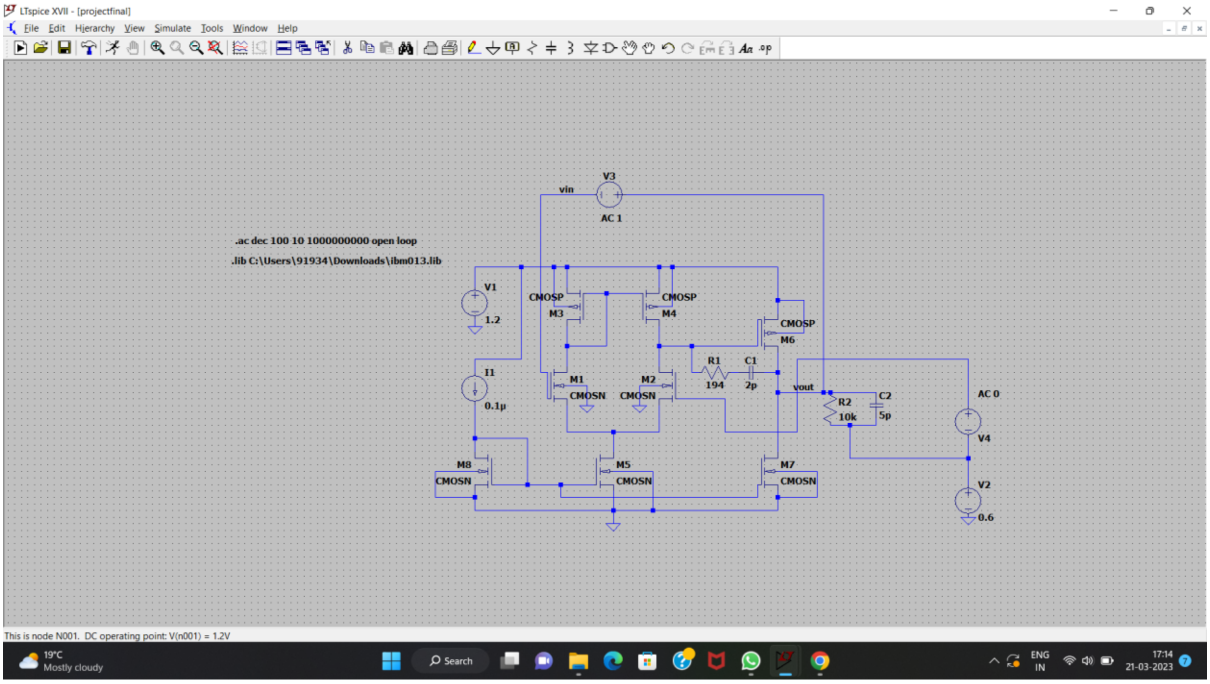
G) Dc operating values obtained from simulation:

Name:	m4	m3	m6	m8	m7
Model:	cmosp	cmosp	cmosp	cmosn	cmosn
Id:	-3.90e-05	-3.90e-05	-6.58e-04	1.00e-07	6.58e-04
Vgs:	-6.37e-01	-6.37e-01	-6.37e-01	1.87e-01	1.87e-01
Vds:	-6.37e-01	-6.37e-01	-3.95e-01	1.87e-01	8.05e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.23e-01	-4.23e-01	-4.29e-01	1.69e-01	1.67e-01
Vdsat:	-1.97e-01	-1.97e-01	-2.08e-01	4.24e-02	4.87e-02
Gm:	3.15e-04	3.15e-04	5.45e-03	2.50e-06	1.62e-02
Gds:	9.30e-06	9.30e-06	1.99e-04	3.62e-08	1.71e-04
Gmb	4.65e-05	4.65e-05	8.52e-04	1.04e-06	2.25e-02
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	8.42e-16	8.42e-16	1.40e-14	3.90e-16	1.90e-12
Cgdov:	8.42e-16	8.42e-16	1.40e-14	3.90e-16	1.90e-12
Cgbov:	1.05e-17	1.05e-17	1.05e-17	9.79e-17	9.79e-17
dQgdVgb:	3.82e-15	3.82e-15	6.28e-14	6.73e-15	3.18e-11
dQgdVdb:	-8.02e-16	-8.02e-16	-1.34e-14	-3.88e-16	-1.84e-12
dQgdVsb:	-2.95e-15	-2.95e-15	-4.84e-14	-6.58e-15	-5.10e-11
dQddVgb:	-1.66e-15	-1.66e-15	-2.76e-14	-2.53e-15	-1.25e-11
dQddVdb:	8.24e-16	8.24e-16	1.37e-14	3.94e-16	1.87e-12
dQddVsb:	9.46e-16	9.46e-16	1.57e-14	3.07e-15	2.53e-11
dQbdVgb:	-5.06e-16	-5.06e-16	-7.68e-15	-1.66e-15	-6.89e-12
dQbdVdb:	-5.11e-18	-5.11e-18	-1.20e-16	-1.02e-17	1.32e-15
dQbdVsb:	2.18e-16	2.18e-16	3.00e-15	4.82e-17	-1.52e-12

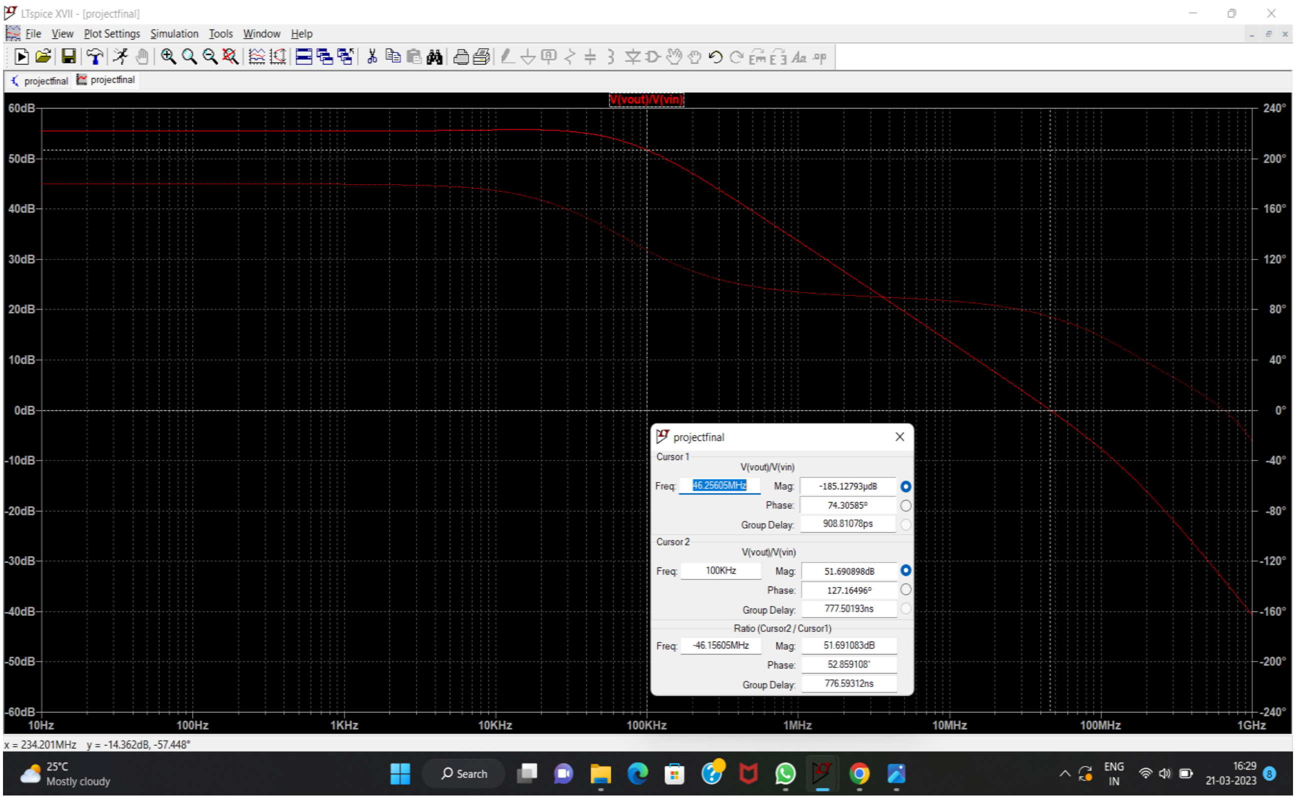
Name:	m5	m2	m1
Model:	cmosn	cmosn	cmosn
Id:	7.81e-05	3.90e-05	3.90e-05
Vgs:	1.87e-01	4.10e-01	4.10e-01
Vds:	1.90e-01	3.72e-01	3.72e-01
Vbs:	0.00e+00	-1.90e-01	-1.90e-01
Vth:	1.69e-01	2.77e-01	2.77e-01
Vdsat:	4.83e-02	9.08e-02	9.08e-02
Gm:	1.95e-03	7.74e-04	7.74e-04
Gds:	2.78e-05	7.20e-06	7.20e-06
Gmb	8.43e-04	9.39e-05	9.39e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00
Cgsov:	2.68e-13	3.14e-15	3.14e-15
Cgdov:	2.68e-13	3.14e-15	3.14e-15
Cgbov:	9.79e-17	3.54e-17	3.54e-17
dQgdVgb:	4.46e-12	3.05e-14	3.05e-14
dQgdVdb:	-2.70e-13	-3.16e-15	-3.16e-15
dQgdVsb:	-4.41e-12	-2.61e-14	-2.61e-14
dQddVgb:	-1.75e-12	-1.29e-14	-1.29e-14
dQddVdb:	2.72e-13	3.16e-15	3.16e-15
dQddVsb:	2.14e-12	1.11e-14	1.11e-14
dQbdVgb:	-9.64e-13	-4.70e-15	-4.70e-15
dQbdVdb:	-5.36e-15	-2.55e-17	-2.55e-17
dQbdVsb:	-1.35e-13	8.40e-16	8.40e-16

The values we calculated like transistor currents and sizing are matching with simulation resuts

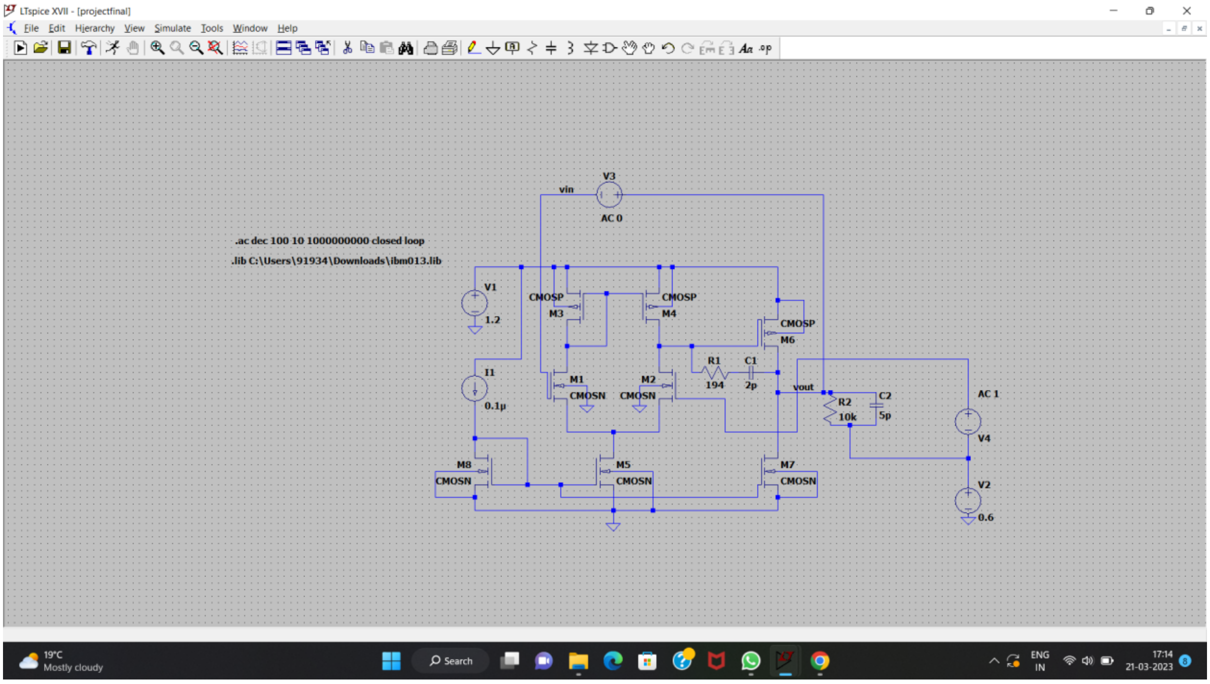
H) open loop plots and output:



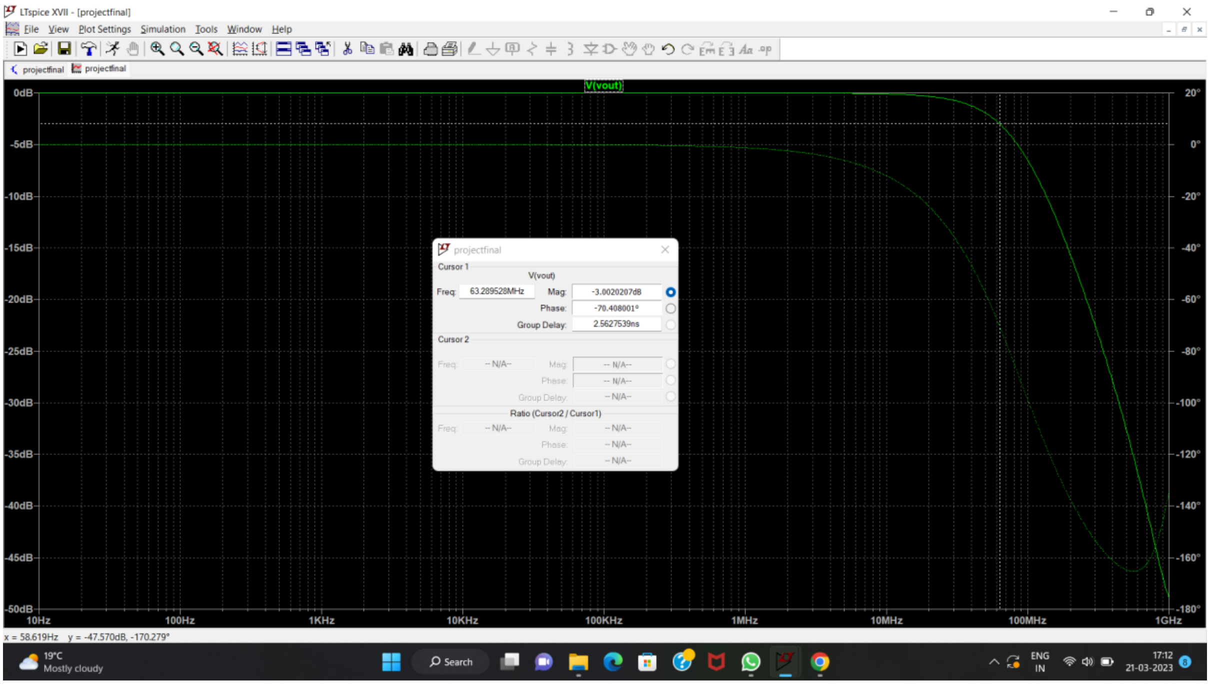
Magnitude and Phase plot:



Closed loop plots and output:



Closed loop Magnitude and phase plots:



Simulated results:

Phase margin =70.4 degrees

Unity gain frequency =63.2 Mhz

Theoretical values:

Phase margin=70 degrees

Unity gain frequency=60Mhz

The phase and unity gain frequency of simulated output are matching with theoretical values

And the closed loop output does not have any peakings