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Academic Task Number: 02 | **Course Code: CSE539**

Date of allotment: 12.10.2023 | **Course Title: Advanced Computer Architecture**

Date of submission: 19.10.2023 | **Maximum Marks: 30M**

Academic Task Type: Objective | **Section: K20MT**

Q. No.	Question Statement	Course Outcome	Bloom's level	Marks per Question
1	Magnetic disk is an example of a. Offline Storage b. Offset Storage **c. Online Storage** d. None of the mentioned	CO3	L3: Apply	1
2	The speed of memory is slower than CPU ____ times a. **1000 times** b. 10 times c. 100 times d. 10,000 times	CO3	L3: Apply	1
3	Caches are built out of _____ **a. Static Ram** b. Dynamic RAM c. PROM d. EEPROM	CO3	L3: Apply	1
4	Round-trip time from the CPU to the ith level memory is known as: _____ a. Execution Time b. **Access Time** c. Slot Time d. None of the mentioned	CO3	L3: Apply	1
5	The data exchange between the CPU and cache is performed in term of _____ **a. Words** b. bits c. bytes d. None of the mentioned	CO3	L3: Apply	1
6	Identify among the following that represents temporal locality a. Structures **b. Loops**	CO3	L3: Apply	1

	c. arrays d. None of the mentioned			
7	The main purpose of CPU is to generate _____ type of address **a. Virtual** b. Login c. Physical d. None of the mentioned	CO3	L3: Apply	1
8	The basic abbreviation of MMU is _____ a. **Memory management unit** b. Main memory unit c. Main management unit d. None of the mentioned	CO3	L3: Apply	1
9	Determine among the following that presents spatial locality a. Loops b. Structures **c. Arrays** d. None of the mentioned	CO3	L3: Apply	1
10	Identify among the following policies, Belady's anomaly occurs a. NRU b. LFU c. **FIFO** d. None of the mentioned	CO3	L3: Apply	1
11	The central arbitration scheme is also known as a. **Daisy Chain** b. Independent requests and grants c. Distribution Arbitration d. None of the mentioned	CO3	L3: Apply	1
12	If the cache size is increased in the system then the hit ratio will _____ a. Decrease b. **Increase** c. Reamins unchanged d. None of the mentioned	CO3	L3: Apply	1
13	A word size is expressed in bytes. The common word sizes are:	CO3	L3: Apply	1

	a. **8, 16, and 32 bits** b. 64 bits c. 256 bits d. 4, 8, and 16 bits			
14	The transformation of data from main memory into the cache memory is known as a. Direct mapping b. Associative mapping c. **Mapping process** d. None of the mentioned	CO3	L3: Apply	1
15	The transformation of data from secondary memory to main memory is called as: a. Mapping process b. Associative mapping c. Direct mapping **d. Paging process**	CO3	L3: Apply	1
16	The effective bandwidth of each PEs is: **a. Inversely proportional to the number of PEs fighting for the bus** b. Directly proportional to the number of PEs fighting for the bus c. Both a and b d. None of the mentioned	CO4	L2: Understand	1
17	Identify the type of parallelism that is implemented by pipelining **a. Temporal Parallelism** b. Spatial Parallelism c. Data Parallelism d. None of the mentioned	CO4	L2: Understand	1
18	Scalar Pipelines are under the control of _____ a. Hardware Control b. Spatial Control c. None of the mentioned **d. Software Control**	CO4	L2: Understand	1
19	Identify the definition of Forbidden Latency a. distance between any two checkmarks in the same column of the reservation table b. distance between all the check marks	CO4	L2: Understand	1

	c. Distance between any two checkmarks in the same row of the reservation table d. None of the mentioned			
20	The values of the latency must always be a. Negative **b. Positive** c. Both Positive and Negative d. None of the mentioned	CO4	L2: Understand	1
21	The utilization pattern of successive stages in the pipelines is specified by a. Reservation table b. Reserved table c. None of the mentioned **d. both space time diagram and reservation table**	CO4	L2: Understand	1
22	The abbreviation of CPA is _____ **a. Carry Propagation Adder** b. Carry Power Adder c. Carry Proportional Adder d. none of the mentioned	CO4	L2: Understand	1
23	The average latency of a constant cycle is ____ a. Constant b. Always less than latency **c. Latency itself** d. None of the mentioned	CO4	L2: Understand	1
24	The abbreviation of CSA is given as **a. Carry Save Adder** b. Carry Storage Adder c. Carry Simple Adder d. None of the mentioned	CO4	L2: Understand	1
25	Identify the algorithm that acts a better choice for pipelining **a. Merge Sort algorithm** b. Hash algorithm c. Hash algorithm d. None of the mentioned	CO4	L2: Understand	1
26	A technique in which the output of one pipeline is directly released into another pipeline is called ____ **a. Chaining**	CO4	L2: Understand	1

	b. Scatter c. Intelligent compiler d. None of the mentioned			
27	The process of shifting computations from run time to the compile time is called _____ a. Code Motion b. Reordering c. None of the mentioned **d. Constant folding**	CO4	L2: Understand	1
28	During Loop Scheduling, when the loop size is large the relative gain is a. Large **b. Less** c. Both a and b d. None of the mentioned	CO4	L2: Understand	1
29	The clock period (T) is given as: a. T + T(m) – T(l) **b. T + T(m) + T(l)** c. T + T(m) * T(l) d. None of the mentioned	CO4	L2: Understand	1
30	In general pipelines are classified as linear and non linear but the actual or real pipelines are _____ a. Linear **b. Non linear** c. Exponential d. None of the mentioned	CO4	L2: Understand	1