Lovely Professional University, Punjab

Course Code	Course Title	Lectures	Tutorials	Practicals	Credits	
CSE539	ADVANCED COMPUTER ARCHITECTURE	3	0	0	3	
Course Weightage	ATT: 5 CA: 25 MTT: 20 ETT: 50					

Course Focus	EMPLOYABILITY

Course Outcomes :Through this course students should be able to

CO1 :: define the aspects of multi-computers and multiprocessors

CO2 :: recognize the concept of scalable and parallel computer architectures for proportional increase in performance with increased system resources.

CO3 :: describe the hierarchy and organization in memory in multiprocessors and digital computers

CO4 :: understand the superscalar techniques in pipelined processors

CO5 :: analyze the significance of multi-computers and coherence of multiprocessors and its organization

CO6 :: outline a deeper insight into the design of high-end microprocessors that will support the future applications.

	TextBooks (T)		
Sr No	**Title**	**Author**	**Publisher Name**
T-1	ADVANCED COMPUTER ARCHITECTURE - PARALLELISM, SCALABILITY AND PROGRAMMABILITY	KAI HWANG, NARESH MOTWANI	MCGRAW HILL EDUCATION

	Reference Books (R)		
Sr No	**Title**	**Author**	**Publisher Name**
R-1	PARALLEL COMPUTERS - ARCHITECTURE & PROGRAMMING	V. RAJARAMAN, C. SIVA RAM MURTHY	PRENTICE HALL
R-2	ADVANCED COMPUTER ARCHITECTURES	DEZSO SIMA	PEARSON

Other Reading (OR)	
Sr No	**Journals articles as Compulsary reading (specific articles, complete reference)**
OR-1	http://www.ddegjust.ac.in/studymaterial/mca-5/mca-502.pdf ,
OR-2	http://www.cse.hcmut.edu.vn/~tnthinh/ACA/ACA_Intro_2013.pdf ,
OR-3	http://www.seas.gwu.edu/~bhagiweb/cs211/lectures/lectures.html ,

Relevant Websites (RW)		
Sr No	**(Web address) (only if relevant to the course)**	**Salient Features**
RW-1	https://chetsarena.files.wordpress.com/2012/10/3-2-performance-evaluations.pdf	Speedup performance laws
RW-2	http://www.cs.cmu.edu/afs/cs/academic/class/15213-f10/www/lectures/09-memory-hierarchy.pdf	Memory hierarchy technology
RW-3	http://www.philadelphia.edu.jo/academics/kaubaidy/uploads/ACA-Lect5.pdf	Arithmetic pipeline design
RW-4	http://arwins2.tripod.com/ec6020_files/publikasi/ch2-3-fadli.pdf	Control flow vs data flow architecture

Audio Visual Aids (AV)		
Sr No	**(AV aids) (only if relevant to the course)**	**Salient Features**
AV-1	http://nptel.ac.in/video.php?subjectId=106102062	NPTEL videos related to several Computer Architecture topics
AV-2	https://www.youtube.com/watch?v=T4VVC3eeZI0	Memory hierarchy

LTP week distribution: (LTP Weeks)	
Weeks before MTE	7
Weeks After MTE	7
Spill Over (Lecture)	7

Detailed Plan For Lectures

Week Number	Lecture Number	Broad Topic(Sub Topic)	Chapters/Sections of Text/reference books	Other Readings, Relevant Websites, Audio Visual Aids, software and Virtual Labs	Lecture Description	Learning Outcomes	Pedagogical Tool Demonstration/ Case Study / Images / animation / ppt etc. Planned	Live Examples

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Week 1	Lecture 1	Parallel Computer Models (The state of computing, Multiprocessors and Multi-computers)	T-1	OR-1	L1: Introduction to the course(Lecture 0) and Computer Development Milestones and Elements of modern Computers; L2: Introduction to the course (Lecture 0), and Computer Development Milestones and Elements of modern Computers, Evolution of Computer Architecture; L2: System Attributes to Performance, Multiprocessors and Multicomputers.	Review computer generations, and understand several types of computer architectures	Case studies and Illustrations with numerical representation	
	Lecture 2	Parallel Computer Models (The state of computing, Multiprocessors and Multi-computers)	T-1	OR-1	L1: Introduction to the course(Lecture 0) and Computer Development Milestones and Elements of modern Computers; L2: Introduction to the course (Lecture 0), and Computer Development Milestones and Elements of modern Computers, Evolution of Computer Architecture; L2: System Attributes to Performance, Multiprocessors and Multicomputers.	Review computer generations, and understand several types of computer architectures	Case studies and Illustrations with numerical representation	
	Lecture 3	Parallel Computer Models (Multi-vector and SIMD Computers)	T-1 R-2	OR-1	L3: Introduction to Vector Super computers and SIMD Supercomputers	Understand the basics of stated types of supercomputer models	Real life examples with detailed explanation	A drill instructor telling his corps to about face, or turn. Instead of ordering each soldier one by one to about face, he can order the entire corps to do so

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Week 2	Lecture 4	Parallel Computer Models (PRAM and VLSI Models)	T-1	OR-1	L4: Introduction to Parallel computers; L5: Introduction to Vector Super computers and SIMD Supercomputers	Understand the basics of stated types of supercomputer models	Numerical Illustrations based on real world scenarios	Changing the brightness of an image
	Lecture 5	Parallel Computer Models (PRAM and VLSI Models)	T-1	OR-1	L4: Introduction to Parallel computers; L5: Introduction to Vector Super computers and SIMD Supercomputers	Understand the basics of stated types of supercomputer models	Numerical Illustrations based on real world scenarios	Changing the brightness of an image
	Lecture 6	Parallel Computer Models (Architectural Development Tracks)	T-1	OR-2	L6: Architectural Development Tracks	Review the evolution of computer architectures with examples of real systems of each type of computer models	Examples of several variants of computer architecture	
Week 3	Lecture 7	Program and Network Properties(Conditions of Parallelism)	T-1		L7: Data and Resource Dependencies; L8: Hardware and Software Parallelism and Role of Compilers	To understand the alternative mechanisms to determine dependence among program instructions	Program based illustrations	The system initialization task may need to run first, before other tasks can run
	Lecture 8	Program and Network Properties(Conditions of Parallelism)	T-1		L7: Data and Resource Dependencies; L8: Hardware and Software Parallelism and Role of Compilers	To understand the alternative mechanisms to determine dependence among program instructions	Program based illustrations	The system initialization task may need to run first, before other tasks can run
	Lecture 9	Program and Network Properties(Program Partitioning and Scheduling)	T-1 R-1		L9: Grain Sizes and Latency, Grain Packing and Scheduling; L10: Static Multiprocessor Scheduling (Node duplication algorithm)	Understand several levels of parallelism and scheduling mechanisms	Numerical/Program Illustrations	Preemptive uniprocessor, Student life schedule
Week 4	Lecture 10	Program and Network Properties(Program Partitioning and Scheduling)	T-1 R-1		L9: Grain Sizes and Latency, Grain Packing and Scheduling; L10: Static Multiprocessor Scheduling (Node duplication algorithm)	Understand several levels of parallelism and scheduling mechanisms	Numerical/Program Illustrations	Preemptive uniprocessor, Student life schedule

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Week 4	Lecture 11	Program and Network Properties(Program Flow Mechanisms)	T-1	RW-1	L11: Control Flow (control-driven), Data Flow (data driven) and Reduction Machine (demand driven) Models. Network Properties and Routing, Static Interconnection Networks	Understand several ways in which processors/memory/oth er elements of computer can be interconnected to form a communication network for data/control information sharing	Program Illustrations	
		Program and Network Properties(System Interconnect Architectures)	T-1	AV-1	L11: Control Flow (control-driven), Data Flow (data driven) and Reduction Machine (demand driven) Models. Network Properties and Routing, Static Interconnection Networks	Understand several ways in which processors/memory/oth er elements of computer can be interconnected to form a communication network for data/control information sharing	Program Illustrations	
	Lecture 12	Principles of Scalable Performance(Parallel Overhead)	R-1	OR-3	L12: Sources of Parallel Overhead, Application Models for Parallel Computers	Identify some reasons why linear speedup/unit efficiency cannot be achieved with parallel processing units.	Numerical Illustrations	Quality of service in Mobile data communication
		Principles of Scalable Performance(Application Models for Parallel Computers)	R-1	OR-3	L12: Sources of Parallel Overhead, Application Models for Parallel Computers	Identify some reasons why linear speedup/unit efficiency cannot be achieved with parallel processing units.	Real life numerical illustration	Quality of service in Mobile data communication
Week 5	Lecture 13	Principles of Scalable Performance(Speedup Performance Laws - Amdahl's, Gustafson's and Sun & Ni's Laws)	T-1 R-2	RW-1	L13: Speedup Performance Laws and tools to measure system performance	Understand the application of Amdahl law, Gustafson Law and Sun-Ni Law to estimate parallel computer performance. Recognize alternative mechanisms to represent system performance estimates	Numerical/Program Illustrations	Disaster management after floodings or earthquakes

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Week 5	Lecture 13	Principles of Scalable Performance(Performance Measurement Tools)	T-1	RW-1	L13: Speedup Performance Laws and tools to measure system performance	Understand the application of Amdahl law, Gustafson Law and Sun-Ni Law to estimate parallel computer performance. Recognize alternative mechanisms to represent system performance estimates	Numerical/Program Illustrations	Disaster management after floodings or earthquakes
	Lecture 14				Test 1			
	Lecture 15	Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Design Space of Processors)	T-1	OR-3 RW-2	L15: Design Space of Processors, Superscalar Processors, VLIW Processors, Vector Processors and Symbolic Processors.	Understand and compare the models of instruction processing in different parallel processors architectures	Time-space graphs with Numerical/Program Illustrations	A person usually responds to a smoke detector alarm before answering the phone
		Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Super scalar and Vector Processors)	T-1	OR-3	L15: Design Space of Processors, Superscalar Processors, VLIW Processors, Vector Processors and Symbolic Processors.	Understand and compare the models of instruction processing in different parallel processors architectures	Time-space graphs with Numerical/Program Illustrations	A person usually responds to a smoke detector alarm before answering the phone
Week 6	Lecture 16	Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Transaction and Interrupt)	T-1	AV-2	L16: Cache Memory Organization - Cache Addressing Models, Cache Mapping Techniques (Direct, Associative, Set associative, Sector Mapping), Transaction and interrupt	Understand alternative implementations of cache memory organization, Transaction and interrupt	Numerical Illustrations	
	Lecture 17	Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Memory hierarchy Technology)	T-1	AV-2	L17: Cache Memory Organization - Cache Addressing Models, Cache Mapping Techniques (Direct, Associative, Set associative, Sector Mapping), Transaction and interrupt	Understand alternative implementations of cache memory organization, Transaction and interrupt	Numerical Illustrations	

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Week 6	Lecture 17	Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Cache Memory Organization)	T-1	AV-2	L17: Cache Memory Organization - Cache Addressing Models, Cache Mapping Techniques (Direct, Associative, Set associative, Sector Mapping), Transaction and interrupt	Understand alternative implementations of cache memory organization, Transaction and interrupt	Numerical Illustrations	
	Lecture 18	Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Back plane Bus Specification)	T-1		L18: Frequent and many updates in the airline reservation database, Back plane bus specification	Backplane Bus Specification, Addressing and Timing Protocols, Timing protocols	Understand the concepts of backplane bus and bus addressing and Timing Protocols	
		Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Addressing and Timing Protocols)	T-1		L18: Frequent and many updates in the airline reservation database, Back plane bus specification	Backplane Bus Specification, Addressing and Timing Protocols, Timing protocols	Understand the concepts of backplane bus and bus addressing and Timing Protocols	
Week 7	Lecture 19	Processors, Memory Hierarchy, Bus, Cache and Shared Memory(Interleaved Memory Organization)	T-1		L19: Interleaved Memory Organization - High order and Low order memory interleaving, Arbitration	To understand alternative memory interleaving techniques	Numerical Illustrations	Frequent and many updates in the airline reservation database
		Processors, Memory Hierarchy, Bus, Cache and Shared Memory (Introduction to DRAM System, DRAM Controllers and Address Mapping)	T-1		L19: Interleaved Memory Organization - High order and Low order memory interleaving, Arbitration	To understand alternative memory interleaving techniques	Numerical Illustrations	Frequent and many updates in the airline reservation database
		SPILL OVER						
Week 7	Lecture 20				Spill Over			
	Lecture 21				Spill Over			
		MID-TERM						
Week 8	Lecture 22	Pipelining and Superscalar Techniques(Linear Pipeline Processors)	T-1		L22: Linear Pipeline Processors - Asynchronous and Synchronous Models, Clocking and Timing Control, Speedup, Reservation latency	Understand the basic design and parameters of linear pipeline models	Numerical/Program Illustrations	

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Week 8	Lecture 23	Pipelining and Superscalar Techniques(reservation and Latency Analysis)	T-1		L23: Linear Pipeline Processors - Asynchronous and Synchronous Models, Clocking and Timing Control, Speedup, Reservation latency	Understand the basic design and parameters of linear pipeline models	Numerical/Program Illustrations	
	Lecture 24	Pipelining and Superscalar Techniques(Instruction Pipeline Design)	T-1	RW-3	L24: Instruction Pipeline Design - Instruction Execution Phases, Mechanisms for Instruction Pipelining	Understand the design issues of Instruction Pipeline like prefetch buffers, multiple functional units, pipeline bottleneck, hazard detection and resolution, etc.	Numerical/Program based Illustrations	
Week 9	Lecture 25	Pipelining and Superscalar Techniques(Arithmetic Pipeline Design)	T-1	RW-3	L25: Arithmetic Pipeline Design - Wallace Tree and and Multi-function pipeline design examples	Understand the design of arithmetic pipeline with the help of Wallace Tree structure (using Carry-save adders and Carry propagation adders)	Numerical/Program based Illustrations	
	Lecture 26	Pipelining and Superscalar Techniques(Super scalar Pipeline Design.)	T-1		L26: Super-scalar Pipeline Design - Design Parameters, Pipeline Structure, Dependencies, Superscalar pipeline scheduling and Performance	To understand several aspects of superscalar pipeline design, and instruction scheduling mechanisms	Numerical examples	
	Lecture 27				Test 2			
Week 10	Lecture 28	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers (Multiprocessor System Interconnects)	T-1		L28: Multiprocessor System Interconnects - Hierarchical Bus Systems, Crossbar switch and Multi-port memory	To study alternative implementations of network design for multiprocessor systems	Numerical example	Optimized tablet support with a new interface is the latest update in the original version of Android

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Week 10	Lecture 29	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(Three Generations of Multi-computers-Past, Present and Future)	T-1		L29: Three Generations of Multi-computers; Message Routing Schemes - Message formats, Store-forward and Wormhole Rouing	Understand the evolution of multicomputer systems (past to present and future) and the message routing schemes in multiprocessor systems	Example computers from the evolution	
		Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(Message Routing schemes)	T-1		L29: Three Generations of Multi-computers; Message Routing Schemes - Message formats, Store-forward and Wormhole Rouing	Understand the evolution of multicomputer systems (past to present and future) and the message routing schemes in multiprocessor systems	Program Illustrations	Fast Fourier Transform, which is used in audio electronics and applications
	Lecture 30	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(The Cache Coherence Problem)	T-1	OR-3	L30: The Cache Coherence Problem	Identify and analyse several possible reasons behind cache inconsistency esp. in multiprocessor environment.	Numerical Illustrations	
Week 11	Lecture 31	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(Snoopy Bus Protocols)	T-1		L31: Snoopy Cache Coherence Protocols	Understand the snoopy cache coherence protocols for writeback cache and writethrough cache	Numerical Illustrations	
	Lecture 32	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(Vector Processing Principles)	T-1	OR-3	L32: Vector Processing Principle and Vector Instructions	Learn several types of Vector instructions and Vector-Access Memory Schemes	Numerical Illustrations	
	Lecture 33	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers (Compound Vector Operations)	T-1		L33: Compound Vector Operations, Vector Loops and Chaining	Understand the applications of compound vector operations and looping/chaining with vectors	Program Illustrations	
		Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(Vector Loops and Chaining)	T-1		L33: Compound Vector Operations, Vector Loops and Chaining	Understand the applications of compound vector operations and looping/chaining with vectors	Program Illustrations	

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Week 12	Lecture 34	Multiprocessors, Multi-computers, Multi-vector and SIMD Computers(SIMD Computer Organization Implementation Models)	T-1		L34: SIMD Computer Models	Understand the alternative implementations of SIMD computer models	Case study overview: Illiac IV and BSP	
	Lecture 35	Data Flow Architecture (Evolution of Data Flow Architecture)	T-1		L35: Data Flow Computers	Understand data flow architecture and its evolution and learn to draw the data flow graphs	Program based Illustrations	
	Lecture 36				Term paper			
Week 13	Lecture 37	Data Flow Architecture (Control Flow vs Data Flow Architecture)	T-1	RW-4	L37: Comparison of Data flow and Control flow architecture	Compare the instruction processing in data flow computer and control flow computer	Numerical Illustrations	
	Lecture 38	Parallel Models, Languages and Compilers(Parallel Programming Models)	T-1		L38: Shared variable model, Message passing model; L39: Data Parallel Model	Understand the alternative parallel programming models	Numerical Illustrations	
	Lecture 39	Parallel Models, Languages and Compilers(Parallel Programming Models)	T-1		L38: Shared variable model, Message passing model; L39: Data Parallel Model	Understand the alternative parallel programming models	Numerical Illustrations	
Week 14	Lecture 40	Parallel Models, Languages and Compilers(Parallel Languages and Compilers)	T-1		L40: Parallel Language Constructs an Optimizing Compilers for Parallelism	Understand the features of parallel languages and parallelizing compilers	Case Study: PFC and Parascope	
		SPILL OVER						
Week 14	Lecture 41				Spill Over			
	Lecture 42				Spill Over			
Week 15	Lecture 43				Spill Over			
	Lecture 44				Spill Over			
	Lecture 45				Spill Over			

Scheme for CA:

CA Category of this Course Code is:A0203 (2 best out of 3)

Component	Weightage (%)	Mapped CO(s)
Test 1	50	

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Test 2	50	
Term paper	50	

Details of Academic Task(s)

Academic Task	Objective	Detail of Academic Task	Nature of Academic Task (group/individuals)	Academic Task Mode	Marks	Allottment / submission Week
Test 1	Online MCQ based test	Online MCQ based test	Individual	Online	30	4 / 5
Test 2	Online MCQ based test	Online MCQ based test	Individual	Online	30	7 / 9
Term paper	To make students understand about research publications	students will write a term paper on the allocated topics. Rubrics a) 5 marks for overall contribution of the research work b) 5 marks for the overall structure of the paper c) 5 marks for plagiarism report analysis d) 5 marks for novelty of the paper e) 10 marks for recent literature/relevant study	Individual	Offline	30	2 / 11

List of suggested topics for term paper[at least 15] (Student to spend about 15 hrs on any one specified term paper)

Sr. No.	Topic
1	Graphics Processing Unit
2	New age microprocessor
3	Super computers (MIMD)
4	Memory system design
5	Hardware reliability.
6	Cache memory advancements
7	Memory Hierarchy analysis
8	Parallel Processing
9	Distributed Processors
10	GPU Acceleration

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11	Energy Efficiency microprocessor
12	sustainability in computer architecture
13	New trends in computer organization
14	Tensor Processing Units (TPUs)
15	Case studies on Intel, Risel