

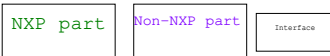
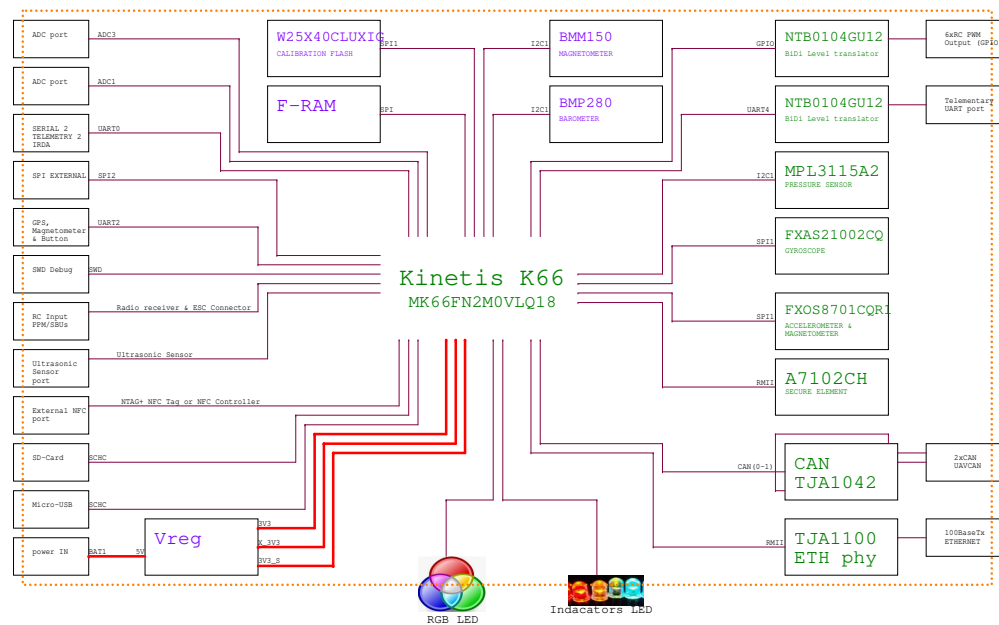
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2	BLOCK DIAGRAM
3	MCU
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8	CAN & ETHERNET

Revisions			
Rev	Description	Date	Approved
X1	First Release	14FEB18	JAIN GALLOWAY
X2	Project Rename & A7102CH IC	SEP18	JAIN GALLOWAY
B	Reference Designator are sync with NXP_NXPPhlite 3.0RC18	23OCT18	JAIN GALLOWAY
BX1		11NOV18	JAIN GALLOWAY
BX2			JAIN GALLOWAY
BX3			JAIN GALLOWAY
BX4			JAIN GALLOWAY
BX5	-Added J28 for external sensors -Added FX4FMU baro sensor	14NOV18	JAIN GALLOWAY
BX6		23NOV18	JAIN GALLOWAY
BX7		24NOV18	JAIN GALLOWAY
BX8	-Added ESD diodes	28NOV18	JAIN GALLOWAY
BX9	- Added MS621FE-FL11E Batery - BMM150 SPI to I2C mode	28NOV18	JAIN GALLOWAY
BX10	- Removed duplicate pullup / down resistors from I2C1_SDA_INTERNAL & I2C1_SCL_INTERNAL - On-Board sensors moved to 'SENSORS' page	03DEC18	JAIN GALLOWAY

# RDDRONE-FMUK66

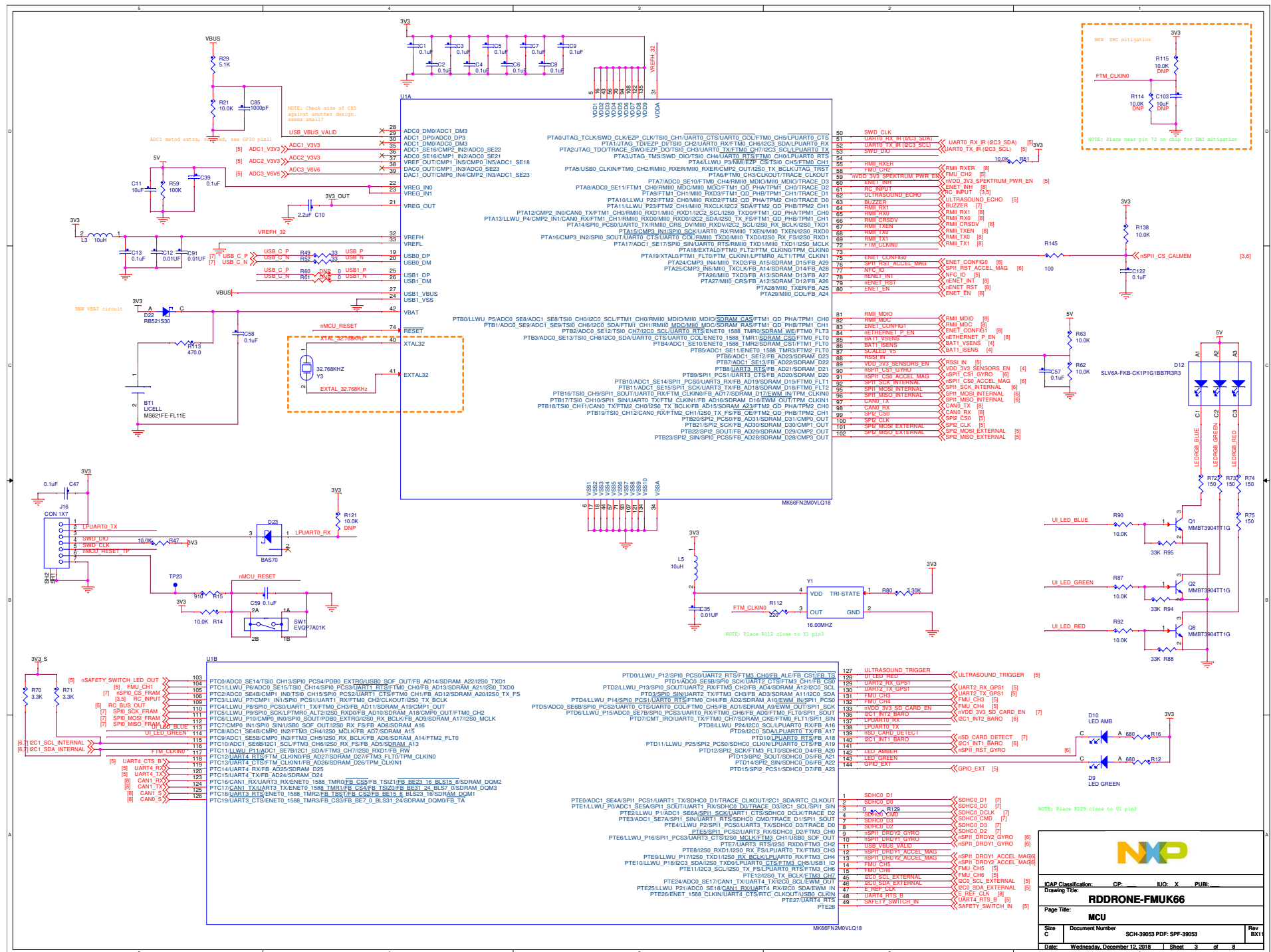
REF DES	ASSY OPT	PAGE NAME
R61,R60,R114,R115,C103,R121	DNP	3. MCU
R77	DNP	4. POWER
R45,R128	DNP	5. CONNECTORS
R65,R132,R134,R64,R133,R131	DNP	6. SENSORS
R111,C108,R120	DNP	7. SDCARD & MEMORY

## RDDRONE-FMUK66 MODULAR AND FLEXIBLE DRONE DEVELOPMENT PLATFORM



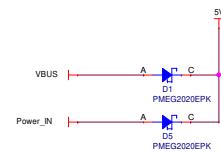
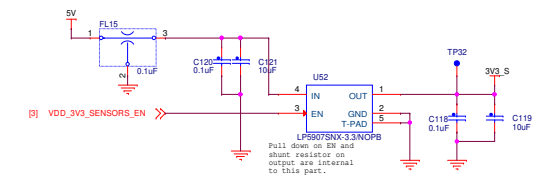
— Power — Signal

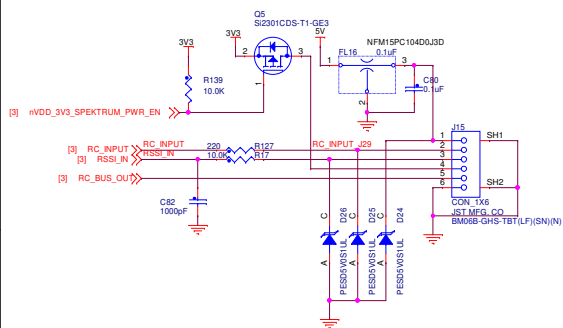
<b>RDDRONE-FMUK66</b>			
<b>BLOCK DIAGRAM</b>			
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NOTE: Extra Low Noise



PPM-RSSI-SBUS-SPEKTRUM  
SERIAL4/FrSky[illegible]

SERIAL 1 / TELEMETRY 1

[illegible][illegible][illegible]

UARTs, Capable of FDCAN IR Comm. IR TX/RX.  
 Separate function I2C3

NFM15P1C104D3D3

5V

0.1μF

1 2 3 4

FL24

C45

0.1μF

3V3

R140 10.0K DNP

R145 10.0K DNP

J7

1 2 3 4

SH1

SH2

CON\_1X4

EST-MFG-CD

BM04B-GHS-TBT(LF)(SN)(N)

D64

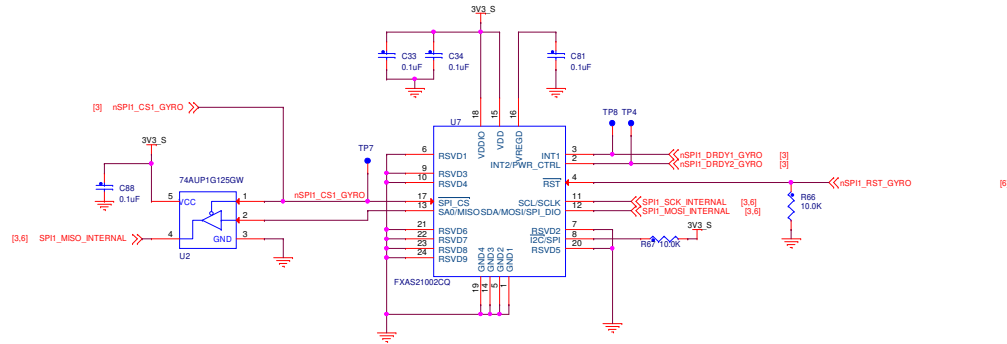
PES25VDS U/L

UART0\_TX/R (EC2\_CD)   
 UART0\_RX/R (EC2\_SD)

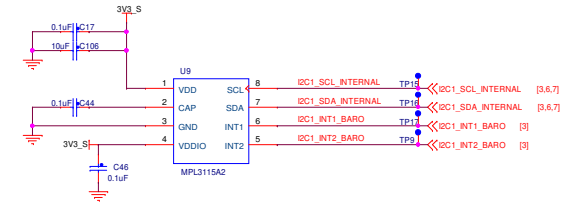


ICAP Classification:		CP:	IJO: X	PUBI:
Drawing Title:				
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Page Title:				
<b>CONNECTORS</b>				
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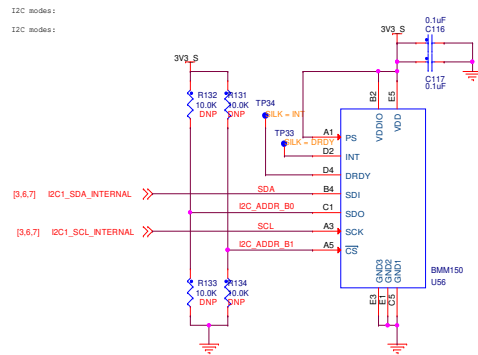
## GYROSCOPE



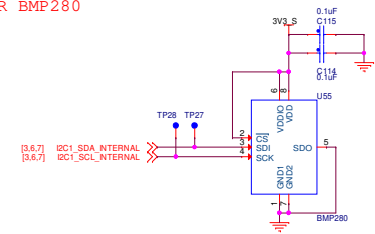
## PRESSURE SENSOR



## MAGNETOMETER BMM150

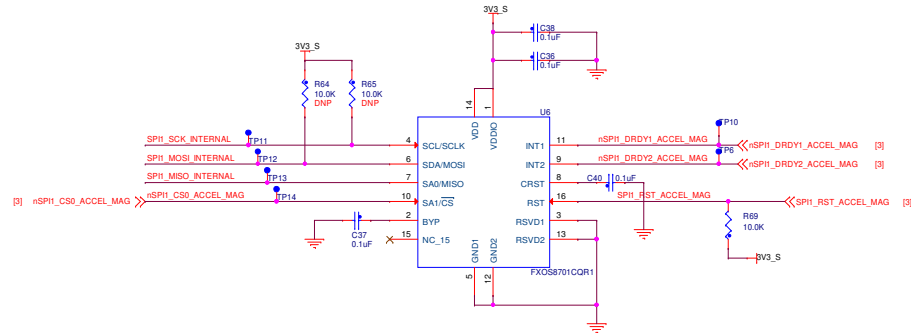


## BAROMETER BMP280

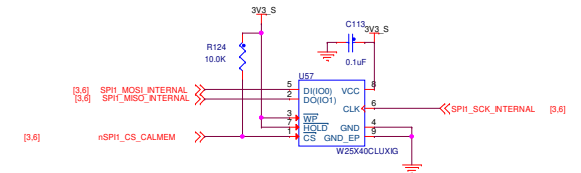


## ACCELEROMETER & MAGNETOMETER

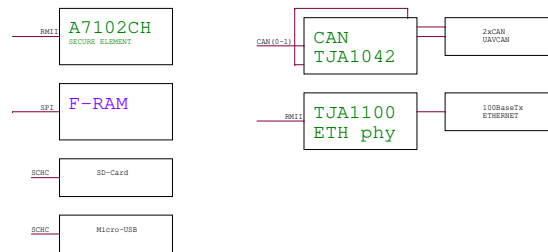
NOTE: keep sensors



## SENSOR MODULE CALIBRATION FLASH

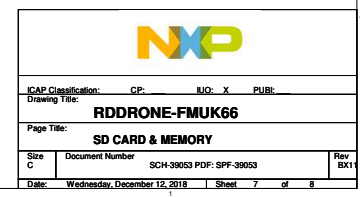



ICAP Classification:		CP:	IJO: X	PUBI:
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### FRAM

The diagram shows the FRAM (Ferroelectric Random Access Memory) component, specifically the FM25V02A-GTR, connected to a 3V3 supply and ground. The SPI interface is shown with signals: SPI0\_MOSI\_FRAM (TP1) connected to MOSI (pin 5), SPI0\_SCK\_FRAM (TP3) connected to SCK (pin 6), and nSPI0\_CS\_FRAM (TP2) connected to CS (pin 1). The device also has pins for VDD (pin 2), VSS (pin 4), WP# (pin 3), and HOLD (pin 7). A 0.1uF capacitor (C72) is connected between VSS and ground.

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ICAP Classification: CP: ECU: X PWB:				
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