

8MMINILPD4-CPU

(i.MX8M Mini Reference Board)

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- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
 - _B Denotes - Active-Low Signal
 - <> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Revision History

Rev. Code	Date	By	Description
A	2018-03-12	Frank	Initial version
A1	2018-03-27	Frank	1. Update U1 I.MX8M Mini symbol naming.
B	2018-05-01	Frank	1. Change PMIC U8 to BD71847; 2. Add external PU resistor R133 for SD2_nRST, as internal is PD and ROM won't pull it to high; 3. DNP R63,R64,C389,C390, as internal VREF works well;
B1	2018-06-19	Frank	1. Remove the IOMUX table;
C	2018-09-12	Frank	1. Remove optional 32K Crystal Circuit for i.MX8M Mini; 2. Remove external DDR VREF Circuit as Internal works well; 3. Add R134, R135 for BOOT_MODE3 option to TESTMODE for compatible design with i.MX8M Nano; 4. Change J4_Pin56 from GND to TESTMODE(BOOT_MODE3) for compatible design with i.MX8M Nano; 5. Remove R50, R62, R107, R128 to simplify the optional design; 6. Remove C7 for NVCC_3V3; 7. Update the symbol of i.MX8M Mini: <ul style="list-style-type: none">> Correct naming for AB13 from PVCC0_1V8 to PVCC0_1P8;> Correct power domain for B27, C26 from NVCC_CLK to VDD_24M_XTAL_1P8;> Correct power domain for J23, J24 from VDDA_1P8 to VDD_ANA1_1P8;> Correct power domain for A22, B22, F22, A23, B23, F23 to VDD_USB_3P3;> Correct power domain for D22, E19, D23, E22 to VDD_USB_1P8, and also adjust the pin locations. 8. Update the description of the Block Diagram and Power Tree; 9. Update some descriptions of the schematic; 10. Add R136, C405 on VDD_MIP1_1V2 for compatible design with i.MX8M Nano;
C1	2018-11-29	Frank	1. Remove the note for R136;
C2	2019-1-31	Frank	1. Update the Min/Typ/Max operating range for I.MX8M Mini power supplies; 2. Add note for changing BD71847 BUCK1/2/5 output voltage according to the new operation range; 3. Add note for all IOs that internal pull up/down is not supported in 3.3V mode;



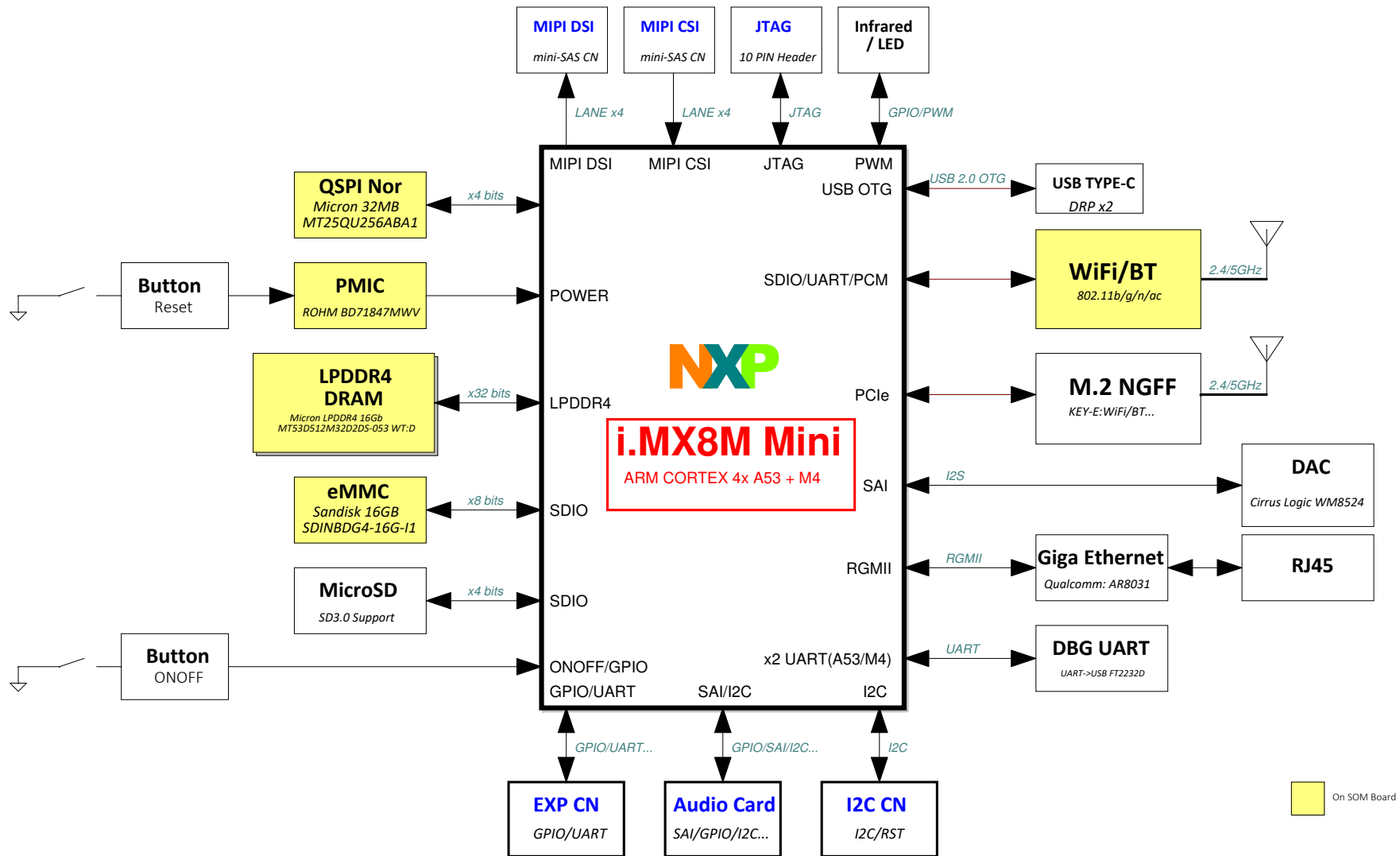
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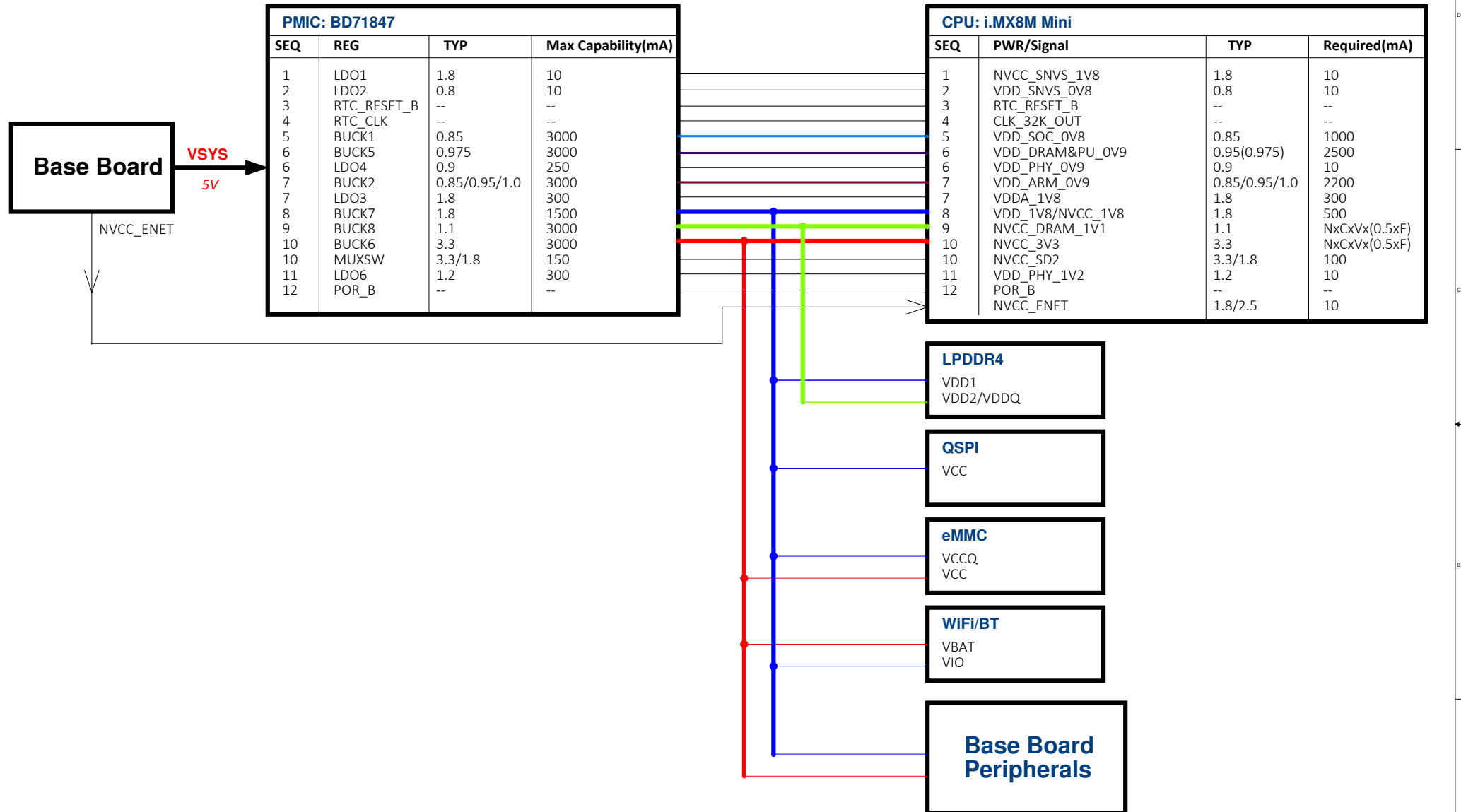
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Drawn by: Frank Liu	Page Title: Title and Rev History		
Approved: <Approver>	Size C	Document Number SCH-31399 PDF: SPF-31399	Rev C2
Date: Friday, March 22, 2019		Sheet 1 of 13	

8MMINILPD4-EVK Block Diagram

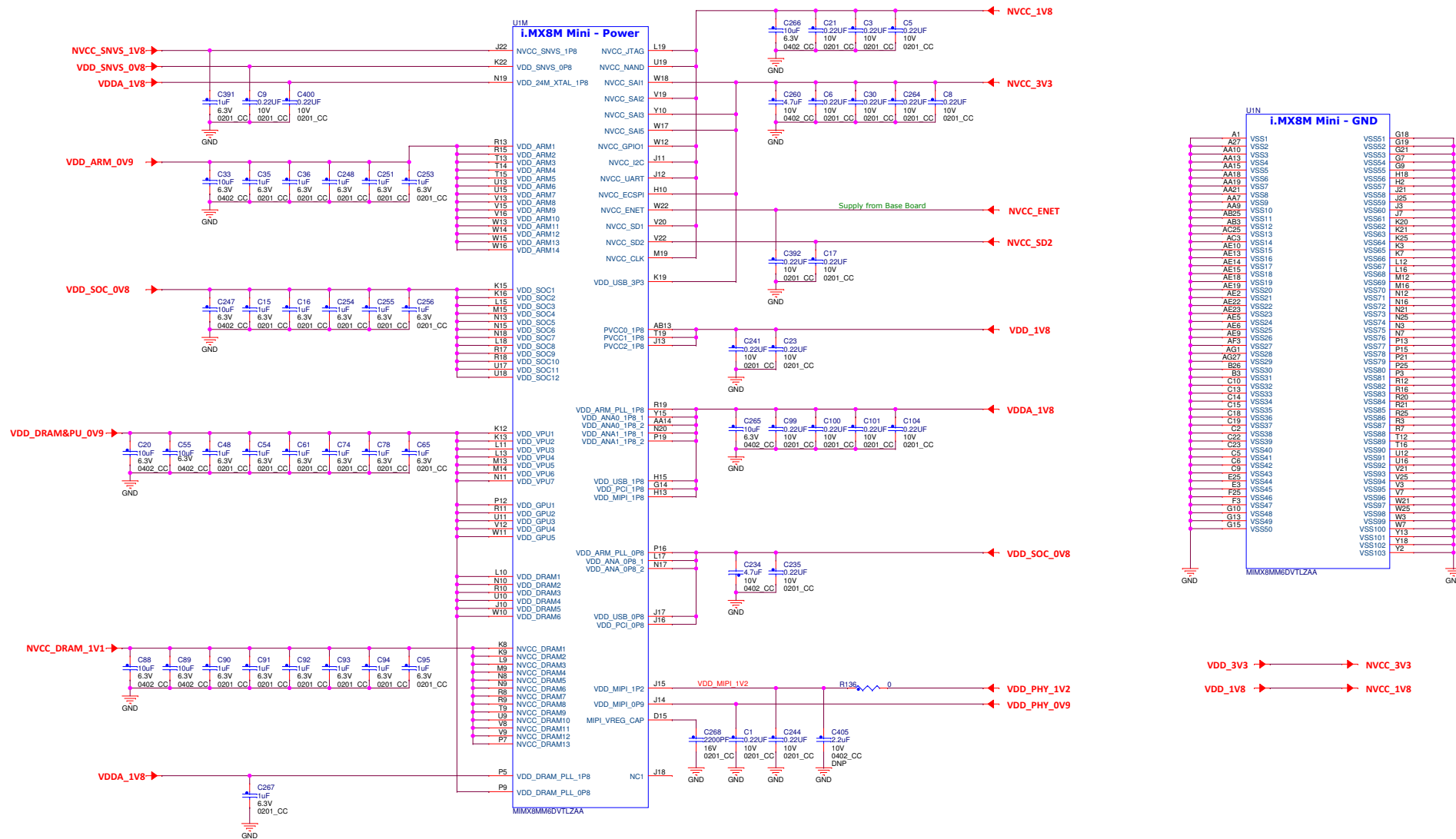


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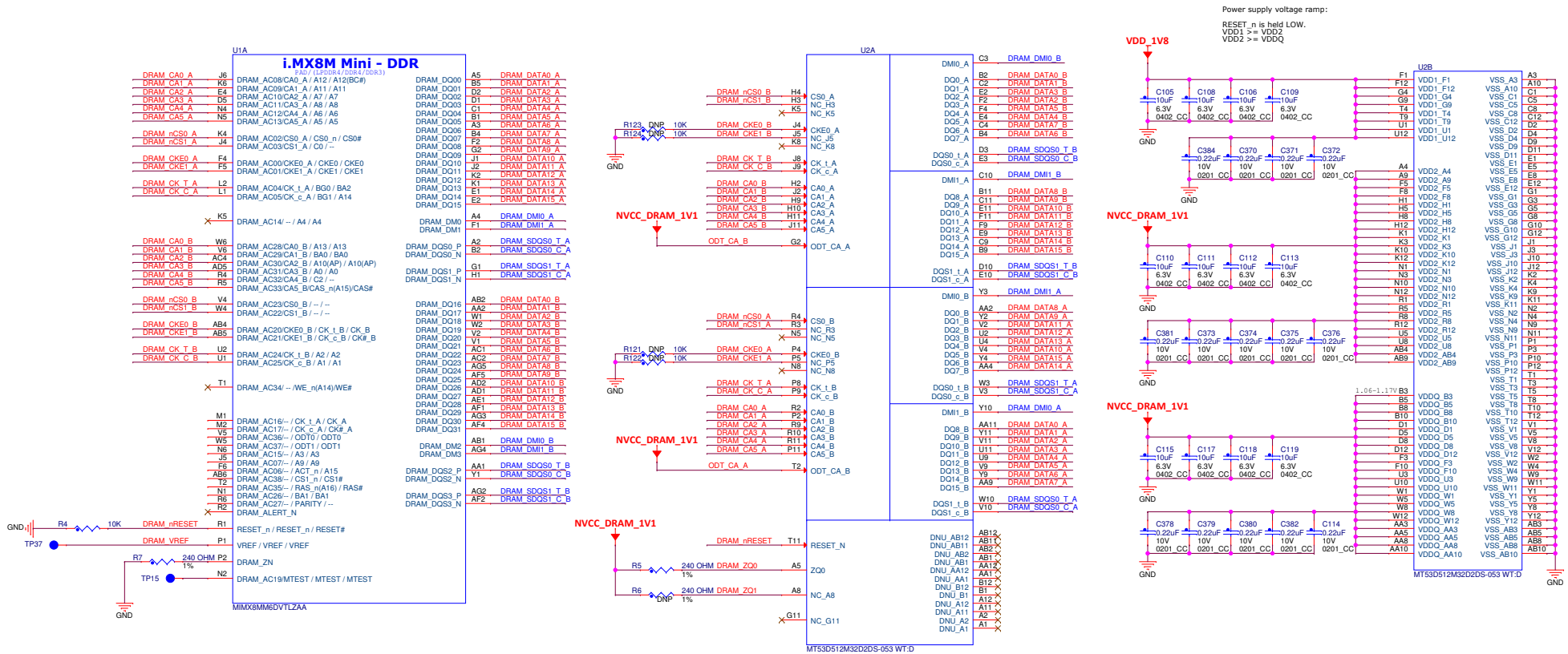
8MMINILPD4-EVK PWR TREE



i.MX8M Mini PWR



LPDDR4 2GB




Data Bus

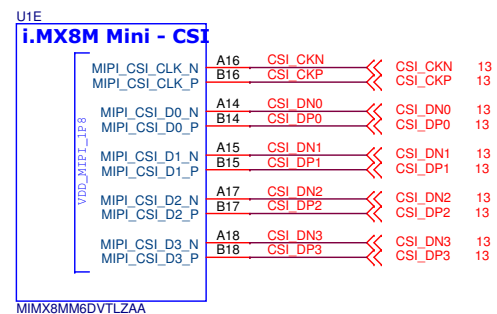
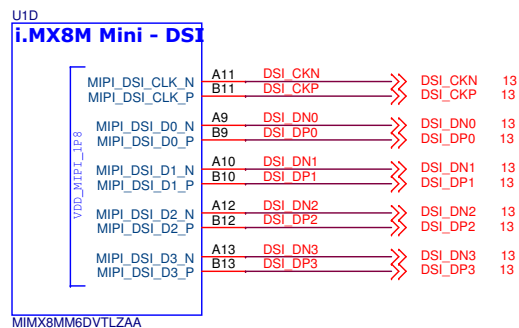
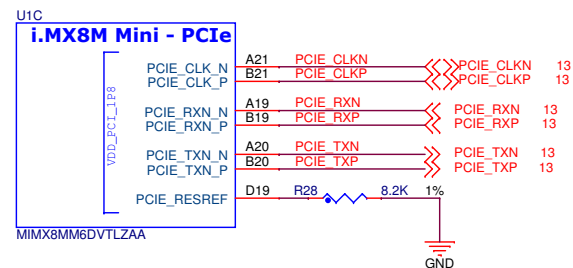
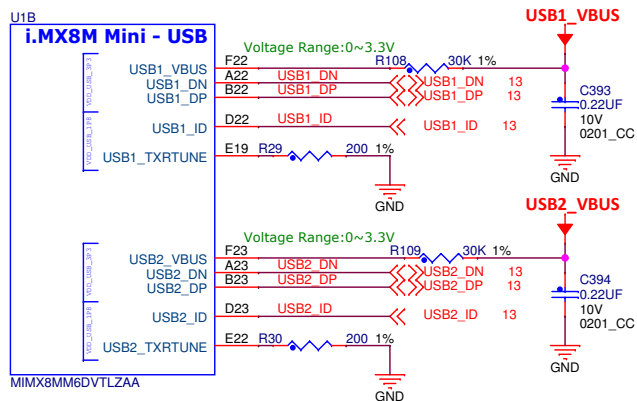
Pin Name	LPDDR4	DDR4
DRAM_DQ05_P	DQ05_0	DQS1_LA
DRAM_DQ05_N	DQ05_1A	DQS1_LB
DRAM_DM0	DM0_0	DM1_nA / DBI_nA
DRAM_DQ06	DQ06_0	DQS2_LA
DRAM_DQ01	DQ1_1A	DQ1_1A
DRAM_DQ02	DQ2_0	DQ2_0
DRAM_DQ03	DQ3_0	DQ3_1A
DRAM_DQ04	DQ4_0	DQ4_0
DRAM_DQ05	DQ5_0	DQ5_0
DRAM_DQ06	DQ6_0	DQ6_1A
DRAM_DQ07	DQ7_0	DQ7_0
DRAM_CS1_P	DQS1_1A	DQS1_1A
DRAM_CS1_N	DQS1_1B	DQS1_1B
DRAM_DM1	DM1_0	DM1_nA / DBIU_nA
DRAM_DQ08	DQ08_0	DQ0_0
DRAM_DQ09	DQ9_0	DQ1_0
DRAM_DQ10	DQ10_0	DQ2_0
DRAM_DQ11	DQ11_0	DQ3_0
DRAM_DQ12	DQ12_0	DQ4_0
DRAM_DQ13	DQ13_0	DQ5_0
DRAM_DQ14	DQ14_0	DQ6_0
DRAM_DQ15	DQ15_0	DQ7_0
DRAM_DQ52_P	DQ50_0	DQS1_LB
DRAM_DQ52_N	DQ50_1	DQS1_LB
DRAM_DM2	DM10_0	DM1_nB / DBIU_nB
DRAM_DQ16	DQ16_0	DQ8_0
DRAM_DQ17	DQ17_0	DQ1_1B
DRAM_DQ18	DQ18_0	DQ2_1B
DRAM_DQ19	DQ19_0	DQ3_1B
DRAM_DQ20	DQ20_0	DQ4_1B
DRAM_DQ21	DQ21_0	DQ5_1B
DRAM_DQ22	DQ22_0	DQ6_1B
DRAM_DQ23	DQ23_0	DQ7_1B
DRAM_DQ23_P	DQS1_1B	DQS1_1B
DRAM_DQ23_N	DQS1_1B	DQS1_1B
DRAM_DM3	DM10_1	DM1_nB / DBIU_nB
DRAM_DQ24	DQ24_0	DQ10_0
DRAM_DQ25	DQ25_0	DQ11_0
DRAM_DQ26	DQ26_0	DQ12_0
DRAM_DQ27	DQ27_0	DQ13_0
DRAM_DQ28	DQ28_0	DQ14_0
DRAM_DQ29	DQ29_0	DQ15_0
DRAM_DQ30	DQ30_0	DQ16_0
DRAM_DQ31	DQ31_0	DQ17_0


Command/Address

Pin Name	LPDDR4	DDR4
DRAWN RESET N	RESET_N	RESET_N
DRAWN ALARM A0	MTEST1	ALERT_N / MTEST1
DRAWN ALARM A0	CKEO A	CKEO
DRAWN ALARM A0	CKET A	CKET
DRAWN ALARM A0	CS0 A	CS0
DRAWN ALARM A0	CS1 A	CS1
DRAWN ALARM A0	CKA A	BGO
DRAWN ALARM A0	CKA A	BG1
DRAWN ALARM A0	CKA A	BG2
DRAWN ALARM A0	CKA A	A12
DRAWN ALARM A0	CA1 A	A11
DRAWN ALARM A0	CA0 A	A7
DRAWN ALARM A0	CA1 A	A8
DRAWN ALARM A0	CA1 A	A5
DRAWN ALARM A0	CA1 A	A6
DRAWN ALARM A0	CA1 A	A4
DRAWN ALARM A0	CA1 A	CK A
DRAWN ALARM A0	CA1 A	CK A
DRAWN ALARM A0	MTEST	MTEST
DRAWN ALARM A0	CKEO B	CKEO
DRAWN ALARM A0	CKET B	CKET
DRAWN ALARM A0	CS1 B	CS1
DRAWN ALARM A0	CS0 B	CS0
DRAWN ALARM A0	CKA B	A1
DRAWN ALARM A0	CKA B	A2
DRAWN ALARM A0	CKA B	B1
DRAWN ALARM A0	CKA B	B1
DRAWN ALARM A0	CKA B	CA0 B
DRAWN ALARM A0	CKA B	CA1 B
DRAWN ALARM A0	CKA B	CA2 B
DRAWN ALARM A0	CKA B	CA3 B
DRAWN ALARM A0	CKA B	CA4 B
DRAWN ALARM A0	CKA B	CA5 B
DRAWN ALARM A0	CKA B	CA6 B
DRAWN ALARM A0	CKA B	CA7 B
DRAWN ALARM A0	CKA B	CA8 B
DRAWN ALARM A0	CKA B	CA9 B
DRAWN ALARM A0	CKA B	CA10 B
DRAWN ALARM A0	CKA B	CA11 B
DRAWN ALARM A0	CKA B	CA12 B
DRAWN ALARM A0	CKA B	CA13 B
DRAWN ALARM A0	CKA B	CA14 B
DRAWN ALARM A0	CKA B	CA15 B
DRAWN ALARM A0	CKA B	CA16 B
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DRAWN ALARM A0	CKA B	CA18 B
DRAWN ALARM A0	CKA B	CA19 B
DRAWN ALARM A0	CKA B	CA20 B
DRAWN ALARM A0	CKA B	CA21 B
DRAWN ALARM A0	CKA B	CA22 B
DRAWN ALARM A0	CKA B	CA23 B
DRAWN ALARM A0	CKA B	CA24 B
DRAWN ALARM A0	CKA B	CA25 B
DRAWN ALARM A0	CKA B	CA26 B
DRAWN ALARM A0	CKA B	CA27 B
DRAWN ALARM A0	CKA B	CA28 B
DRAWN ALARM A0	CKA B	CA29 B
DRAWN ALARM A0	CKA B	CA30 B
DRAWN ALARM A0	CKA B	CA31 B
DRAWN ALARM A0	CKA B	CA32 B
DRAWN ALARM A0	CKA B	CA33 B
DRAWN ALARM A0	CKA B	CA34 B
DRAWN ALARM A0	CKA B	CA35 B
DRAWN ALARM A0	CKA B	CA36 B
DRAWN ALARM A0	CKA B	CA37 B
DRAWN ALARM A0	CKA B	CA38 B
DRAWN ALARM A0	CKA B	CA39 B
DRAWN ALARM A0	CKA B	CA40 B
DRAWN ALARM A0	CKA B	CA41 B
DRAWN ALARM A0	CKA B	CA42 B
DRAWN ALARM A0	CKA B	CA43 B
DRAWN ALARM A0	CKA B	CA44 B
DRAWN ALARM A0	CKA B	CA45 B
DRAWN ALARM A0	CKA B	CA46 B
DRAWN ALARM A0	CKA B	CA47 B
DRAWN ALARM A0	CKA B	CA48 B
DRAWN ALARM A0	CKA B	CA49 B
DRAWN ALARM A0	CKA B	CA50 B
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DRAWN ALARM A0	CKA B	CA52 B
DRAWN ALARM A0	CKA B	CA53 B
DRAWN ALARM A0	CKA B	CA54 B
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DRAWN ALARM A0	CKA B	CA92 B
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DRAWN ALARM A0	CKA B	CA126 B
DRAWN ALARM A0	CKA B	CA127 B
DRAWN ALARM A0	CKA B	CA128 B
DRAWN ALARM A0	CKA B	CA129 B
DRAWN ALARM A0	CKA B	CA130 B
DRAWN ALARM A0	CKA B	CA131 B
DRAWN ALARM A0	CKA B	CA132 B
DRAWN ALARM A0	CKA B	CA133 B
DRAWN ALARM A0	CKA B	CA134 B
DRAWN ALARM A0	CKA B	CA135 B
DRAWN ALARM A0	CKA B	CA136 B
DRAWN ALARM A0	CKA B	CA137 B
DRAWN ALARM A0	CKA B	CA138 B
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DRAWN ALARM A0	CKA B	CA227 B
DRAWN ALARM A0	CKA B	CA228 B
DRAWN ALARM A0	CKA B	CA229 B
DRAWN ALARM A0	CKA B	CA230 B
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DRAWN ALARM A0	CKA B	CA232 B
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DRAWN ALARM A0	CKA B	CA239 B
DRAWN ALARM A0	CKA B	CA240 B
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DRAWN ALARM A0	CKA B	CA246 B
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DRAWN ALARM A0	CKA B	CA251 B
DRAWN ALARM A0	CKA B	CA252 B
DRAWN ALARM A0	CKA B	CA253 B
DRAWN ALARM A0	CKA B	CA254 B
DRAWN ALARM A0	CKA B	CA255 B
DRAWN ALARM A0	CKA B	CA256 B
DRAWN ALARM A0	CKA B	CA257 B
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DRAWN ALARM A0	CKA B	CA280 B
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DRAWN ALARM A0	CKA B	CA286 B
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DRAWN ALARM A0	CKA B	CA288 B
DRAWN ALARM A0	CKA B	CA289 B
DRAWN ALARM A0	CKA B	CA290 B
DRAWN ALARM A0	CKA B	CA291 B
DRAWN ALARM A0	CKA B	CA292 B
DRAWN ALARM A0	CKA B	CA293 B
DRAWN ALARM A0	CKA B	CA294 B
DRAWN ALARM A0	CKA B	CA295 B
DRAWN ALARM A0	CKA B	CA296 B
DRAWN ALARM A0	CKA B	CA297 B
DRAWN ALARM A0	CKA B	CA298 B
DRAWN ALARM A0	CKA B	CA299 B
DRAWN ALARM A0	CKA B	CA300 B
DRAWN ALARM A0	CKA B	CA301 B
DRAWN ALARM A0	CKA B	CA302 B
DRAWN ALARM A0	CKA B	CA303 B
DRAWN ALARM A0	CKA B	CA304 B
DRAWN ALARM A0	CKA B	CA305 B
DRAWN ALARM A0	CKA B	CA306 B
DRAWN ALARM A0	CKA B	CA307 B
DRAWN ALARM A0	CKA B	CA308 B
DRAWN ALARM A0	CKA B	CA309 B
DRAWN ALARM A0	CKA B	CA310 B
DRAWN ALARM A0	CKA B	CA311 B
DRAWN ALARM A0	CKA B	CA312 B
DRAWN ALARM A0	CKA B	CA313 B
DRAWN ALARM A0	CKA B	CA314 B
DRAWN ALARM A0	CKA B	CA315 B
DRAWN ALARM A0	CKA B	CA316 B
DRAWN ALARM A0	CKA B	CA317 B
DRAWN ALARM A0	CKA B	CA318 B
DRAWN ALARM A0	CKA B	CA319 B
DRAWN ALARM A0	CKA B	CA320 B
DRAWN ALARM A0	CKA B	CA321 B
DRAWN ALARM A0	CKA B	CA322 B
DRAWN ALARM A0	CKA B	CA323 B
DRAWN ALARM A0	CKA B	CA324 B
DRAWN ALARM A0	CKA B	CA325 B
DRAWN ALARM A0	CKA B	CA326 B
DRAWN ALARM A0	CKA B	CA327 B
DRAWN ALARM A0	CKA B	CA328 B
DRAWN ALARM A0	CKA B	CA329 B
DRAWN ALARM A0	CKA B	CA330 B
DRAWN ALARM A0	CKA B	CA331 B
DRAWN ALARM A0	CKA B	CA332 B
DRAWN ALARM A0	CKA B	CA333 B
DRAWN ALARM A0	CKA B	CA334 B
DRAWN ALARM A0	CKA B	CA335 B
DRAWN ALARM A0	CKA B	CA336 B
DRAWN ALARM A0	CKA B	CA337 B
DRAWN ALARM A0	CKA B	CA338 B
DRAWN ALARM A0	CKA B	CA339 B
DRAWN ALARM A0	CKA B	CA340 B
DRAWN ALARM A0	CKA B	CA341 B
DRAWN ALARM A0	CKA B	CA342 B
DRAWN ALARM A0	CKA B	CA343 B
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DRAWN ALARM A0	CKA B	CA345 B
DRAWN ALARM A0	CKA B	CA346 B
DRAWN ALARM A0	CKA B	CA347 B
DRAWN ALARM A0	CKA B	CA348 B
DRAWN ALARM A0	CKA B	CA349 B
DRAWN ALARM A0	CKA B	CA350 B
DRAWN ALARM A0	CKA B	CA351 B
DRAWN ALARM A0	CKA B	CA352 B
DRAWN ALARM A0	CKA B	

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Designer: Frank Liu	Drawing Title:	8MMINILPD4-CPU	
	Page Title:	LPDDR4	
Drawn by: Frank Liu	Size	C	
Approved: ckipraver	Document Number	SCH-31399 PDF: SPF-31399	
Date:	Model:	Version:	Sheet # of 18

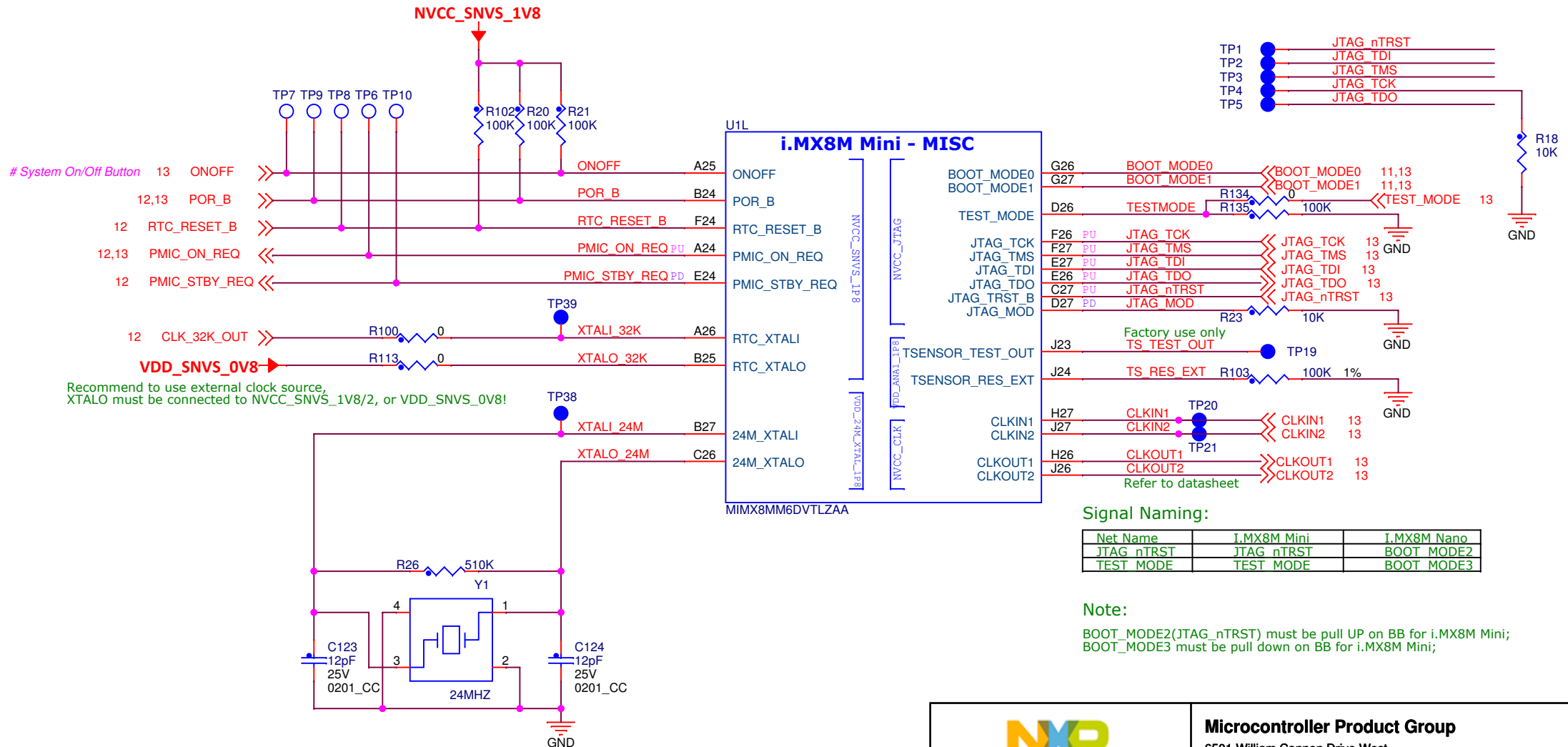
i.MX8M Mini PHYs



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Drawn by: Frank Liu		Page Title: CPU PHY	
Approved: <Approver>		Size B	Document Number SCH-31399 PDF: SPF-31399
Date: Monday, January 07, 2019		Sheet 7	of 13
		Rev C2	

i.MX8M Mini MISC

JTAG Debug



Signal Naming:

Net Name	i.MX8M Mini	i.MX8M Nano
JTAG nTRST	JTAG nTRST	BOOT_MODE2
TEST MODE	TEST MODE	BOOT_MODE3

Note:

BOOT_MODE2(JTAG_nTRST) must be pull UP on BB for i.MX8M Mini;
BOOT_MODE3 must be pull down on BB for i.MX8M Mini;



Microcontroller Product Group

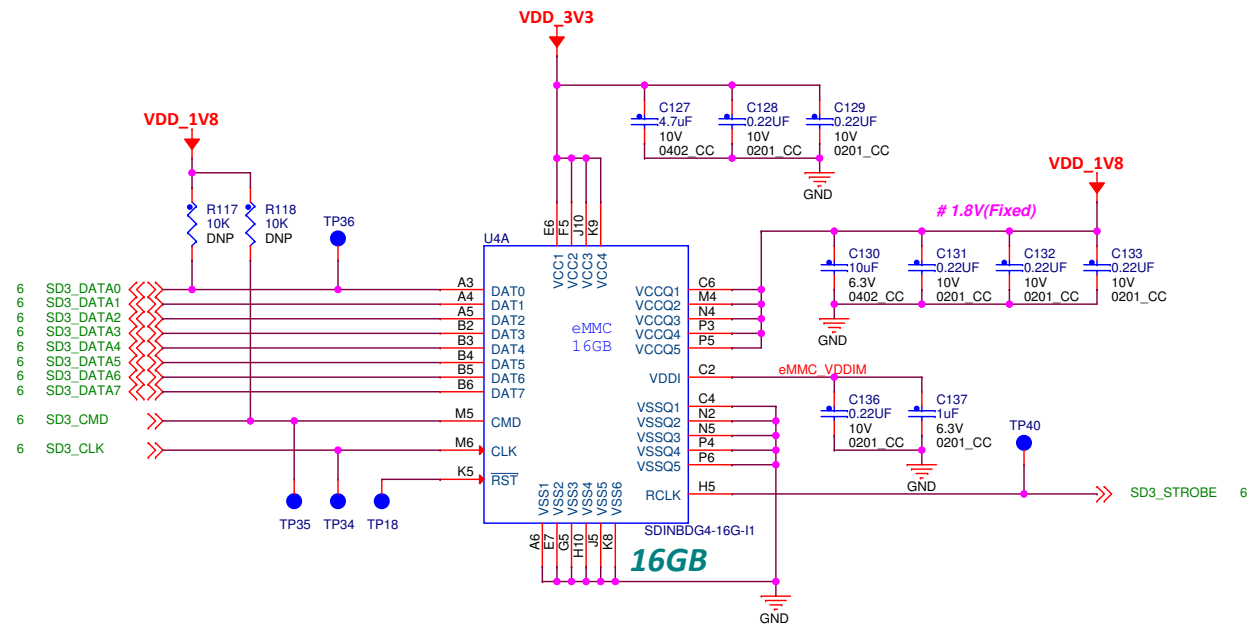
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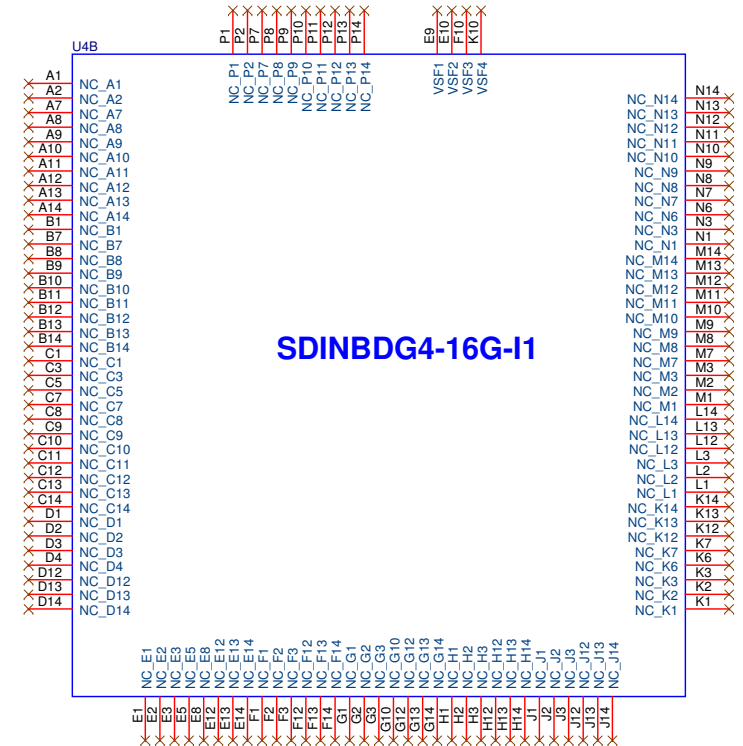
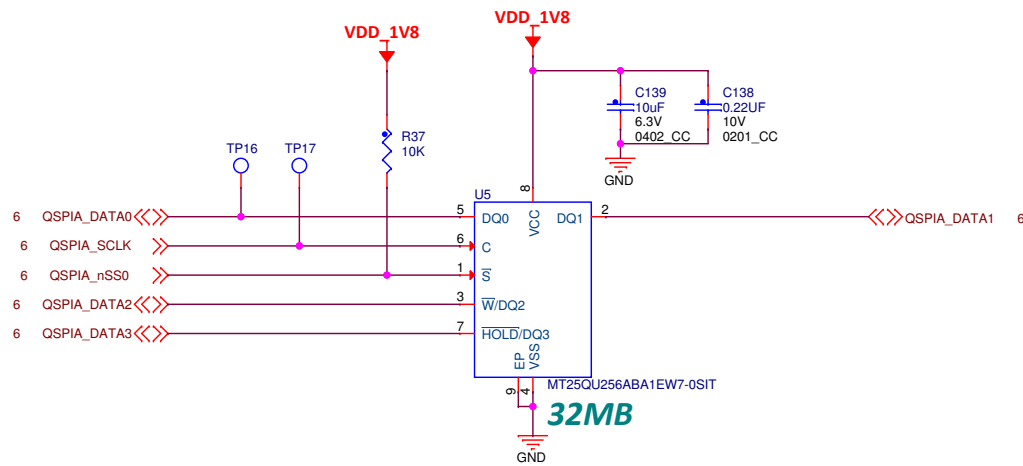
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Designer: Frank Liu	Drawing Title: 8MMINILPD4-CPU		
Drawn by: Frank Liu	Page Title: CPU MISC		
Approved: <Approver>	Size A4	Document Number SCH-31399 PDF: SPF-31399	Rev C2
Date:	Monday, January 07, 2019	Sheet 8 of 13	

eMMC

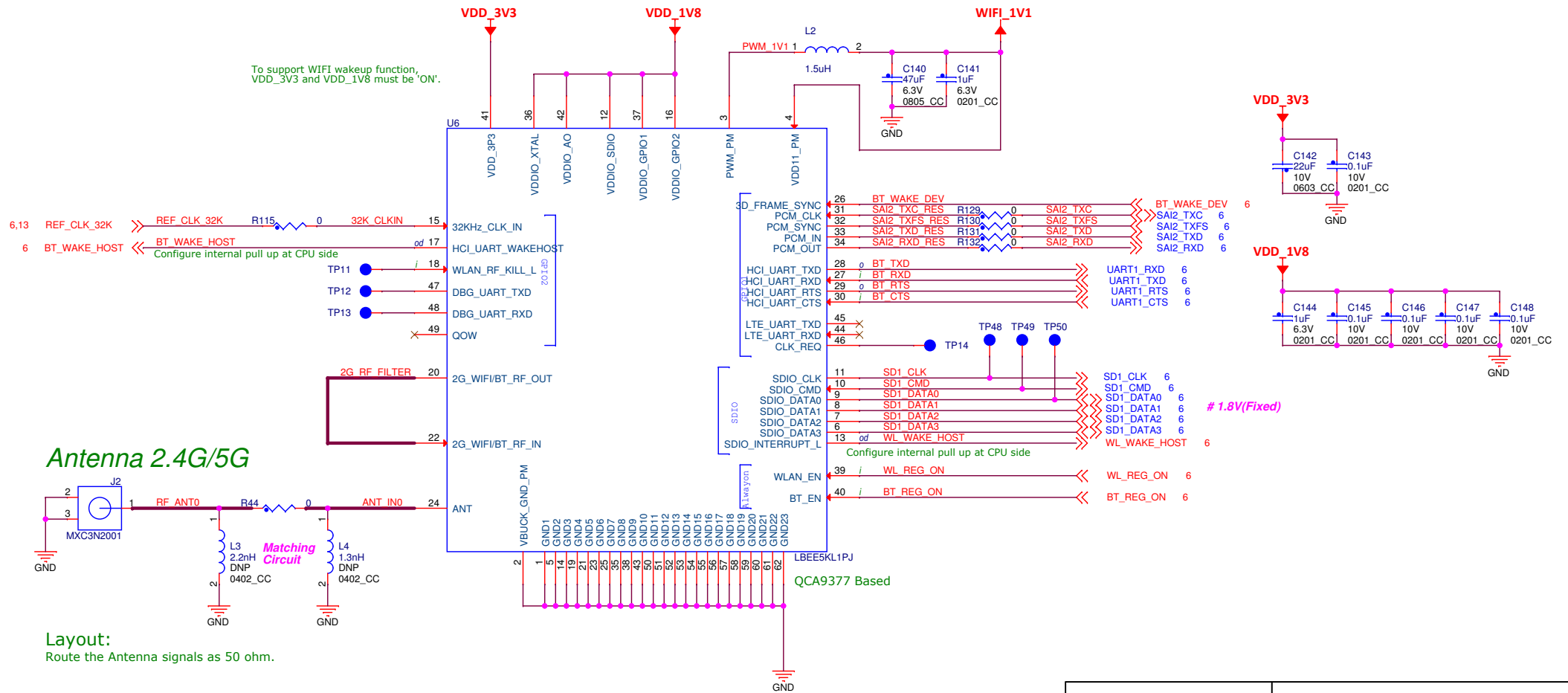


QSPI Flash




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Designer: Frank Liu		Drawing Title: <div style="text-align: center;"> 8MMINILPD4-CPU </div>	
Drawn by: Frank Liu		Page Title: <div style="text-align: center;"> eMMC/QSPI </div>	
Approved: <Approver>		Size B	Document Number SCH-31399 PDF: SPF-31399
		Date: Monday, February 11, 2019	Sheet 9 of 13
			Rev C2

2.4G/5G WIFI/BT Module



Power Sequence



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		ICAP Classification: CP: IUC: A PUBI:	
Designer: Frank Liu	8MMINILPD4-CPU		
Drawn by: Frank Liu	WIFI/BT Module		
Approved: <Approver>	Size B	Document Number SCH-31399 PDF: SPF-31399	Rev C2
Date: Monday, January 07, 2019		Sheet 10 of 13	

Boot Mode and CFG Switch

Caution:

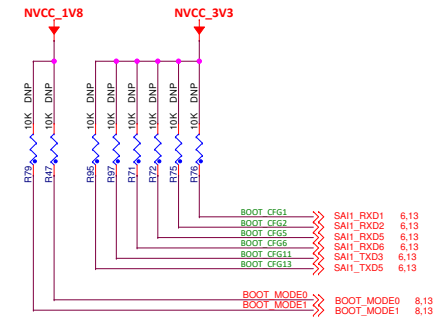
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

i.MX8M Mini ROM Fuse

Address		7	6	5	4	3	2	1	0	
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	
	0x470[15:8]	Infini-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD		Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via		SD Loopback Clock Source Sel (for SDR5 and SDR104 only) '0' - through SD pad '1' - direct	
	0x470[15:8]		010 - MMC/eMMC							
	0x470[15:8]		011 - NAND		Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5			
	0x470[15:8]		100 - QSPI		Flash Auto Probe		FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			
	0x470[15:8]		110 - SPI NOR				Port Select: 000 - eCSP11 001 - eCSP12 010 - eCSP13		SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	
	0x470[15:8]		Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]	
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved	
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.		Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved	USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V			
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.				Reserved	
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle				
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	

BT_CFG Pins:

SAI1_RXD0	BOOT_CFG0
SAI1_RXD1	BOOT_CFG1
SAI1_RXD2	BOOT_CFG2
SAI1_RXD3	BOOT_CFG3
SAI1_RXD4	BOOT_CFG4
SAI1_RXD5	BOOT_CFG5
SAI1_RXD6	BOOT_CFG6
SAI1_RXD7	BOOT_CFG7
SAI1_RXD8	BOOT_CFG8
SAI1_RXD9	BOOT_CFG9
SAI1_RXD10	BOOT_CFG10
SAI1_RXD11	BOOT_CFG11
SAI1_RXD12	BOOT_CFG12
SAI1_RXD13	BOOT_CFG13
SAI1_RXD14	BOOT_CFG14
SAI1_RXD15	BOOT_CFG15




Note:

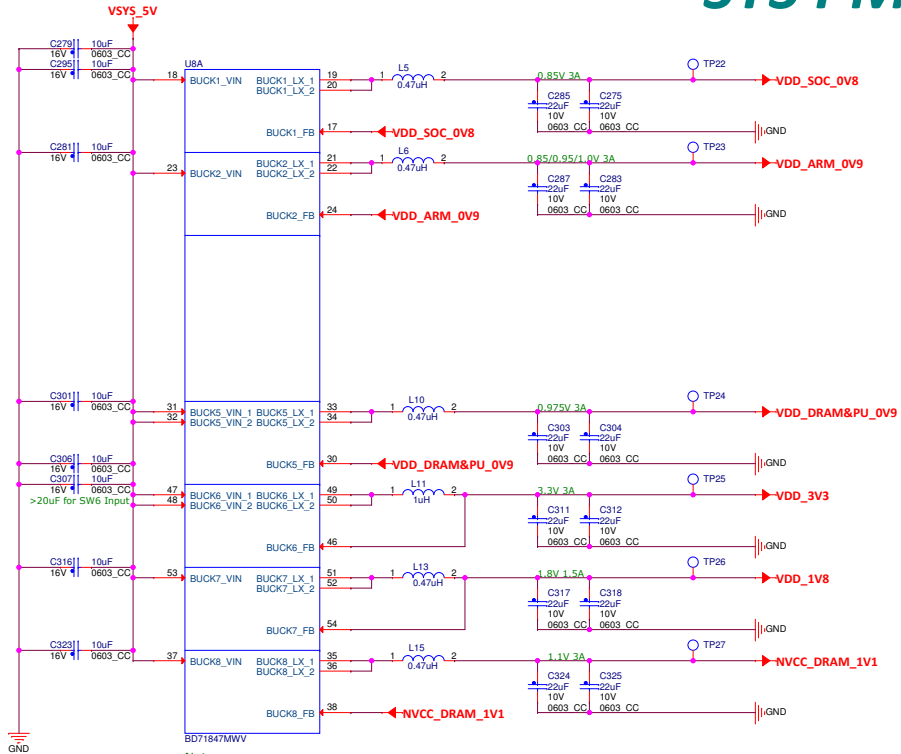
- Bootcfg/SAI1 singals have internal PD before and after POR_B reset is deasserted!
- Standalone SOM board can support eMMC/SDHC3 boot, by populating R71, R72, R75, R76, R79, R95, R97!
- When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

Boot Mode

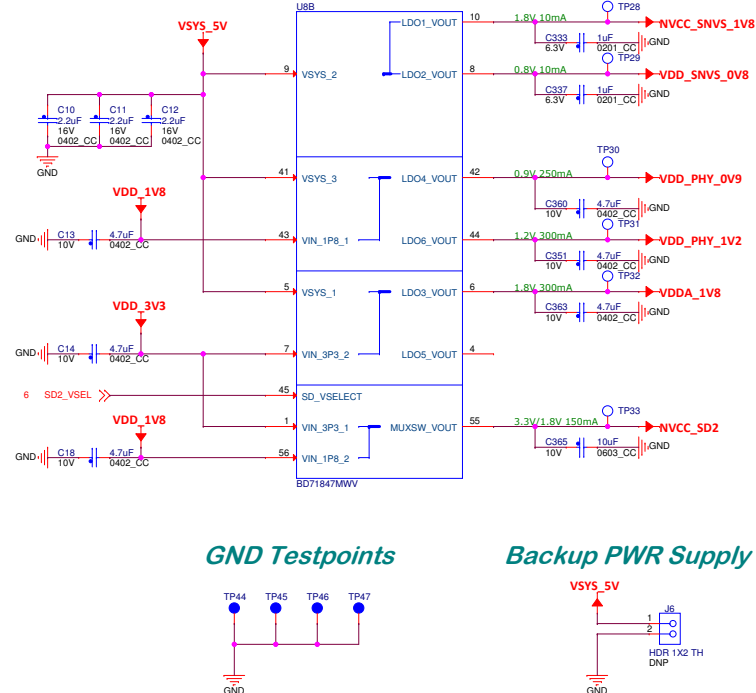
BOOT_MODE1	BOOT_MODE0
BOOT TYPE: 00 Boot From Fuses 01 Serial Downloader 10 Internal Boot (Development) 11 Reserved	

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ICAP Classification: CP:		IUC: X PUB:	
Designer: Frank Liu	Drawing Title: 8MMINILPD4-CPU		
Drawn by: Frank Liu	Page Title: BOOT_CFG		
Approved: Approver:	Size C	Document Number SCH-31399 PDF: SPF-31399	Rev C2
Date: Friday, January 25, 2019		Sheet 11 of 18	

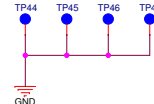
SYS PMIC



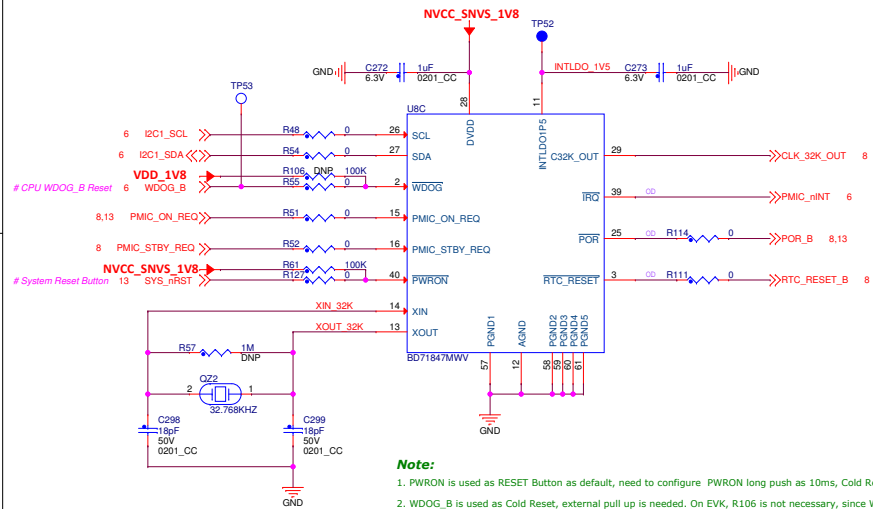
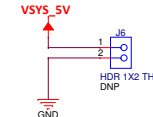
BUCK1 default output voltage is 0.8V. Software will change it to 0.85V in SPL before DDR initialization.
 BUCK5 default output voltage is 0.9V. Software will change it to 0.975V(BD71847 BUCK5 doesn't support 0.95V output) in SPL before DDR initialization.
 BUCK2 default output voltage is 0.9V. Software will change it to 0.85V for 1.2GHz operation, 0.95V for 1.6GHz, 1.0V for 1.8GHz.



GND Testpoints



Backup PWR Supply



1. PWRON is used as RESET Button as default, need to configure PWRON long push as 10ms, Cold Reset, and short push detect should be disabled !
2. WDOG_B is used as Cold Reset, external pull up is needed. On EVK, R106 is not necessary, since WDOG_B/GPIO1_IO02 of CPU has internal pull up.

i.MX8M Mini LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNV5_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNV5_OV8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_OV8	BUCK1	0.78/0.805	0.82/0.85	0.9	3000
6	VDD_DRAM&PU_OV9	BUCK5	0.805/0.855	0.85/0.95	0.9/1.0	3000
6	VDD_PHY_OV9	LDO4	0.855	0.9	1.0	250
7	VDD_ARM_OV9	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.95/1.0/1.05	3000
7	VDDA_1V8	LDO3	1.71	1.8	1.89	300
8	VDD_1V8/NVCC_1V8	BUCK7	1.65	1.8	1.95	1500
9	NVCC_DRAM_1V1	BUCK8	1.06	1.1	1.14	3000
10	VDD_3V3/NVCC_3V3	BUCK6	3	3.3	3.6	3000
10	NVCC_SD2	MUXSW	3.0/1.65	3.3/1.8	3.6/1.95	150
11	VDD_PHY_1V2	LDO6	1.14	1.2	1.26	300
12	POR_B	POR_B	--	--	--	--



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ICAB Classification: CB: ILO: Y DURE:

Designer:	Drawing Title:
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8MMINILPD4-CPU

Frank Liu	PMIC
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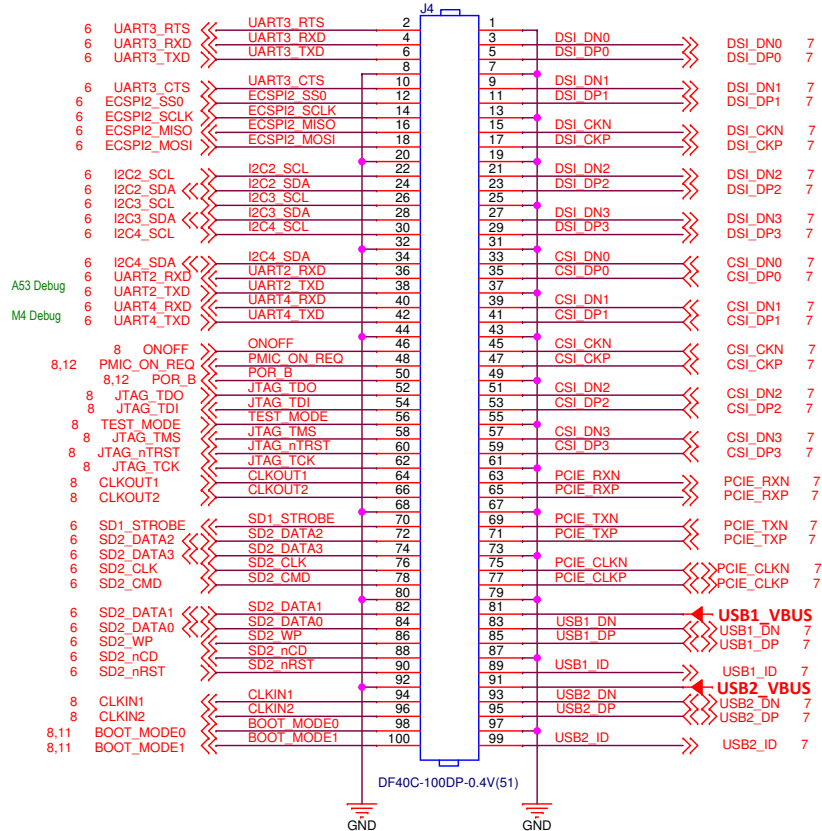
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B2B Connector for CPU Board

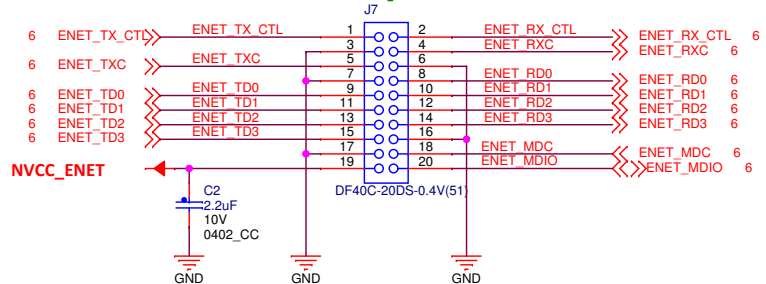
Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
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See Errata e50080 for detailed information.

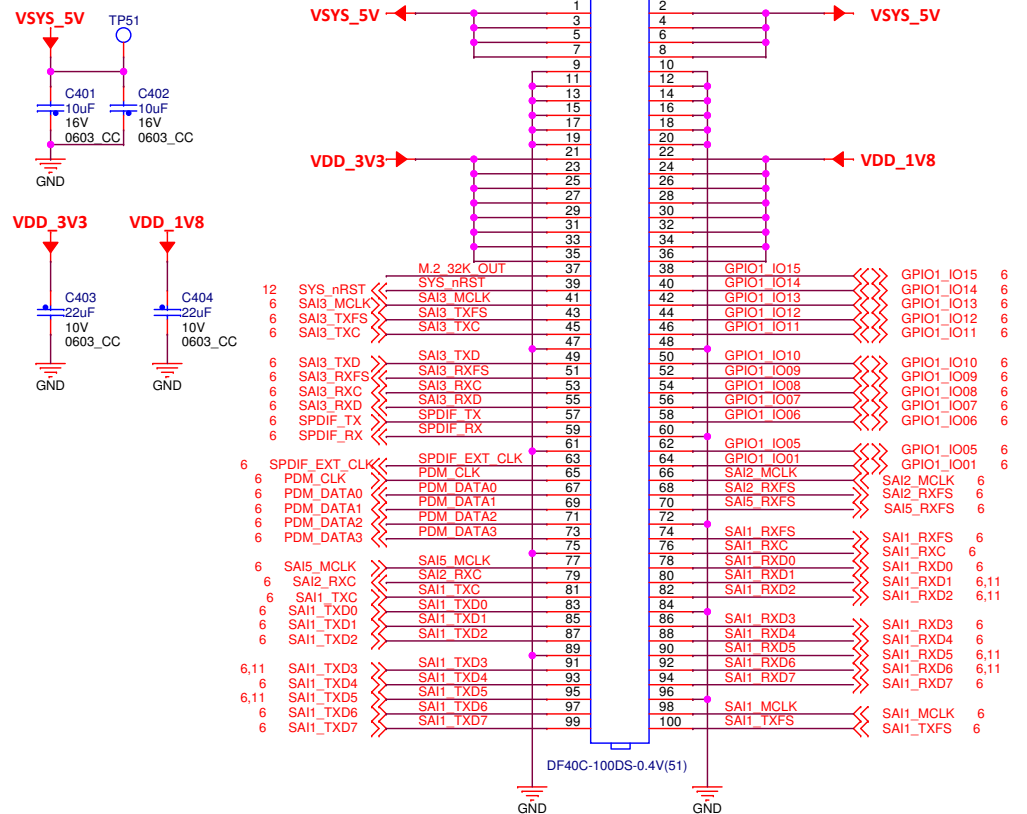
Header



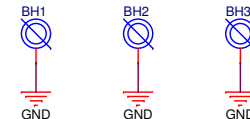
Receptacle




Receptacle



6,10 REF_CLK_32K >> REF_CLK_32K R116 DNP 0 M.2_32K_OUT
When using M.2 WIFI Module, remove R115, populate R116!



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Drawing Title:		8MMINILPD4-CPU	
Drawn by: Frank Liu		Page Title: SOM Interface	
Approved: <Approver>		Size B	Document Number SCH-31399 PDF: SPF-31399
Date: Friday, January 25, 2019		Sheet 13	of 13