AJAYA DAHAL

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EXPERIENCE

Sr. FPGA & Network System Engineer

Advanced Micro Devices (AMD) **Jan 2023 - Present, Remote-Based in Austin, TX**

- **Technical Lead for Ethernet Architecture:** Lead engineer for 15+ Ethernet reference designs ranging from 1G to 800G, integrating Hard IP (DCMAC/MRMAC) with DMA subsystems on Versal ACAP and Zynq UltraScale+ platforms.
- **High-Speed SerDes Tuning:** Expertly debugged GTY/GTM transceivers to optimize Eye Diagrams and resolve signal integrity issues for 100G links, ensuring physical layer reliability.
- **Full-Stack Optimization:** executed cross-layer debugging from RTL (Verilog) up to the OS (PetaLinux/Yocto) and Kernel Drivers, resolving complex hardware-software integration blockers.
- **Versal ACAP Implementation:** Architected solutions on VMK180, VPK120, and VCK190 evaluation boards, configuring Network-on-Chip (NoC) and PL-to-PS AXI interfaces for high-bandwidth data movement.
- **Knowledge Base Contribution:** Authored official AMD technical documentation (Answer Records) and tutorials, including the "MRMAC 4x25G Design Guide" and "DCMAC Survival Guide," resolving critical customer issues globally.
- **Lab & Signal Integrity:** Directed FPGA digital design labs bridging HDL logic with embedded Linux and lab-based signal integrity tuning for Ethernet IPs from 10M to 800G.

Graduate Research Assistant

Mississippi State University **Aug 2019- Dec 2023, Starkville, Mississippi**

- RF & SDR Systems: Architected real-time RF signal processing systems using Software Defined Radios (SDR) for contraband detection and spectrum monitoring, analyzing raw IQ data streams for passive microwave sensing.
- Autonomous Perception: Developed autonomous vehicle perception pipelines using TensorFlow and OpenCV, leveraging GPU acceleration for real- time lane tracking and camera-LIDAR sensor fusion (SqueezeSeg).
- 5G Network Research: Collaborated on multi-university 5G research initiatives utilizing srsLTE/RAN, OpenAirInterface (OAI), and Amarisoft stacks to validate open-source cellular network performance.
- Research Leadership: Selected as 1 of 10 researchers for the competitive MSU/USDA Summer Research Experience; operated as an FAA Part 107 certified drone pilot for autonomous field testing.

PCB Design Engineer Co-Op

Hunter Engineering Company **Jan 2020 – Jan 2022, Raymond, Mississippi**

- Automated Test Systems: Designed and built system-level functional testers for custom PCBs, creating end-to-end test architectures including custom hardware interfaces and displays.
- C++ & Embedded Control: Developed robust C/C++ backend software and LabVIEW GUIs to control hardware testers, ensuring reliable operation for non-technical operators.
- Computer Vision Integration: Integrated camera-based defect detection systems using OpenCV to automate quality verification on production lines.
- Engineering Practice: Applied digital design principles to architect automated verification systems, bridging the gap between hardware control and embedded software execution.

SKILLS

FPGA & Hardware Acceleration:

- Languages: Verilog, SystemVerilog
- Tools: Xilinx Vivado, Vitis HLS, ChipScope, IBERT (Eye Diagram Tuning), ModelSim, Quartus
- Platforms: Xilinx Versal ACAP (VMK180/VPK120), Zynq UltraScale+ MPSoC, RFSoC
- Interfaces: GTY/GTM SerDes (58G PAM4), PCIe, AXI4-Stream, I2C/SPI/UART
- Embedded Systems & Software:
  - Languages: C, C++ (Systems/Embedded), Python, Bash
  - OS & Kernel: Embedded Linux, PetaLinux, Yocto Project, Linux Device Drivers, RTOS
  - Networking: 10G-800G Ethernet (DCMAC/MRMAC/CMAC), TCP/IP, UDP, RDMA, Wireshark
- DevOps & Tools:
  - CI/CD: Jenkins, Docker, Git/GitHub
  - Robotics/AI: ROS/ROS2, TensorFlow, OpenCV, MATLAB/Simulink
  - Hardware Design: Altium Designer, KiCad, SolidWorks

PROJECT

Asynchronous FIFO (Clock Domain Crossing)

- CDC Architecture: Designed a parameterizable Asynchronous FIFO in Verilog to manage safe data transfer between independent clock domains, mitigating metastability issues.
- Robust Synchronization: Implemented Gray code pointers and dual-rank synchronizers to ensure reliable empty/full flag generation, adhering to Clifford E. Cummings' industry-standard design principles.
- Verification: Validated design functionality through simulation to ensure data integrity across asynchronous boundaries, a critical component for low-latency hardware pipelines.

Versal ACAP & MPSoC Ethernet Architectures (Open Source)

- High-Speed Network Design: Developed and maintained open-source production-grade Ethernet reference designs for Versal ACAP (VPK120/ VCK190) and Zynq UltraScale+ (ZCU102).
- IP Integration: Integrated 100G DCMAC, MRMAC, and 10G/25G Soft MACs with DMA subsystems, enabling high-bandwidth packet processing and traffic generation.
- Full-Stack Validation: Provided complete Vivado block designs and PetaLinux BSP configurations, validating designs with live traffic tests and eye diagram tuning on real hardware.

Autonomous Drone System (NXP HoverGames Bonus Prize Winner)

- Real-Time Flight Control: engineered a full-stack autonomous flight system integrating PX4 flight stacks and ROS2 navigation nodes for precision mission planning.
- Sensor Fusion: Implemented sensor fusion algorithms on embedded hardware to combine GPS, LIDAR, and optical flow data for stable autonomous navigation.
- Award Recognition: Awarded Bonus Prize by NXP Semiconductors/Hackster.io for technical execution in integrating contactless payload delivery with autonomous flight

EDUCATION

Master of Science

MSU • Starkville, Mississippi • May 2024 • MSU GPA 4.0/4.0

- Electrical and Computer Engineering.

Bachelor of Science

MSU • Starkville, Mississippi • December 2022 • MSU GPA 4.0/4.0

- Electrical and Computer Engineering.

INVOLVEMENT

Software Lead - Unmanned Aircraft System Integrated Products Team

Mississippi State University • Xipiter • 2021 - 2023

- Technical Leadership: Led the software division in architecting the autonomous flight stack for the AUVSI SUAS competition, integrating path planning, computer vision, and embedded control subsystems.
- Managed cross-functional teams (Airframe, Embedded, Software), overseeing design reviews, system integration timelines, and budget allocation for competition-grade UAVs.
- System Integration: Directed the migration to ROS (Robot Operating System) and validated inter-process communication between onboard NVIDIA Jetsons and flight controllers

President

Mississippi State University • Nepalese Student Association • 2021 - 2022

- Academic Leadership: Organized technical workshops and professional development events to bridge the gap between academic theory and industry skills for engineering students.
- Coordinated induction ceremonies and managed member engagement initiatives, increasing active participation in the college of engineering.

AWARDS & HONORS

AMD Technical Recognition (2023–2025)

AMD

• Awarded WTS NA Field Recognition and "Team Player 2024" for technical leadership. Recipient of 8+ Internal Spotlight Awards for resolving critical architectural blockers in MRMAC, AXI Ethernet, and QSGMII subsystems.

NXP Hover Games Winner (2021)

• Bonus Prize Winner for "Autonomous Drone System," recognized for excellence in embedded sensor fusion, real-time flight control, and C++ system integration.

Academic Excellence(MSU)

• Recipient of Undergraduate Research Grant (Autonomous Perception), MAMA Scholarship, and Certificate of Excellence in Microprocessors (Top of Class for dsPIC33EP robot design).