



Applications Places System



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Save



Un

not\_c.v X

```
module not_c(a,y);

    input a;
    output y;
    supply1 vdd;
    supply0 vss;

    pmos P1(y,vdd,a);
    nmos N1(y,vss,a);
endmodule
```



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Undo



not\_c\_tb.v X

```
module not_c_tb();

    reg a;
    wire y;

    not_c DUT(a,y);

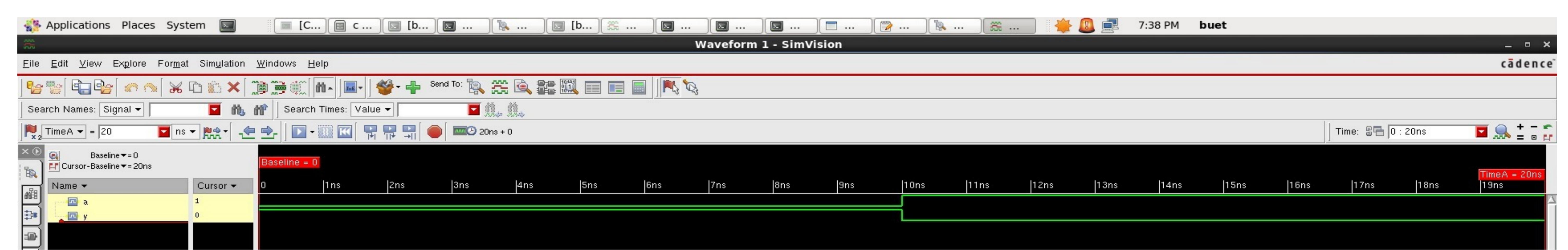
    initial
    begin

        $monitor("a=%b,y=%b",a,y);

    end

    initial
    begin

        #0;a=0;
        #10;a=1;
        #10;
        $finish;
    end
endmodule
```





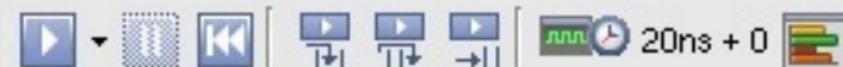
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Text Search:



20ns + 0

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm not_c_tb.a not_c_tb.y
Created probe 1
ncsim> run
a=0, y=1
a=1, y=0
Simulation complete via $finish(1) at time 20 NS + 0
./not_c_tb.v:21      $finish;
ncsim>
```



Applications Places System



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Save



Und

File nand\_c.v X

```
module nand_c(a,b,y);

    input a,b;
    output y;
    supply1 vdd;
    supply0 vss;
    wire w;
    pmos P1(y,vdd,a);
    pmos P2(y,vdd,b);
    nmos N1(w,vss,b);
    nmos N2(y,w,a);

endmodule
```



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Save



Undo



nand\_c\_tb.v

```
module nand_c_tb();

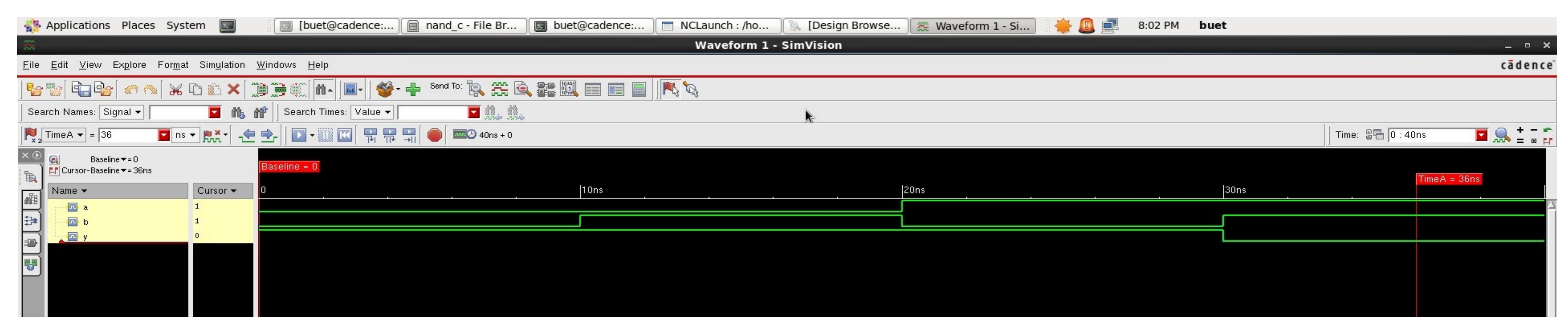
    reg a, b;
    wire y;

    nand_c NA1(a, b, y);

    initial
    begin
        $monitor("Time=%t,a=%b, b=%b, y=%b",$time, a, b, y);
    end

    initial
    begin
        #0; {a, b} = 2'd0;
        #10; {a, b} = 2'd1;
        #10; {a, b} = 2'd2;
        #10; {a, b} = 2'd3;
        #10;
        $finish;
    end

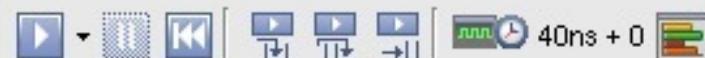
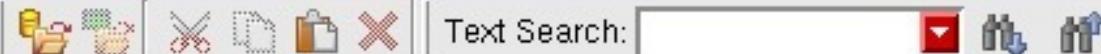
endmodule
```



Applications Places System [buet@cade...]



File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm nand_c_tb.a nand_c_tb.b nand_c_tb.y
Created probe 1
ncsim> run
Time=                      0, a=0, b=0, y=1
Time=                      10, a=0, b=1, y=1
Time=                     20, a=1, b=0, y=1
Time=                     30, a=1, b=1, y=0
Simulation complete via $finish(1) at time 40 NS + 0
./nand_c_tb.v:20           $finish;
ncsim>
```



Applications Places System



[buet@...]



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Save



Undo



and\_c.v X

```
module and_c(a,b,y);

    input a,b;
    output y;
    wire w;

    nand_c NA1(a,b,w);
    not_c NOT1(w,y);

endmodule
```



File Edit View Search Tools Documents Help



and\_c\_tb.v

```
module and_c_tb();

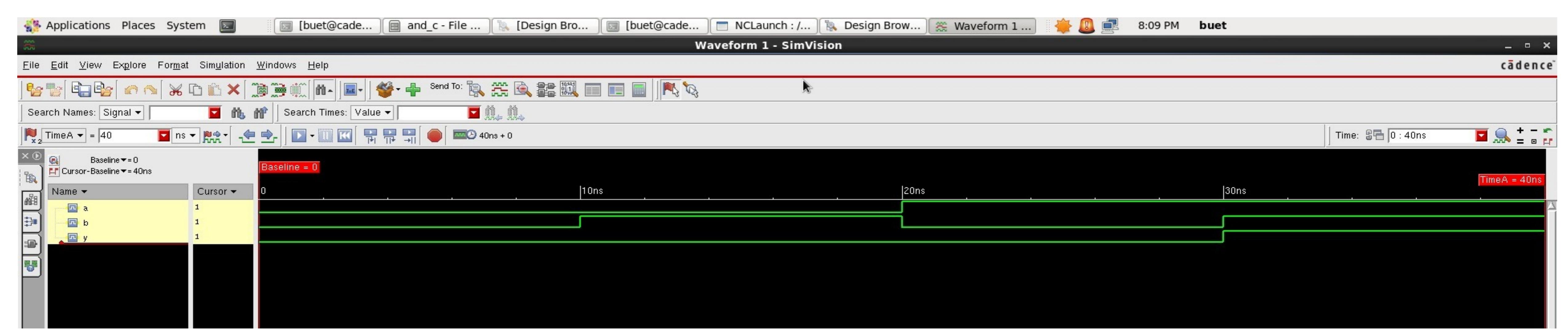
    reg a, b;
    wire y;

    and_c A1(a, b, y);

    initial
    begin
        $monitor("Time=%t,a=%b, b=%b, y=%b",$time, a, b, y);
    end

    initial
    begin
        #0; {a, b} = 2'd0;
        #10; {a, b} = 2'd1;
        #10; {a, b} = 2'd2;
        #10; {a, b} = 2'd3;
        #10;
        $finish;
    end

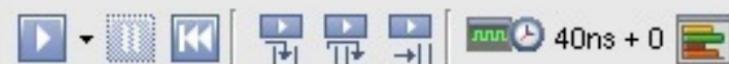
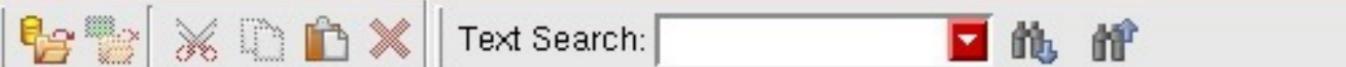
endmodule
```



Applications Places System [buet@ca... and\_c



File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm and_c_tb.a and_c_tb.b and_c_tb.y
Created probe 1
ncsim> run
Time= 0, a=0, b=0, y=0
Time= 10, a=0, b=1, y=0
Time= 20, a=1, b=0, y=0
Time= 30, a=1, b=1, y=1
Simulation complete via $finish(1) at time 40 NS + 0
./and_c_tb.v:20      $finish;
ncsim>
```



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Save



Undo



xnor\_c.v

```
module xnor_c(a,b,y);

    input a,b;
    output y;
    supply1 vdd;
    supply0 vss;
    wire [4:0]w;

    not_c NOT1(a,w[0]);
    not_c NOT2(b,w[1]);
    pmos P1(w[2],vdd,w[0]);
    pmos P2(w[2],vdd,b);
    pmos P3(y,w[2],w[1]);
    pmos P4(y,w[2],a);
    nmos N1(y,w[3],b);
    nmos N2(w[3],vss,w[0]);
    nmos N3(y,w[4],w[1]);
    nmos N4(w[4],vss,a);

endmodule
```



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Undo



xnor\_c\_tb.v

```
module xnor_c_tb();

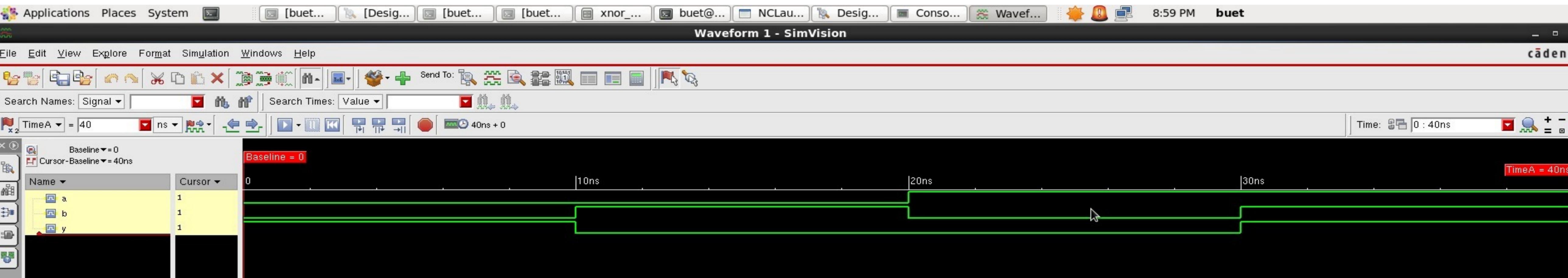
    reg a, b;
    wire y;

    xnor_c A1(a, b, y);

    initial
    begin
        $monitor("Time=%t,a=%b, b=%b, y=%b",$time, a, b, y);
    end

    initial
    begin
        #0; {a, b} = 2'd0;
        #10; {a, b} = 2'd1;
        #10; {a, b} = 2'd2;
        #10; {a, b} = 2'd3;
        #10;
        $finish;
    end

endmodule
```



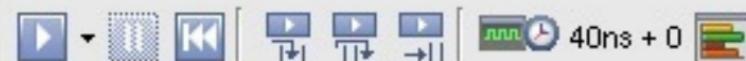
Applications Places System [buet...]



File Edit View Simulation Windows Help



Text Search:



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm xnor_c_tb.a xnor_c_tb.b xnor_c_tb.y
Created probe 1
ncsim> run
Time= 0, a=0, b=0, y=1
Time= 10, a=0, b=1, y=0
Time= 20, a=1, b=0, y=0
Time= 30, a=1, b=1, y=1
Simulation complete via $finish(1) at time 40 NS + 0
./xnor_c_tb.v:20      $finish;
ncsim> |
```



Applications Places System



File Edit View Search Tools Documents



Open ▾



Save



xor\_c.v X

```
module xor_c(a,b,y);

    input a,b;
    output y;
    wire w;

    xnor_c XN1(a,b,w);
    not_c NOT1(w,y);
endmodule
```





File Edit View Search Tools Documents Help



Open

Save



Undo



xor\_c\_tb.v

```
module xor_c_tb();

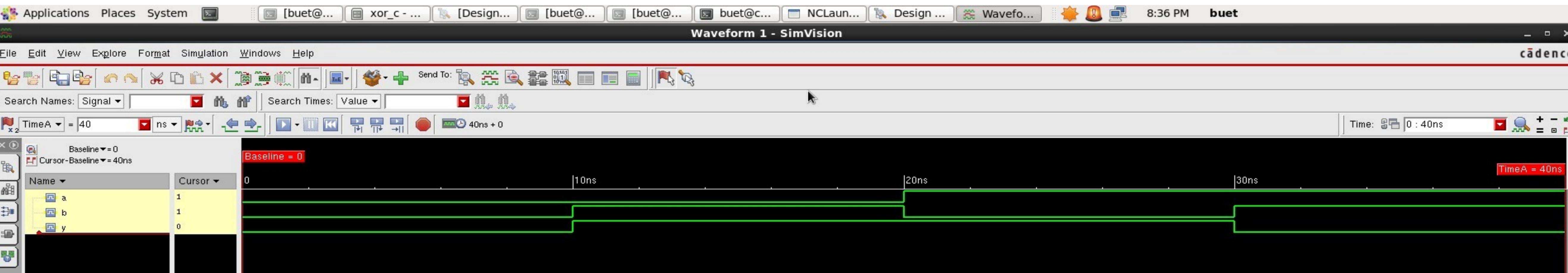
    reg a, b;
    wire y;

    xor_c A1(a, b, y);

    initial
    begin
        $monitor("Time=%t,a=%b, b=%b, y=%b",$time, a, b, y);
    end

    initial
    begin
        #0;  {a, b} = 2'd0;
        #10; {a, b} = 2'd1;
        #10; {a, b} = 2'd2;
        #10; {a, b} = 2'd3;
        #10;
        $finish;
    end

endmodule
```



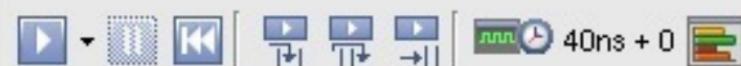
Applications Places System [buet... xor\_c ...]



File Edit View Simulation Windows Help



Text Search:



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm xor_c_tb.a xor_c_tb.b xor_c_tb.y
Created probe 1
ncsim> run
Time= 0, a=0, b=0, y=0
Time= 10, a=0, b=1, y=1
Time= 20, a=1, b=0, y=1
Time= 30, a=1, b=1, y=0
Simulation complete via $finish(1) at time 40 NS + 0
./xor_c_tb.v:20 $finish;
ncsim>
```

Applications Places System [buet@cadence:~/Doc... nor\_c - File Browser buet@cadence:~/Docu... nor\_c.v (~/Documents/Simulation /full adder/c/full\_adder\_c/nor\_c) - gedit 10:32 PM buet

File Edit View Search Tools Documents Help

Open Save Undo | Scissors Copy Paste Find Replace

nor\_c.v

```
module nor_c(a,b,y);  
    input a,b;  
    output y;  
    wire w;  
    supply1 vdd;  
    supply0 vss;  
    pmos P1(w,vdd,a);  
    pmos P2(y,w,b);  
    nmos N1(y,vss,a);  
    nmos N2(y,vss,b);  
endmodule
```

Verilog Tab Width: 8 Ln 5, Col 16 INS

Applications Places System [buet@cadence:~/Doc... nor\_c - File Browser buet@cadence:~/Docu... nor\_c\_tb.v (~/Docume... 10:33 PM buet

nor\_c\_tb.v (~/Documents/Simulation /full adder/c/full\_adder\_c/nor\_c) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace

nor\_c\_tb.v

```
module nor_c_tb();
    reg a, b;
    wire y;

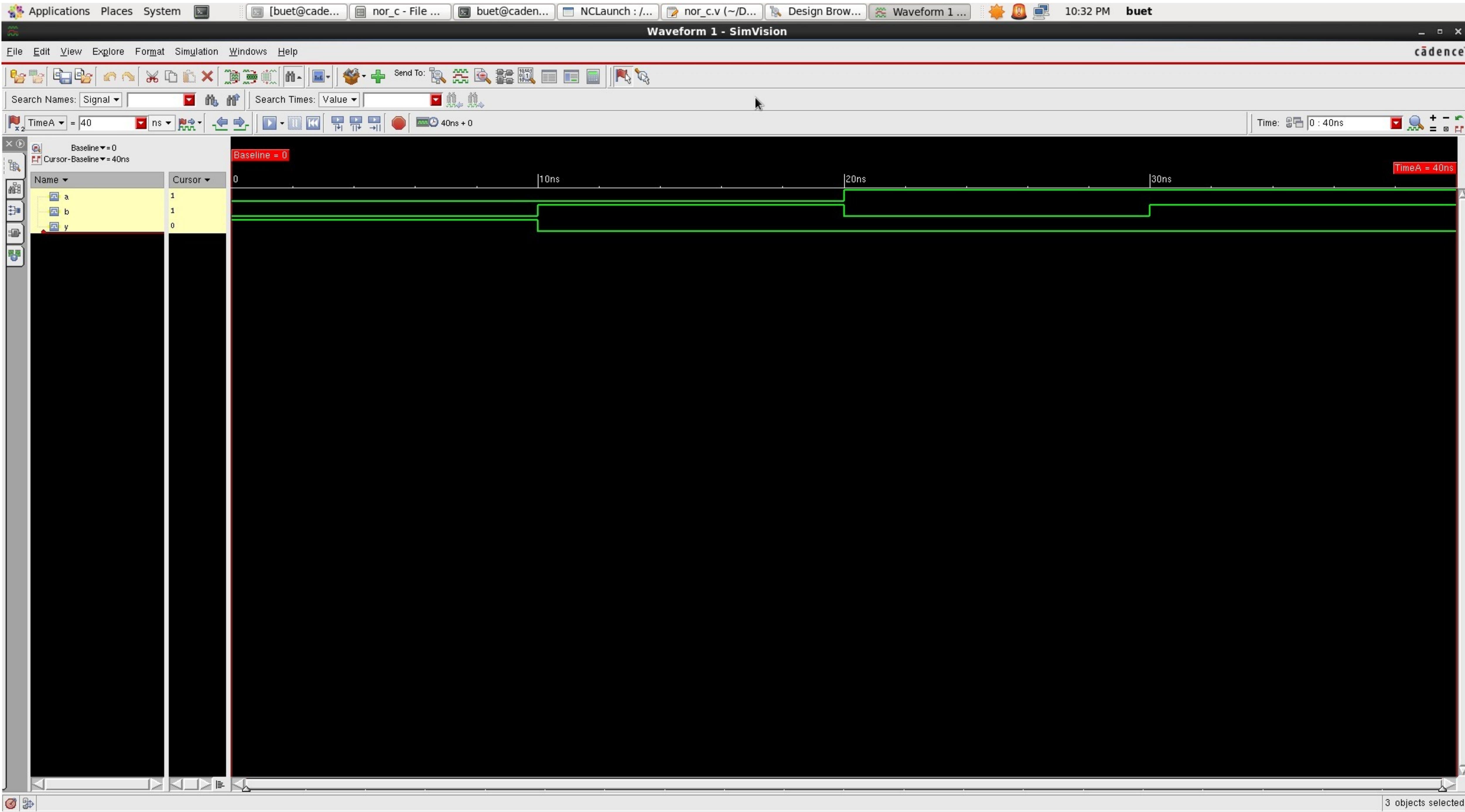
    nor_c N01(a, b, y);

    initial
    begin
        $monitor("Time=%t,a=%b, b=%b, y=%b",$time, a, b, y);
    end

    initial
    begin
        #0; {a, b} = 2'd0;
        #10; {a, b} = 2'd1;
        #10; {a, b} = 2'd2;
        #10; {a, b} = 2'd3;
        #10;
        $finish;
    end

endmodule
```

Loading file '/home/buet/Documents/Simulation /full adder/c/full\_adder\_c/nor\_c\_tb.v'... Verilog Tab Width: 8 Ln 6, Col 13 INS



## Console - SimVision

x

File Edit View Simulation Windows Help

cadence

Text Search: 

40ns + 0



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm nor_c_tb.a nor_c_tb.b nor_c_tb.y
Created probe 1
ncsim> run
Time=          0, a=0, b=0, y=1
Time=         10, a=0, b=1, y=0
Time=         20, a=1, b=0, y=0
Time=         30, a=1, b=1, y=0
Simulation complete via $finish(1) at time 40 NS + 0
./nor_c_tb.v:20      $finish;
ncsim>
```



File Edit View Search Tools Documents Help

Open Save Print Undo Redo Cut Copy Paste Find Replace

or\_c.v X

```
module or_c(a,b,y);  
    input a,b;  
    output y;  
    wire w;  
  
    nor_c N01(a,b,w);  
    not_c N1(w,y);  
endmodule
```

or\_c\_tb.v (~/Documents/Simulation /full adder/c/full\_adder\_c/or\_c) - gedit

File Edit View Search Tools Documents Help

Open Save Undo | Cut Copy Paste Find Replace

or\_c\_tb.v X

```
module or_c_tb();
    reg a, b;
    wire y;

    or_c O1(a, b, y);

    initial
    begin
        $monitor("Time=%t,a=%b, b=%b, y=%b",$time, a, b, y);
    end

    initial
    begin
        #0; {a, b} = 2'd0;
        #10; {a, b} = 2'd1;
        #10; {a, b} = 2'd2;
        #10; {a, b} = 2'd3;
        #10;
        $finish;
    end

endmodule
```

## Waveform 1 - SimVision

x

cadence

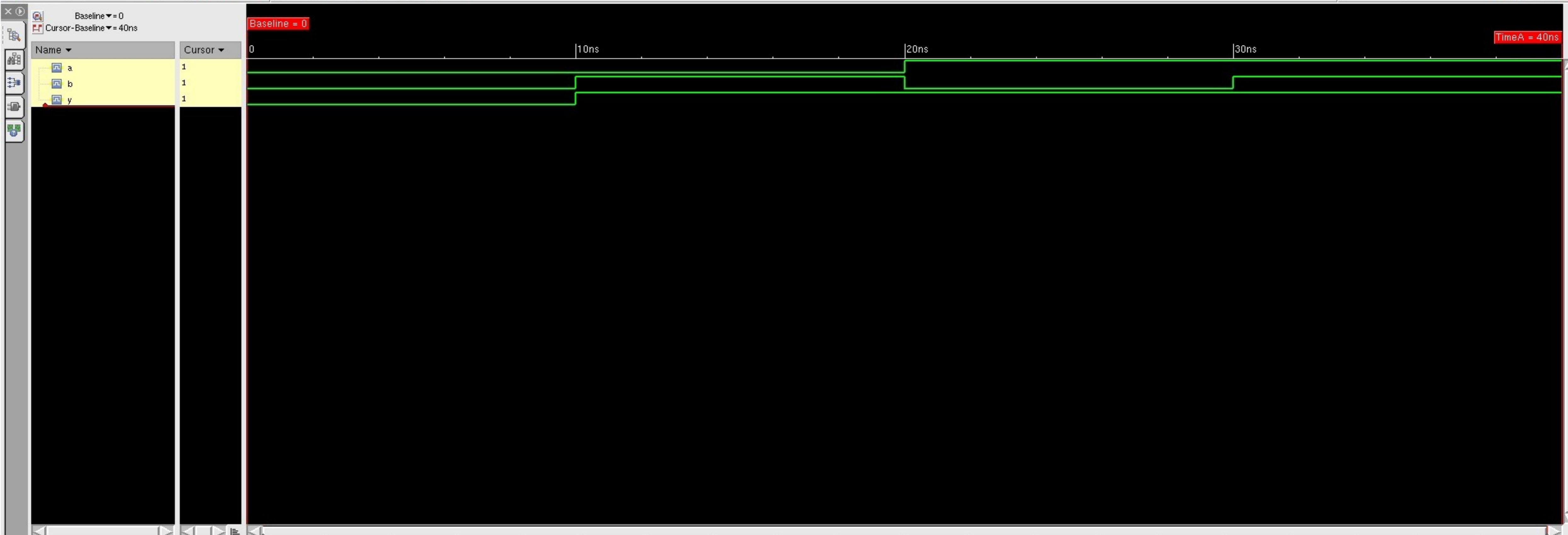
File Edit View Explore Format Simulation Windows Help



Search Names: Signal ▾ | Search Times: Value ▾

TimeA ▾ = 40 ns | 40ns + 0

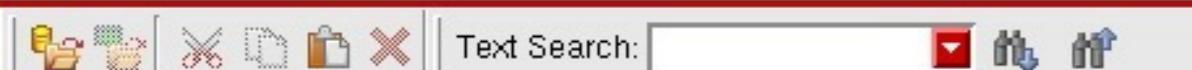
Time: 0 : 40ns



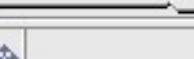
## Console - SimVision

cadence

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm or_c_tb.a or_c_tb.b or_c_tb.y
Created probe 1
ncsim> run
Time=          0, a=0, b=0, y=0
Time=         10, a=0, b=1, y=1
Time=         20, a=1, b=0, y=1
Time=         30, a=1, b=1, y=1
Simulation complete via $finish(1) at time 40 NS + 0
./or_c_tb.v:20      $finish;
ncsim>
```



SimVision

simulator

full\_adder\_c.v (~/Documents/Simulation /full adder/c/full\_adder\_c) - gedit

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Open Save Undo | Cut Copy Paste Find Replace

full\_adder\_c.v

```
module full_adder_c(a,b,cin,sum,cout);

    input a,b,cin;
    output sum,cout;
    wire [4:0]w;

    xor_c X1(a,b,w[0]);
    xor_c X2(w[0],cin,sum);
    and_c A1(a,b,w[1]);
    and_c A2(b,(cin,w[2]));
    and_c A3((cin,a,w[3]));
    or_c O3(w[1],w[2],w[4]);
    or_c O4(w[3],w[4],cout);
endmodule
```

## full\_adder\_c\_tb.v (~/Documents/Simulation /full adder/c/full\_adder\_c) - gedit

File Edit View Search Tools Documents Help



full\_adder\_c\_tb.v

```
module full_adder_c_tb();
    reg a,b,cin;
    wire sum,cout;
    full_adder_c FA1(a,b,cin,sum,cout);

    initial
    begin
        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,cin,sum,cout);
    end
    initial
    begin
        #0; {a,b,cin}=3'd0;
        #10; {a,b,cin}=3'd1;
        #10; {a,b,cin}=3'd2;
        #10; {a,b,cin}=3'd3;
        #10; {a,b,cin}=3'd4;
        #10; {a,b,cin}=3'd5;
        #10; {a,b,cin}=3'd6;
        #10; {a,b,cin}=3'd7;
        #10;
        $finish;
    end
endmodule
```

## Waveform 1 - SimVision

cadence®

File Edit View Explore Format Simulation Windows Help



Search Names: Signal ▾ Search Times: Value ▾

TimeA ▾ = 14 ns

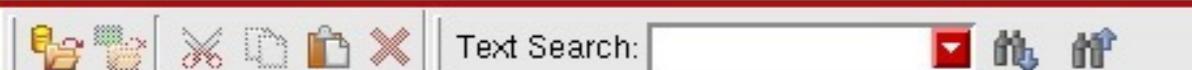
Baseline = 0 Cursor-Baseline = 14ns

Name ▾
Cursor ▾
a
b
cin
cout
sum



## Console - SimVision

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_c_tb.a full_adder_c_tb.b full_adder_c_tb.cin full_adder_c_tb.cout full_adder_c_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=         10 a=0 b=0 cin=1 sum=1 cout=0
Time=         20 a=0 b=1 cin=0 sum=1 cout=0
Time=         30 a=0 b=1 cin=1 sum=0 cout=1
Time=         40 a=1 b=0 cin=0 sum=1 cout=0
Time=         50 a=1 b=0 cin=1 sum=0 cout=1
Time=         60 a=1 b=1 cin=0 sum=0 cout=1
Time=         70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_c_tb.v:26  $finish;
ncsim>
```

## full\_adder\_g.v (~/Documents/Simulation /full adder/g) - gedit

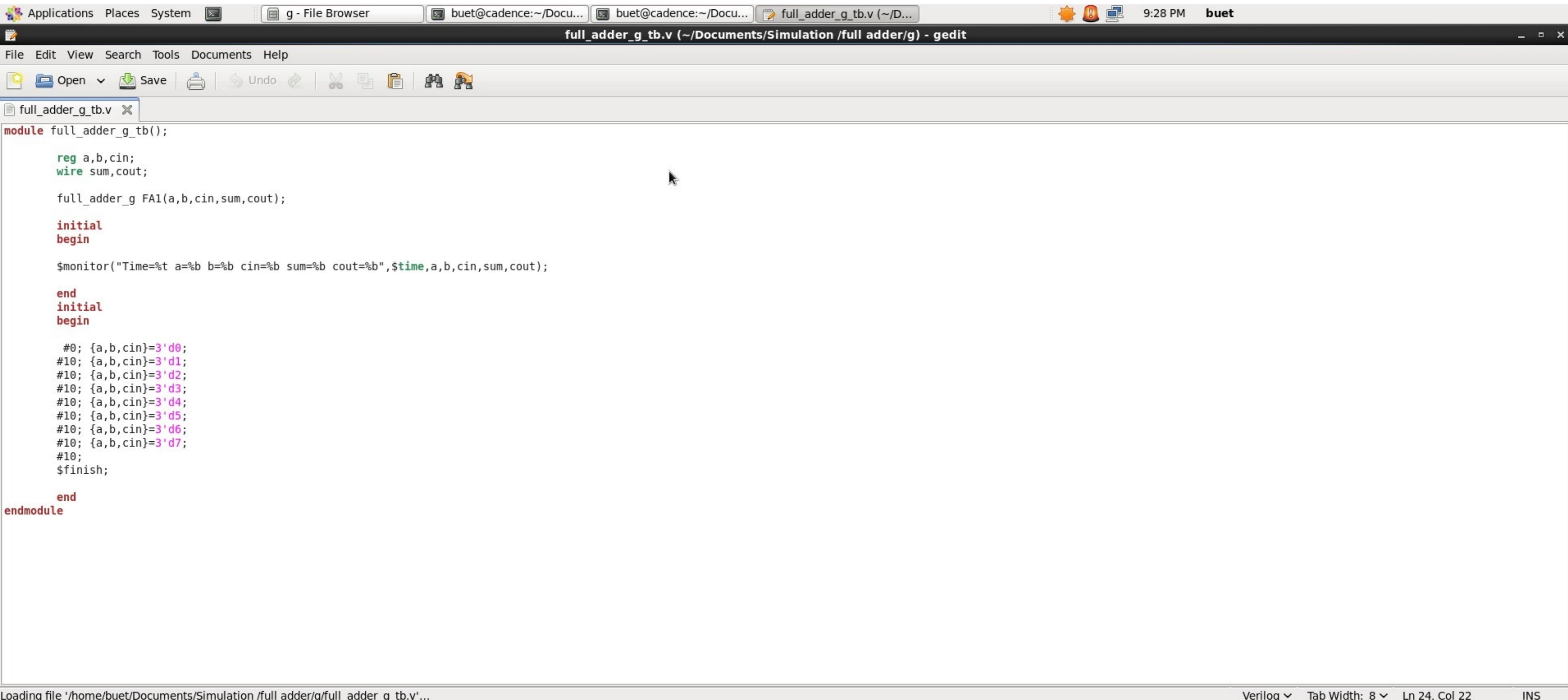
File Edit View Search Tools Documents Help



full\_adder.g.v X

```
module full_adder_g(a,b,cin,sum,cout);  
    input a,b,cin;  
    output sum,cout;  
    wire [2:0]w;  
  
    xor X1(sum,a,b,cin);  
    and A1(w[0],a,b);  
    and A2(w[1],b,cin);  
    and A3(w[2],cin,a);  
    or O3(cout,w[0],w[1],w[2]);  
endmodule
```





## Waveform 1 - SimVision

cadence

File Edit View Explore Format Simulation Windows Help



Search Names: Signal ▾

Search Times: Value ▾

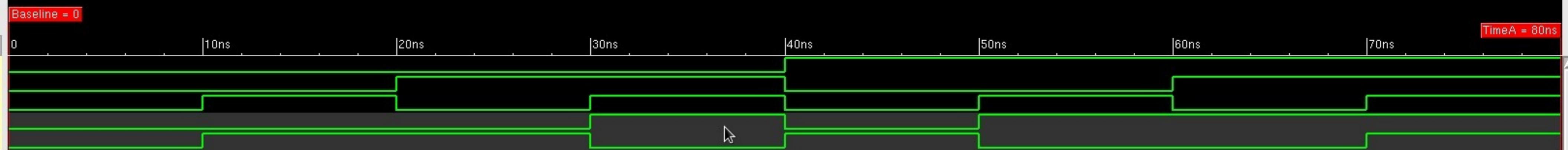
TimeA ▾ = 80 ns

Baseline ▾ = 0

Cursor-Baseline ▾ = 80ns

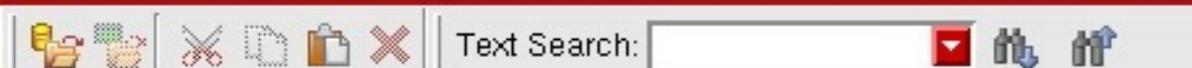
Name ▾

Cursor ▾

a  
b  
cin  
cout  
sum

## Console - SimVision

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_g_tb.a full_adder_g_tb.b full_adder_g_tb.cin full_adder_g_tb.cout full_adder_g_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=         10 a=0 b=0 cin=1 sum=1 cout=0
Time=         20 a=0 b=1 cin=0 sum=1 cout=0
Time=         30 a=0 b=1 cin=1 sum=0 cout=1
Time=         40 a=1 b=0 cin=0 sum=1 cout=0
Time=         50 a=1 b=0 cin=1 sum=0 cout=1
Time=         60 a=1 b=1 cin=0 sum=0 cout=1
Time=         70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_g_tb.v:26  $finish;
ncsim>
```

## full\_adder\_d.v (~/Documents/Simulation /full adder/d) - gedit

File Edit View Search Tools Documents Help



full\_adder\_d.v X

```
module full_adder_d(a,b,cin,sum,cout);  
    input a,b,cin;  
    output sum,cout;  
  
    assign {cout,sum}={(a&b)|(b&cin)|(cin&a),a^b^cin};  
endmodule
```



## full\_adder\_d\_tb.v (~/Documents/Simulation /full adder/d) - gedit

File Edit View Search Tools Documents Help

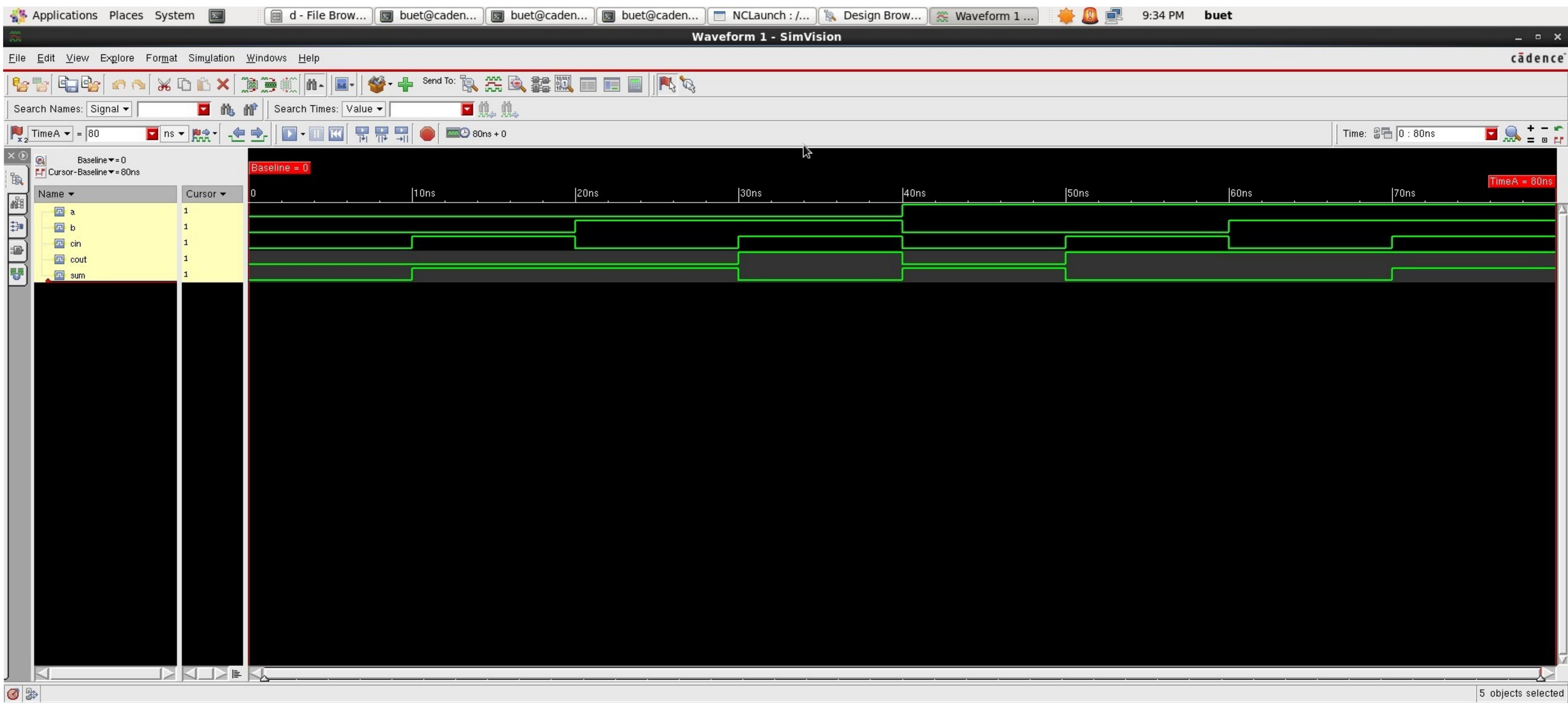


full\_adder\_d\_tb.v

```
module full_adder_d_tb();
    reg a,b,cin;
    wire sum,cout;
    full_adder_d FA1(a,b,(cin,sum,cout);

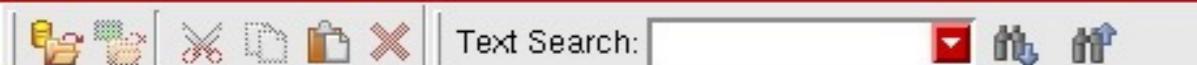
    initial
    begin
        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,(cin,sum,cout);
    end
    initial
    begin
        #0; {a,b,(cin)=3'd0;
        #10; {a,b,(cin)=3'd1;
        #10; {a,b,(cin)=3'd2;
        #10; {a,b,(cin)=3'd3;
        #10; {a,b,(cin)=3'd4;
        #10; {a,b,(cin)=3'd5;
        #10; {a,b,(cin)=3'd6;
        #10; {a,b,(cin)=3'd7;
        #10;
        $finish;
    end
endmodule
```





## Console - SimVision

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_d_tb.a full_adder_d_tb.b full_adder_d_tb.cin full_adder_d_tb.cout full_adder_d_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=         10 a=0 b=0 cin=1 sum=1 cout=0
Time=         20 a=0 b=1 cin=0 sum=1 cout=0
Time=         30 a=0 b=1 cin=1 sum=0 cout=1
Time=         40 a=1 b=0 cin=0 sum=1 cout=0
Time=         50 a=1 b=0 cin=1 sum=0 cout=1
Time=         60 a=1 b=1 cin=0 sum=0 cout=1
Time=         70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_d_tb.v:26  $finish;
ncsim>
```

## full\_adder\_b.v (~/Documents/Simulation /full adder/b) - gedit

File Edit View Search Tools Documents Help

full\_adder\_b.v X

```
module full_adder_b(a,b,cin,sum,cout);  
    input a,b,cin;  
    output reg sum,cout;  
  
    always@(a,b,cin)  
    case({a,b,cin})  
        3'd0:{cout,sum}=2'd0;  
        3'd1:{cout,sum}=2'd1;  
        3'd2:{cout,sum}=2'd1;  
        3'd3:{cout,sum}=2'd2;  
        3'd4:{cout,sum}=2'd1;  
        3'd5:{cout,sum}=2'd2;  
        3'd6:{cout,sum}=2'd2;  
        3'd7:{cout,sum}=2'd3;  
        default:{cout,sum}=2'dx;  
    endcase  
endmodule
```



## full\_adder\_b\_tb.v (~/Documents/Simulation /full adder/b) - gedit

File Edit View Search Tools Documents Help



full\_adder\_b\_tb.v

```
module full_adder_b_tb();

    reg a,b,cin;
    wire sum,cout;

    full_adder_b FA1(a,b,cin,sum,cout);

    initial
    begin

        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,cin,sum,cout);

    end
    initial
    begin

        #0; {a,b,cin}=3'd0;
        #10; {a,b,cin}=3'd1;
        #10; {a,b,cin}=3'd2;
        #10; {a,b,cin}=3'd3;
        #10; {a,b,cin}=3'd4;
        #10; {a,b,cin}=3'd5;
        #10; {a,b,cin}=3'd6;
        #10; {a,b,cin}=3'd7;
        #10;
        $finish;

    end
endmodule
```

## Waveform 1 - SimVision

cadence®

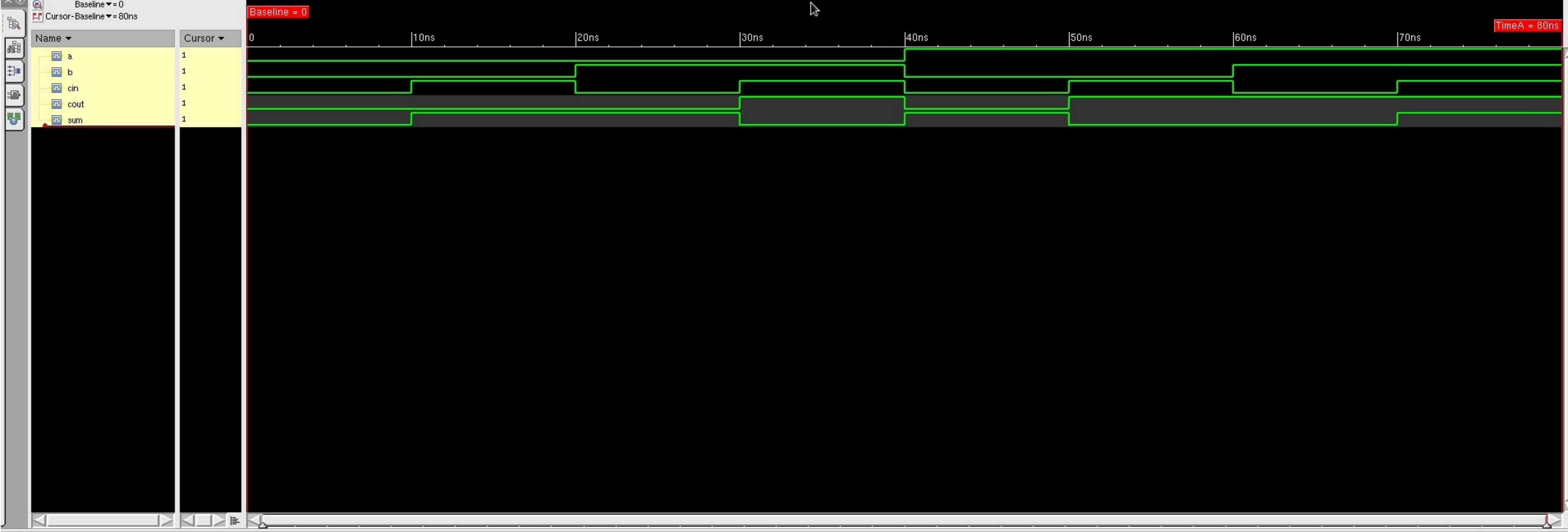
File Edit View Explore Format Simulation Windows Help



Search Names: Signal ▾ Search Times: Value ▾

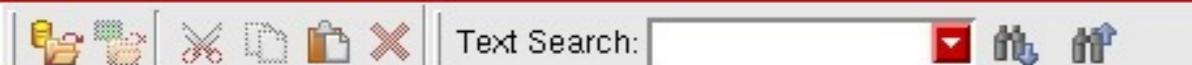
TimeA ▾ = 80 ns ▾

Baseline ▾ = 0 Cursor-Baseline ▾ = 80ns Time: 0 : 80ns



## Console - SimVision

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_b_tb.a full_adder_b_tb.b full_adder_b_tb.cin full_adder_b_tb.cout full_adder_b_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=         10 a=0 b=0 cin=1 sum=1 cout=0
Time=         20 a=0 b=1 cin=0 sum=1 cout=0
Time=         30 a=0 b=1 cin=1 sum=0 cout=1
Time=         40 a=1 b=0 cin=0 sum=1 cout=0
Time=         50 a=1 b=0 cin=1 sum=0 cout=1
Time=         60 a=1 b=1 cin=0 sum=0 cout=1
Time=         70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_b_tb.v:26  $finish;
ncsim>
```

Applications Places System na - File Browser buet@cadence:~/Docu... full\_adder\_na.v (~/Doc... 6:58 PM buet

full\_adder\_na.v (~/Documents/Simulation /full adder/na) - gedit

File Edit View Search Tools Documents Help

Open Save Undo | Cut Copy Find Find Next

full\_adder\_na.v X

```
module full_adder_na(a,b,cin,sum,cout);
    input a,b,cin;
    output sum,cout;
    wire [6:0]w;
    nand NA1(w[0],a,b);
    nand NA2(w[1],a,w[0]);
    nand NA3(w[2],b,w[0]);
    nand NA4(w[3],w[1],w[2]);
    nand NA5(w[4],w[3],cin);
    nand NA6(w[5],w[3],w[4]);
    nand NA7(w[6],cin,w[4]);
    nand NA8(sum,w[5],w[6]);
    nand NA9(cout,w[0],w[4]);
endmodule
```

Verilog Tab Width: 8 Ln 13, Col 30 INS

## full\_adder\_na\_tb.v (~/Documents/Simulation /full adder/na) - gedit

File Edit View Search Tools Documents Help



full\_adder\_na\_tb.v X

```
module full_adder_na_tb();
    reg a,b,cin;
    wire sum,cout;
    full_adder_na FA1(a,b,cin,sum,cout);
    initial
    begin
        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,cin,sum,cout);
    end
    initial
    begin
        #0; {a,b,cin}=3'd0;
        #10; {a,b,cin}=3'd1;
        #10; {a,b,cin}=3'd2;
        #10; {a,b,cin}=3'd3;
        #10; {a,b,cin}=3'd4;
        #10; {a,b,cin}=3'd5;
        #10; {a,b,cin}=3'd6;
        #10; {a,b,cin}=3'd7;
        #10;
        $finish;
    end
endmodule
```

Applications Places System

na - File Browser

buet@cadence:...

buet@cadence:...

NCLaunch : /ho...

Design Browser...

Waveform 1 - Si...



6:57 PM

buet

## Waveform 1 - SimVision

- □ ×

cadence™

File Edit View Explore Format Simulation Windows Help

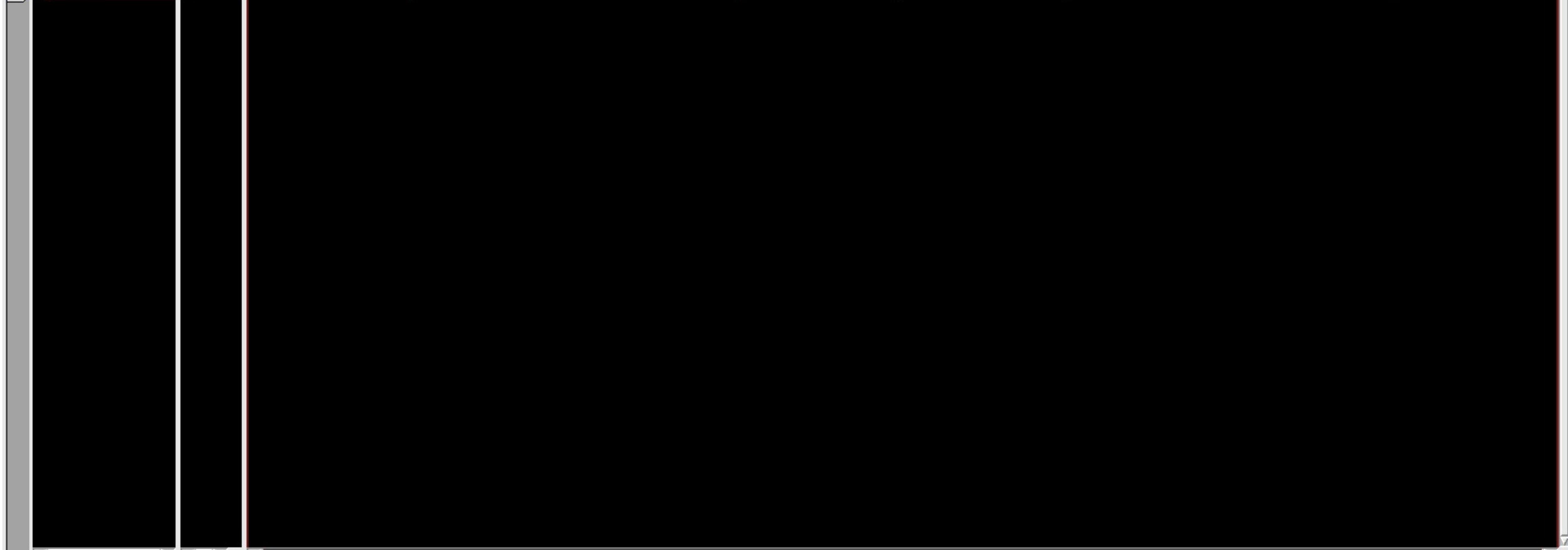


Search Names: Signal ▾ Search Times: Value ▾

TimeA ▾ = 80 ns Time: 0 : 80ns

Baseline ▾ = 0 Cursor-Baseline ▾ = 80ns

Name ▾ Cursor ▾



5 objects selected

Applications Places System na - File Bro... buet@cadence... buet@cadence... NCLaunch : /... Design Brow... Console - Si... Waveform 1 ... 6:57 PM buet

Console - SimVision

File Edit View Simulation Windows Help cadence

| Text Search: |

80ns + 0

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_na_tb.a full_adder_na_tb.b full_adder_na_tb.cin full_adder_na_tb.cout full_adder_na_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=         10 a=0 b=0 cin=1 sum=1 cout=0
Time=         20 a=0 b=1 cin=0 sum=1 cout=0
Time=         30 a=0 b=1 cin=1 sum=0 cout=1
Time=         40 a=1 b=0 cin=0 sum=1 cout=0
Time=         50 a=1 b=0 cin=1 sum=0 cout=1
Time=         60 a=1 b=1 cin=0 sum=0 cout=1
Time=         70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_na_tb.v:26      $finish;
ncsim>
```

Applications Places System no - File Browser full\_adder\_no.v (~/Doc... 7:11 PM buet

full\_adder\_no.v (~/Documents/Simulation /full adder/no) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace

full\_adder\_no.v X

```
module full_adder_no(a,b,cin,sum,cout);
    input a,b,cin;
    output sum,cout;
    wire [6:0]w;
    nor N01(w[0],a,b);
    nor N02(w[1],a,w[0]);
    nor N03(w[2],b,w[0]);
    nor N04(w[3],w[1],w[2]);
    nor N05(w[4],cin,w[3]);
    nor N06(w[5],cin,w[4]);
    nor N07(w[6],w[4],w[3]);
    nor N08(sum,w[5],w[6]);
    nor N09(cout,w[0],w[4]);
endmodule
```

Loading file '/home/buet/Documents/Simulation /full adder/no/full\_adder\_no.v'... Verilog Tab Width: 8 Ln 5, Col 21 INS

Applications Places System no - File Browser full\_adder\_no\_tb.v (~/...)

full\_adder\_no\_tb.v (~/Documents/Simulation /full adder/no) - gedit

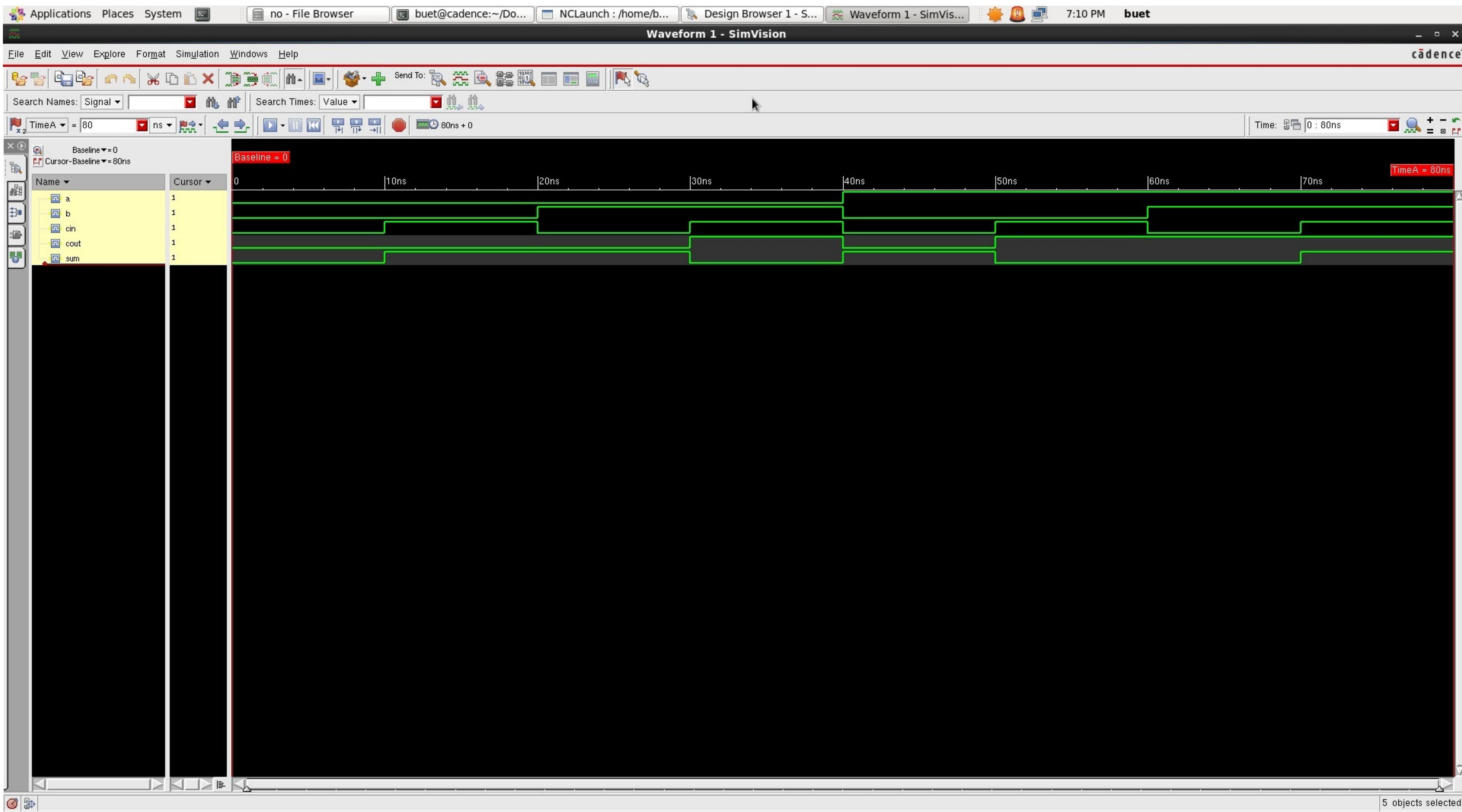
File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace

full\_adder\_no\_tb.v

```
module full_adder_no_tb();
    reg a,b,cin;
    wire sum,cout;
    full_adder_no FA1(a,b,cin,sum,cout);
    initial
    begin
        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,cin,sum,cout);
    end
    initial
    begin
        #0; {a,b,cin}=3'd0;
        #10; {a,b,cin}=3'd1;
        #10; {a,b,cin}=3'd2;
        #10; {a,b,cin}=3'd3;
        #10; {a,b,cin}=3'd4;
        #10; {a,b,cin}=3'd5;
        #10; {a,b,cin}=3'd6;
        #10; {a,b,cin}=3'd7;
        #10;
        $finish;
    end
endmodule
```

Loading file '/home/buet/Documents/Simulation /full adder/no/full\_adder\_no\_tb.v'... Verilog Tab Width: 8 Ln 6, Col 22 INS



Applications Places System no - File Browser buet@cadence:... NCLaunch : /ho... Design Browser ... Console - SimVi... Waveform 1 - Si... 7:10 PM buet

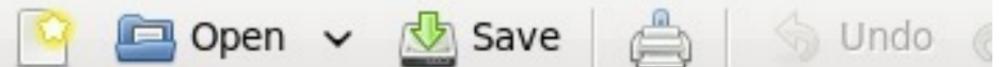
Console - SimVision

File Edit View Simulation Windows Help cadence

| Text Search: |

80ns + 0

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_no_tb.a full_adder_no_tb.b full_adder_no_tb.cin full_adder_no_tb.cout full_adder_no_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=         10 a=0 b=0 cin=1 sum=1 cout=0
Time=         20 a=0 b=1 cin=0 sum=1 cout=0
Time=         30 a=0 b=1 cin=1 sum=0 cout=1
Time=         40 a=1 b=0 cin=0 sum=1 cout=0
Time=         50 a=1 b=0 cin=1 sum=0 cout=1
Time=         60 a=1 b=1 cin=0 sum=0 cout=1
Time=         70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_no_tb.v:26      $finish;
ncsim>
```



half\_adder\_g.v

```
module half_adder_g(a,b,sum,cout);
    input a,b;
    output sum,cout;
    xor X1(sum,a,b);
    and A1(cout,a,b);
endmodule
```



File Edit View Search Tools Documents Help



Open



Save



Undo



half\_adder\_tb\_g.v



```
module half_adder_tb_g();

    reg a,b;
    wire sum,cout;

    half_adder_g HA1(a,b,sum,cout);

    initial
    begin

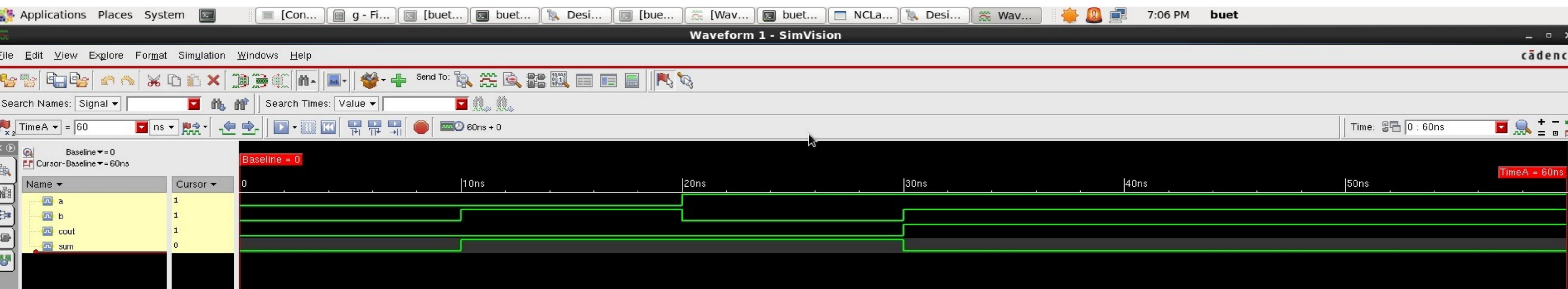
        #0; {a,b}= 2'd0;
        #10; {a,b}= 2'd1;
        #10; {a,b}= 2'd2;
        #10; {a,b}= 2'd3;
        #30;
        $finish;

    end

    initial
    begin

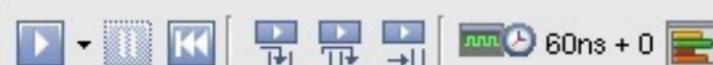
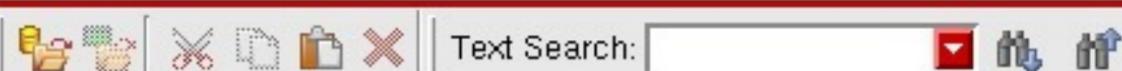
        $monitor("Time=%t a=%b b=%b sum=%b cout=%b",$time,a,b,sum,cout);

    end
endmodule
```



Applications Places System [Co... g - ... [bu... bue... Des... [bu...

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm half_adder_tb_g.a half_adder_tb_g.b half_adder_tb_g.cout half_adder_tb_g.sum
Created probe 1
ncsim> run
Time= 0 a=0 b=0 sum=0 cout=0
Time= 10 a=0 b=1 sum=1 cout=0
Time= 20 a=1 b=0 sum=1 cout=0
Time= 30 a=1 b=1 sum=0 cout=1
Simulation complete via $finish(1) at time 60 NS + 0
./half_adder_tb_g.v:16  $finish;
ncsim>
```

Applications Places System ha - File Browser buet@cadence:... buet@cadence:... buet@cadence:... buet@cadence:... full\_adder\_ha.v 10:06 PM buet

full\_adder\_ha.v (~/Documents/Simulation /full adder/ha) - gedit

File Edit View Search Tools Documents Help

Open Save Undo |

full\_adder\_ha.v

```
module full_adder_ha(a,b,cin,sum,cout);
    input a,b,cin;
    output sum,cout;
    wire [2:0]w;
    half_adder_g HA1(a,b,w[0],w[1]);
    half_adder_g HA2(w[0],cin,sum,w[2]);
    or O1(cout,w[1],w[2]);
endmodule
```

Applications Places System ha - File Browser buet@cadence:... buet@cadence:... buet@cadence:... buet@cadence:... full\_adder\_ha\_tb.v (~/Documents/Simulation /full adder/ha) - gedit 10:06 PM buet

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace

full\_adder\_ha\_tb.v

```
module full_adder_ha_tb();
    reg a,b,cin;
    wire sum,cout;
    full_adder_fa1 FA1(a,b,cin,sum,cout);
    initial
    begin
        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,cin,sum,cout);
    end
    initial
    begin
        #0; {a,b,cin}=3'd0;
        #10; {a,b,cin}=3'd1;
        #10; {a,b,cin}=3'd2;
        #10; {a,b,cin}=3'd3;
        #10; {a,b,cin}=3'd4;
        #10; {a,b,cin}=3'd5;
        #10; {a,b,cin}=3'd6;
        #10; {a,b,cin}=3'd7;
        #10;
        $finish;
    end
endmodule
```

Verilog Tab Width: 8 Ln 6, Col 22 INS

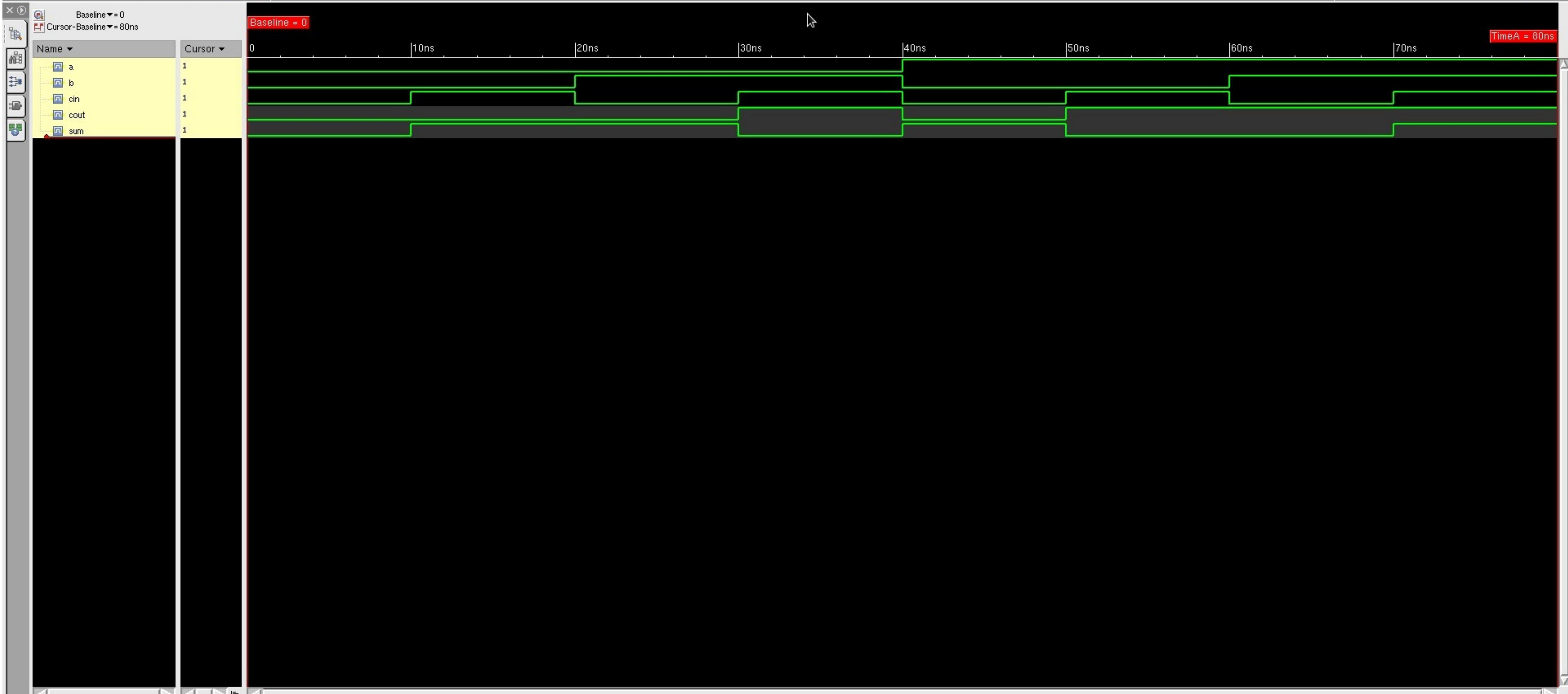
## Waveform 1 - SimVision

cadence

File Edit View Explore Format Simulation Windows Help



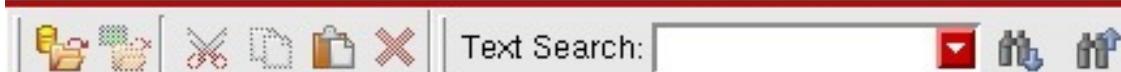
Search Names: Signal ▾ Search Times: Value ▾ Time: 0 : 80ns + 0



## Console - SimVision

cadence

File Edit View Simulation Windows Help

Text Search: 

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_ha_tb.a full_adder_ha_tb.b full_adder_ha_tb.cin full_adder_ha_tb.cout full_adder_ha_tb.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 cin=0 sum=0 cout=0
Time=        10 a=0 b=0 cin=1 sum=1 cout=0
Time=        20 a=0 b=1 cin=0 sum=1 cout=0
Time=        30 a=0 b=1 cin=1 sum=0 cout=1
Time=        40 a=1 b=0 cin=0 sum=1 cout=0
Time=        50 a=1 b=0 cin=1 sum=0 cout=1
Time=        60 a=1 b=1 cin=0 sum=0 cout=1
Time=        70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_ha_tb.v:26      $finish;
ncsim> n
```





Applications Places System



[bu]



File Edit View Search Tools Documents Help



Open ▾



Save



Undo



half\_subtractor\_g.v X

```
module half_subtractor_g(a,b,diff,bout);

    input a,b;
    output diff,bout;
    wire w;

    xor X1(diff,a,b);
    not N1(w,a);
    and A1(bout,w,b);

endmodule
```



File Edit View Search Tools Documents Help



Open



Save



Undo



half\_subtractor\_g\_tb.v



```
module half_subtractor_tb_g();

    reg a,b;
    wire diff,bout;

    half_subtractor_g HS1(a,b,diff,bout);

    initial
    begin

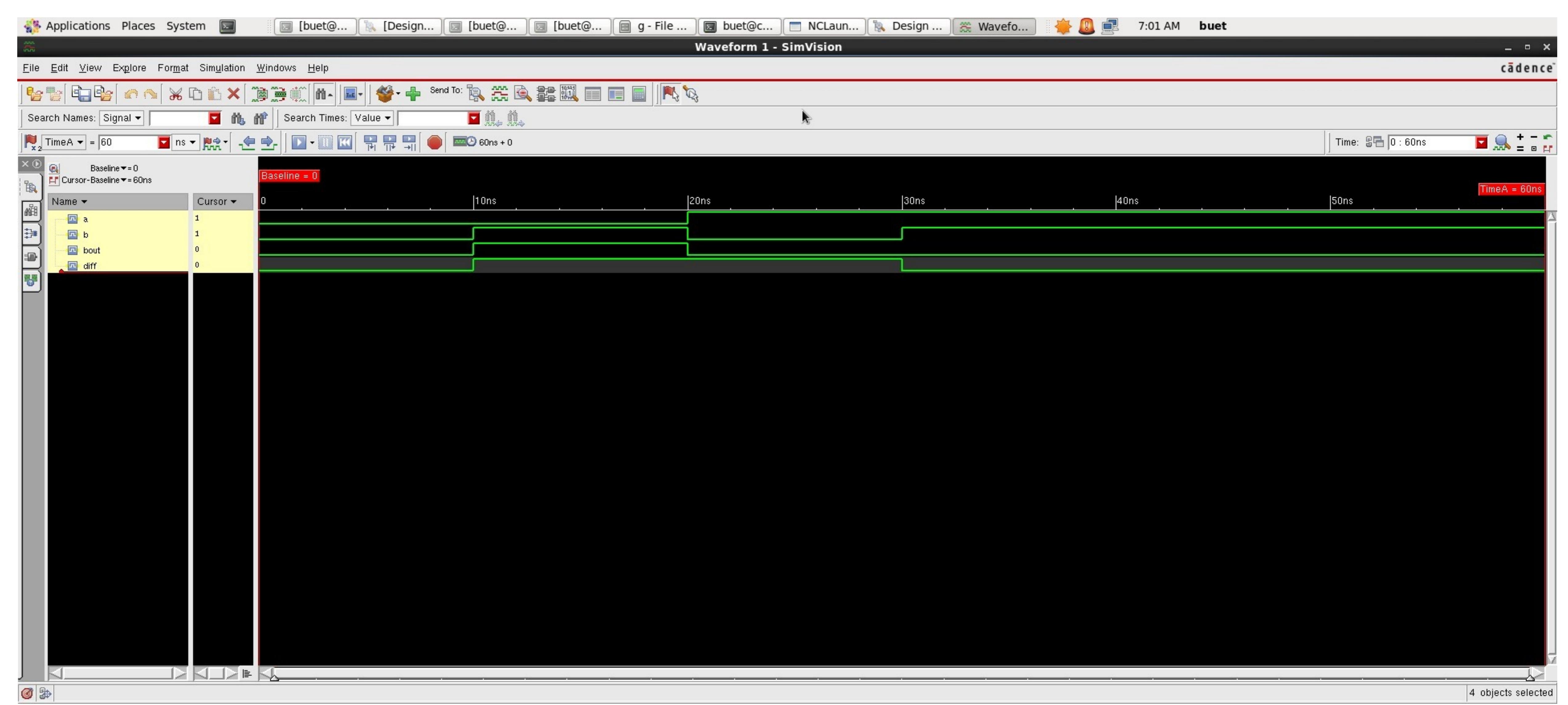
        #0; {a,b}= 2'd0;
        #10; {a,b}= 2'd1;
        #10; {a,b}= 2'd2;
        #10; {a,b}= 2'd3;
        #30;
        $finish;

    end

    initial
    begin

        $monitor("Time=%t a=%b b=%b diff=%b bout=%b",$time,a,b,diff,bout);

    end
endmodule
```



Applications Places System [buet...][Design...][buet...][buet...][g - Fil...][buet@...]

File Edit View Simulation Windows Help

[Text Search: ]

[Run] 60ns + 0

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm half_subtractor_tb_g.a half_subtractor_tb_g.b half_subtractor_tb_g.bout half_subtractor_tb_g.diff
Created probe 1
ncsim> run
Time=          0 a=0 b=0 diff=0 bout=0
Time=         10 a=0 b=1 diff=1 bout=1
Time=         20 a=1 b=0 diff=1 bout=0
Time=         30 a=1 b=1 diff=0 bout=0
Simulation complete via $finish(1) at time 60 NS + 0
./half_subtractor_g_tb.v:16      $finish;
ncsim>
```

Applications Places System hs - File Browser [buet@cadence:~/Doc... full\_adder\_hs.v (~/Doc...) 10:20 PM buet

full\_adder\_hs.v (~/Documents/Simulation /full adder/hs) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace

full\_adder\_hs.v X

```
module full_adder_hs(a,b,cin,sum,cout);
    input a,b,cin;
    output sum,cout;
    wire [4:0]w;
    not N1(w[0],a);
    half_subtractor_g HS1(w[0],b,w[1],w[2]);
    half_subtractor_g HS2(w[1],cin,w[3],w[4]);
    not N2(sum,w[3]);
    or O1(cout,w[2],w[4]);
endmodule
```

Loading file '/home/buet/Documents/Simulation /full adder/hs/full\_adder\_hs.v'... Verilog Tab Width: 8 Ln 5, Col 21 INS

## full\_adder\_hs\_tb.v (~/Documents/Simulation /full adder/hs) - gedit

File Edit View Search Tools Documents Help



full\_adder\_hs\_tb.v

```
module full_adder_hs_tb();
    reg a,b,cin;
    wire sum,cout;
    full_adder_hs FA1(a,b,cin,sum,cout);
    initial
    begin
        $monitor("Time=%t a=%b b=%b cin=%b sum=%b cout=%b",$time,a,b,cin,sum,cout);
    end
    initial
    begin
        #0; {a,b,cin}=3'd0;
        #10; {a,b,cin}=3'd1;
        #10; {a,b,cin}=3'd2;
        #10; {a,b,cin}=3'd3;
        #10; {a,b,cin}=3'd4;
        #10; {a,b,cin}=3'd5;
        #10; {a,b,cin}=3'd6;
        #10; {a,b,cin}=3'd7;
        #10;
        $finish;
    end
endmodule
```

Applications Places System

hs - File Browser

[buet@cadence:~/D...

NCLaunch : /home/b...

Design Browser 1 - S...

Waveform 1 - SimVis...

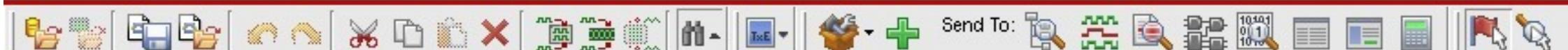
10:20 PM buet

## Waveform 1 - SimVision

- □ ×

cadence™

File Edit View Explore Format Simulation Windows Help

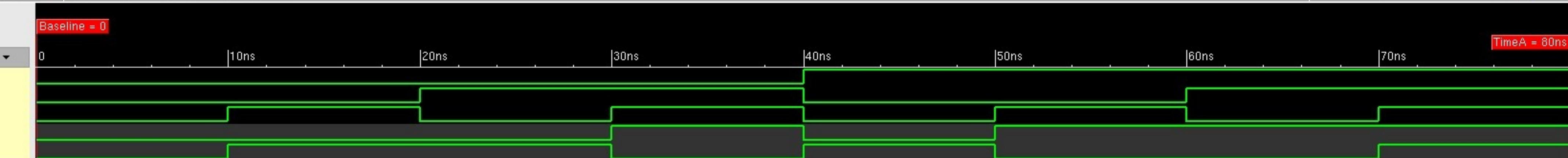


Search Names: Signal ▾ Search Times: Value ▾

TimeA ▾ = 80 ns

Time: 0 : 80ns

Baseline ▾ = 0  
Cursor-Baseline ▾ = 80ns



5 objects selected

Applications Places System hs - File Browser [buet@cadence... NCLaunch : /ho... Design Browser ... Console - SimVi... Waveform 1 - Si... 10:20 PM buet

Console - SimVision

File Edit View Simulation Windows Help cadence

| Text Search: |

80ns + 0

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm full_adder_hs_tb.a full_adder_hs_tb.b full_adder_hs_tb.cin full_adder_hs_tb.cout full_adder_hs_tb.sum
Created probe 1
ncsim> run
Time= 0 a=0 b=0 cin=0 sum=0 cout=0
Time= 10 a=0 b=0 cin=1 sum=1 cout=0
Time= 20 a=0 b=1 cin=0 sum=1 cout=0
Time= 30 a=0 b=1 cin=1 sum=0 cout=1
Time= 40 a=1 b=0 cin=0 sum=1 cout=0
Time= 50 a=1 b=0 cin=1 sum=0 cout=1
Time= 60 a=1 b=1 cin=0 sum=0 cout=1
Time= 70 a=1 b=1 cin=1 sum=1 cout=1
Simulation complete via $finish(1) at time 80 NS + 0
./full_adder_hs_tb.v:26      $finish;
ncsim>
```

half\_adder\_hs.v (~/Documents/Simulation /Halfadder/hs) - gedit

File Edit View Search Tools Documents Help

Open Save Undo | Cut Copy Paste Find Replace

half\_adder\_hs.v

```
module half_adder_hs(a,b,sum,cout);
    input a,b;
    output sum,cout;
    wire [1:0]w;
    not N1(w[0],b);
    half_subtractor_g HA1(a,w[0],w[1],cout);
    not N2(sum,w[1]);
endmodule
```

Verilog Tab Width: 8 Ln 9, Col 15 INS

half\_adder\_tb\_hs.v (~/Documents/Simulation /Halfadder/hs) - gedit

File Edit View Search Tools Documents Help

Open Save Undo | Cut Copy Paste Find Replace

half\_adder\_tb\_hs.v X

```
module half_adder_tb_hs();
    reg a,b;
    wire sum,cout;
    half_adder_hs HA1(a,b,sum,cout);

    initial
    begin
        #0; {a,b} = 2'd0;
        #10; {a,b} = 2'd1;
        #10; {a,b} = 2'd2;
        #10; {a,b} = 2'd3;
        #30;
        $finish;
    end

    initial
    begin
        $monitor("Time=%t a=%b b=%b sum=%b cout=%b", $time, a, b, sum, cout);
    end
endmodule
```

Loading file '/home/buet/Documents/Simulation /Halfadder/hs/half\_adder\_tb\_hs.v'...

Verilog Tab Width: 8 Ln 18, Col 12 INS

## Waveform 1 - SimVision

x

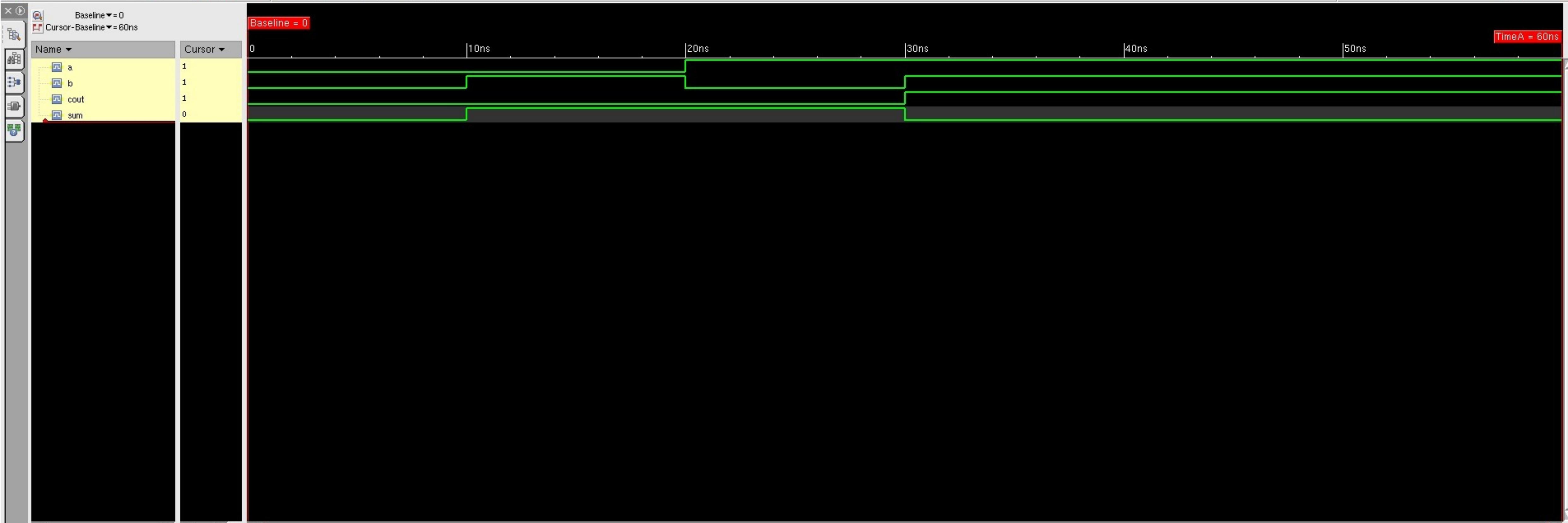
File Edit View Explore Format Simulation Windows Help

cadence



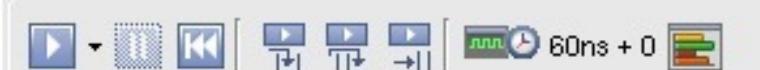
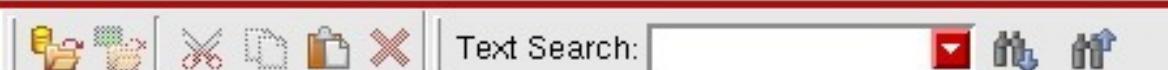
Search Names: Signal ▾ | Search Times: Value ▾

TimeA ▾ = 60 ns ▾ | Time: 0 : 60ns



## Console - SimVision

File Edit View Simulation Windows Help



```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm half_adder_tb_hs.a half_adder_tb_hs.b half_adder_tb_hs.cout half_adder_tb_hs.sum
Created probe 1
ncsim> run
Time=          0 a=0 b=0 sum=0 cout=0
Time=         10 a=0 b=1 sum=1 cout=0
Time=         20 a=1 b=0 sum=1 cout=0
Time=         30 a=1 b=1 sum=0 cout=1
Simulation complete via $finish(1) at time 60 NS + 0
./half_adder_tb_hs.v:16      $finish;
ncsim>
```