







#### File Edit View Search Tools Documents





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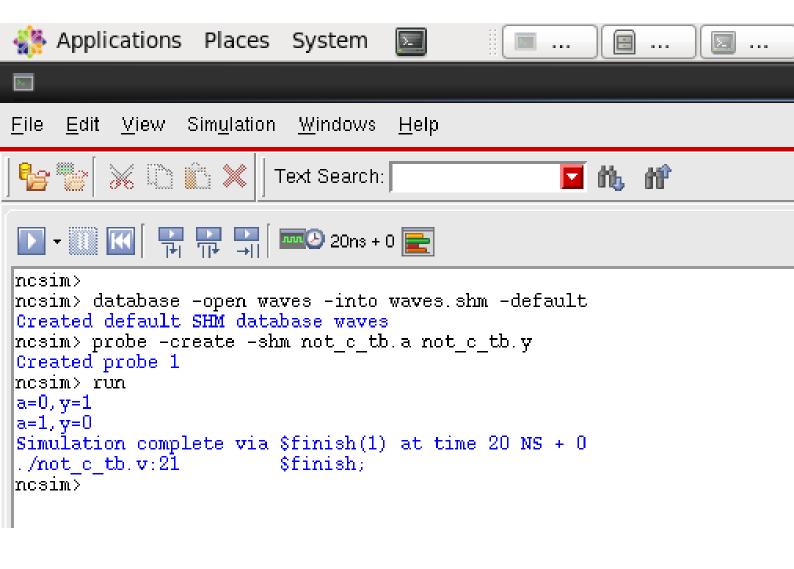
not c.v 💥

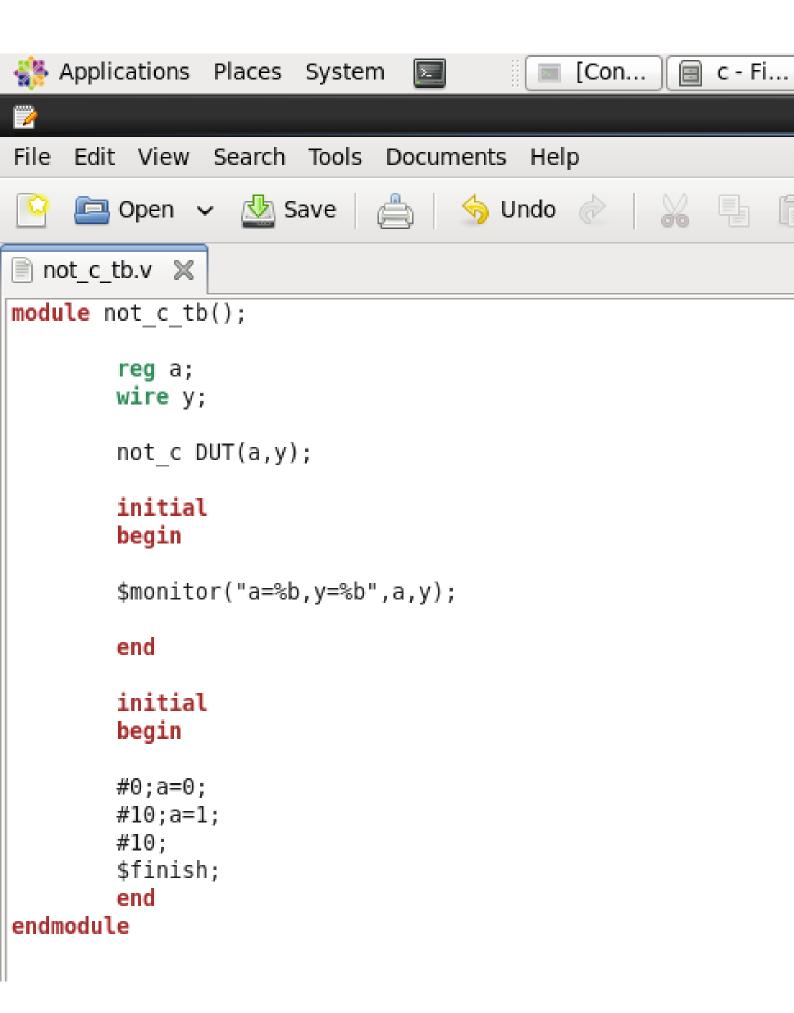


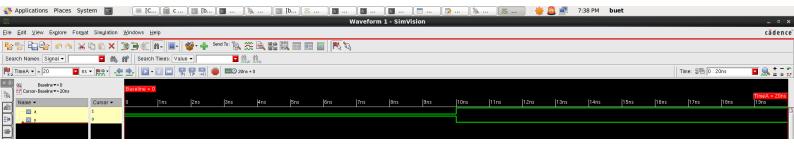
```
module not c(a,y);
```

```
input a;
output y;
supply1 vdd;
supply0 vss;
```

```
pmos P1(y,vdd,a);
        nmos N1(y,vss,a);
endmodule
```















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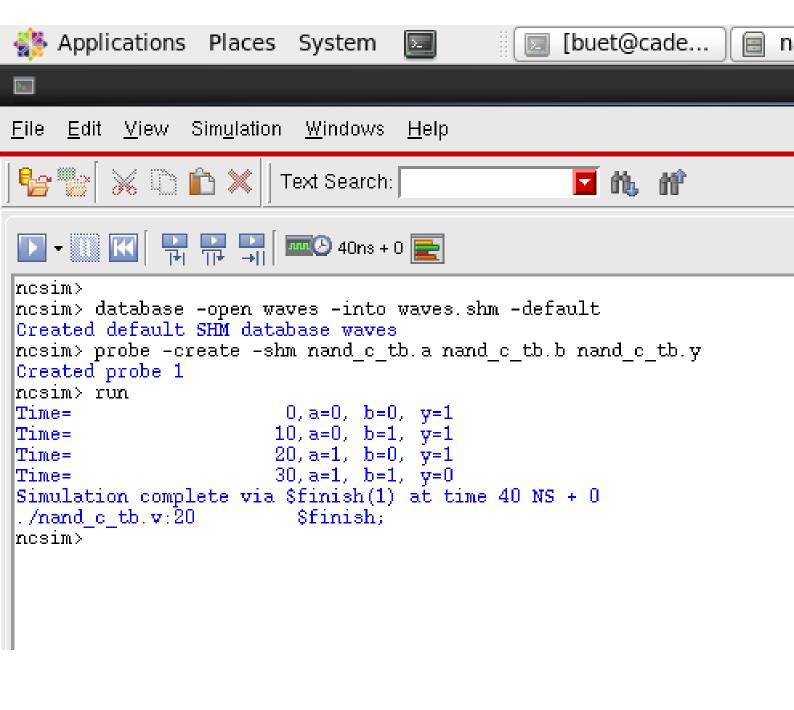


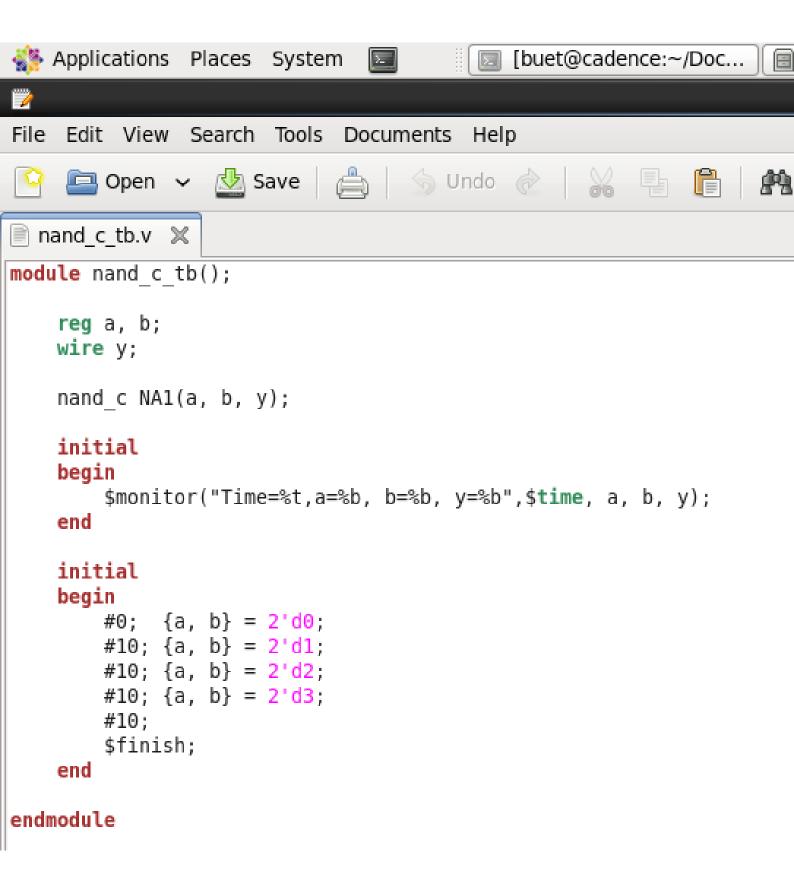


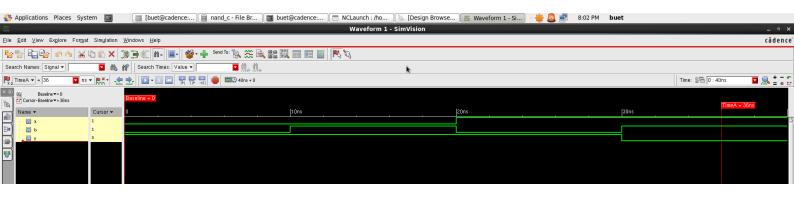
nand c.v 💥

```
module nand c(a,b,y);
```

```
input a,b;
output y;
supply1 vdd;
supply0 vss;
wire w;
pmos P1(y,vdd,a);
pmos P2(y,vdd,b);
nmos N1(w,vss,b);
nmos N2(y,w,a);
```

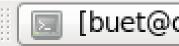














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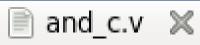
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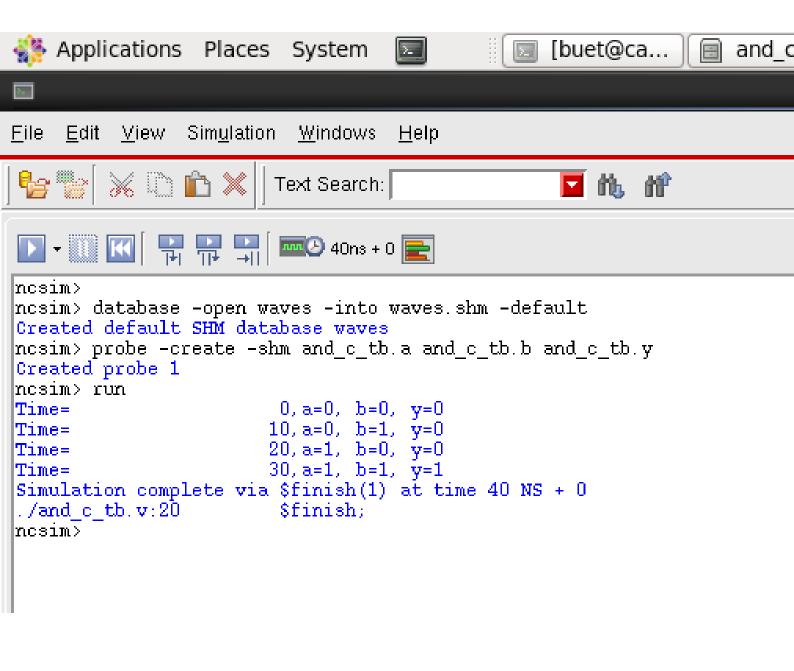


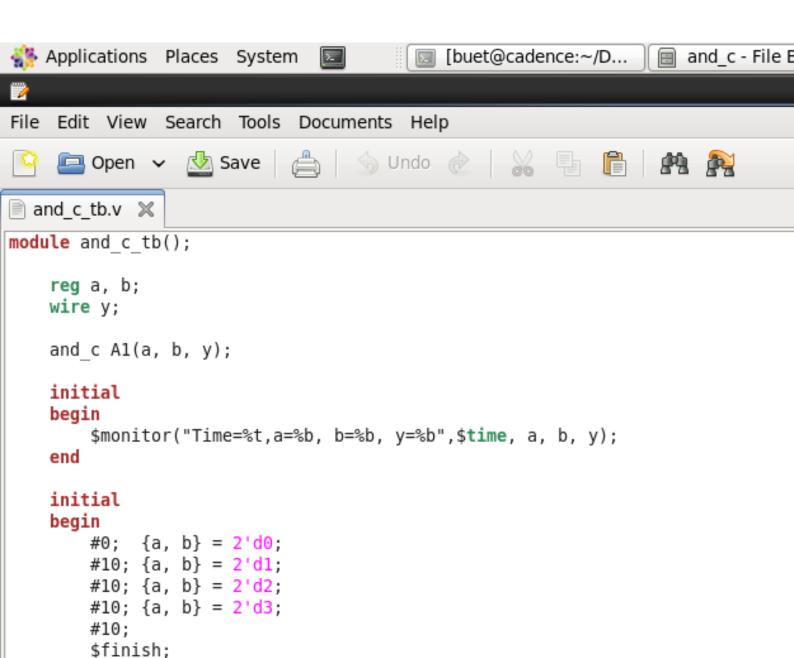




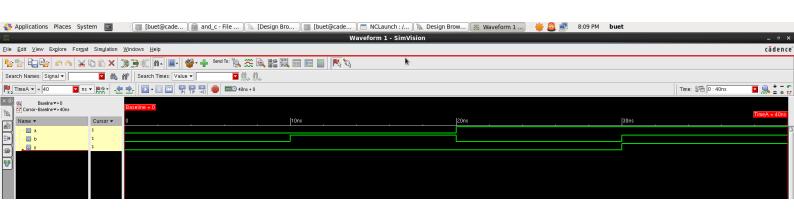


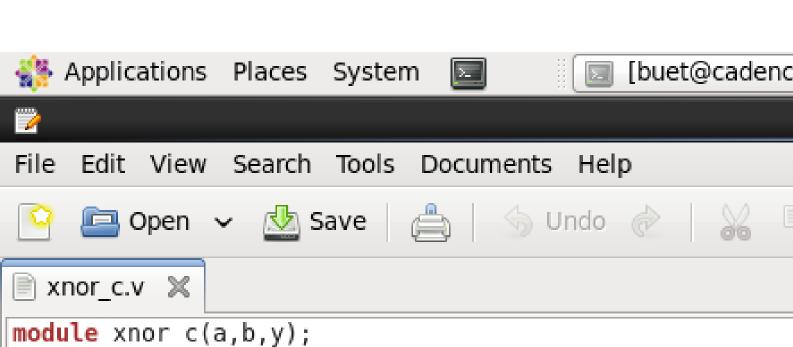
```
module and c(a,b,y);
        input a,b;
        output y;
        wire w;
        nand c NA1(a,b,w);
        not c NOT1(w,y);
```



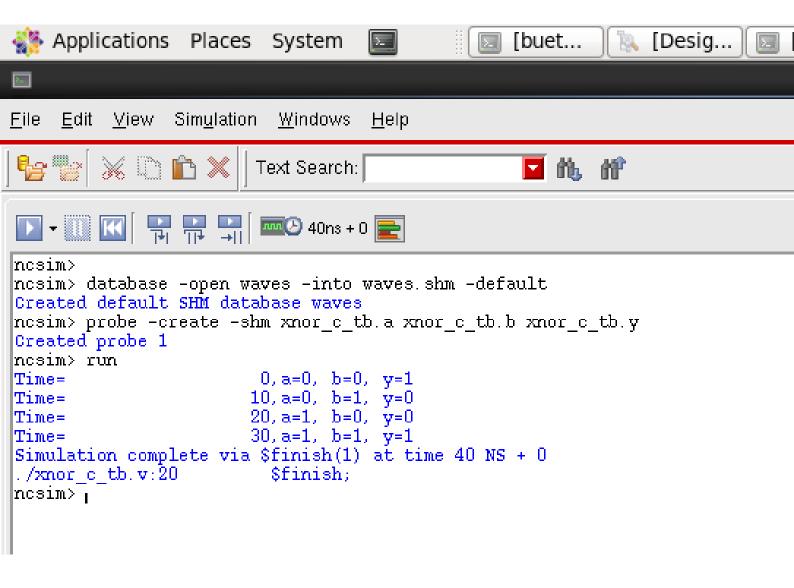


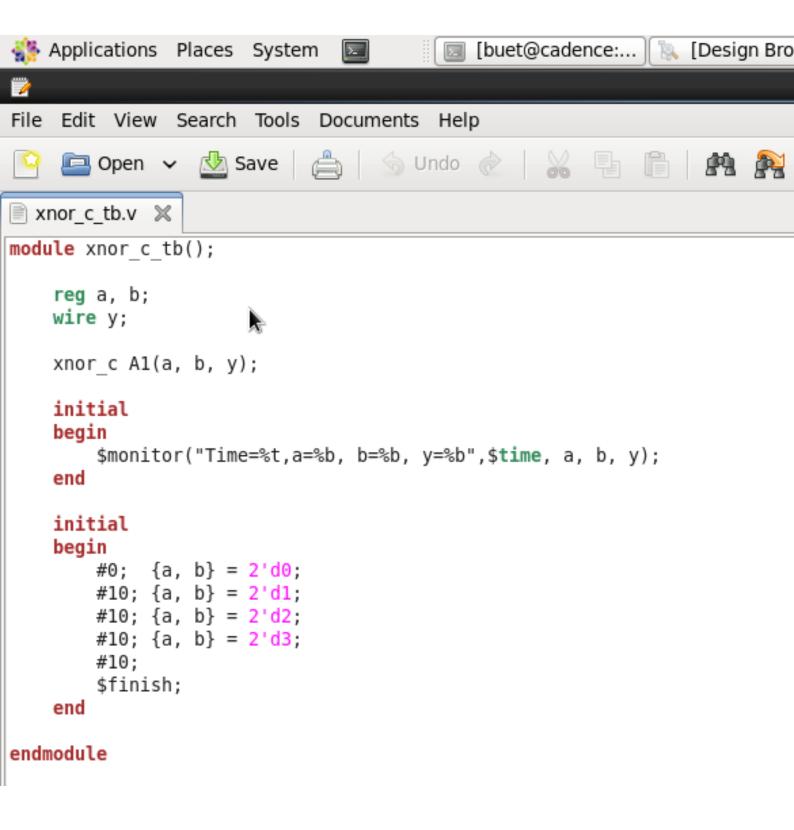
end

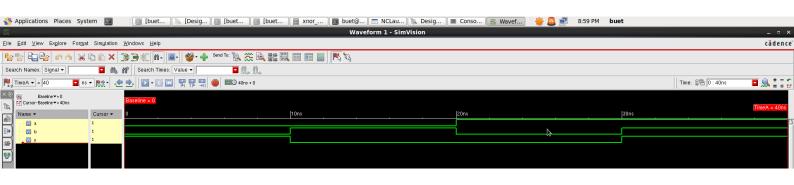




```
input a,b;
        output y;
        supply1 vdd;
        supplyθ vss;
        wire [4:0]w;
        not c NOT1(a,w[0]);
        not c NOT2(b,w[1]);
        pmos P1(w[2],vdd,w[0]);
        pmos P2(w[2], vdd, b);
        pmos P3(y,w[2],w[1]);
        pmos P4(y,w[2],a);
        nmos N1(y,w[3],b);
        nmos N2(w[3],vss,w[0]);
        nmos N3(y,w[4],w[1]);
        nmos N4(w[4],vss,a);
endmodule
```















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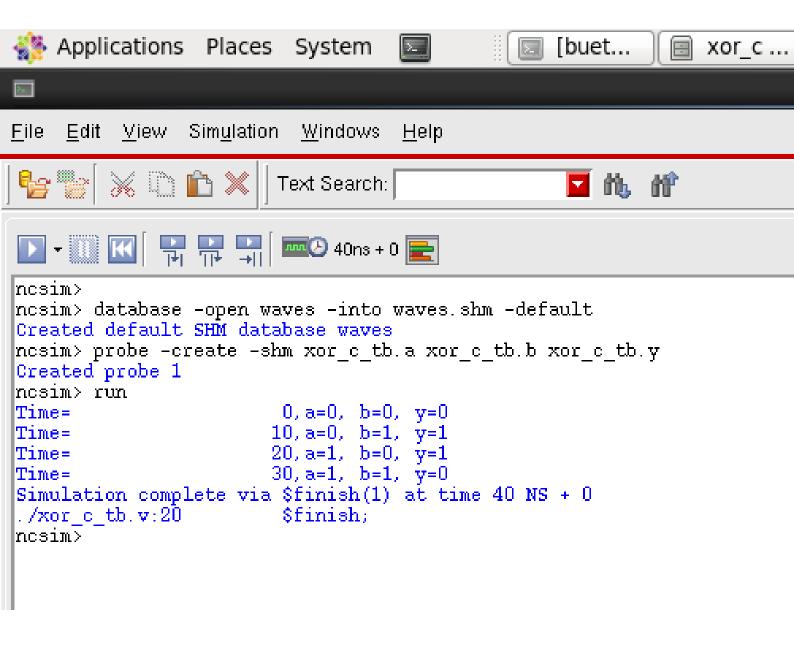


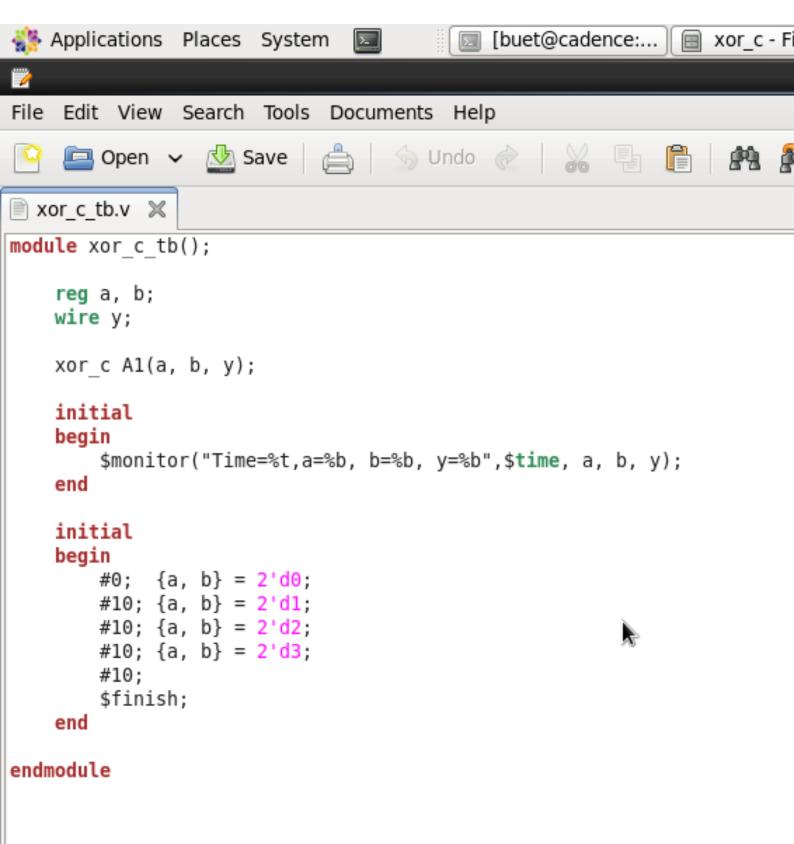
```
module xor c(a,b,y);
```

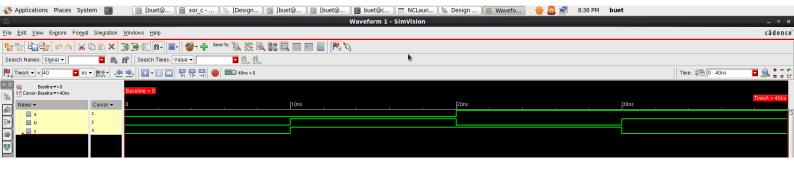
```
input a,b;
output y;
wire w;
```

```
xnor c XN1(a,b,w);
not c NOT1(w,y);
```



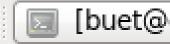














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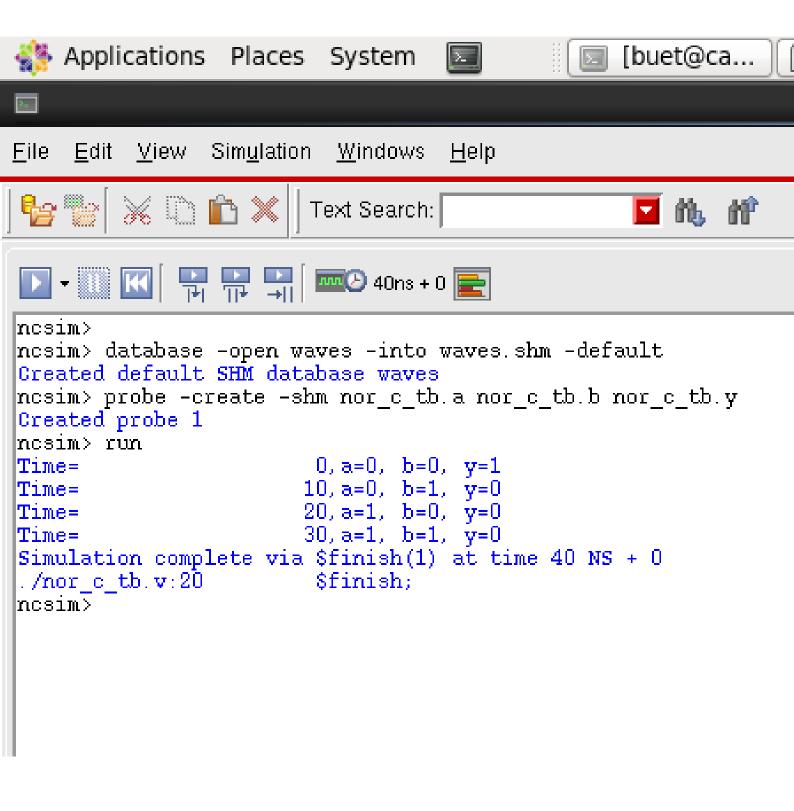


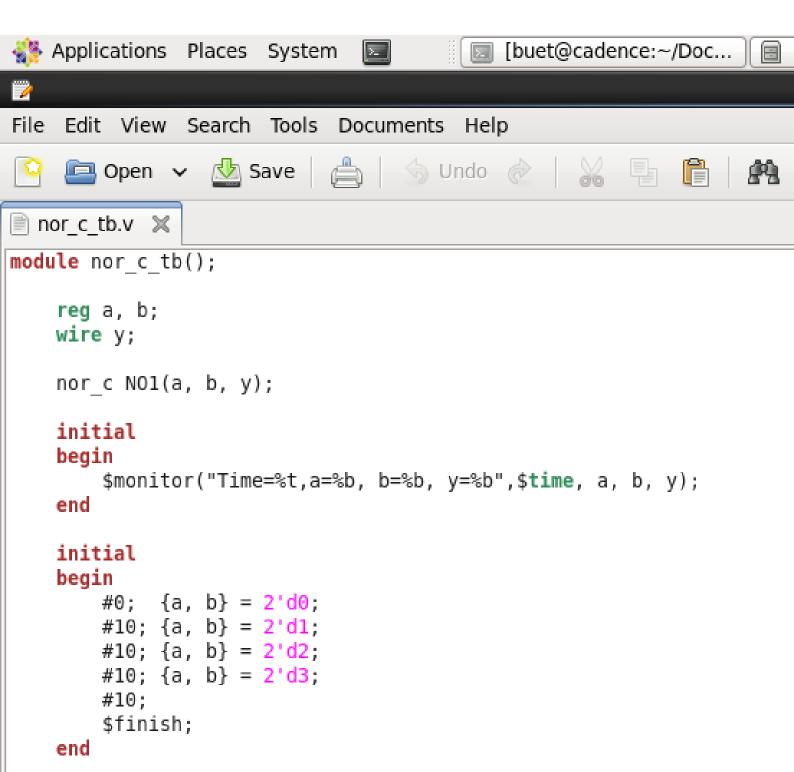


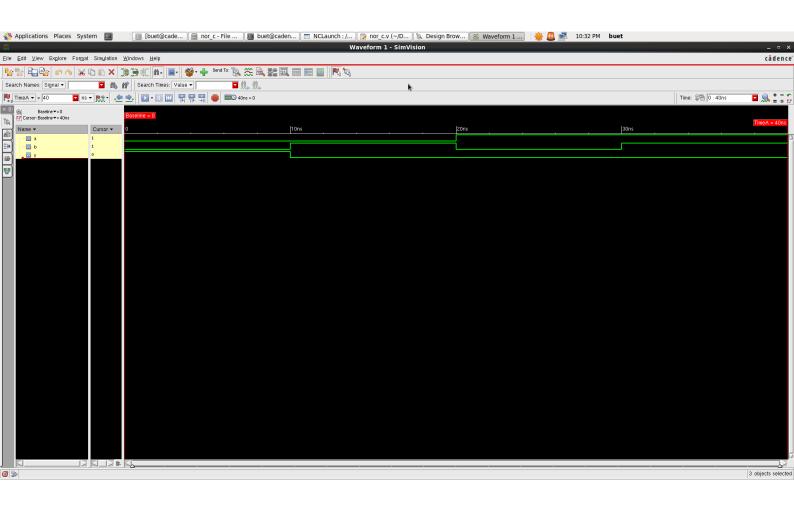




```
module nor c(a,b,y);
        input a,b;
        output y;
        wire w;
        supply1 vdd;
        supply0 vss;
        pmos P1(w,vdd,a);
        pmos P2(y,w,b);
        nmos N1(y,vss,a);
        nmos N2(y,vss,b);
endmodule
```















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or c.v 💥

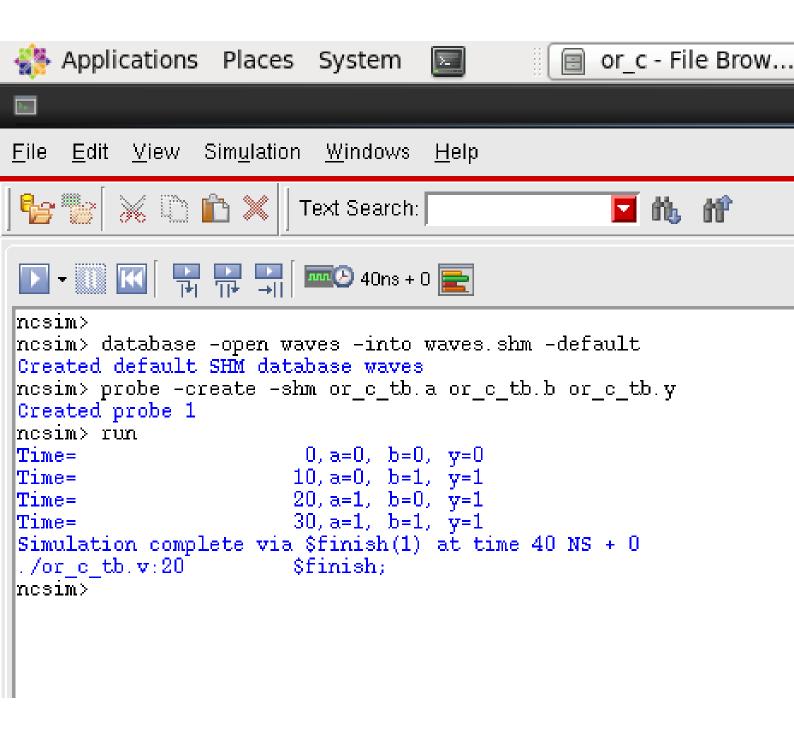


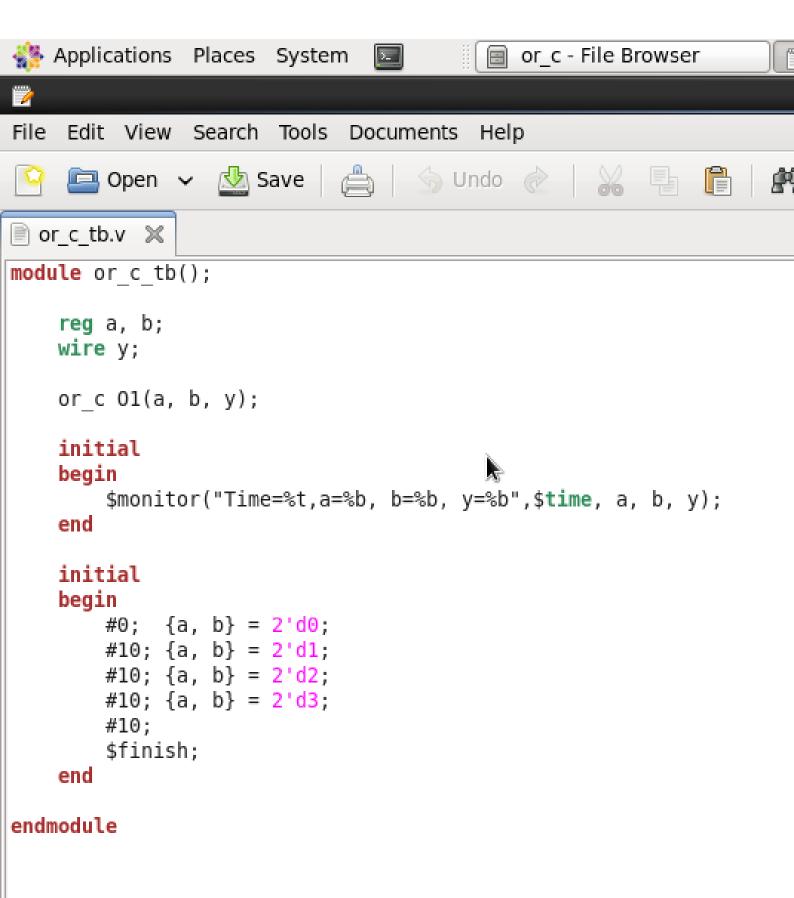
```
module or c(a,b,y);
```

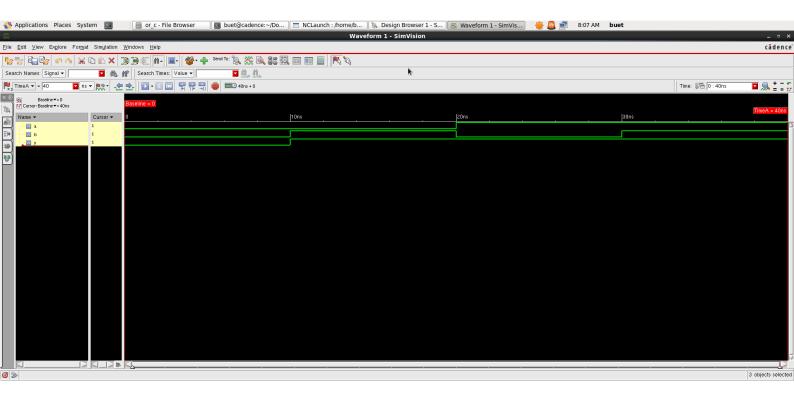
```
input a,b;
output y;
wire w;
```

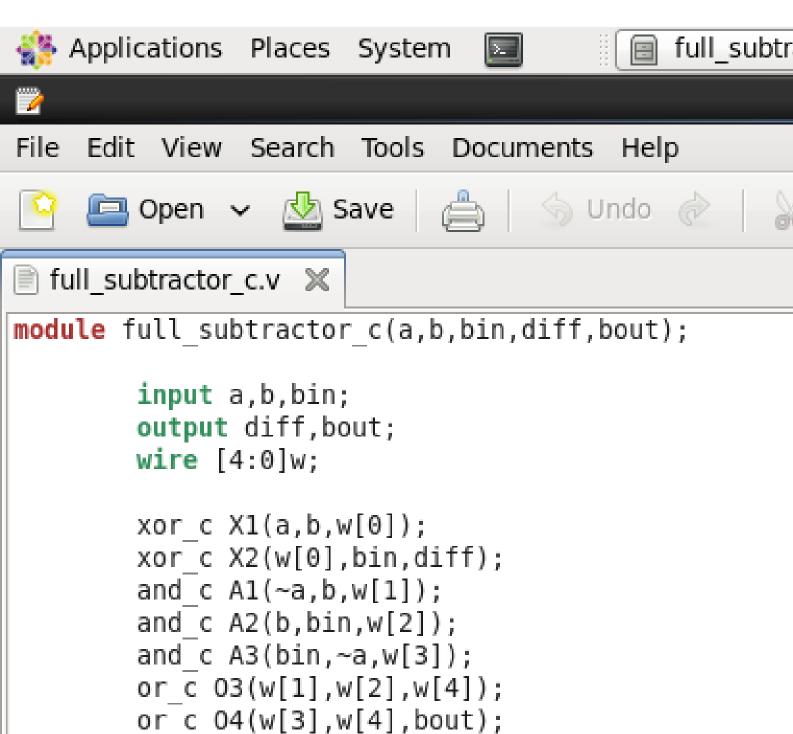
```
nor c N01(a,b,w);
not c N1(w,y);
```

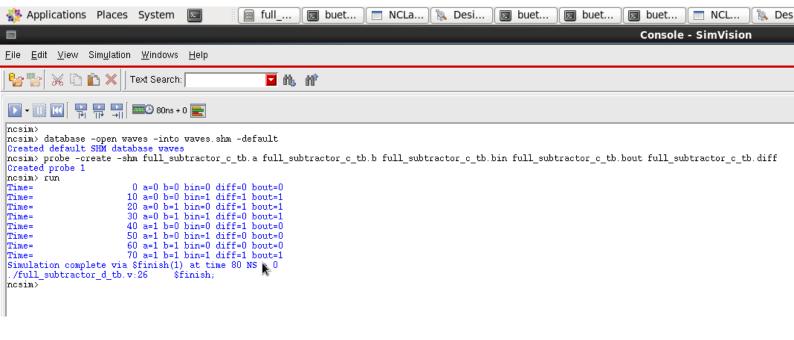


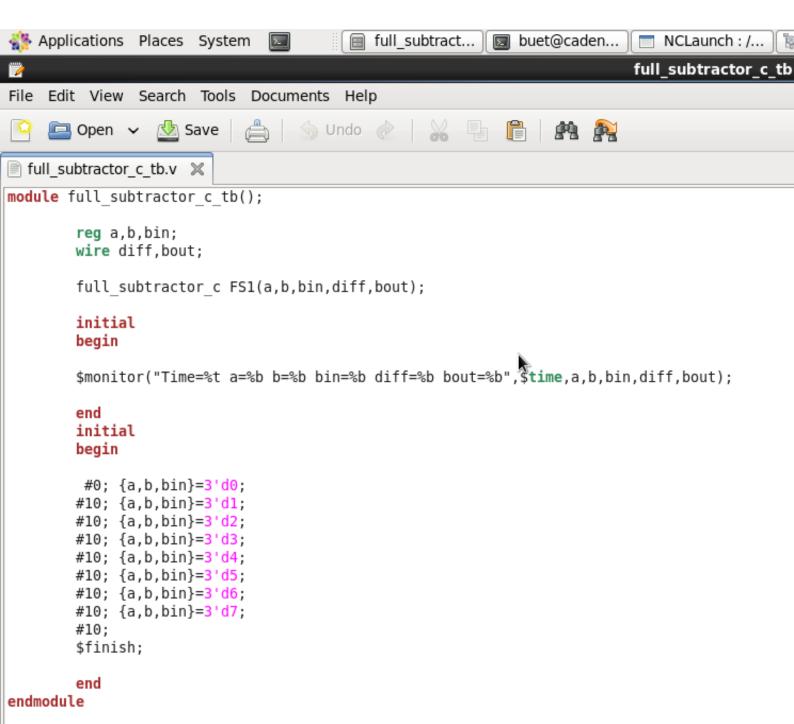


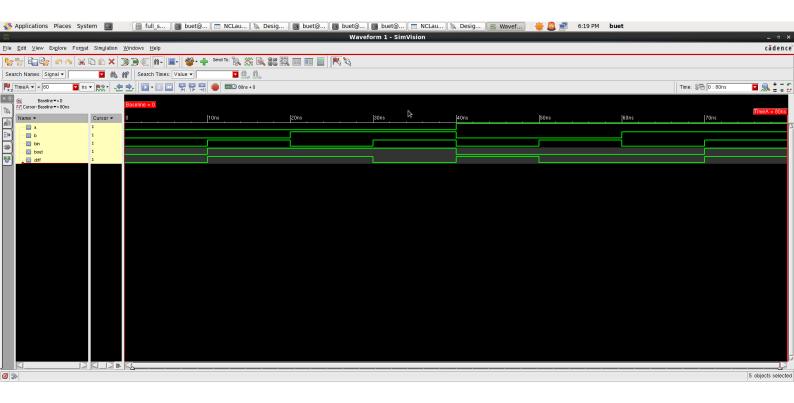


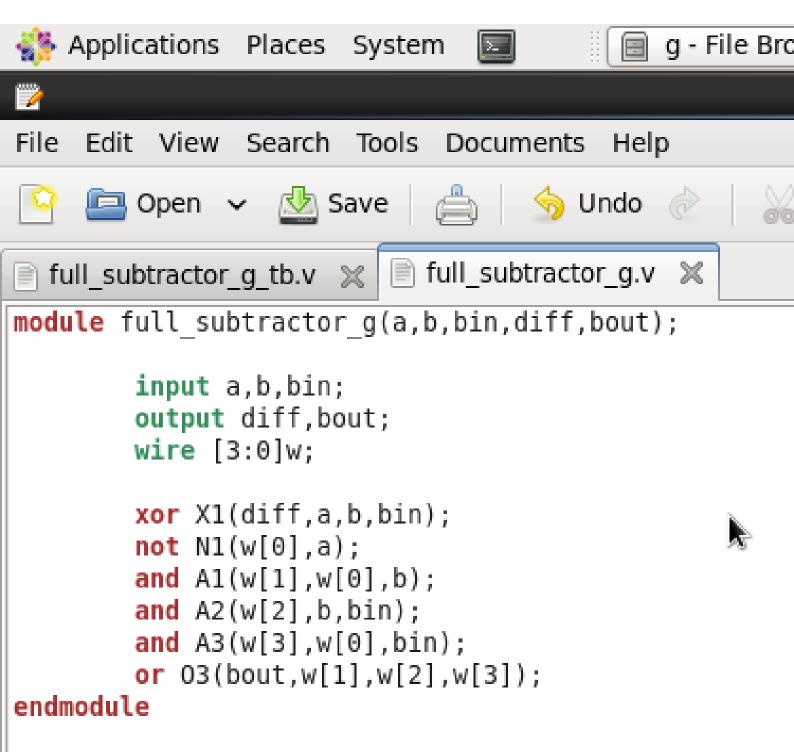


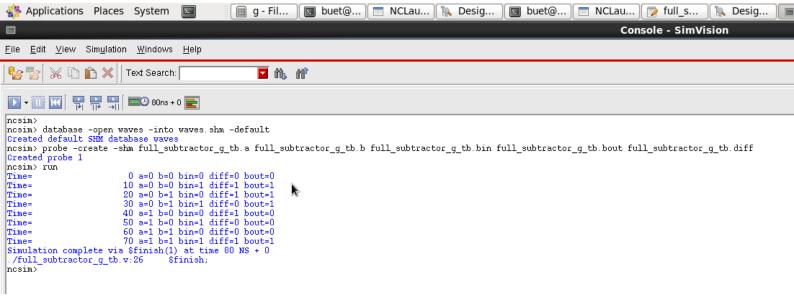


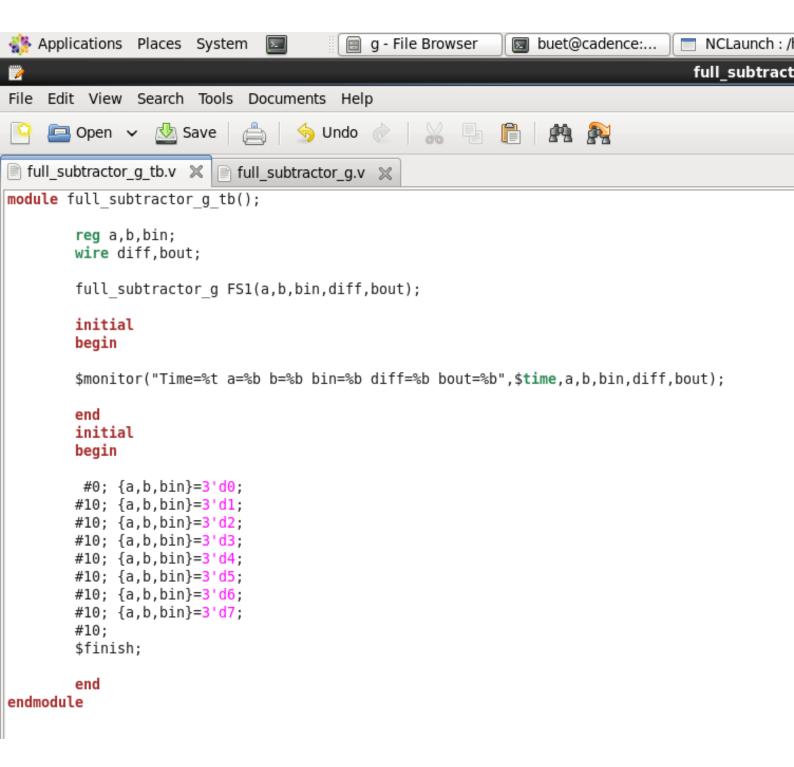


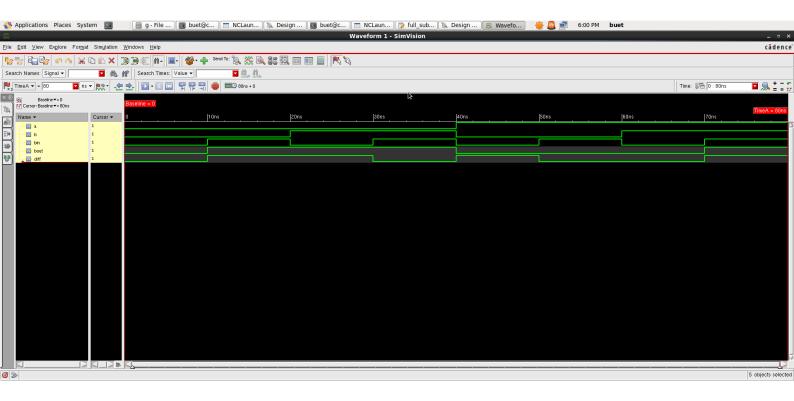


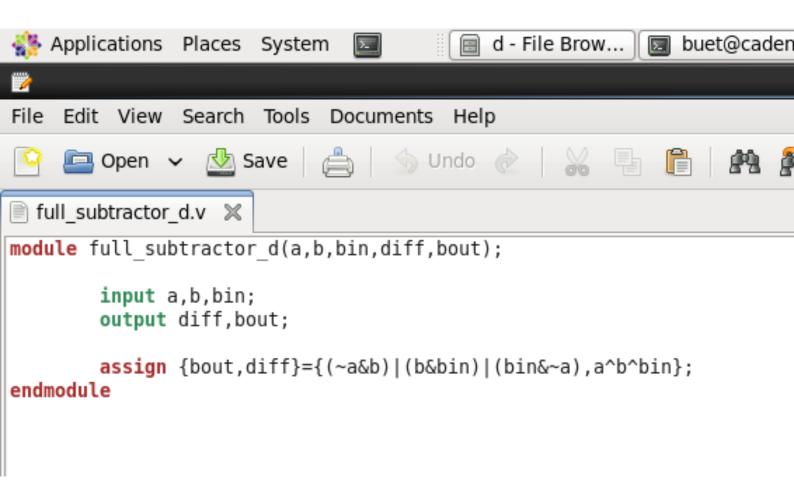


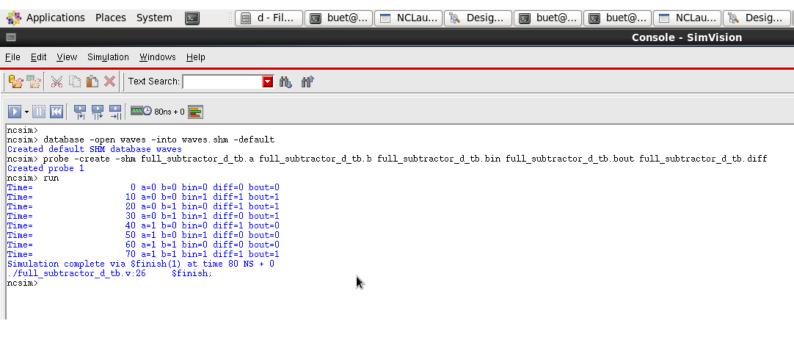


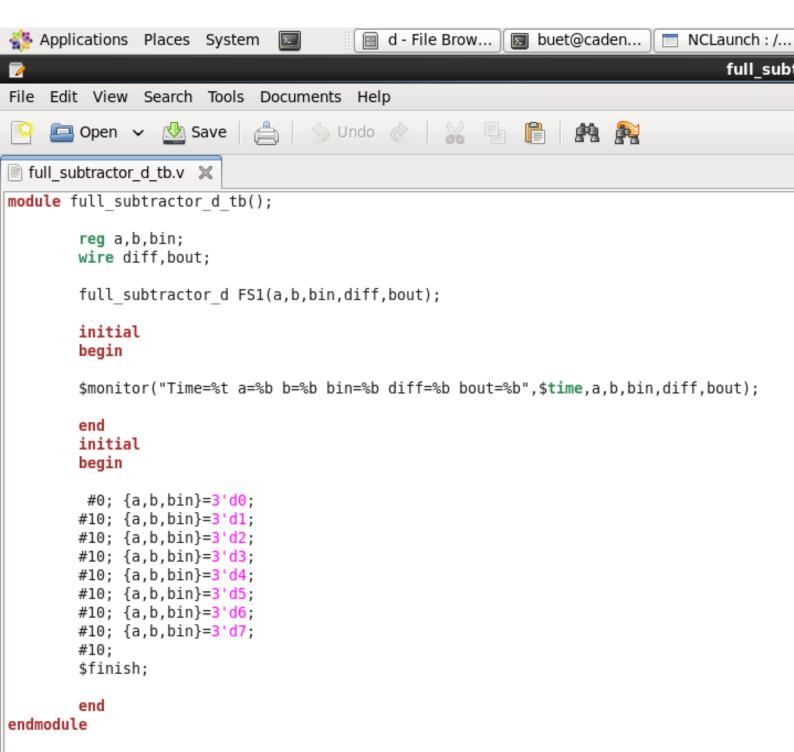


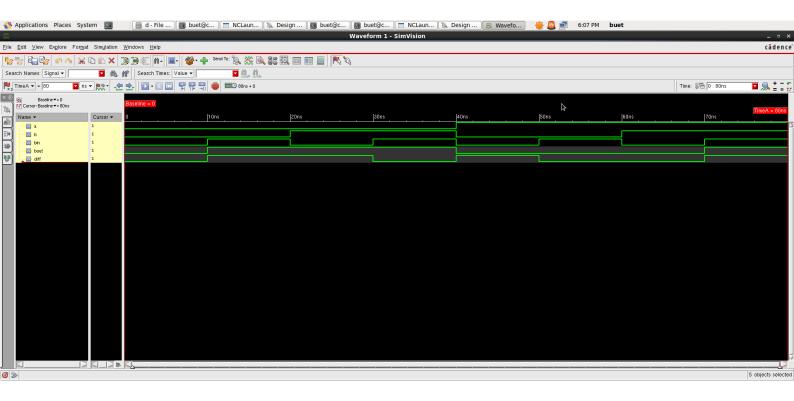


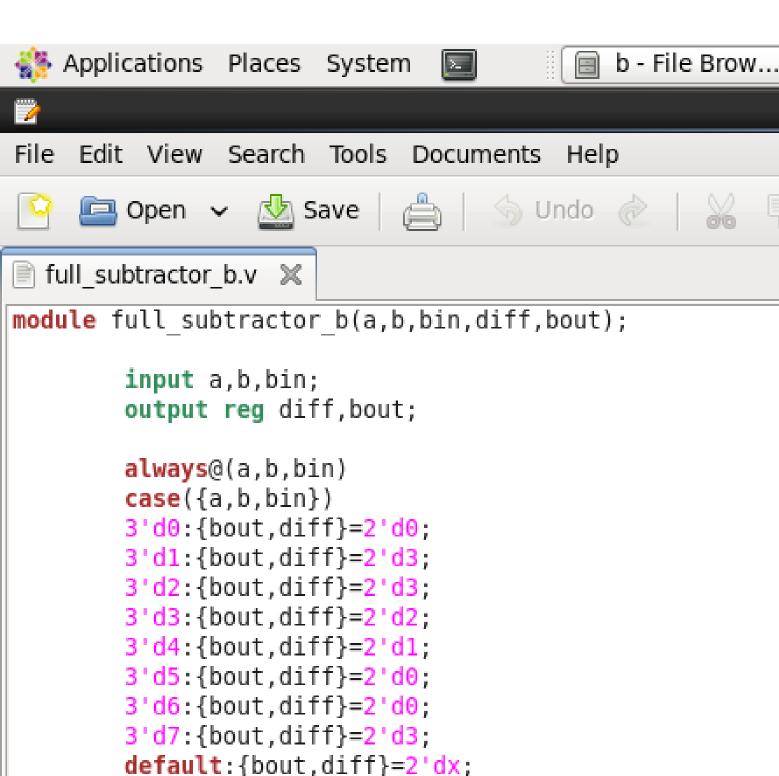






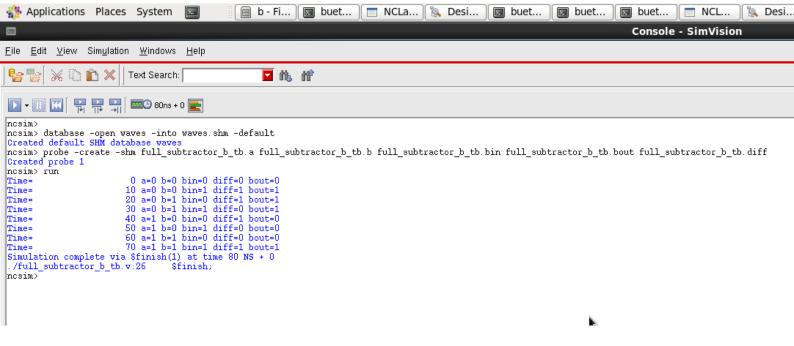


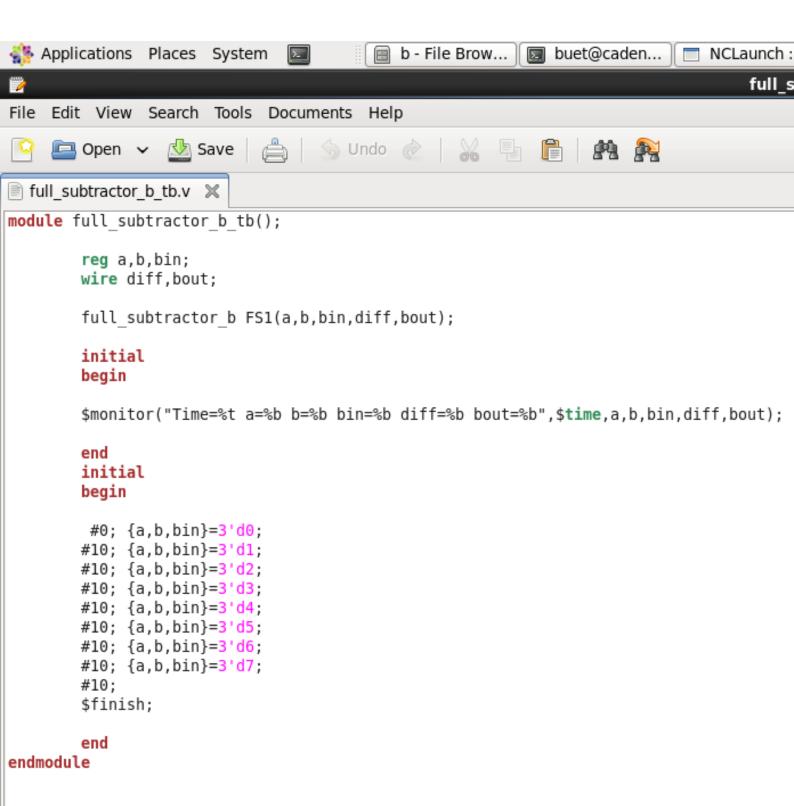


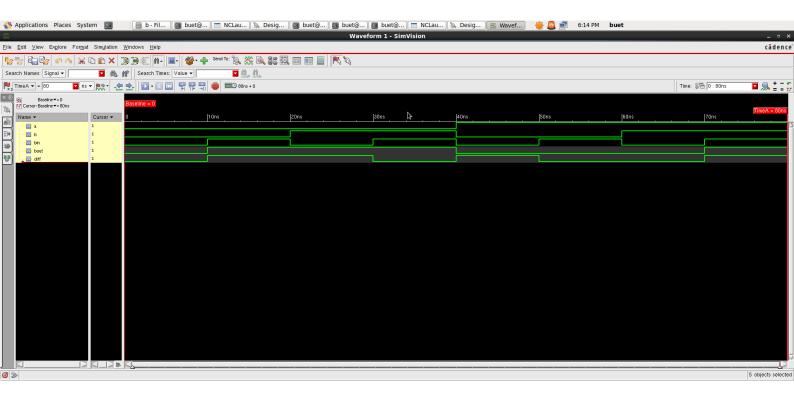


endcase

endmodule









## Applications Places System







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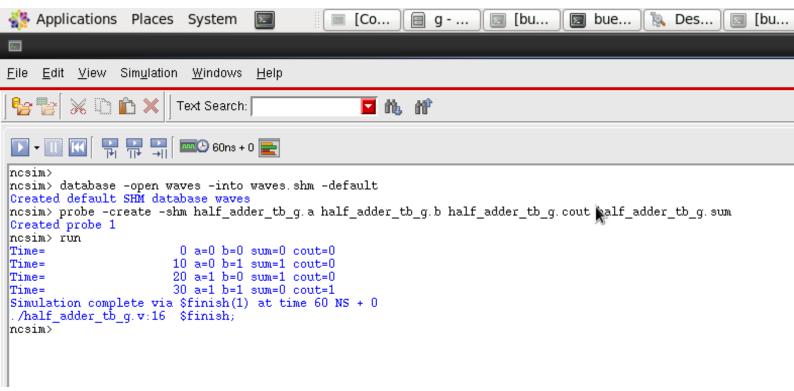


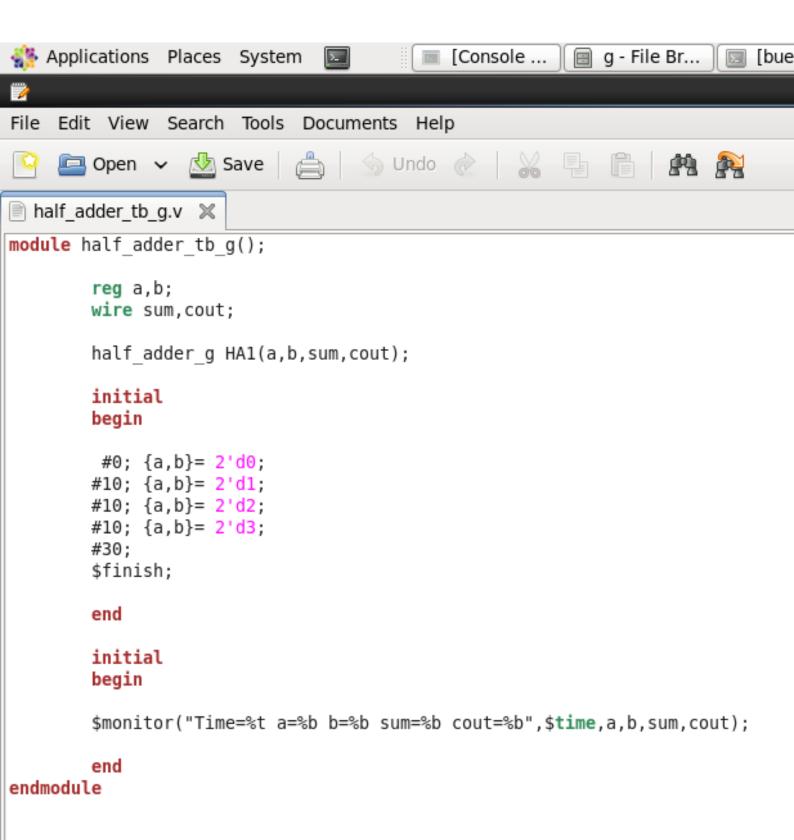
🖹 half adder g.v 💥

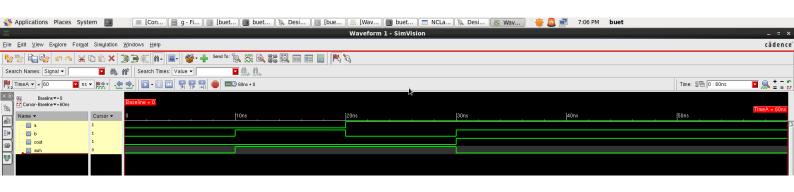
```
module half_adder_g(a,b,sum,cout);
        input a,b;
        output sum,cout;
```

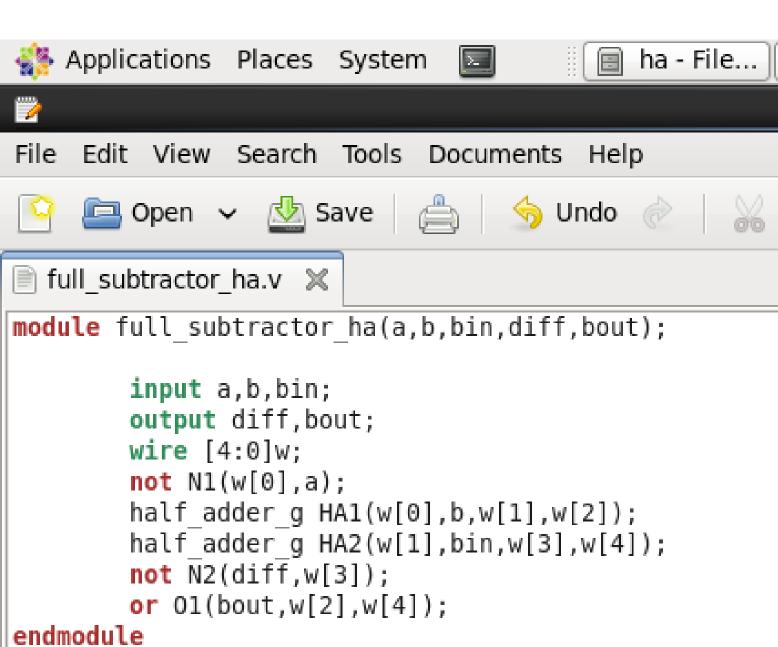
xor X1(sum,a,b); and A1(cout,a,b);

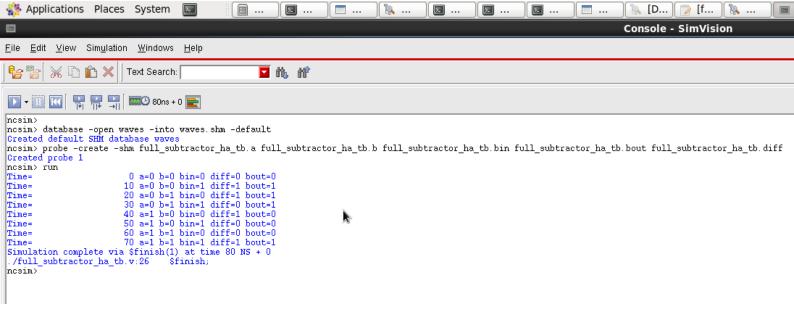
endmodule

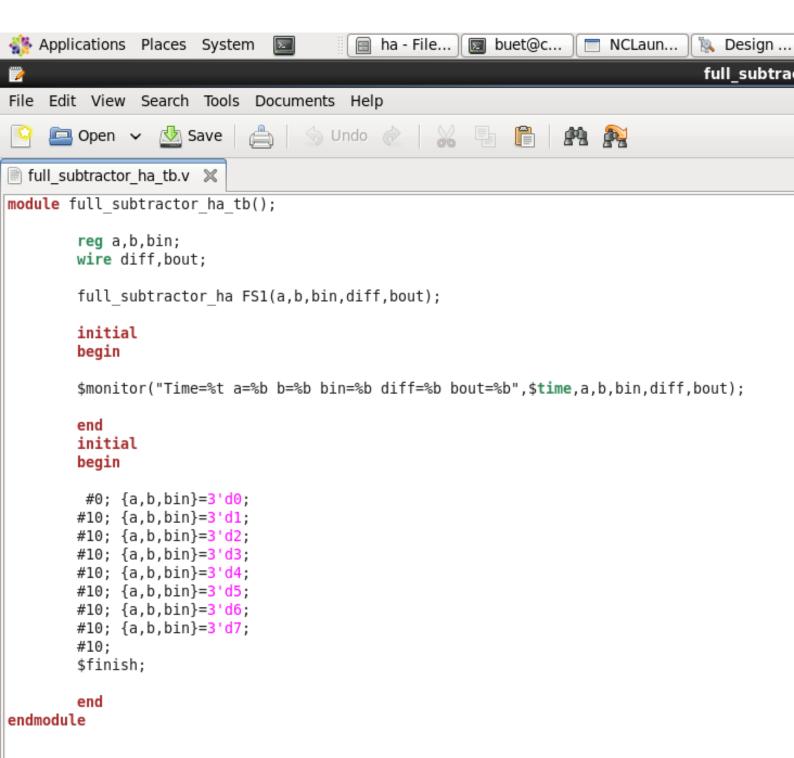


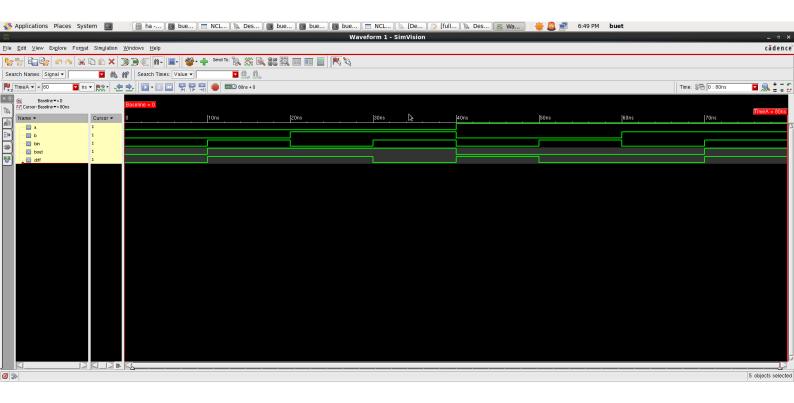














## Applications Places System







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half subtractor g.v 💥



```
module half subtractor g(a,b,diff,bout);
```

```
input a,b;
output diff,bout;
wire w;
xor X1(diff,a,b);
not N1(w,a);
```

and A1(bout,w,b);

endmodule

