





#### Edit View Search Tools Documents File



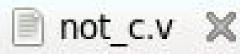








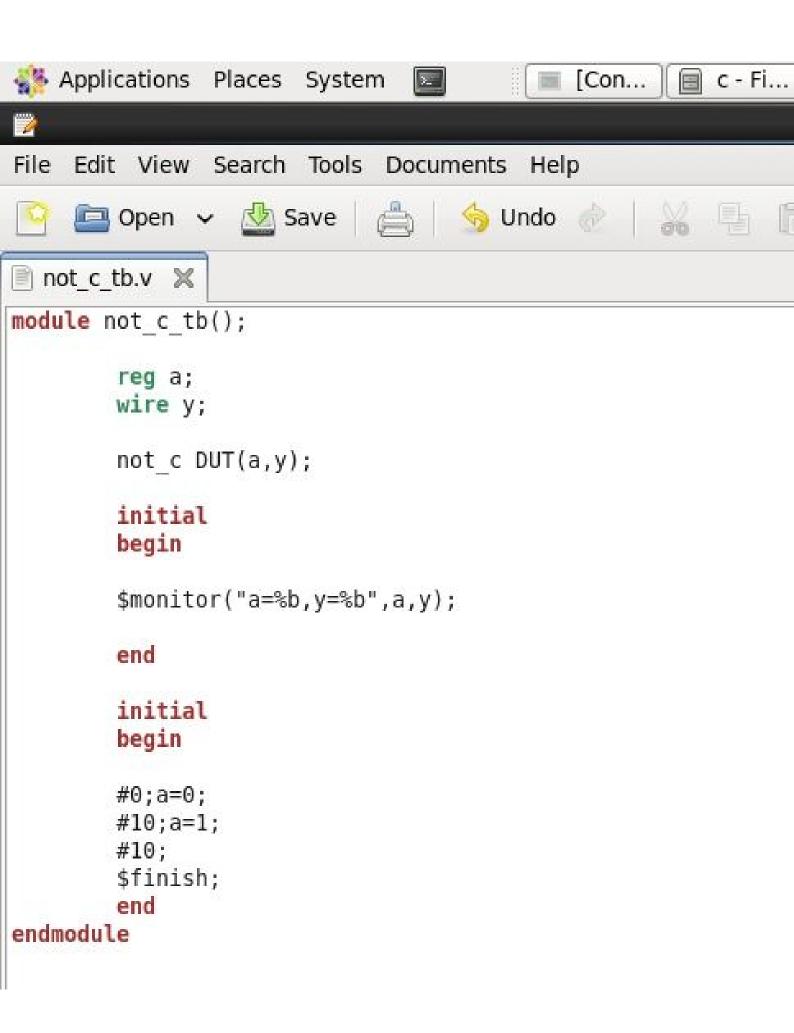


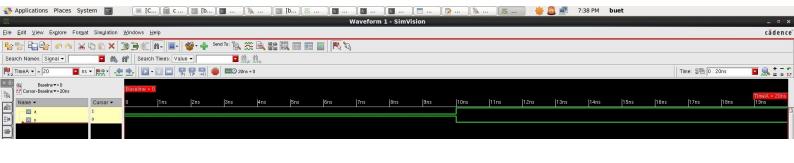


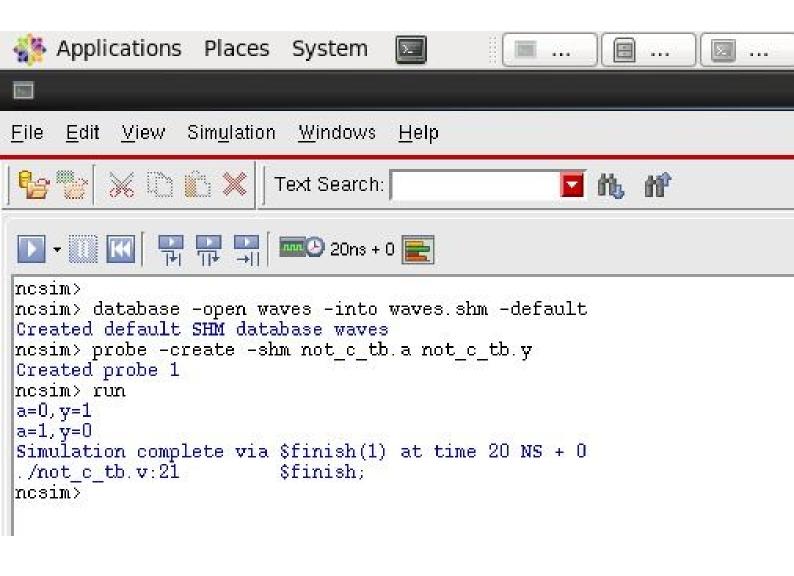
```
module not c(a,y);
```

```
input a;
output y;
supply1 vdd;
supplyθ vss;
```

```
pmos P1(y,vdd,a);
nmos N1(y, vss,a);
```

















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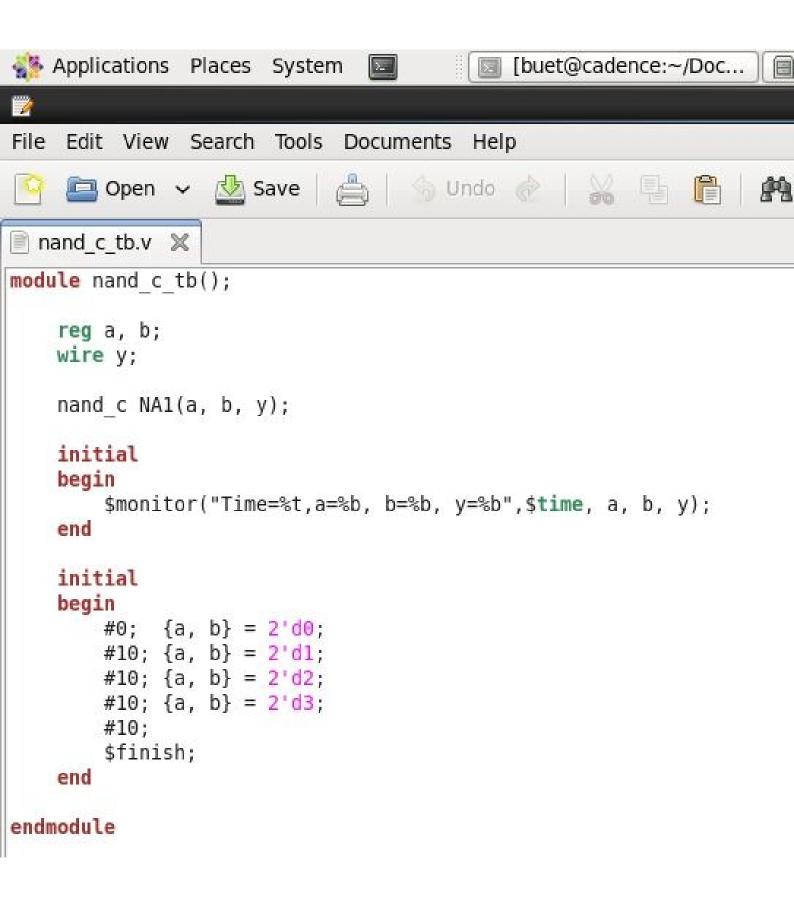


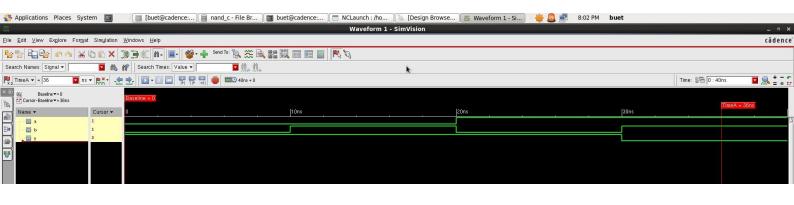


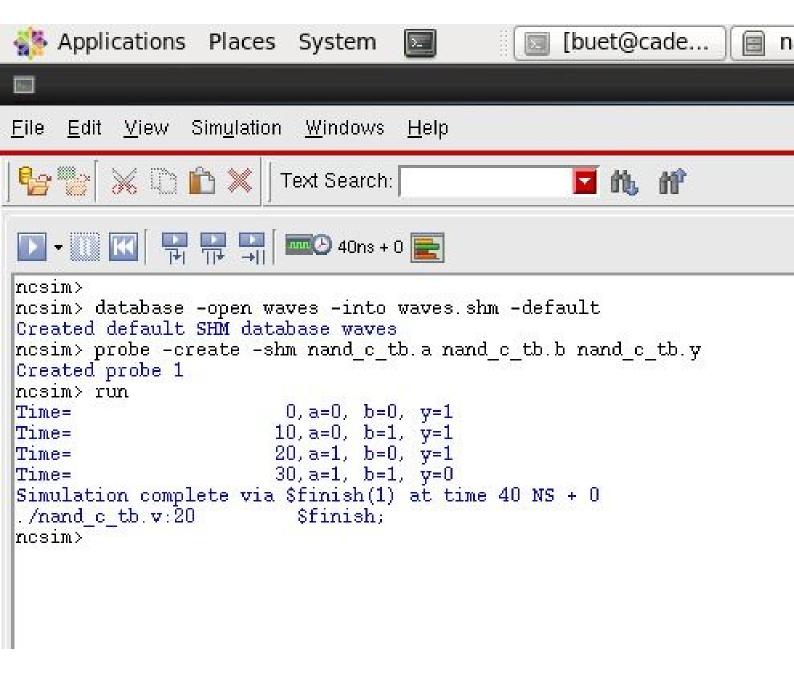
nand c.v 💥

```
module nand c(a,b,y);
```

```
input a,b;
output y;
supply1 vdd;
 supplyθ vss;
wire w;
pmos P1(y,vdd,a);
 pmos P2(y,vdd,b);
 nmos N1(w,vss,b);
 nmos N2(y,w,a);
```

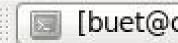














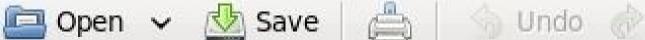
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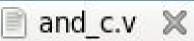




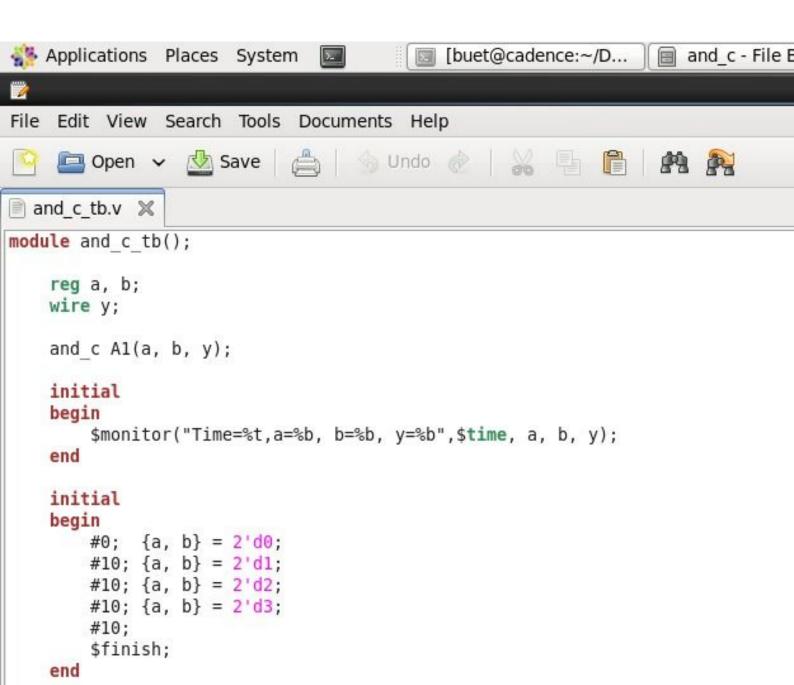


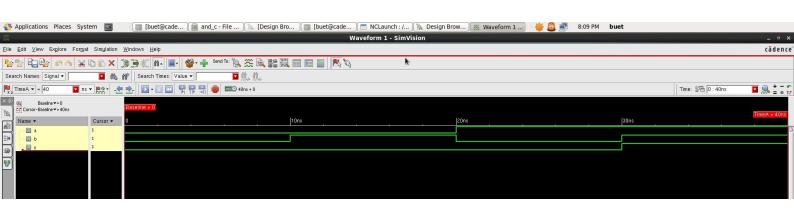


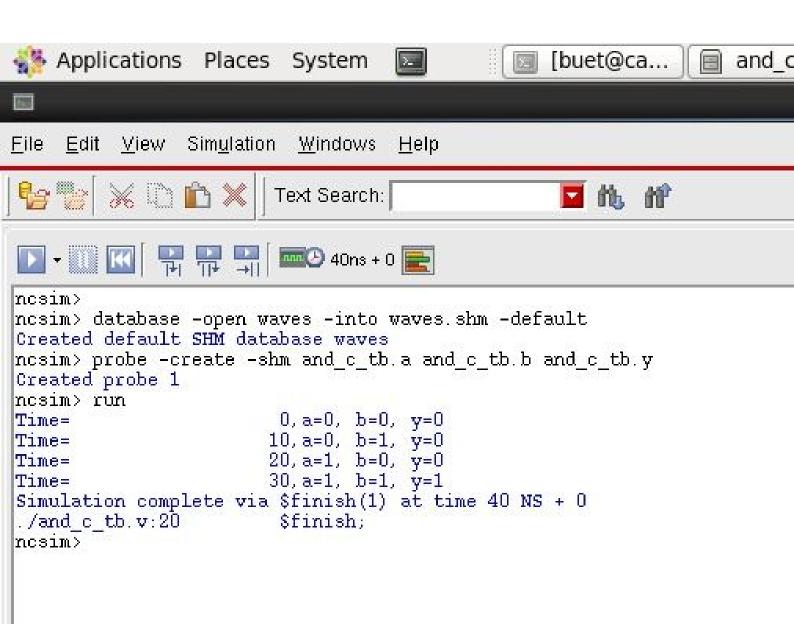


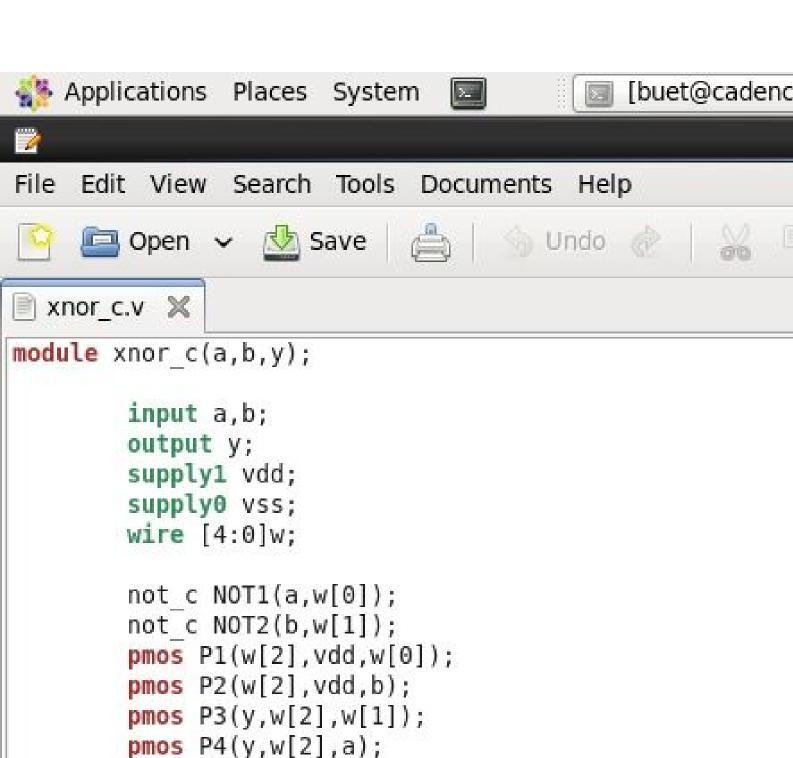


```
module and c(a,b,y);
        input a,b;
        output y;
        wire w;
        nand c NA1(a,b,w);
        not c NOT1(w,y);
```







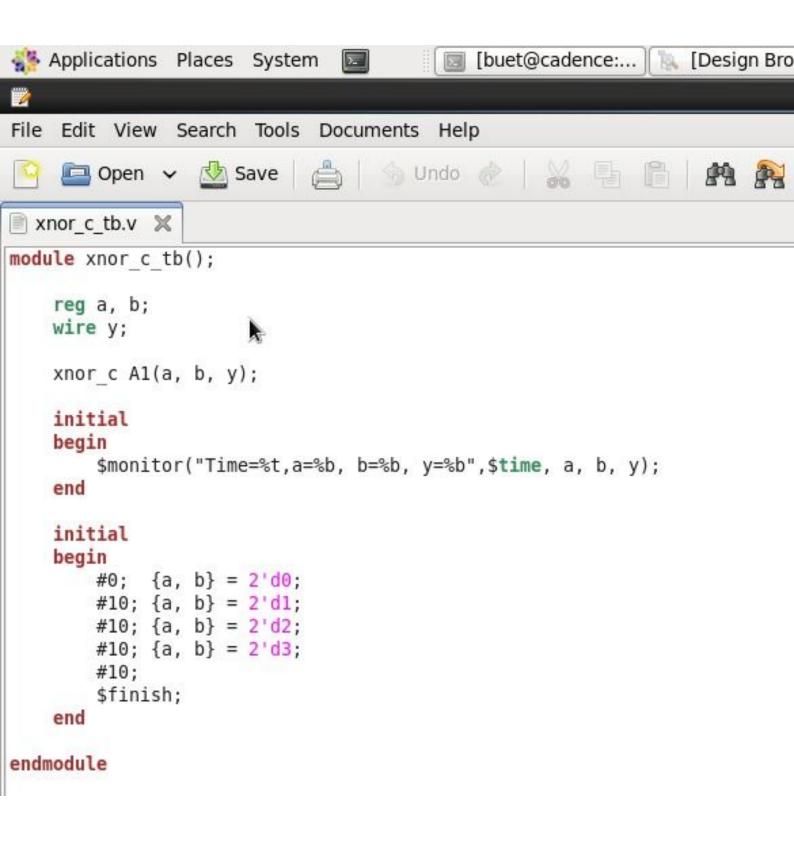


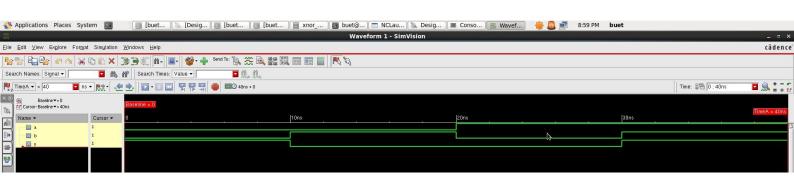
nmos N1(y,w[3],b);

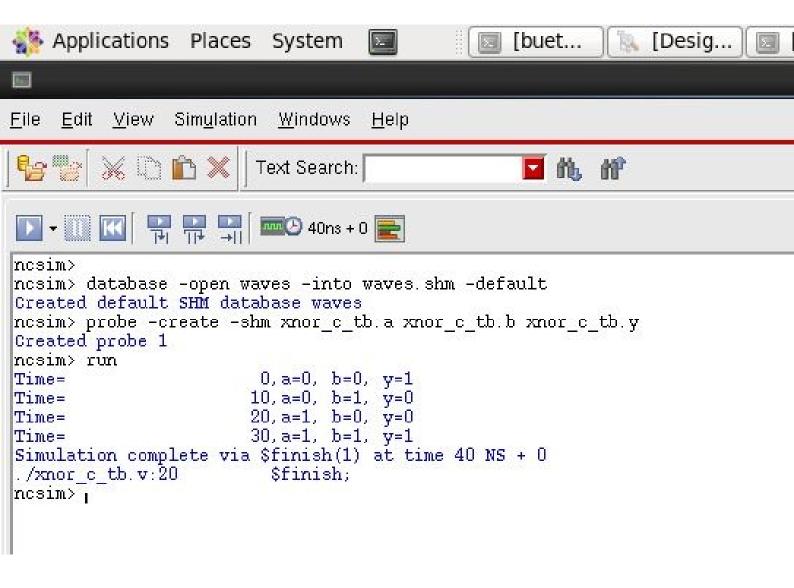
nmos N2(w[3], vss, w[0]);

nmos N3(y,w[4],w[1]);

nmos N4(w[4],vss,a);













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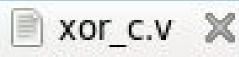
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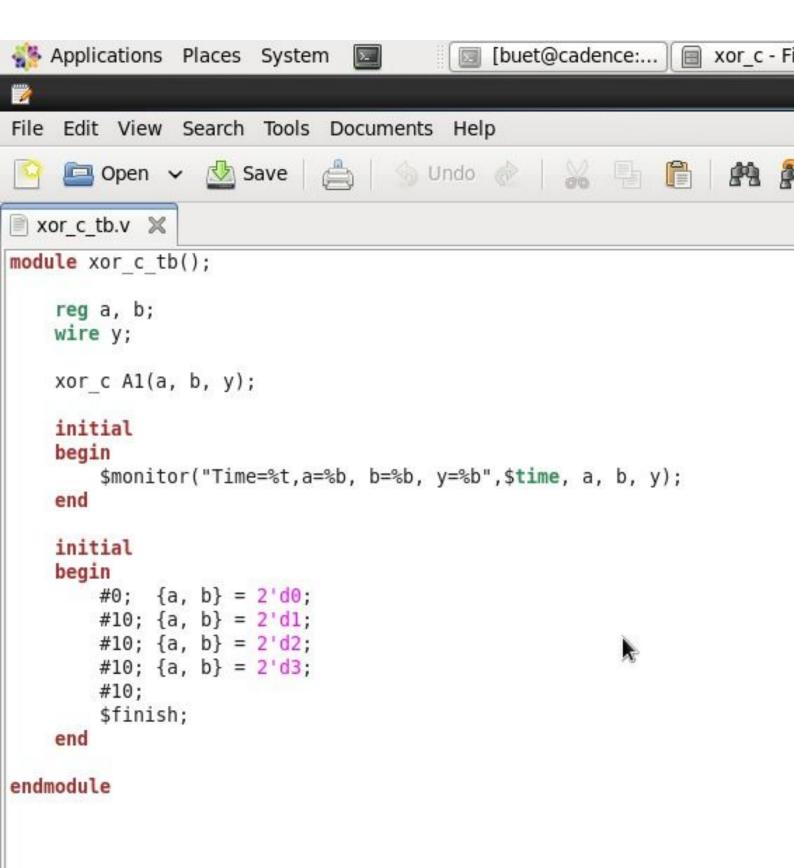


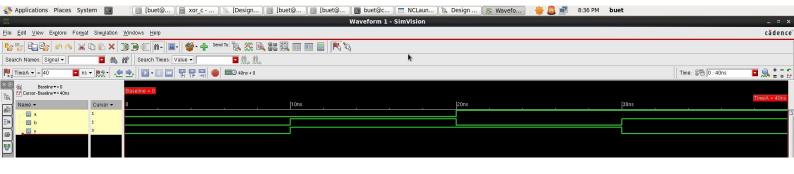
```
module xor c(a,b,y);
```

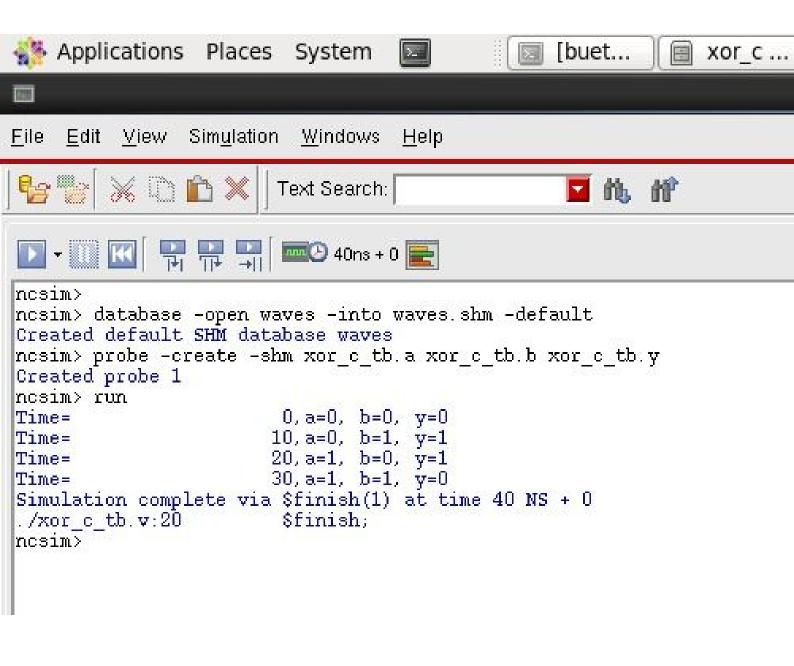
```
input a,b;
output y;
wire w;
```

```
xnor c XN1(a,b,w);
not c NOT1(w,y);
```

















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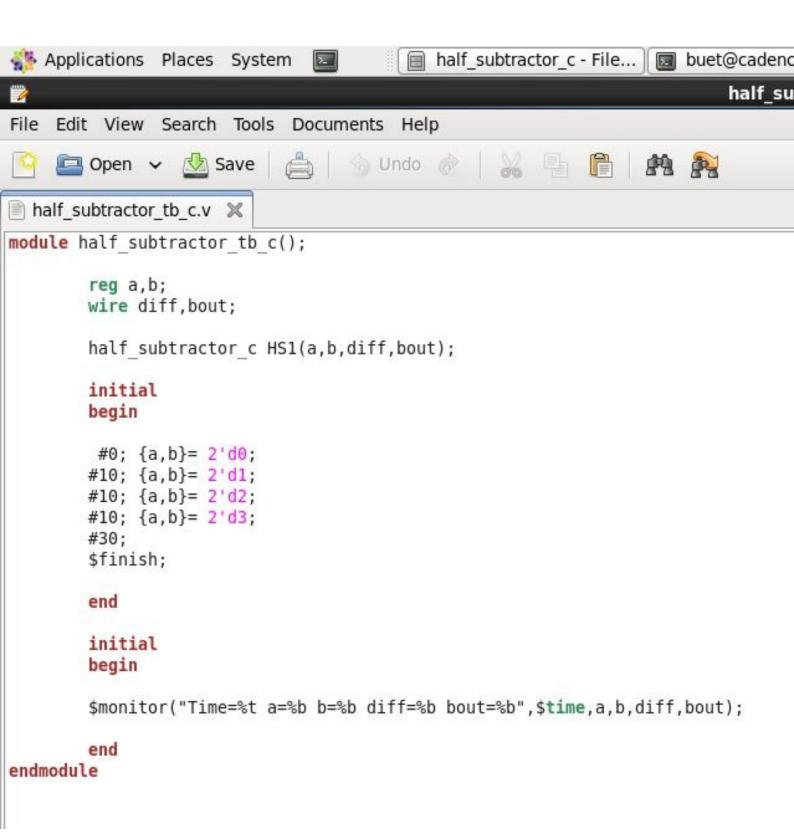
half subtractor c.v 💥

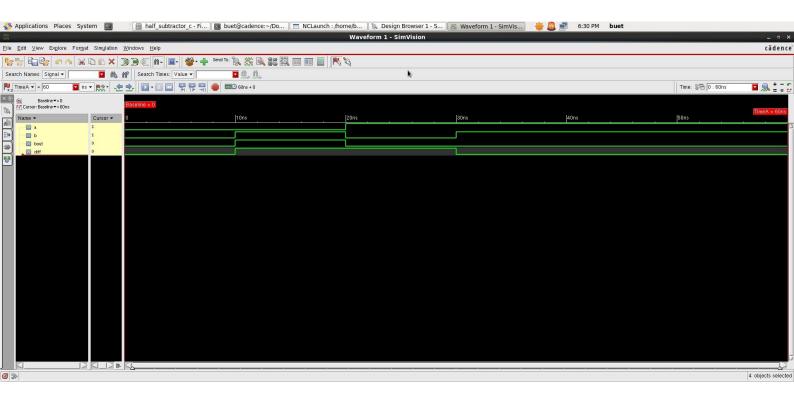


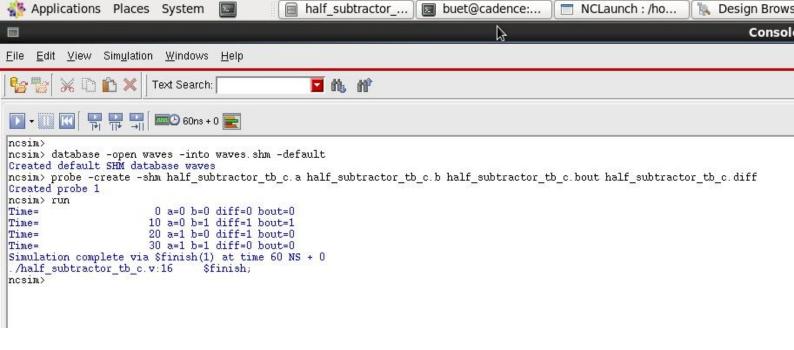
module half subtractor c(a,b,diff,bout);

```
input a,b;
output diff, bout;
```

```
xor c X1(a,b,diff);
not c N1(a,w);
and c A1(w,b,bout);
```















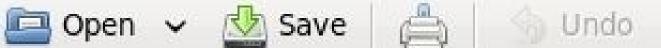
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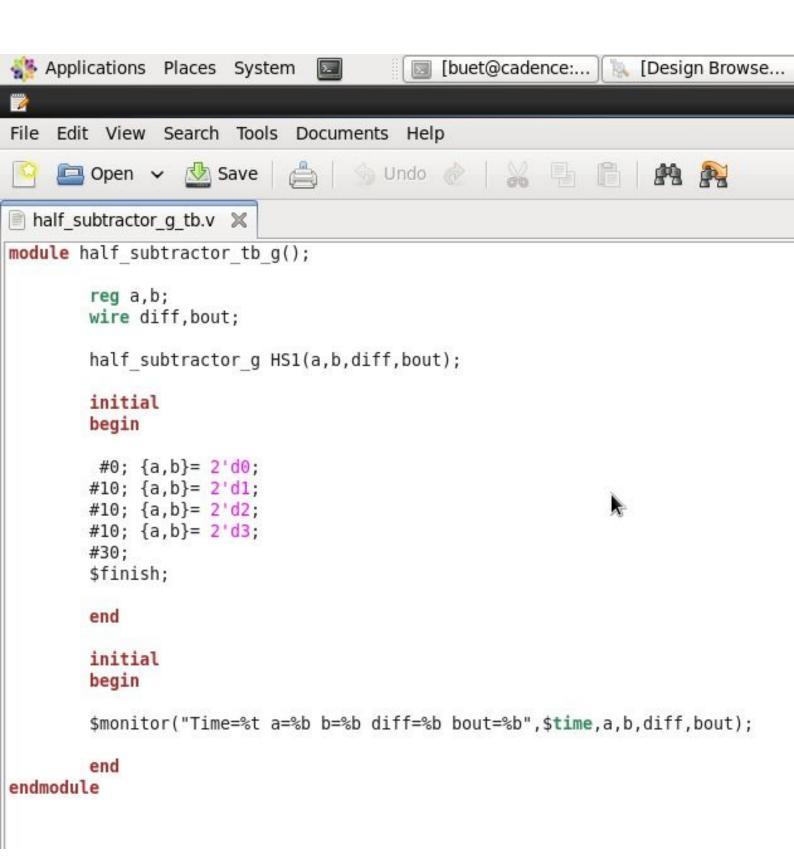
half subtractor g.v 💥

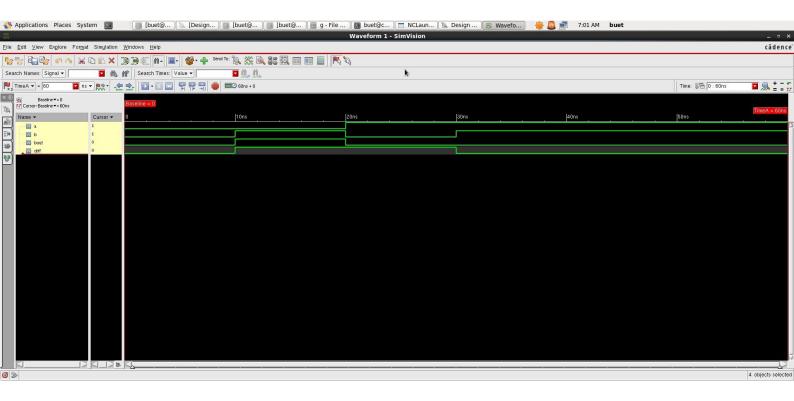


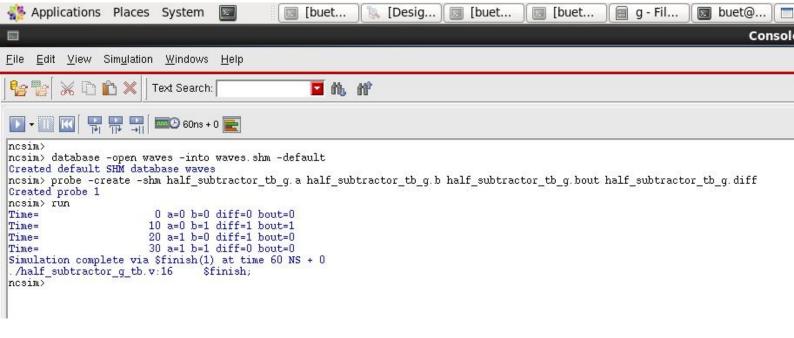
module half subtractor g(a,b,diff,bout);

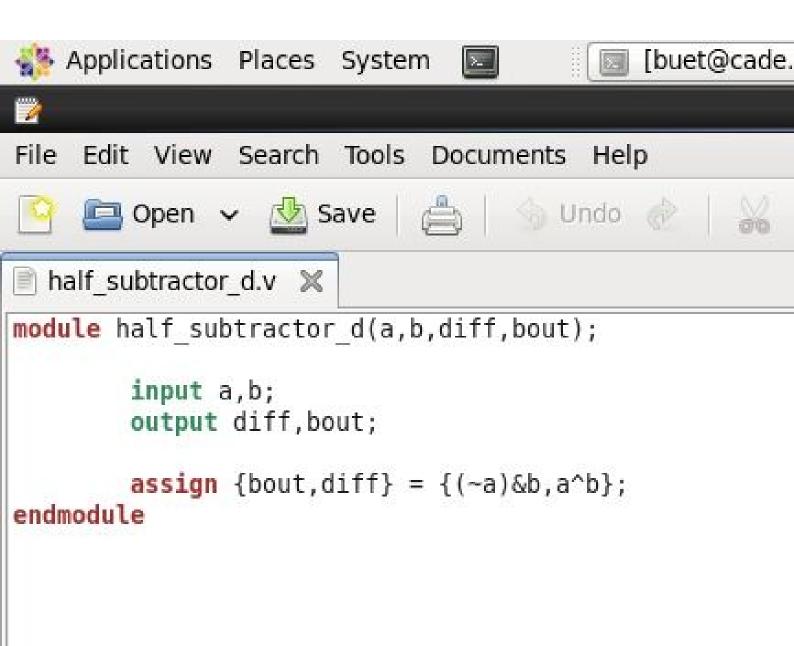
```
input a,b;
output diff, bout;
wire w;
```

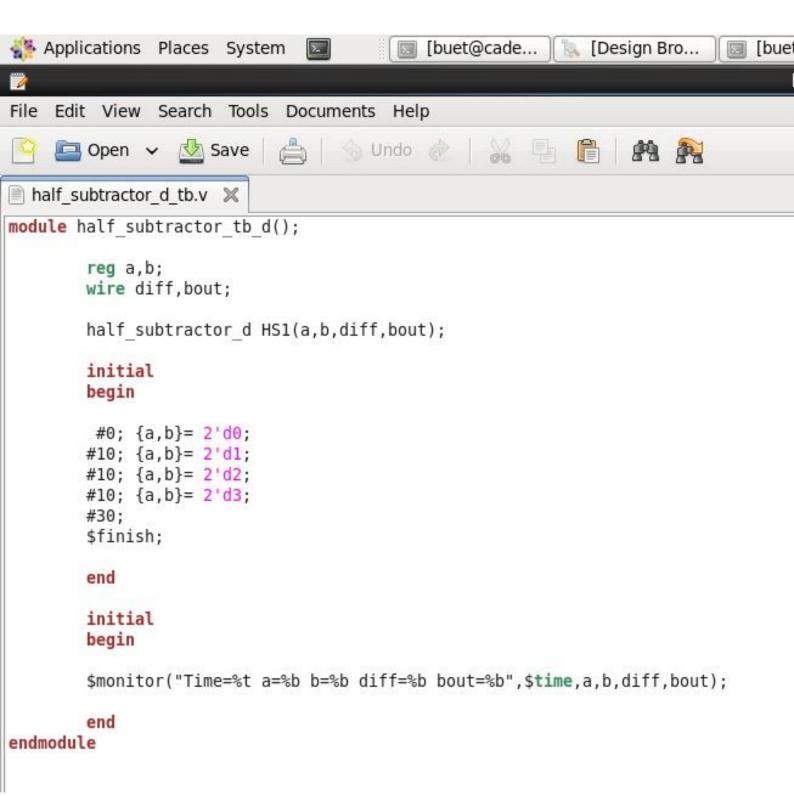
```
xor X1(diff,a,b);
not N1(w,a);
and A1(bout, w, b);
```

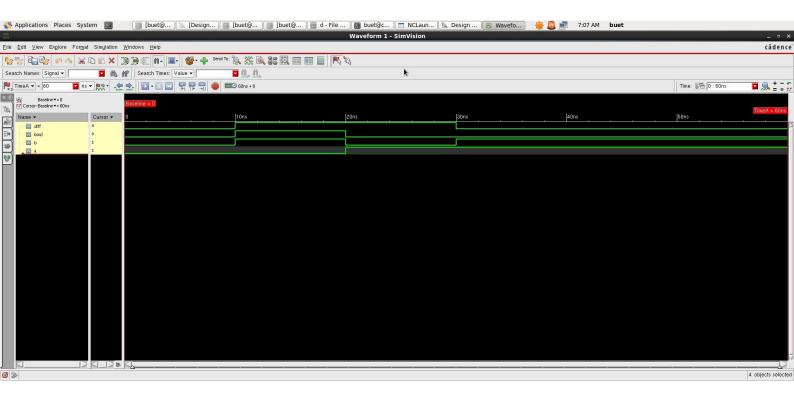


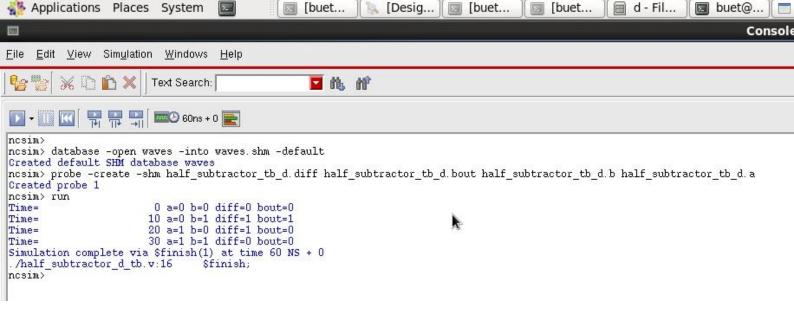




















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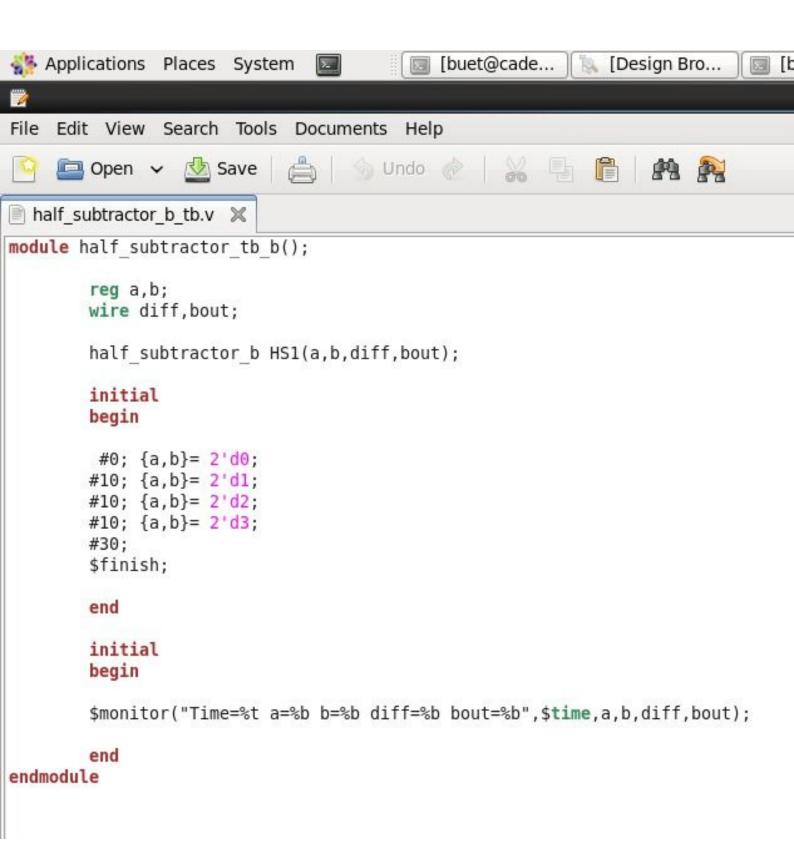


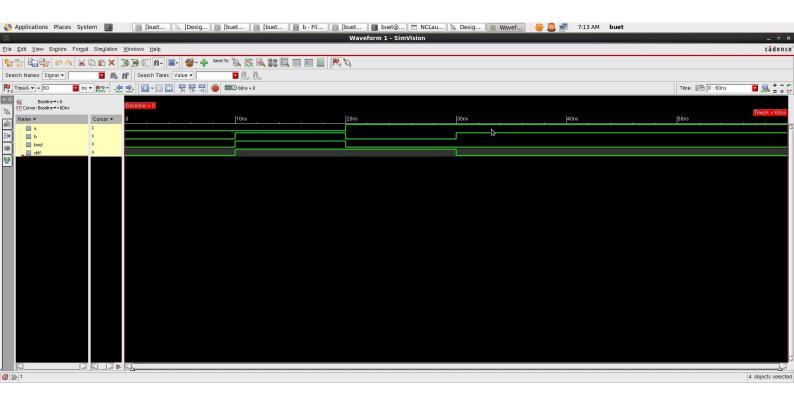
half subtractor b.v

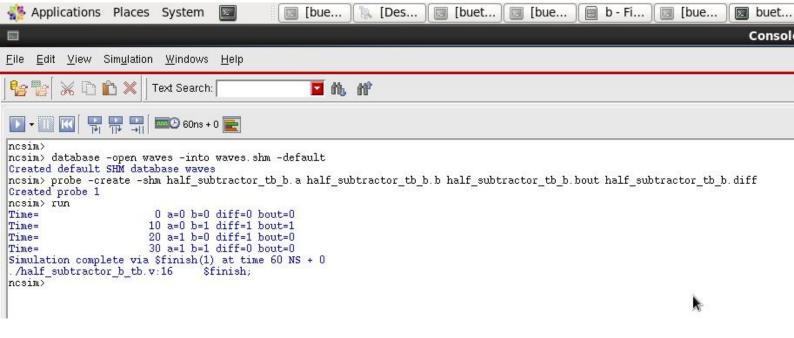
```
module half subtractor b(a,b,diff,bout);
```

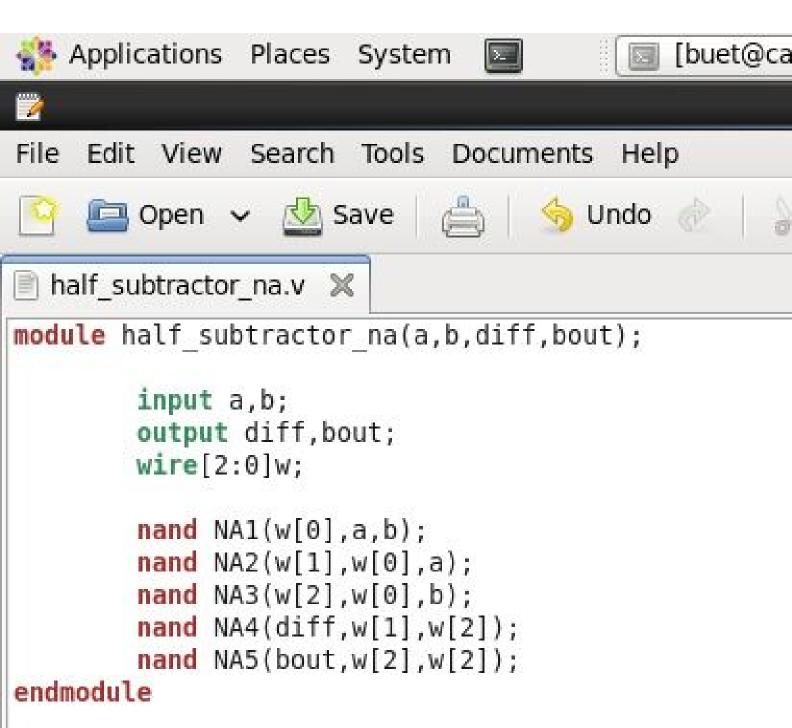
```
input a,b;
output reg diff, bout;
```

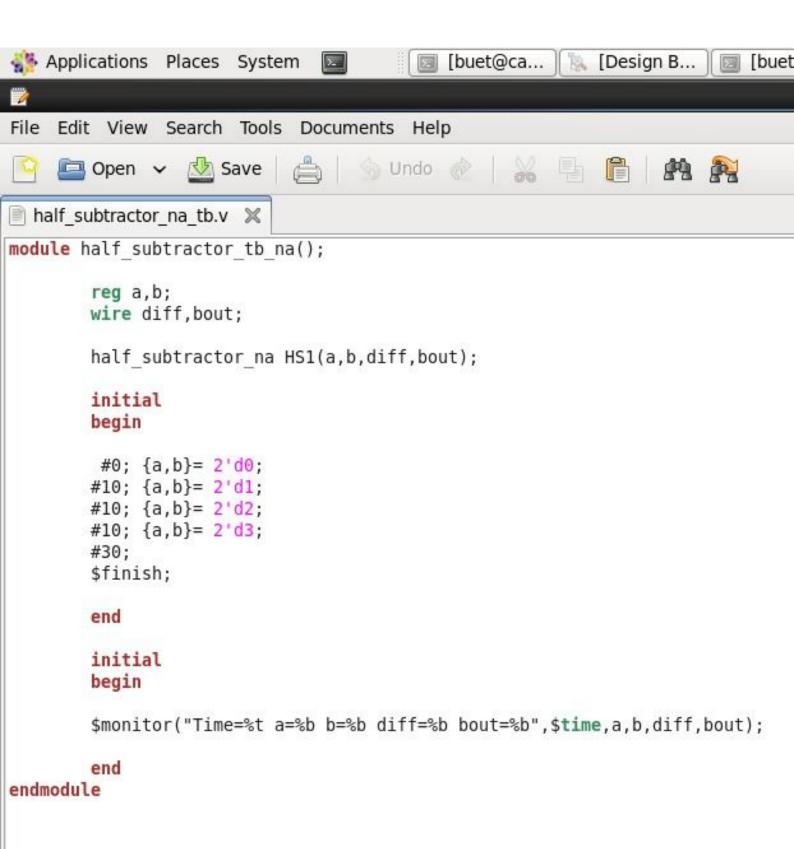
```
always@(a or b)
case({a,b})
2'd0:{bout,diff}=2'd0;
2'd1:{bout,diff}=2'd3;
2'd2:{bout,diff}=2'd1;
2'd3:{bout,diff}=2'd0;
endcase
```

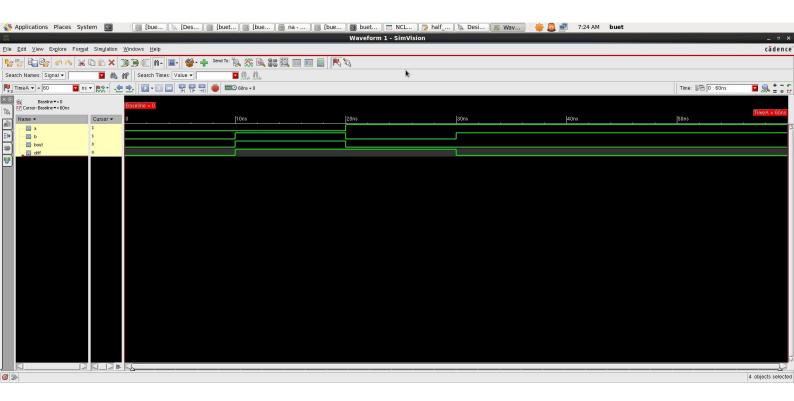


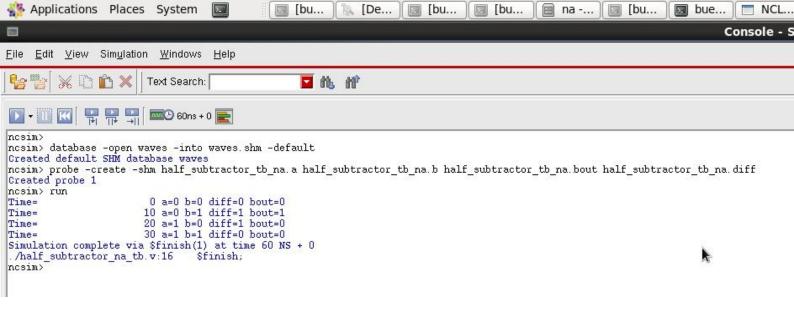














### Applications Places System







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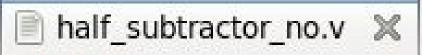
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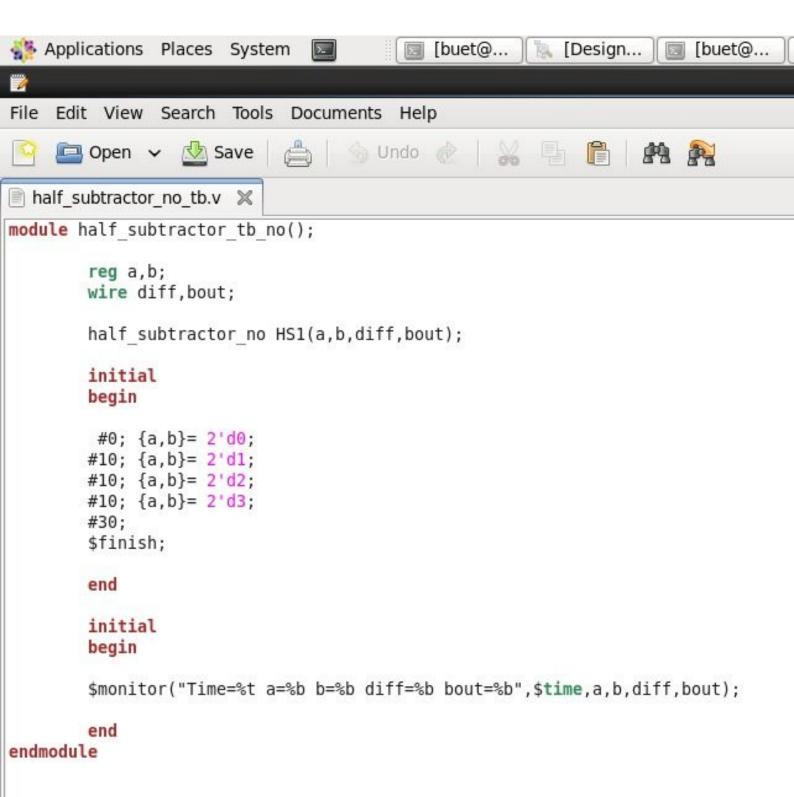


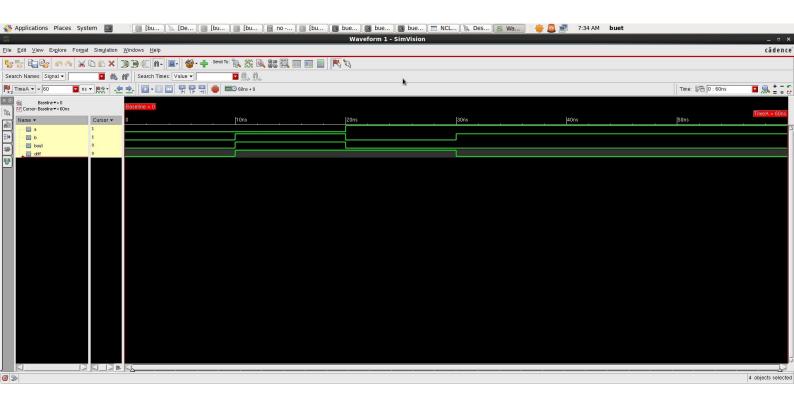


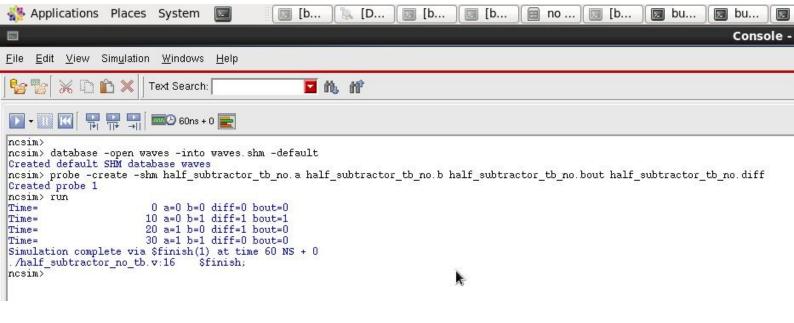


```
module half subtractor no(a,b,diff,bout);
```

```
input a,b;
        output diff, bout;
        wire [2:0]w;
        nor N01(w[0],a,b);
        nor N02(bout,w[0],a);
        nor N03(w[1],b,w[0]);
        nor N04(w[2],w[1],bout);
        nor N05(diff,w[2],w[2]);
endmodule
```









## Applications Places System







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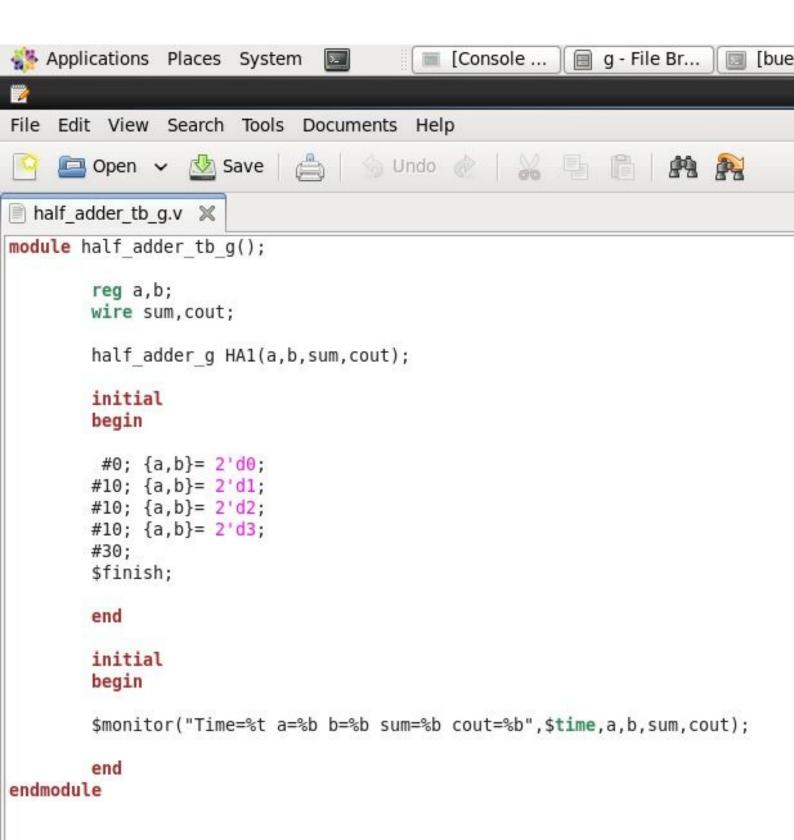
half adder g.v 💥

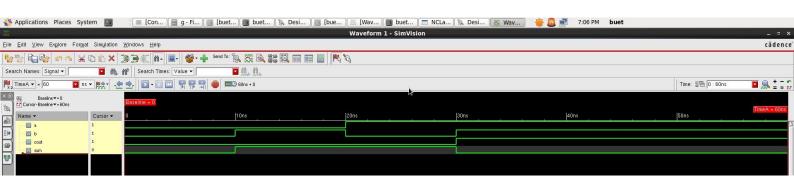
```
module half adder g(a,b,sum,cout);
```

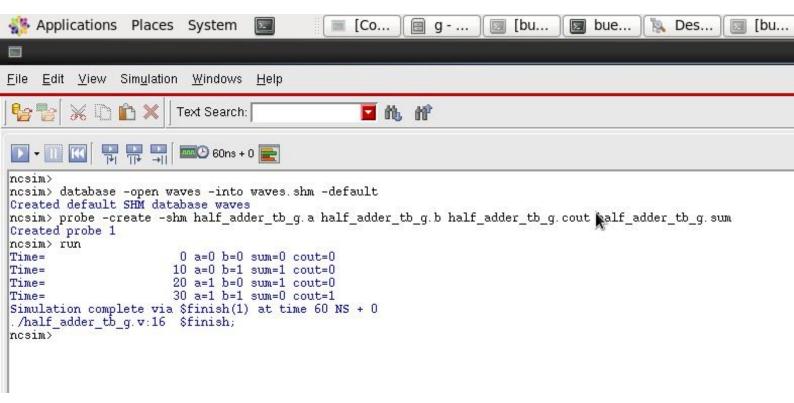
```
input a,b;
output sum, cout;
```

```
xor X1(sum,a,b);
and A1(cout,a,b);
```

endmodule









# Applications Places System







#### File Edit View Search Tools Documents He













half subtractor c.v 💥



module half subtractor c(a,b,diff,bout);

```
input a,b;
output diff, bout;
```

```
xor c X1(a,b,diff);
not c N1(a,w);
and c A1(w,b,bout);
```

endmodule

