1. Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt.
• This is tricky because precisely 60 Hz is impossible with our system; instead, think about the process and minimize the error. Many combinations of PSC and ARR values work—not just one!

PSC = 0

To get 60hz, we need ARR value of about (8000000/60)=133,333

2. Look through the Table 13 "STM32F072x8/xB pin definitions" in the chip datasheet and list
all pins that can have the timer 3 capture/compare channel 1 alternate function.
• If the pin is included on the LQFP64 package that we are using, list the alternate function
number that you would use to select it.

PA6, PB4, PE3, PC6

3. List your measured value of the timer UEV interrupt period from first experiment.
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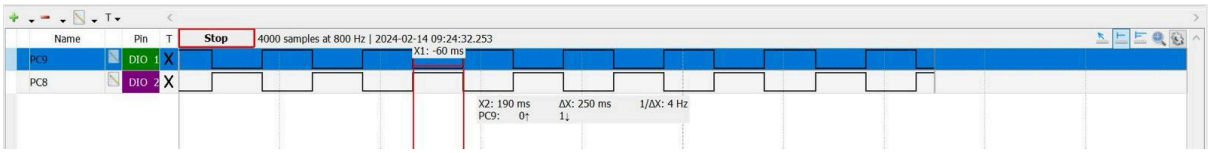
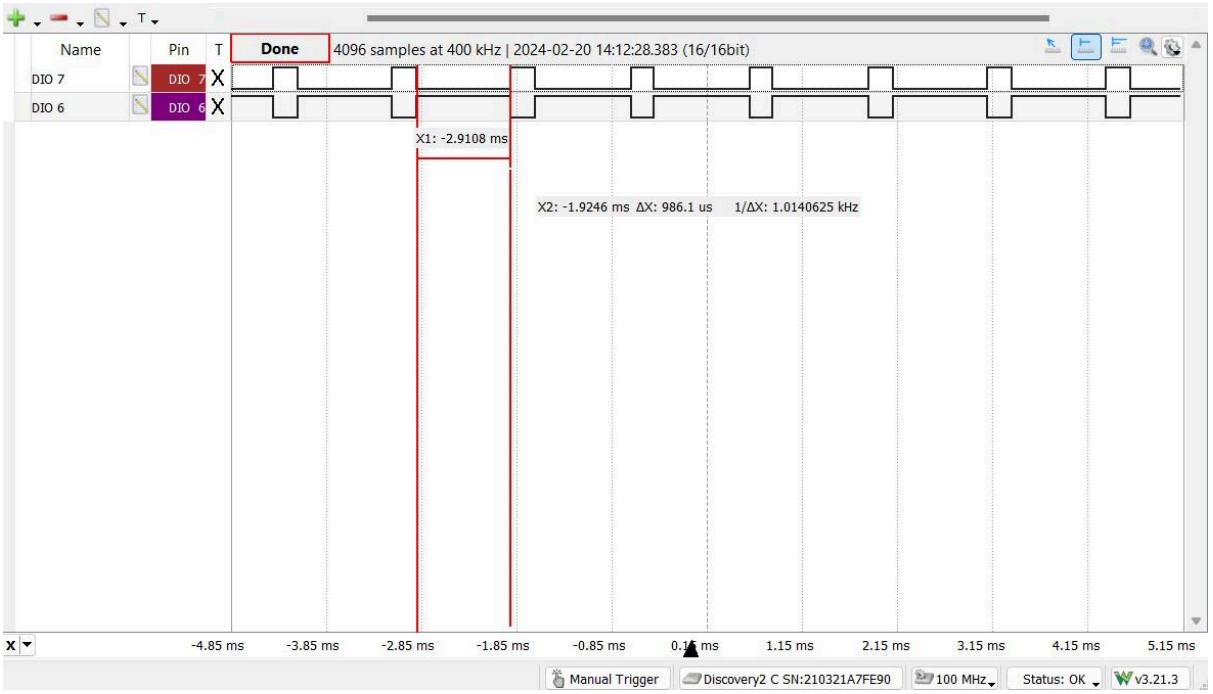
The measured value from experiment 1 is 4Hz



4. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM
mode 1.
The Duty cycle increases as CCR1 value increases

5. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM
mode 2.
The Duty cycle decreases as CCR1 value increases

6. Include at least one logic analyzer screenshot of a PWM capture.



7. What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?
It is PWM mode 2.

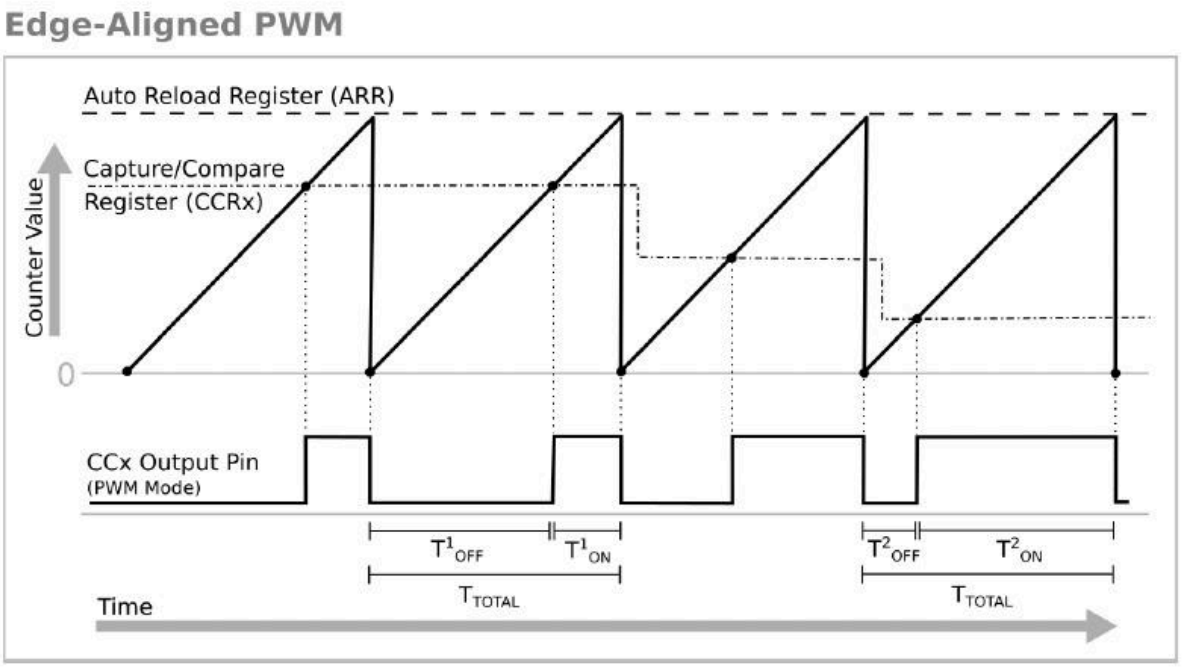


Figure 3.6: Edge-aligned PWM mode and output pin state.