1. Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?

PA0 and PC0 both control the MUX that drives EXTI0, so it cannot be used at the same time.

2. What software priority level gives the highest priority? What level gives the lowest?

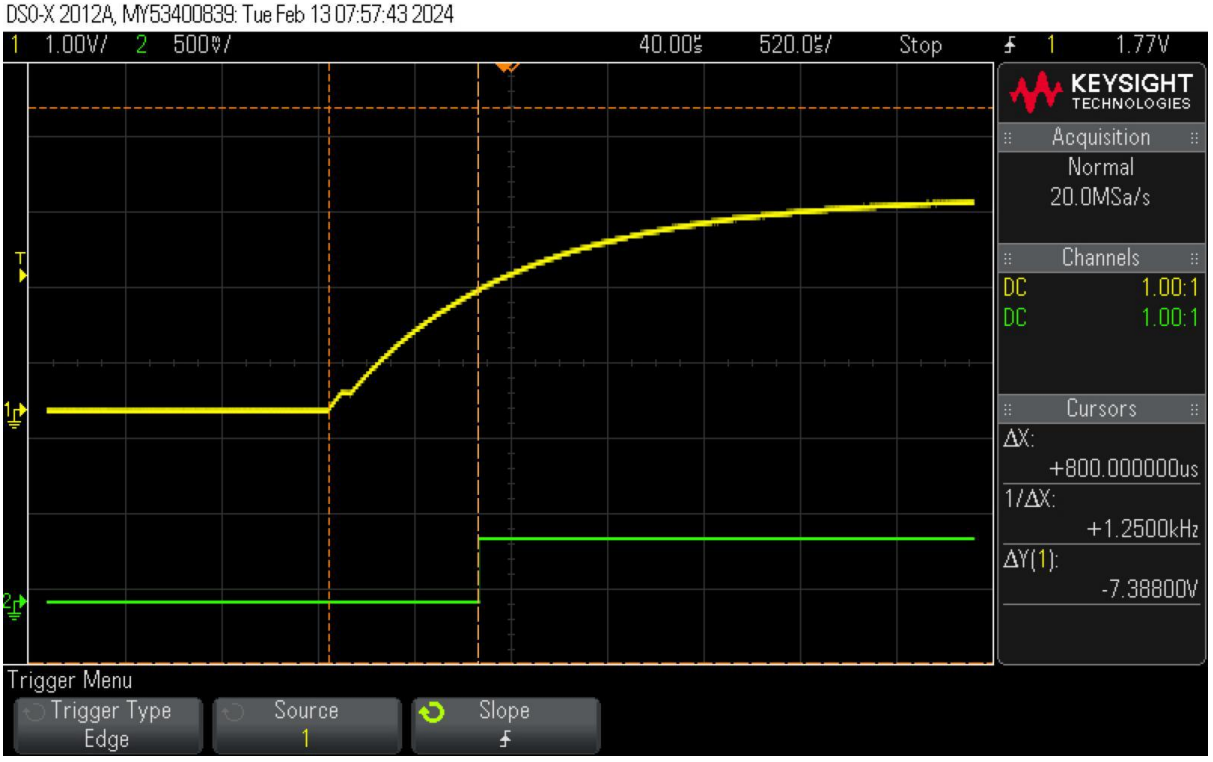
Priority 0 is highest level and priority 4 is the lowest level

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt
(including non-implemented bits)? Which bits in the group are implemented?

NVIC has 8- bits reserved in its priority registers for each interrupt. In that the bits [7:6] are implemented.

4. What was the latency between pushing the Discovery board button and the LED change
(interrupt handler start) that you measured with the logic analyzer? Make sure to include a
screenshot in the post-lab submission.

800 microseconds was the latency



5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

The status flag has to be cleared to note that the interrupt has been handled, if not the interrupt handler will be called continuously.