Computer Architecture: answers to unaccessed tutorial exercises

Exercise 4.1

(a) The references are as follows:

Reference	Cache Address	Hit or Miss
1	1	M
4	4	M
8	8	M
5	5	M
20	4	M
17	1	M
19	3	M
56	8	M
9	9	M
11	11	M
4	4	M
43	11	M
5	5	H
6	6	M
9	9	H
17	1	H

The final state of the cache is:

Block No.	Address
0	
1	17
2	
3	19
4	4
5	5
6	6
7	
8	56
9	9
10	
11	43
12	
13	
14	
15	

(b) The references are as follows:

Reference	Hit or Miss	Block Address	Block Number	New Addresses in Block
1	M	0	0	0–3
4	M	1	1	4–7
8	M	2	2	8–11
5	H	1	1	
20	M	5	1	20–23
17	M	4	0	16–19
19	H	4	0	
56	M	14	2	56–59
9	M	2	2	8–11
11	H	2	2	
4	M	1	1	4–7
43	M	10	2	40–43
5	H	1	1	
6	H	1	1	
9	M	2	2	8–11
17	H	4	0	

The final state of the cache is:

Block No.	Starting Address
0	16
1	4
2	8
3	

Exercise 4.2

(a) The shortest reference string will have 4 misses for C1 and 3 misses for C2; this leads to 32 miss cycles for C1 and 33 miss cycles for C2.

The following reference string will do: 0, 4, 8, 11.

(b) For C2 to have more misses, we must have a situation where a block is replaced in C2 and then another reference occurs to a different word (in the cache of C1) that was replaced. This has to happen more than once. Here is one example string:

Addresses	Cache 1	Cache 2
0	Miss	Miss
1	Miss	Hit
16	Miss	Miss
1	Hit	Miss
16	Hit	Miss
Total Misses	3	4