Computer Architecture: unassessed tutorial exercises

Exercise 4.1

Here is a string of address references given as word addresses:

1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17

(a) Assuming a direct mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss, and show the final contents of the cache.

(b) Using the same string of addresses, show the hits, misses and final cache contents for a direct mapped cache with four-word blocks and a *total size* of 16 words.

Exercise 4.2

Cache C1 is direct mapped with 16 one-word blocks. Cache C2 is direct mapped with 4 four-word blocks. Assume that:

- the miss penalty for C1 is eight clock cycles,
- the miss penalty for C2 is eleven clock cycles,
- the caches are initially empty.

(a) Find a reference string for which C2 has a lower miss rate but spends more cycles on cache misses than C1. Use word addresses.

(b) Find a reference string for which C2 has more misses than C1. Use word addresses.