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Total No. of Questions : 5] [Total No. of Printed Pages : 4

EY-225

B.Tech. III[rd] Semester (New Scheme) CSE

Examination, 2023-24

Digital Electronics

Paper - CS - 302

Time : 3 Hours] **[Maximum Marks : 60**

Note :- Attempt all questions. Each question carry equal marks.

Unit - I

1. (a) Describe the following codes with example : 12

(i) EBDCI code

(ii) Excess three code

(b) Convert the following :

(i) $(510)_{10}$ to Hexadecimal

(ii) $(427)_{10}$ to octal

OR

(a) Write any 04 (four) boolean laws and explain with example.

(b) Convert the following :

(i) $(327)_{10}$ to binary

(ii) $(38A)_{16}$ to decimal

Unit - II

2. Simplify the following boolan expressinon and obtain (i) minimal SOP and (ii) minimal POS expression y $\sum_{m} = (1, 5, 7, 8, 9, 13, 14, 15, 18, 21, 25) + \Sigma_{d} (6, 19, 23, 30)$. 12

OR

Obtain minimal SOP and POS expression a for the following boolean expression $f = \Sigma (1, 2, 3, 4, 5, 8, 9, 11, 14, 15)$ using

Quine - Mc Cluskey method.

Unit - III

3. Describe working 4 bit full adder and subtraction circuit with the help of logic diagrams and truth table. 12

OR

Design 1 : 16 demultiplexer and explain it's working with the help of logic diagram and truth table.

Unit - IV

4. (a) Differential between combinational and sequential circuit with example (any three). 12

(b) Design BCD counter and describe its working in detail.

OR

(a) Differentiate between asynchronous and syrchronous digital circuits with example.

(b) Describe the working of 4 bit series and parallel shift register in detail.

Unit - V

5. Compare RTL, DTL and CMOS logic family (any four parameters). 12

OR

Design MOD-6 unit distance counter and prepare the following for the same

(i) State daigram

(ii) State table

(iii) Excitation table

(iv) Excitation maps

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