## AJEETNSON [ons:6]

## EX-275

## B.Tech. III<sup>rd</sup> Semester (New Scheme) Inform. Tech. Examination, 2022-23 Digital Electronics Paper - IT - 303

Time: 3 Hours

[Maximum Marks: 60

Note: - Ques. No. 1 is compulsory. There is internal choice Ques. no. 2 to Ques. no 6.

- 1. Write short answers.
  - (a) Convert BCD 01010011 to excess 3.

EX-275 (1) P.T.O.

- (b) Simplify the Boolean expression F = A'B'C' + B'CD' + A'BCD' + AB'C'.
- (c) Explain universal gates with truth table
- (d) Define full adder.
- (e) State the application of CMOS logic Inverter.
- 2. Convert the following
- (i)  $(101111101)_2 = ()_8$
- (ii)  $(C3A6)_{16} = ()_2$
- (iii)  $(3906)_{10} = ()_{BCB}$
- (iv)  $(370)_8 = ()_{16}$
- (v)  $(0.8)_{10} = ()_2$

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- Explain with the example Excess three codes, parity code and ASCII codes. Also give the difference between them.
- State and Explain De-Morgan's Theorem. Prove the following using De-Morgan's theorem:

EX-275

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 $AB + CD = \overline{AB.CD}$  and hence prove that an AND-OR configuration is equivalent to NAND-NAND configuration.

9

Write short note on Karnaugh's map method. Minimize the following Boolean Expression using k-map and realize with NAND gate.

$$F(A,B,C,D) = \sum M(2,3,6,7,8,9,10,11,12,13,14,15)$$

 Explain BCD adder with logic diagram. Also Design combinational circuit that converts 4-bit BCD to grey code.

9

What is flip-flop? Explain RS flip flop. State the disadvantages of RS flip flop. How can they be avoided?

5. Describe two bit asynchronous binary up counter with timing diagram? Draw the state diagram of 3-bit up counter. Assume the initial state to be 000.

OR

(3)

EX-275

P.T.O

Explain the operation of 4-bit shift register. Explain how we convert a serial signal into parallel and vice versa using shift register.

6. Explain TTL and CMOS in detail with circuit diagram. Also compare various logic families in terms of basic gates, power supply, fan out and power dissipation.

OR

For the given state table draw state diagram and design the circuit using TFF for Moore machine.

PS	NS,Z (O/P)	
	X = 0	X=1
P	P,00	Q,01
Q	Q,01	R,10
R	R,10	S,11
S	S,11	P,00

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EX-275

(4)

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