9.3 PENTIUM PRO

Intel introduced Pentium Pro 32 bit CISC processor in 1995. It follows data flow architecture which is different from the earlier Intel processors which used Von Neumann architecture. It operates at 3.3V and clock frequencies of 150MHz, 166MHz and 200MHz. It contains all the features of Pentium processor and in addition a second-level cache memory of 256 KB or 512 KB. It has first level cache of 8KB each for data cache and instruction cache. It has 36 address lines which can address 64GB memory and 64 data lines.

In data flow architecture, the processors fetch/decode unit fetches many instructions from the instruction cache, decodes them and keeps the microcode in the instruction pool. The processor then checks the instructions in the instruction pool one by one. If the data for the first instruction is not available in the cache, then it is cache miss. The processor goes to the second instruction without waiting for the data of first instruction to be fetched. If the second instruction requires the data from the first instruction, the processor goes to the third instruction. If the data is available it executes it and goes to the fourth instruction. Likewise, it executes all the instructions in the instruction pool whose data is ready and can be executed. The instructions whose data are not available are executed in the second round. Thus in data flow architecture the processor does not wait, which increases the processor speed.

9.4 PENTIUM II

Intel introduced Pentium II 32 bit CISC processor in 1997 for multimedia computers. It is built on Pentium Pro architecture with additional MMX technology. It uses on-chip MMX pipeline for MMX

technology. It has 57 MMX instructions. It operates at 3.3 V and clock frequency of 233 MHz – 700 MHz. It has two first level on-chip cache of 16KB each (one for instruction and other for data). Pentium II XEON has second level cache of 1MB or 2MB.

9.5 CELERON

Intel introduced Celeron a low cost 32 bit processor in 1999. It is built on Pentium Pro architecture. Celeron processor included MMX technology to support multimedia. It has two first level on-chip cache of 16 KB each (one for instruction and other for data). It has second level cache of 128 KB. Earlier it had different versions with clock frequency 266 MHz and 300 MHz which did not contain second level cache. The new versions increased the clock frequency to 2.6 GHz which used internet streaming SIMD instructions used to enhance multimedia performance on internet. it contains 75 new instructions for multimedia. It has an additional pipeline for MMX technology. Celeron is used in cheaper desktop computers. The new version of Celeron is Celeron D.

9.6 PENTIUM III

Intel introduced Pentium III 32 bit superscalar CISC processor in 1999. It has on-chip MMX pipeline for multimedia features. It has additional 70 multimedia instructions for internet known as Internet streaming SIMD instructions. These instructions are used to enhance multimedia performance on internet such as streaming audio, video, animation, speech recognition etc.

Pentium III like Pentium pro uses data flow architecture. It has 36 address lines which can address 64 GB memory and 64 data lines. It operates at 3.3 V and clock frequency 650 MHz to 1.2 GHz. it contains two on-chip first level cache of 16 KB each (one for instruction and other for data). It also has 256/512 KB on-chip second level cache. It uses 10 stage pipeline.

Pentium XEON has large second level cache of 1MB or 2MB and is used in workstations and servers.

9.7 PENTIUM IV

Intel developed 32 bit and 64 bit Pentium IV processors. It introduced Pentium 4 32 bit superscalar CISC processor in 2000. Pentium IV was improved version of P III. It has 144 internet streaming SIMD instruction which are known as internet SSE2 (internet streaming SIMD extension 2) instruction. Like Pentium Pro, it follows data flow architecture. It has 36 address lines to address 64 GB memory and 64 data lines. It operates at 3.3 V clock frequency of 3.2 GHz. It has two first level cache (one for instruction and other for data). The data cache capacity is 8 KB and instruction cache of 12KB. It uses second level cache of 256 KB or 512 KB. It uses 20 stage pipeline.

Figure 9.2 shows the block diagram of Pentium IV processor.

9.8 ITANIUM

Itanium was first released in 2001and the later improved versions were released in 2006, 2008 and 2009. It is a family of 64 bit Intel microprocessors that implement the Intel Itanium architecture. The processors are used in enterprise servers and high-performance computing systems. The architecture originated at Hewlett-Packard (HP), and was later jointly developed by HP and Intel. The Itanium architecture is based on explicit instruction-level parallelism, in which the compiler makes the decisions about which instructions to execute in parallel. It can fetch several instructions at a time to implement instruction level parallelism. These instructions are then examined to find which instructions can be executed in parallel. The compiler reorders and schedules these instructions. The compiler also checks the instructions for dependencies and finds out whether the functional units needed for execution are available. As the compiler handles this work, the hardware becomes simple. It contains four integer units, four floating point units, four MMX units etc. It has two first level cache memory of 16 KB each, second level cache of 256KB and third level cache of 6/4/2 MB. It operates at 1.3, 1.4 and 1.5 GHz clock frequency.