UDYAM'22

DIGISIM ROUND – 1

Theme:

Sunny is a digital design engineer at Tecsas instruments. His company is working on a prototype of a calculator capable of performing various mathematical operations. During the testing phase, it was found that the square root function of the calculator is not working properly and thus Sunny has been assigned the task to fix this issue. As the design of the calculator is too complex, he is planning to make an external circuit for the square root function so that the issue can be fixed without hampering the original circuit. But being an online batch engineer, Sunny got stuck while implementing the circuit. As you are an intern in the same company, he is asking for your help in designing the circuit.

Task Description:

You have to design a circuit which is capable of calculating the square root of a 10-Bit binary input and producing a 5-Bit binary output. The output should be the integer value and if the input is not a prefect square, then the output should be the integer which is just less than the actual square root value.

Sample Input and Output:

i) Input: 1001000000
   Output: 11000
ii) Input: 1001110001
   Output: 11001
iii) Input: 1001011000
   Output: 11000

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List of components allowed:

ROM(2732)
Comparator(7485)
Register(74179/74194)
Adder(74283)
Multiplexer(74157/74153)
Counter (74LS590,74161,74163,74L5169)
Decoder(74LS139/74HC154)
Encoder(74HC148)
Buffer(74HC241/74125)
Flip flops(74273/7474,74LS175,74LS109)
BCD to 7 segment decoder(74LS347/7448)
7 segment/BCD display
Logic Gates
Clock

Cost of components:

IC	Cost
ROM(2732)	25
Clock	10
7485, 74283, 74157, 74153, 74179, 74194, 74273, 74161, 74163, 74LS590, 74LS169, 74HC154, 74HC241, 74LS175, 7448, 74LS347	2
74LS139, 74HC148, 7474, 74LS109	1
Logic gates, 74125	0.1
Logic states, Logic probes	Free

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Scoring:

- Submissions are accepted till 23rd March.
- Submit the simulation file named "team_name.zip" on the D2C portal. The ZIP file should contain the Proteus Design file, screen recording of the working of the circuit and a PDF file containing description of your approach, the number of each components used and your team information.
- 500 points will be awarded to the team on completing the PS.
- Total cost of the circuit will be deducted from the score.
- Bonus marks (max 100) will be given based on following factors:
  1. Time taken for submission
  2. Addition of some innovative features
  3. Readability/Clarity of circuit and its labelling
  4. Technical complexity/efficiency
  5. Structure and reusability

General Rules:

- The organizers reserve the right to change the rules as they deem fit. Change in rules, if any, will be notified on the D2C portal or via mail.
- The decision of the organizers shall be final and binding.
- **In case of any type of cheating/plagiarism suspected, the team will be immediately disqualified and no certificate will be given.**

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Round Rules:

- If multiple ROM(s) are used all of them shall be fed with the same binary file.
- Simulations based on components other than specified should be avoided. However, if you are not able to complete the design with the specified components you can choose your component whose cost will be decided later, which surely will be higher than mentioned cost.
- Only Proteus simulation file will be accepted in this Round.

For other details you can visit D2C Portal

Feel free to contact us for any help:

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