Ajinkya Bankar

Contact Information

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Research Interests

Artificial Intelligence, Deep Neural Network Sensitivity Estimation, Thermal/Power-aware Computing, Advanced Real-Time Computing System Design

Education

Florida International University, Miami, Florida USA

Ph.D. Candidate, Electrical & Computer Engineering, April 2021

- Dissertation Topic: "Thermal Aware Electronic Control System Optimization for Distributed Automotive Applications"
- Advisor: Dr. Gang Quan

Savitribai Phule Pune University, Pune, Maharashtra India

M.E., Electronics (Digital Systems), September, 2013
B.E., Electronics & Telecommunication, August, 2010

Academic Experience

Florida International University, Miami, Florida USA

Graduate Student **August, 2018 - present**
Includes current Ph.D. research, Ph.D. and Masters level coursework.

Teaching Assistant **August, 2018 - present**
Duties at various times have included leading weekly computer lab exercises and office hours.

Savitribai Phule Pune University, Pune, Maharashtra India

Assistant Professor **July, 2013 - July, 2018**
Delivered various theory and lab courses at undergraduate level, and worked as a senior design project coordinator

Graduate Student **August, 2011 - September, 2013**
Includes Master level Coursework & research

Undergraduate Student **August, 2006 - August, 2010**
Undergraduate level Coursework & curriculum projects

Peer-Reviewed Publications

Ajinkya S. Bankar, Shi Sha, Vivek Chaturvedi, and Gang Quan. Thermal Aware Lifetime Reliability Optimization for Automotive Distributed Computing Applications. 2020 IEEE 38th International Conference on Computer Design (ICCD), pages 498–505, 2020.

Shi Sha, Ajinkya S. Bankar, Xiaokun Yang, Wujie Wen, and Gang Quan. On Fundamental Principles for Thermal-Aware Design on Periodic Real-Time Multi-Core Systems. ACM Transactions on Design Automation Electronic Systems, Vol. 25(2), 2020.

Anjali S. Patil, Jayanand P. Gawande, Ajinkya Bankar. Heart Sound Signal Analysis and Its Implementation in VHDL. Innovations in Electronics and Communication Engineering, Vol 33. pp 221-228, 2019.

Ajinkya S. Bankar, Bhavika S. Shaha, P.K. Kadbe. Interstage Pipeline VLSI Architecture for 2-D DWT. International Journal of Engineering Research & Tech., Vol. 2(5), 2013.

Conference Presentations

Ajinkya S. Bankar, Shi Sha, Vivek Chaturvedi, and Gang Quan. Thermal Aware Lifetime Reliability Optimization for Automotive Distributed Computing Applications. 2020 IEEE 38th International Conference on Computer Design (ICCD), Hartford, Connecticut USA, October 2020.

Invited Talks

Ajinkya S. Bankar. Emerging Trends and Technology in Electronics. National Webinar, Tuljaram Chaturchand College, Baramati, India, February 2021.

Professional Experience

Sujlam Electronics, Baramati, Maharashtra India

Consultant **January, 2016 - December, 2017**

Solution was provided to interface alternating current of C.T. with PIC16F685 and software coding for read/write operations of internal EEPROM of the microcontroller.

Research Grants

A Pipeline VLSI Architecture for 2-D DWT

Board of College and University Development, Savitribai Phule Pune University, India, ₹ 170,000

July, 2014 - June, 2016

Role: Co-Principal Investigator

The project carried processing unit's hardware optimization, and computation speed enhancement with pipelined architecture. Physical realization on Digilent Genesys 2 FPGA board for image compression.

Computer Skills

- Machine learning library: PyTorch.
- Languages: Python, Matlab, C, C++, Embedded C, VHDL.
- Optimization Solvers: CPLEX, AMPL Knitro.
- Operating Systems: Unix/Linux, Windows.