NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION

TECHNOLOGY, CALICUT

VLSI for Beginners

Verilog HDL Exercises

Contact Point for the Lab

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1. ***Design & test the following basic Logic Gates using Verilog HDL and capture the waveforms: a)OR, B)AND, c)NOT, d)NAND, e)XOR, f)NOR***
2. ***Design a Half Adder using Verilog HDL, Simulate and capture the waveforms in a)Dataflow modelling, b)Behavioral modelling and c)Structural modelling***
3. ***Design a Full Adder using Verilog HDL, Simulate and capture the waveforms in a)Dataflow modelling, b)Behavioral modelling and c)Structural modelling***
4. ***Design a Half Subtractor using Verilog HDL, Simulate and capture the waveforms in a)Dataflow modelling, b)Behavioral modelling and c)Structural modelling***
5. ***Design a Full Subtractor using Verilog HDL, Simulate and capture the waveforms in a)Dataflow modelling, b)Behavioral modelling and c)Structural modelling***
6. ***Design and simulate 4:1 Multiplexer using Verilog HDL and capture the waveforms***
7. ***Design and test a 4-Bit Up Counter (Synchronous) , write it's test bench and capture the waveforms in Behavioral modelling***