Fundamentals of FPGAs – Part 3: Getting Started with Microchip Technology's FPGAs

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Editor's Note: Optimal processing solutions are often provided by combinations of RISC, CISC, graphics processors and FPGAs, FPGAs on their own, or by FPGAs that boast hard processor cores as part of their fabric. However, many designers are unfamiliar with the capabilities of FPGAs, how they've evolved, and how to use them. Part 1 of this multi-part series provides a high-level introduction to FPGAs. Part 2 focused on FPGA offerings from Lattice Semiconductor. Here, Part 3 concentrates on the FPGA device families and design tools from Microchip Technology (via its subsidiary Microsemi Corporation). Part 4 and Part 5 will look at FPGAs and tools from Altera, and Xilinx.

As discussed in Part 1, field-programmable gate arrays (FPGAs) have many characteristics that make them an invaluable computing asset, either used standalone or in a heterogeneous architecture, but many designers are unfamiliar with FPGAs and how to go about incorporating these devices into their designs.

One way to overcome this impediment is to look more deeply at FPGA architectures and associated tools from major vendors. This article looks at Microchip Technology's lineup.

High-level FPGA options overview

There are many different types of FPGAs on the market, each with different combinations of capabilities and functions. At the heart of any FPGA is its programmable fabric. This is presented as an array of programmable logic blocks, also known as logic elements (LEs) (Figure 1a). The next step up in the FPGA fabric is to include things like blocks of SRAM, called block RAM (BRAM), phase lock loops (PLLs), and clock managers (Figure 1b). Digital signal processing (DSP) blocks (called DSP slices) and high-speed serializer/deserializer (SERDES) blocks can also be added (Figure 1c).

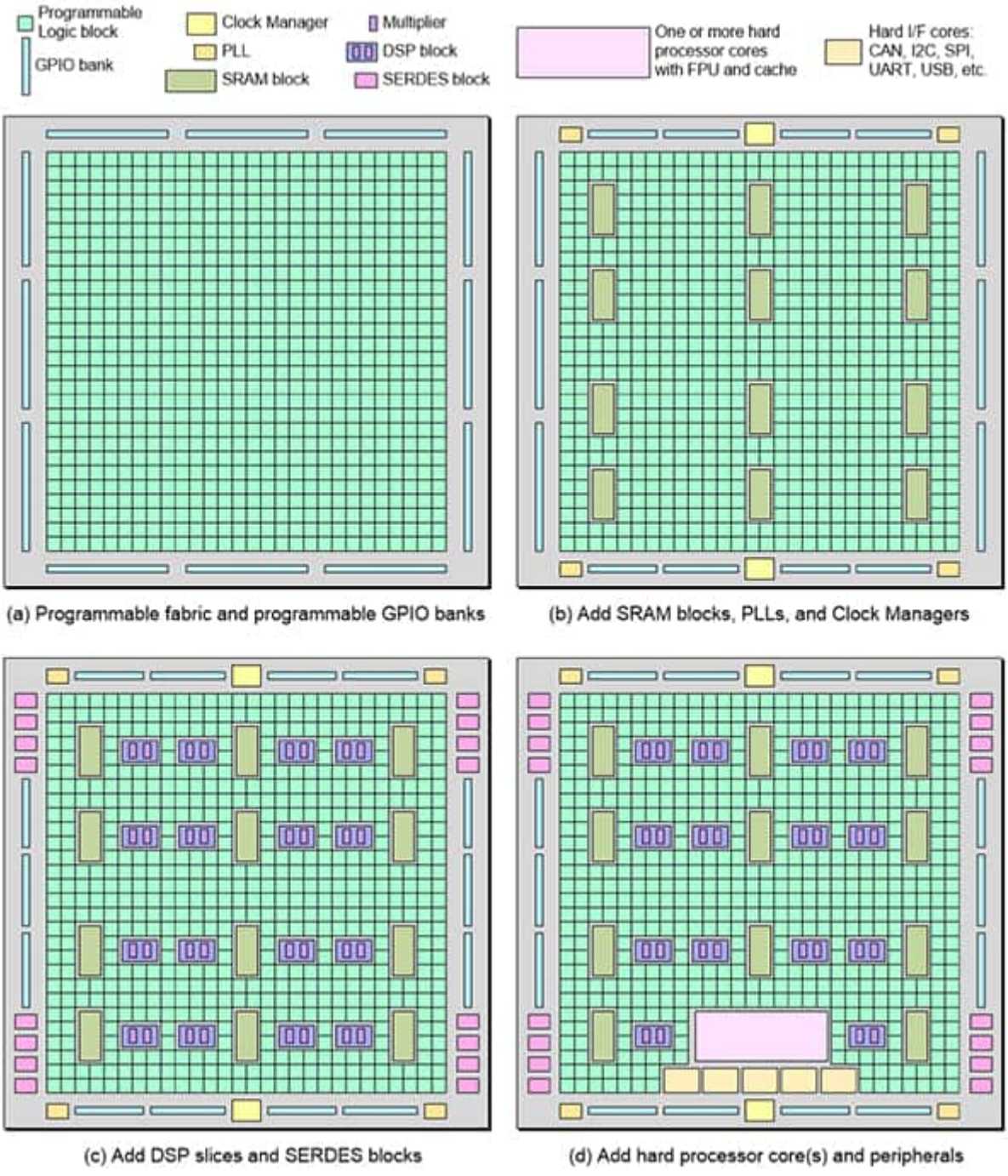

Figure 1: The simplest FPGAs contain only programmable fabric and configurable general-purpose IO (GPIO) (a); different architectures augment this fundamental fabric with SRAM blocks, PLLs, and clock managers (b); DSP blocks and SERDES interfaces (c); and hard processor cores and peripherals (d). (Image source: Max Maxfield)

Peripheral interface functions like CAN, I^2C, SPI, UART, and USB can be implemented as soft cores in the programmable fabric, but many FPGAs include them as hard cores in the silicon. Similarly, microprocessors can be implemented as soft cores in the programmable fabric or as hard cores in the silicon (Figure 1d). FPGAs with hard processor cores are referred to as system-on-chip (SoC) FPGAs. Different FPGAs offer different collections of functions, features, capabilities, and capacities targeted at different markets and applications.

There are a number of FPGA vendors, including Altera (which was acquired by Intel), Atmel (which was acquired by Microchip Technology), Lattice Semiconductor, Microsemi (which was also acquired by

Microchip Technology), and Xilinx.

All these vendors field multiple families of FPGAs; some offer SoC FPGAs, and some offer radiation tolerant devices that are targeted at high radiation environments like space. Choosing the best device for the task at hand can be tricky because there are so many families, each offering different resources.

Introducing Microchip Technology's FPGAs

Microchip Technology's FPGA offerings span the low- to mid-range, with a focus on low-power, high-security devices with exceptional reliability. Finding wide deployment in wired and wireless communications, defense and aviation, and industrial embedded applications, Microchip's FPGAs boast robust DSP and memory resources and demonstrate value in applications such as hardware acceleration, artificial intelligence, image processing, and edge computing.

Microchip offers three main FPGA families:

- IGLOO®2 FPGAs: Low-density devices with significant resources
- SmartFusion®2 SoC FPGAs: Low-density devices with significant resources and a 32-bit hard processor core
- PolarFire™ FPGAs and SoC FPGAs: Cost-optimized, high-performance devices implemented on 28 nanometer (nm) process technology

All FPGAs have configuration cells that determine the functionality of each of the programmable logic blocks, and the way in which the logic blocks are connected to each other and to the outside world. These cells are also used to configure the GPIO’s interface standard, input impedance, and output slew rate, etc.

Some FPGAs use SRAM-based configuration cells, but these are volatile, which means they lose their contents when power is removed from the system. In turn, this means that the configuration data has to be loaded from an external source—typically a flash memory device—when the system is powered up. These FPGAs take the longest time to power up and be ready for use.

Some FPGAs use on-chip flash memory to store the configuration data, but they still have SRAM-based configuration cells. In this case, on power-up, an on-chip controller copies the configuration data from the flash configuration memory to the SRAM configuration cells. These FPGAs power up faster than their pure SRAM cousins.

Microchip's IGLOO2 FPGAs and SmartFusion2 SoC FPGAs employ a different mechanism in which both the on-chip configuration memory and on-chip configuration cells are both implemented using flash technology. In the case of PolarFire devices, the configuration cells are based on silicon-oxide-nitride-oxide-silicon (SONOS) non-volatile memory (NVM) technology, which may be thought of as "like flash, but better."

Since the configuration data is stored in non-volatile flash (or SONOS) cells, Microchip's FPGAs and SoC FPGAs are "instant-on." That is, they power-up faster than any other type of FPGA. The reason these devices also feature a flash configuration memory is that a new configuration can be loaded into this configuration while the FPGA continues to run using the existing configuration in its configuration cells.

Once the download of the new configuration has been completed and verified (the configuration can be encrypted and accompanied by a cyclic redundancy check (CRC)), the device can be put into a safe state while the new configuration stored in the configuration memory is used to overwrite the original configuration stored in the configuration cells.

Traditional devices: IGLOO2 FPGAs

IGLOO2 are good all-around low- to mid-range FPGAs. These are what many designers would consider to be "traditional" FPGAs. These flash FPGA devices are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video and image processing, system management, and secure connectivity. Applications run the gamut, including communications, industrial, medical, defense, and aviation.

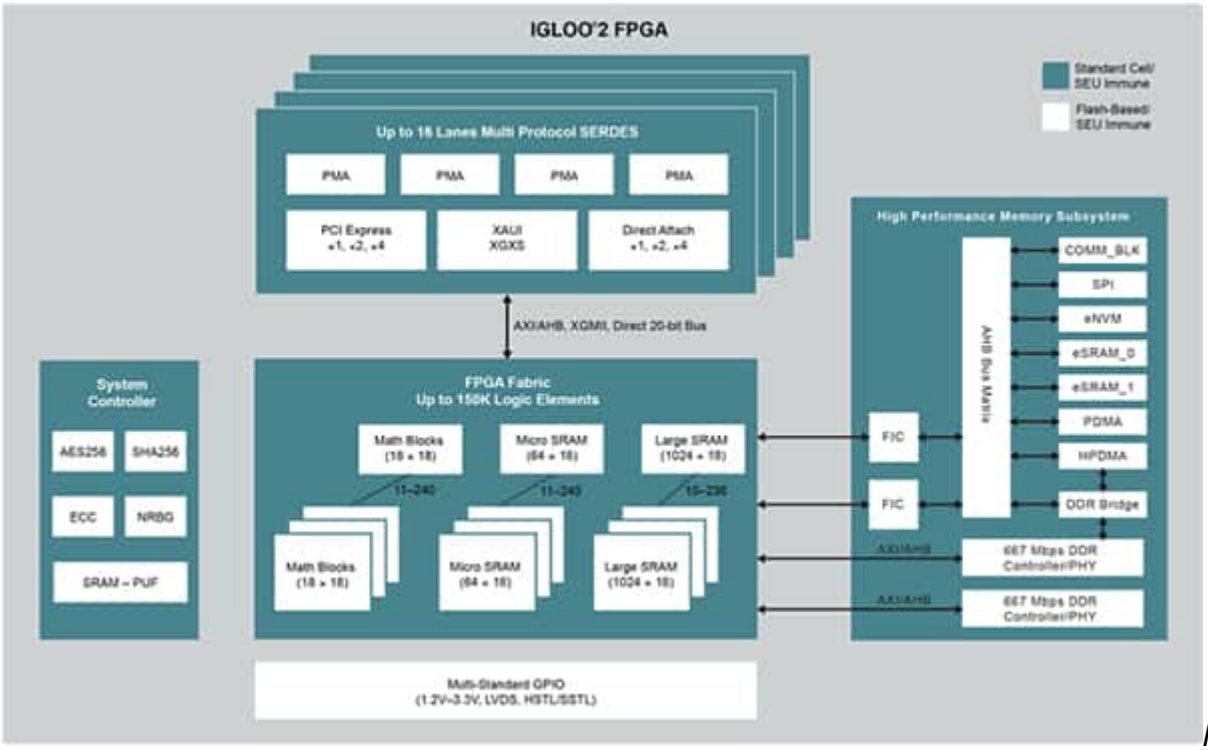

Figure 2: IGLOO2 FPGAs are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, I/O expansion and conversion, video and image processing, system management, and secure connectivity. (Image source: Microchip Technology)

IGLOO2 FPGAs offer 5,000 to 150,000 LEs with a high performance memory subsystem, up to 512 kilobytes (Kbytes) of embedded flash, 2 x 32 Kbytes of embedded static random-access memory (SRAM), two direct memory access (DMA) engines, and two double data rate (DDR) controllers. The devices also feature up to 16 transceiver lanes, integrated DSP processor blocks, and single event upset (SEU) protected/tolerant memories. For security, they are differential power analysis (DPA) hardened and use AES256 and SHA256 encryption and on-demand NVM data integrity checking.

A good example of an IGLOO2 device is the M2GL025-FGG484I with 27,696 LEs, 1,130,496 bits of RAM, and 267 I/O. To allow designers to investigate and experiment with the features of the IGLOO2 FPGA family, Microchip also provides a corresponding IGLOO2 Evaluation Kit, the M2GL-EVAL-KIT (Figure 3).

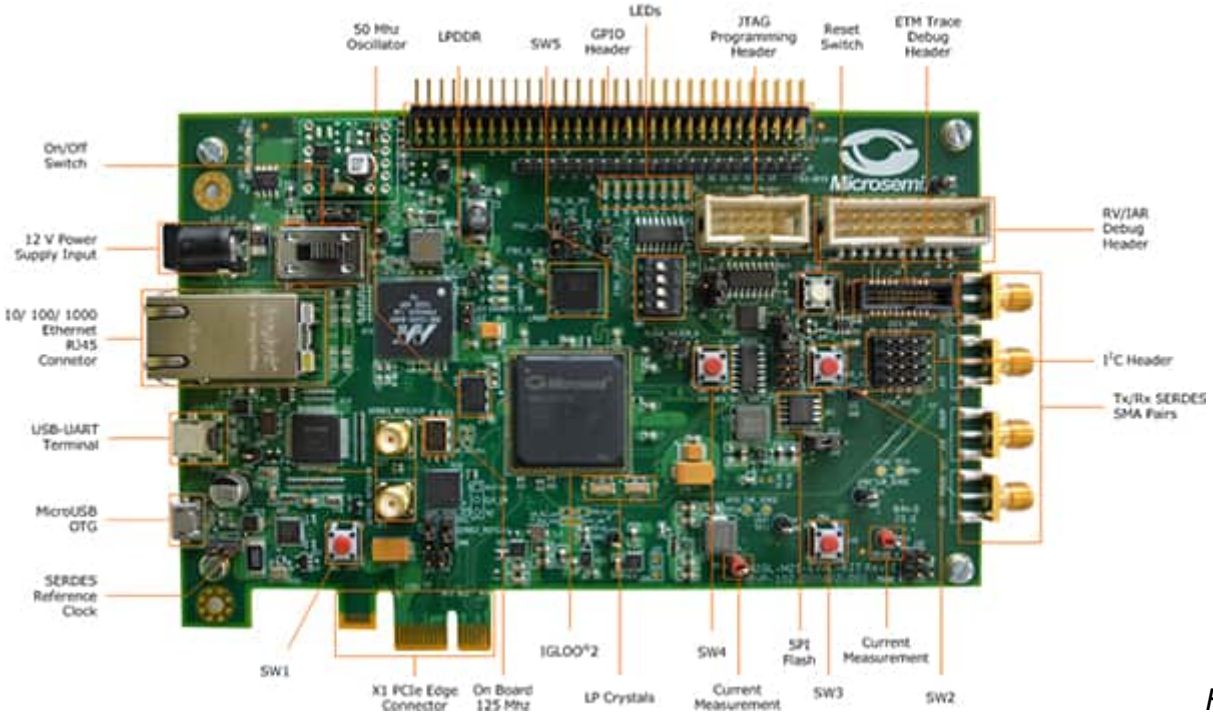

Figure 3: The M2GL-EVAL-KIT is an evaluation kit for the IGLOO2 and comes with a high level of feature integration coupled with low power, high reliability, and advanced security. (Image source: Microchip Technology)

The M2GL-EVAL-KIT makes it easy to develop embedded applications that involve motor control, system management, industrial automation and high-speed serial I/O applications, as well as PCI Express and Gigabit Ethernet. The kit offers a high degree of feature integration as well as low power, high reliability, and advanced security. The board is also small form factor PCIe compliant which lets developers prototype using any desktop PC or laptop with a PCIe slot.

Entry-level SoCs: SmartFusion2 SoC FPGAs

SmartFusion2 SoC FPGAs are based on the traditional programmable fabric found in IGLOO2 devices augmented with a 32-bit hard processor core. Since the processor is a well-known member of the Arm® Cortex® family, the SmartFusion2 family provides a great entry point into the world of SoC FPGAs.

These SoC FPGAs offer 5,000 to 150,000 LEs with a 166 megahertz (MHz) Arm Cortex-M3 processor, including embedded trace macrocell (ETM) and instruction cache with on-chip eSRAM and embedded NVM (eNVM), along with a complete microcontroller subsystem augmented with an extensive suite of peripherals including CAN, TSE, and USB.

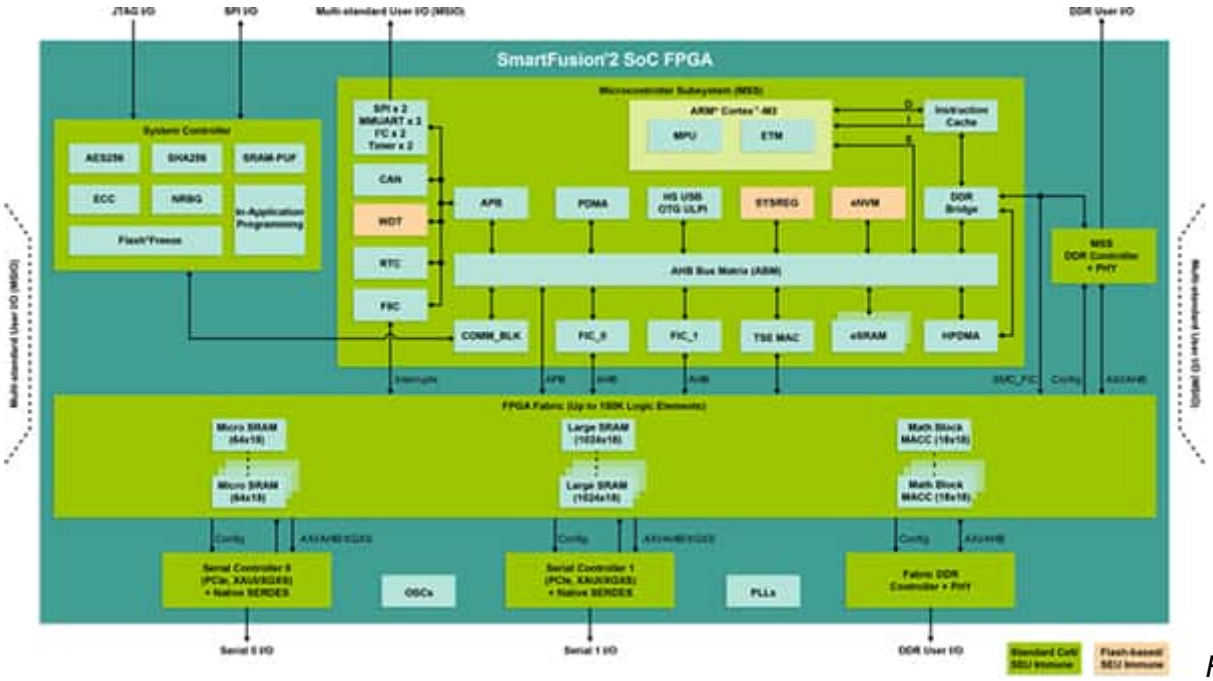

Figure 4: SmartFusion2 SoC FPGAs offer 5,000 to 150,000 LEs with a 166 MHz Arm Cortex-M3 processor, including ETM and instruction cache with on-chip eSRAM and eNVM, along with a complete microcontroller subsystem augmented with an extensive suite of peripherals including CAN, TSE, and USB. (Image source: Microchip Technology)

These flash SoC FPGA devices are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, I/O expansion and conversion, video/image processing, system management and secure connectivity. Again, applications are many and varied from communications, industrial, and medical, to defense and aviation.

A good example of a SmartFusion2 device is the M2S025-FCSG325I with 25,000 LEs, 256 Kbytes of flash, 64 Kbytes of RAM, and a 32-bit Arm Cortex-M3 processor subsystem running at 166 MHz. To allow designers to investigate and experiment with the features of the SmartFusion2 SoC FPGA family, Microchip also provides a corresponding SmartFusion2 Maker Board, the M2S010-MKR-KIT (Figure 5).

Figure 5: The SmartFusion2 Maker Board is a low-cost evaluation kit for the SmartFusion2 SoC FPGA that combines an Arm Cortex-M3 processor with flash-based FPGA fabric on a single chip, along with many of the peripherals SoC users are accustomed to such as RAM and DSP blocks. (Image source: Microchip Technology)

The low-cost SmartFusion2 Maker Board, sold exclusively by DigiKey, provides designers with access to the SmartFusion2 family. This particular device offers a flash-based FPGA fabric with 12,000 LEs, a 32-bit 166 MHz Arm Cortex-M3 processor, DSP blocks, SRAM, eNVM, and GPIO interfaces all on a single chip.

The SmartFusion2 Maker Board adds on an Ethernet interface, an ambient light sensor, SPI flash, eight user LEDS, and two user pushbuttons.The board also has two unpopulated laid out connections that support the ESP32 and the ESP8266 Wi-Fi/Bluetooth modules (not included). It supports a USB port for JTAG programming, UART communications, and powering the board. The board also features SPI flash, a 50 MHz clock source, and Microchip's VSC8541 physical layer (PHY) for 100 megabits per second (Mbits/s) or 1 gigabit per second (Gbit/s) Ethernet.

Cost-optimized, high-performance: PolarFire FPGAs and SoC FPGAs

PolarFire FPGAs are cost-optimized, high-performance devices implemented in 28 nm process technology. These devices are designed to consume the lowest power at mid-range densities with a high degree of security and reliability.

The product family spans from 100,000 to 500,000 LEs, features 12.7 Gbit transceivers, and is designed to consume up to 50% less power than competing mid-range FPGAs. The devices are ideal for a wide range of applications within wireline access networks and cellular infrastructure, defense and commercial aviation markets, as well as industrial automation and IoT markets.

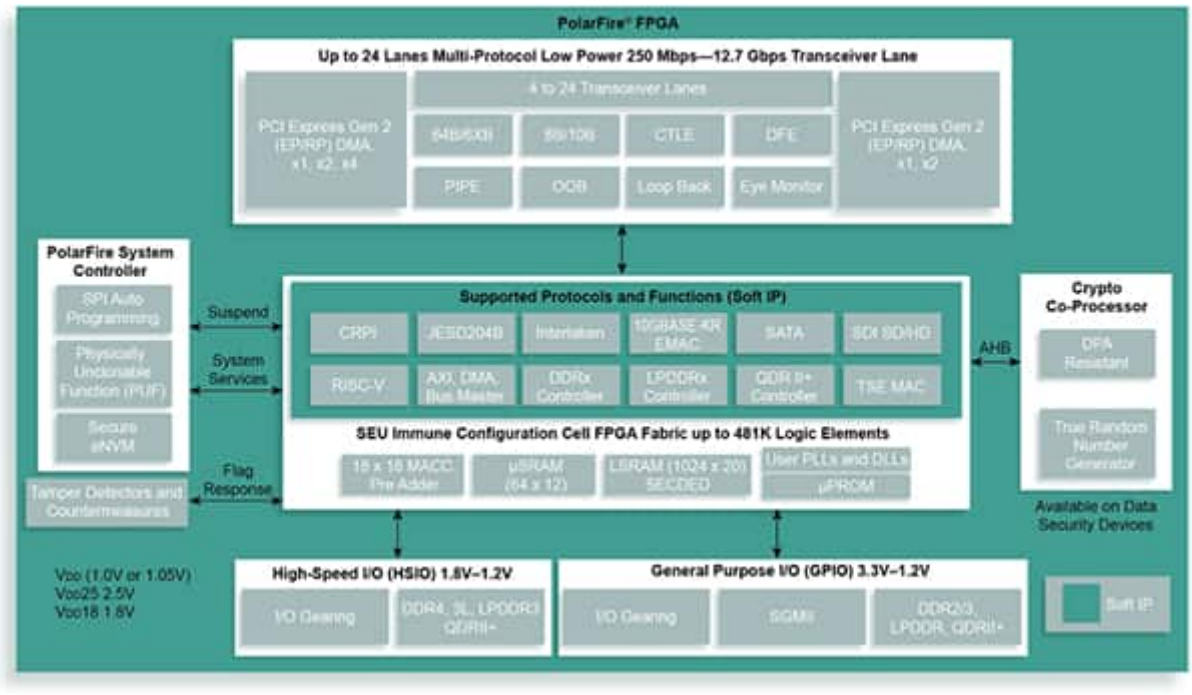

Figure 6: PolarFire FPGAs span from 100,000 to 500,000 LEs, feature 12.7 Gbit transceivers, and are designed to consume up to 50% less power than competing mid-range FPGAs. (Image source: Microchip Technology)

The main reason PolarFire FPGAs consume up to 50% less total power than competitive FPGAs is that they use NVM technology for both the on-chip configuration memory and the on-chip configuration cells. This yields inherently low leakage between configuration cells, and it also means that these devices are also true “instant-on” at power up, resulting in no in-rush current and zero configuration current.

Cybersecurity is the number one concern for connected devices on the network edge, so it is not enough for developers to simply meet the functional requirements of their design—they must do so securely. Security begins during silicon manufacturing and continues through system deployment and operation. PolarFire FPGAs are presented by Microchip as the industry's most advanced secure programmable FPGAs.

Many applications for complex electronic equipment have some degree of safety requirements in their design. PolarFire FPGAs are designed for high reliability, high availability, and safety and mission-critical systems in applications including industrial, aviation, military, and communications. Features that make PolarFire suited to these applications include:

- Zero failure in time (FIT) rate FPGA configuration
- SEU protected memories
- Memory controllers with single error correction, double error detection (SECDED)
- Built-in self-test
- No external configuration device required

A good example of a PolarFire device is the MPF100T-FCSG325I with 109,000 LEs, 7,782,400 bits of RAM, and 170 I/O. To allow designers to investigate and experiment with the features of the PolarFire FPGA family, Microchip also provides a corresponding PolarFire FPGA evaluation kit, the MPF300-EVAL-KIT (Figure 7).

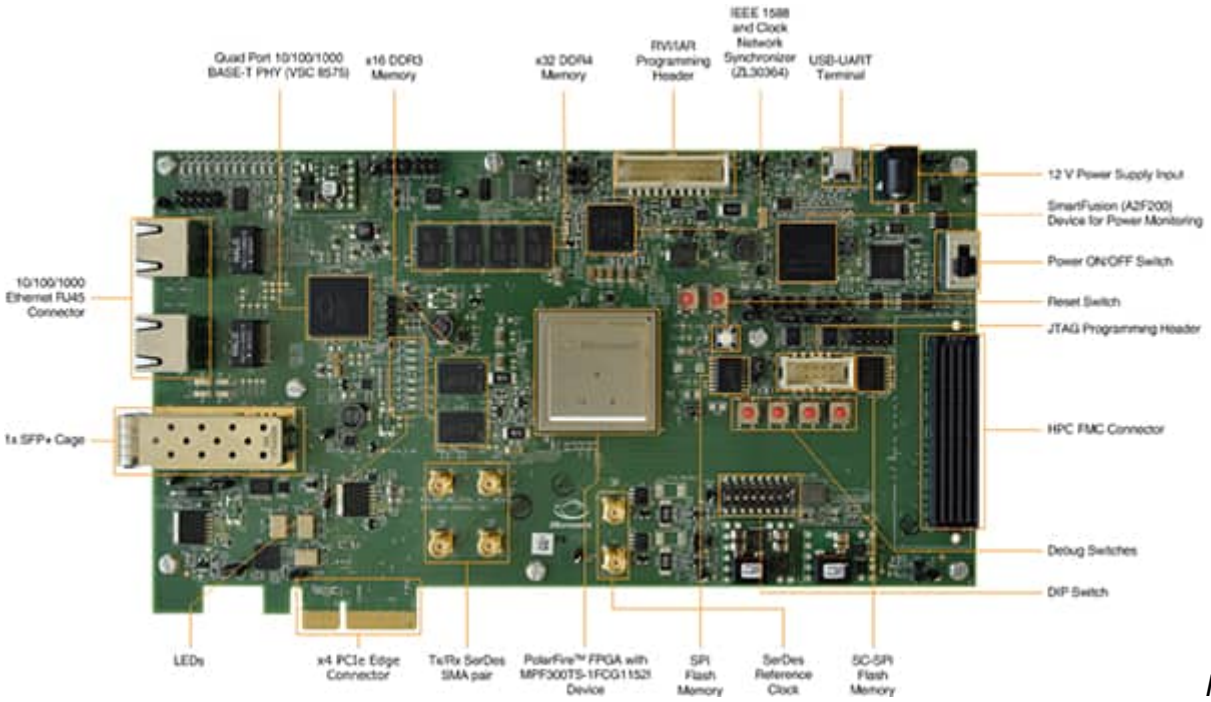

Figure 7: To allow designers to investigate and experiment with the features of its PolarFire FPGA family, Microchip also provides the corresponding MPF300-EVAL-KIT FPGA evaluation kit. (Image source: Microchip Technology)

The MPF300-EVAL-KIT offers high-performance evaluation across a broad class of applications. It's ideally suited for high-speed transceiver evaluation, 10 Gbit Ethernet, IEEE1588, JESD204B, SyncE, and CPRI, among others. The kit connections include a high pin count (HPC) FPGA mezzanine card (FMC), numerous SMAs, PCIe, Dual Gigabit Ethernet RJ45, SFP+, and USB. A 300,000 LE PolarFire FPGA with DDR4, DDR3 and SPI flash allows a broad class of high-performance designs to be developed.

Advances in the PolarFire line continue. At the time of this writing, Microchip Technology unveiled details regarding their forthcoming PolarFire SoC FPGA family boasting a hardened real-time, Linux-capable, open source 64-bit RISC-V-based microprocessor subsystem.

Design and development with Microchip Technology's FPGAs

One of the most common techniques used to develop with FPGAs is that of language-driven design (LDD). This involves capturing the design intent at a level of abstraction known as register transfer level (RTL) using a hardware description language (HDL) such as Verilog, VHDL, or SystemVerilog. Following verification via logic simulation, this representation is then fed into a synthesis engine, along with additional information such as the target FPGA type, pin assignments, and timing constraints (e.g., maximum input to output delays). The output from the synthesis engine is a configuration file which is loaded directly into the FPGA in the case of a Microchip FPGA or SoC FPGA, or loaded into an external memory device in the case of SRAM-based devices (Figure 6).

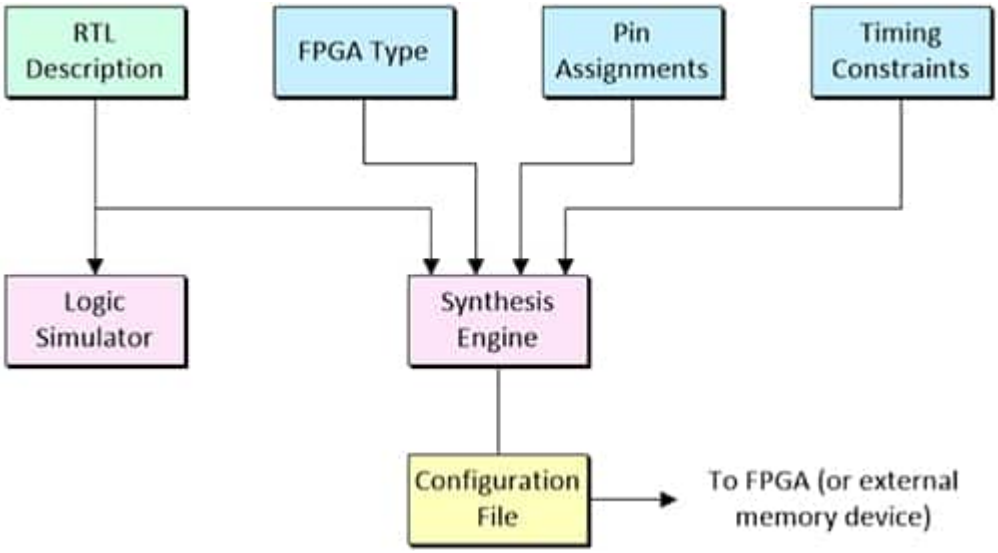

Figure 8: Following verification via logic simulation, the RTL design description is fed into a synthesis engine, along with additional design details like the FPGA type, pin assignments, and timing constraints. The output from the synthesis engine is a configuration file which is loaded directly into the FPGA. (Image source: Max Maxfield)

Microchip's Libero SoC Design Suite falls into this class of tool. This software offers a comprehensive suite of integrated, easy-to-learn, easy-to-adopt development tools for designing with Microchip's IGLOO2 and PolarFire FPGAs, and SmartFusion2 and PolarFire SoC FPGAs. The suite integrates industry standard Synopsys Synplify Pro synthesis and Mentor Graphics' ModelSim simulation with constraints management, programming and debug tools, and secure production programming support.

In addition to capturing designs in textual format using Verilog, VHDL, or SystemVerilog, the suite also includes graphical entry whereby the system can be defined as a hierarchy of connected blocks, with the lower level blocks being represented in user-defined HDL or as third-party IP.

There's also the System Builder, which is an easy-to-use design tool that walks users through a set of high-level questions that will define the intended system. The System Builder starts by asking questions about the desired system architecture, adds any additional peripherals that are to be implemented as soft cores in the programmable fabric, and ends up creating a correct-by-design complete system.

Last but not least is the SoftConsole integrated development environment (IDE) that facilitates the rapid development of bare-metal and RTOS-based C/C++ software for 32-bit soft processors instantiated in Microchip's FPGA and SoC FPGAs, along with the 32-bit and 64-bit hard processor cores found in SmartFusion2 and PolarFire SoC FPGAs, respectively.

Conclusion

Optimal processing design solutions are often provided by combinations of processors and FPGAs, by FPGAs on their own, or by FPGAs that boast hard processor cores as part of their fabric. As a technology, FPGAs have evolved rapidly over the years and are able to address many design requirements in terms of flexibility, processing speed, and power, making them very useful for a wide range of applications from intelligent interfaces to machine vision and AI.

As shown, Microchip Technology's FPGA and SoC FPGA offerings span the low- to mid-range, with a focus on low-power, high-security devices with exceptional reliability. The FPGAs have robust signal processing and memory resources and are an excellent platform upon which to develop applications such as hardware acceleration, artificial intelligence, image processing, and edge computing in industries ranging from communications and industrial, to military and aviation.

About this author

Clive "Max" Maxfield

Clive "Max" Maxfield received his BSc in Control Engineering in 1980 from Sheffield Hallam University, England and began his career as a designer of central processing units (CPUs) for mainframe computers. Over the years, Max has designed everything from silicon chips to circuit boards and from brainwave amplifiers to steampunk Prognostication Engines (don't ask). He has also been at the forefront of Electronic Design Automation (EDA) for more than 30 years.

Max is the author and/or co-author of a number of books, including Designus Maximus Unleashed (banned in Alabama), Bebop to the Boolean Boogie (An Unconventional Guide to Electronics), EDA: Where Electronics Begins, FPGAs: Instant Access, and How Computers Do Math. Check out his “Max’s Cool Beans” blog.

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