DAY 5

FULL ADDER

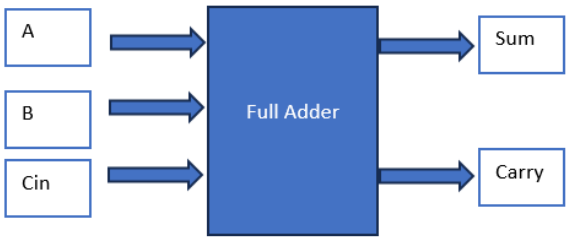
The full-adder accepts two input bits and an input carry and generates a sum output and an output carry.

The basic difference between a full-adder and a half-adder is that the full-adder accepts an input carry.

Truth Table

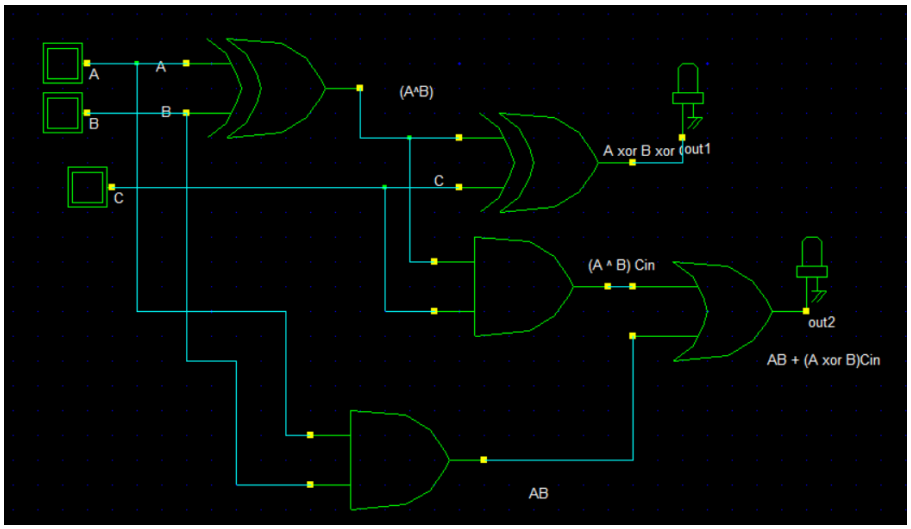
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Diagram



Gate level

```
module  Full_Adder( A,B,Cin,Sum,Carry);
   input A,B,Cin;
   output Sum,Carry;
   wire w1,w2,w3,w4,w5;
   xor G1(w1,A,B);
   xor G2(w2,w1,Cin);
   and G3(w3,w1,Cin);
   and G4(w4,A,B);
   or G5(w5,w4,w3);
endmodule
```



Dataflow

```
module Adder(A,B,Sum,Carry,Cin);
  input A,B,Cin;
  output Sum,Carry;
assign Sum = (A^B^Cin);
assign Carry = ((A&B)|(A^B)&Cin);
endmodule
```

Behavioral

```
module Adder(A,B,Cin,Sum,Cout);
  input A,B,Cin;
  output  Sum,Cout;
  reg Sum,Cout;
  always @(A,B,Cin)
  begin
     Sum = (A^B^Cin);
     Carry = ((A&B)|(A^B)&Cin);
  end
endmodule
```

Simulation Waveform