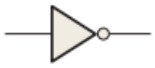
DAY 1

NOT GATE

Theory :-

It performs the complement of input. ie it changes a 1 to a 0 and a 0 to a 1.

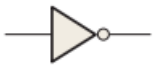
Symbol:-



When a HIGH level is applied to an inverter input, a LOW level will appear on its output. When a LOW level is applied to its input, a HIGH will appear on its output,This operation is called " inversion or complementation"

Truth Table :

INPUT	OUTPUT
0	1
1	0



A = A'

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Gate level modelling

```
module Not_gate(A,Y);
 input A;
output Y;
not (Y,A);
endmodule
```

Design Flow Modelling

```
module not_design(A<Y);
 input A;
output Y;
assign y = (~A);
endmodule
```

NOT_GATE Using PMOS and NMOS

The PMOS transistor will activate when the input is logic 0 (0V), and the NMOS transistor will activate when the input is logic 1 (Vcc).

Components:

1. PMOS transistor (P1)
2. NMOS transistor (N1)
3. Input button
4. Output LED
5. Power supply (Vcc)

Description:

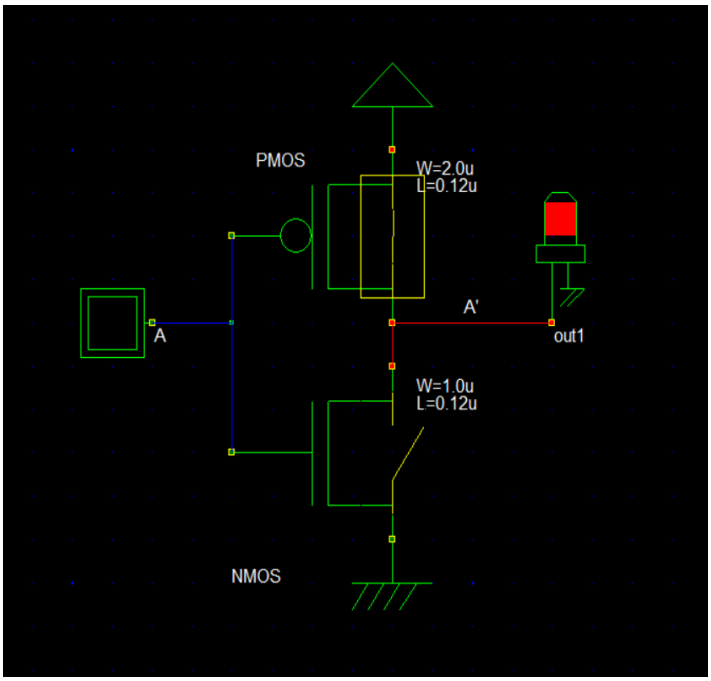
- Connect the source terminal of the PMOS transistor (P1) to the power supply Vcc (usually a positive voltage).
- Connect the source terminal of the NMOS transistor (N1) to the ground (0V).
- Connect the gate terminal of P1 to the input button, and connect the gate terminal of N1 to the same input button.
- Connect the drain terminal of P1 to the drain terminal of N1.
- Connect the output LED between the common drain connection of P1 and N1 and the ground (0V).

Operation:

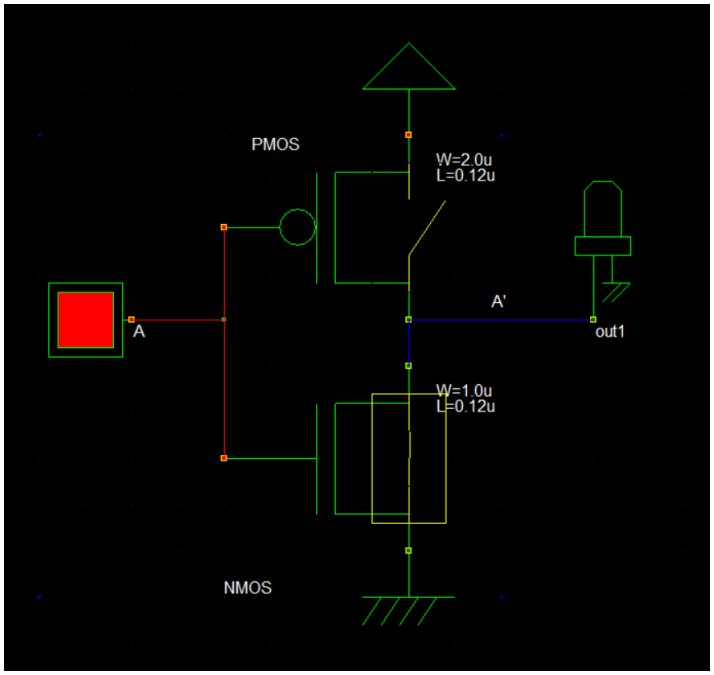
- When the input button is pressed (logic 1), the NMOS transistor (N1) turns ON, creating a low-resistance path to ground. This allows current to flow from Vcc through N1 to ground, and the output LED remains OFF.
- When the input button is released (logic 0), the PMOS transistor (P1) turns ON, creating a low-resistance path between Vcc and the common drain connection. This turns ON the output LED because the connection to ground is effectively cut off, and the LED illuminates.

NOT_GATE Using PMOS and NMOS

1] when no button is pressed .



2] when button is pressed .



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