Day 8

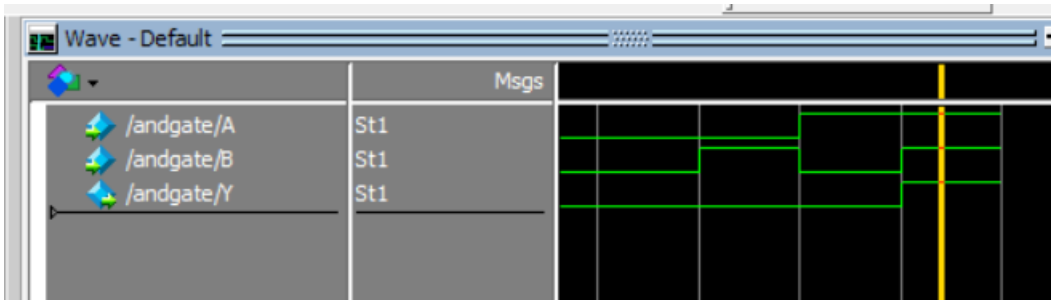
All gates Using Nand

1] And gate :

A.B = A''B''.

```
module andgate(A,B,Y);
 input A,B;
 output Y;
 assign Y = (~(~(A and B)));
endmodule;
```

Simulation waveform :

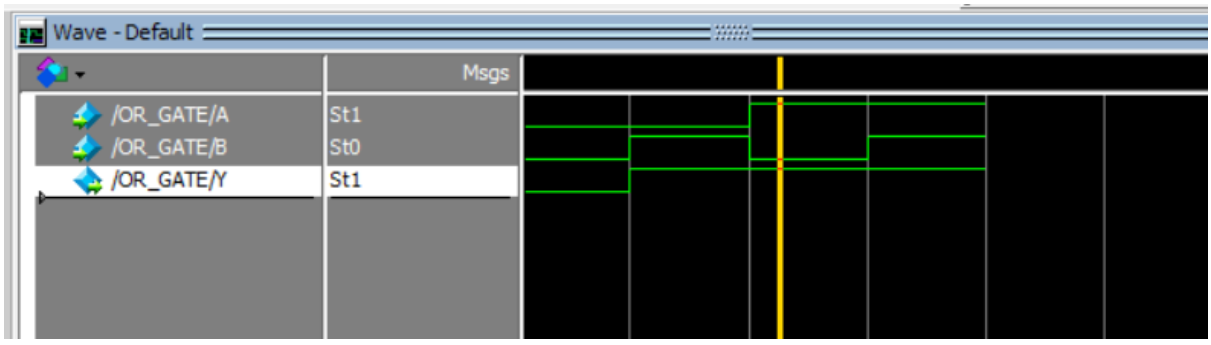


2] OR Gate :

A+B = (A'.B')'

```
module orgate(A,B,Y);
 input A,B;
 output Y;
 assign Y = ~((~A) & (~B));
endmodule
```

Simulation waveform:



3] Not gate

A’ = (A’A’)

```
module notgate(A,Y);
 input A;
 output Y;
 assign Y = (~A & ~A);
endmodule
```

Simulation waveform: