DAY – 6

HALF SUBSTRACTOR

Theory :-

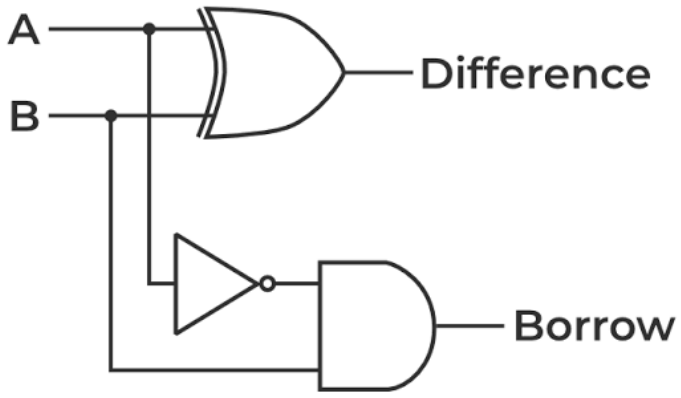
The half subtractor is a building block for subtracting two binary numbers. It has the following characteristics:

Two inputs, A and B

Two outputs, Difference and Borrow

The Difference output is the resultant of the Exclusive-OR gate

Circuit Diagram



Expression

D = A ^ B

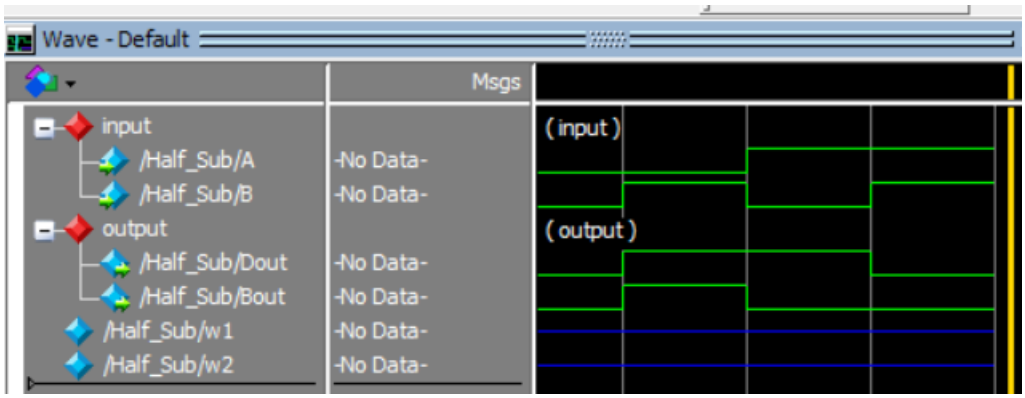
Bout = A’ B;

Truth Table

A	B	Dout	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

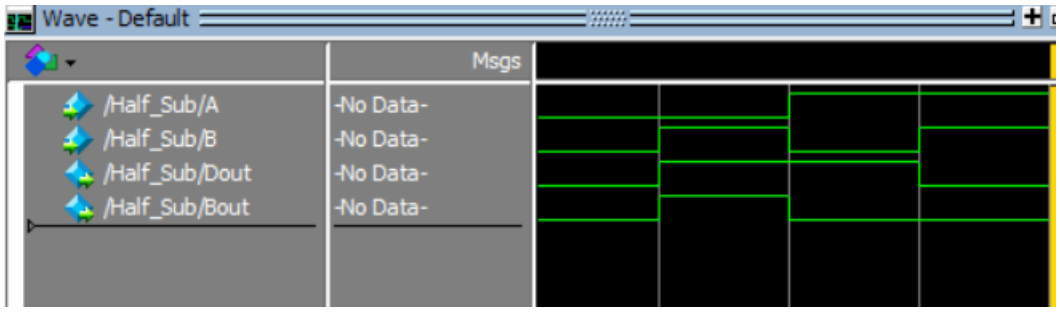
Verilog Code using Gate Level:

```
module Half_Sub(A,B,Dout,Bout);
 input A,B;
 output Dout,Bout;
 wire  w1 ,w2;
 xor g1(Dout,A,B);
 and  g2(Bout , ~A , B);
endmodule
```



Data Flow

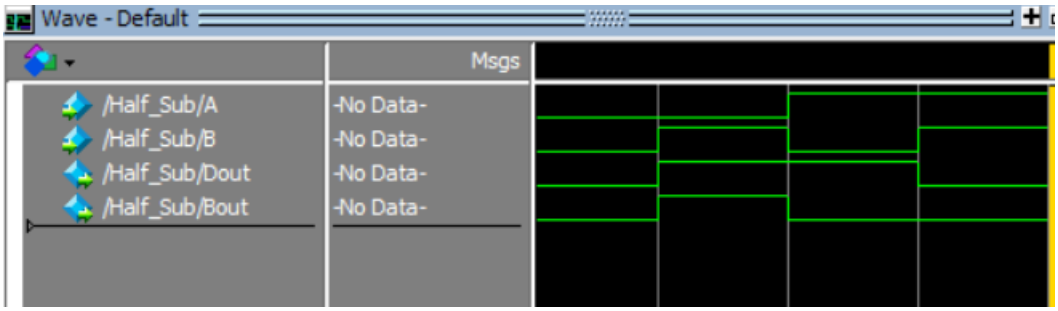
```
module Half_Sub(A,B Dout,Bout);
 input A,B;
 output Dout,Bout;
 assign Dout = (A^B);
 assign Bout = (~A & B);
endmodule
```

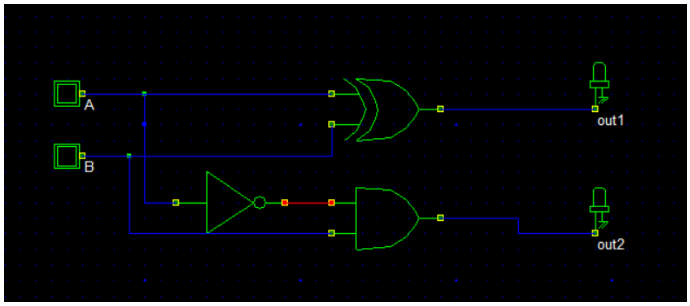


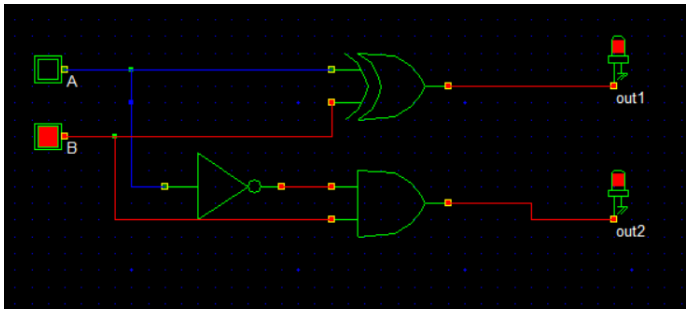
Behavioral

```
module half_subtractor( A,B,Dout,Bout);
input A,B;
output reg Dout,Bout;


always @(*)
   begin
      Dout = A^B;
      Bout = (~A) & B ;
   end
endmodule
```




A
B
out1
out2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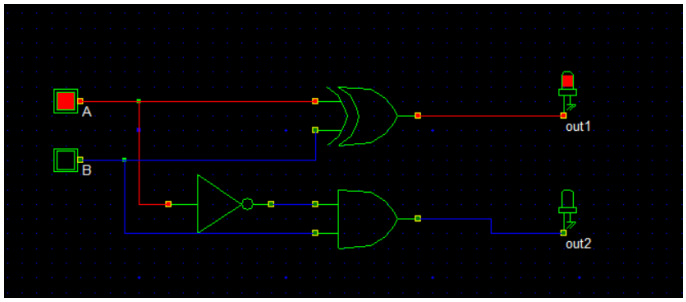
B
out1
out2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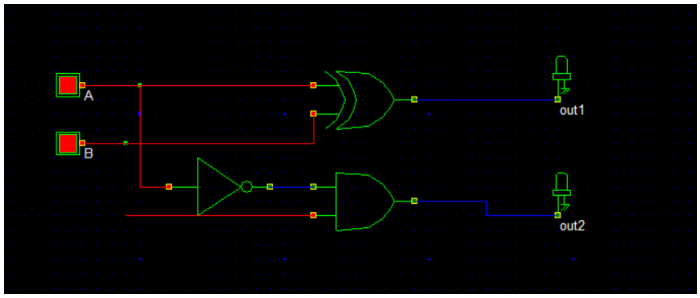
out1
out2


A
B
out1
out2