Day 2

OR Gate

Theory –

It perform the logical OR operation ie if any input is 1 then the output is 1 and if all the input is zero then the output is zero.

Symbol :-

Expression –

A or B = Y

Truth table :-

X1	X1	Y(output)
0	0	0
0	1	1
1	0	1
1	1	1

Verilog Modelling

Gate Level –

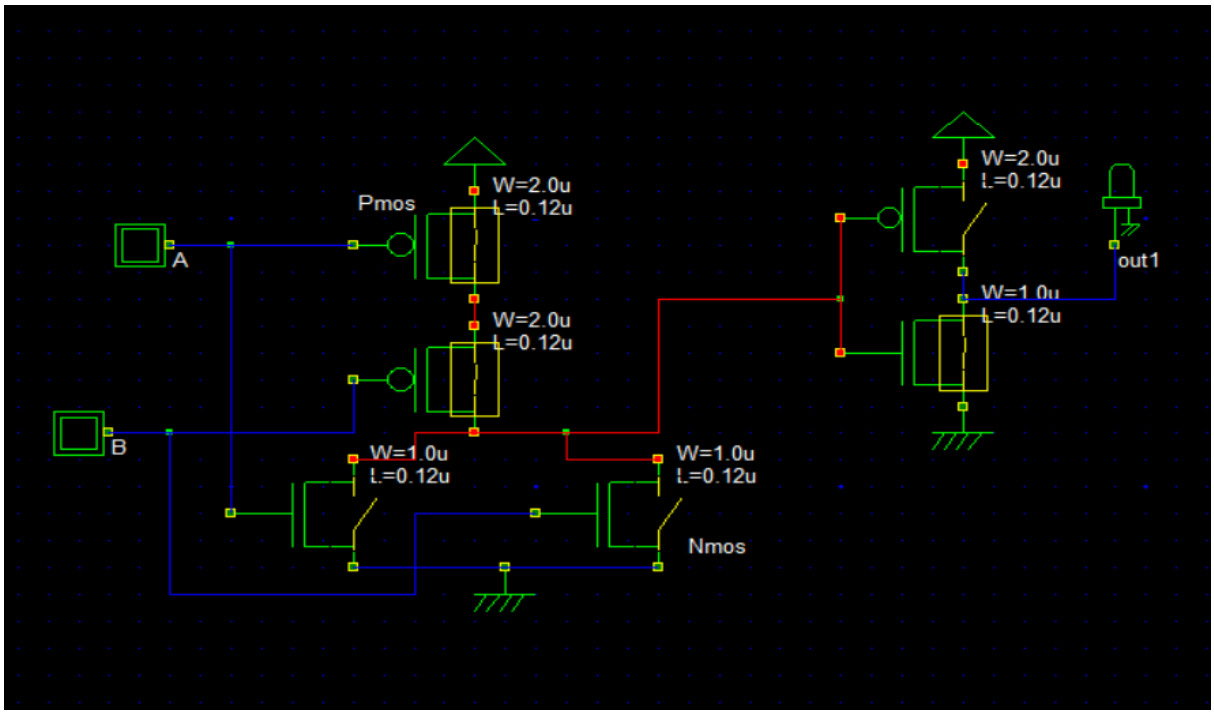
```
module OR_GATE( input A,B,
                output Y);
  or gate(Y,A,B);
endmodule
```

DataFlow –

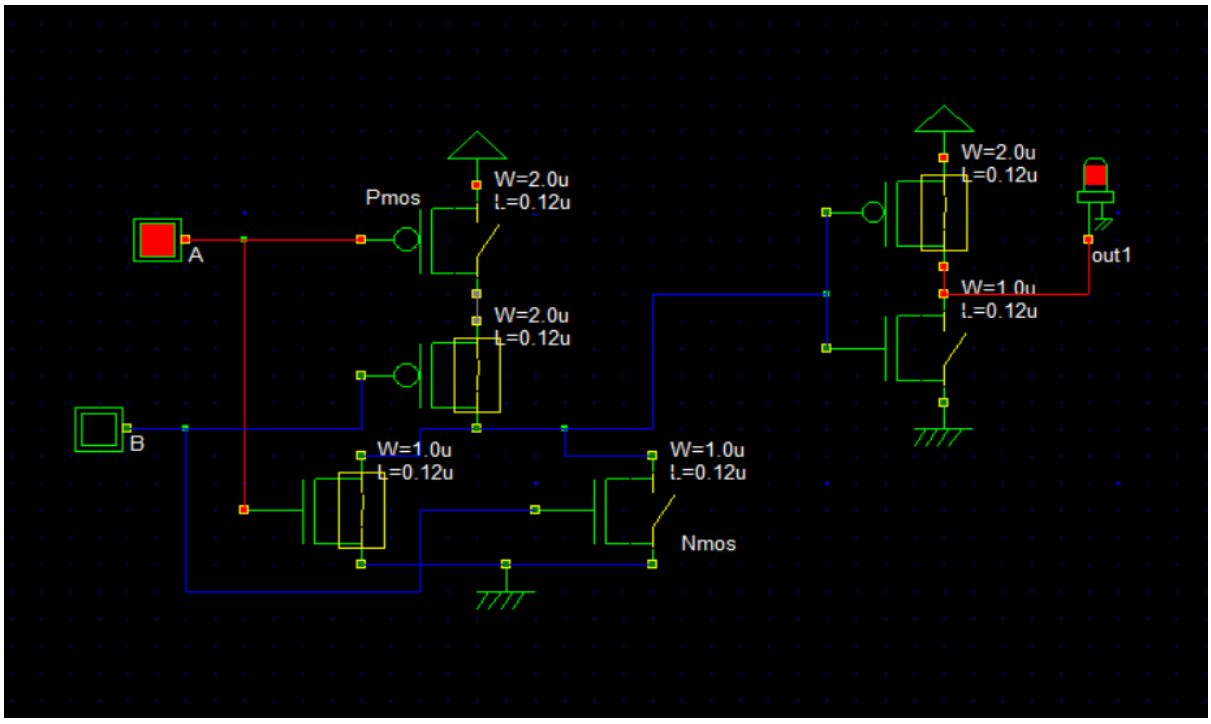
```
module  or_gate(A,B,C,Y);
 input A,B,C;
 output Y;
 assign Y = (A||B||C);
endmodule
```

OR_GATE Using PMOS and NMOS

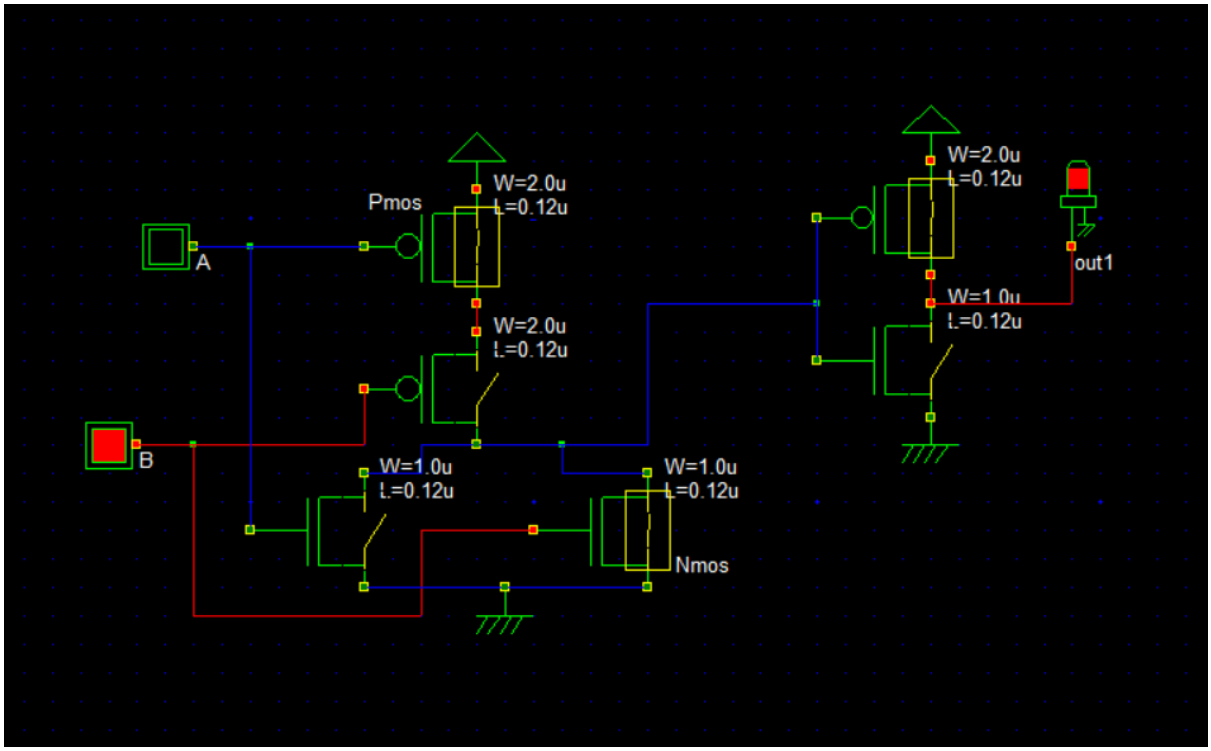
When input is : A=0 and B=0



When input is : A=1 and B=0



When input is : A=0 and B=1



When input is : A=1 and B = 1