CMOS Project

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1 Specifications:

- Single ended output
- Open loop small signal low-frequency voltage gain > 100 dB
- Unity gain bandwidth > 10 MHz
- Input CM voltage range : 100 mV to 1.7 V
- Output voltage range : 100 mV to 1.7 V
- Phase margin > 60^0 (Load Capacitance = 5 pF)
- Slew rate > 2 V/us (Load Capacitance = 5 pF)

1.1 Values taken for 180um length:

- $\lambda_n = 0.1\text{V}^{-1}$
- $\lambda_p = 0.2\text{V}^{-1}$
- V_{thn} = 0.3999 V
- V_{thp} = -0.42 V
- $k_n = 0.3 * 10^{-3} uA/V^2$
- $k_p = 68 * 10^{-6} uA/V^2$

2 Op-amp design flow

2.1 Design flow

The design flow of the op-amp is as follows:
1. Slew Rate :

$$SlewRate > 2V/us$$

To start the calculations, we assume a slew rate which is higher**(let's say 5 V/us)**

$$Iss/Cc = SR$$

Since we have no power specification, we start by assuming a value of Iss = 24 us.
Therefore,

$$20/Cc = SR$$

so, **Cc = 4pF** for initial considerations.

2. Unity Gain Frequency > 10 MHz :

Considering the value on higher side**(15 MHz)**

$$gm_1/(2\pi Cc) = Fugf$$

Therefore, gm is calculated. Now as the gm of the driving mosfets will be same so,

$$gm_1 = gm_2 = gm_3 = gm_4$$

Design of M1, M2, M3 and M4.

Vdsat1 is calculated for M1 using gm1 and

$$Idm1 = Iss/2$$

Therefore $(W/L)_1$ is calculated.
Since M1 and M2 should be identical for Differential amplifier.
Therefore, $(W/L)_1 = (W/L)_2$

Considering same gm for M3 and M4.

We calculate (W/L) for M3 and M4.

3 . Input Common Mode Range (100 mV to 1700 mV) :

We assume a common mode of 900 mV for design of M5 and M6.
Above 900 mV $->$ NMOS is considered to be operational.
Similiarly, below 900 mV $->$ PMOS is considered to be operational.
For NMOS considering,

$$Vinp_{min} = 900mV$$

and using relation,

$$Vdsat_5 = Vinp_{min} - Vdsat_1 - Vtn$$

we calculated Vdsat5.
Since, **I = Iss**
(W/L) of M5 is calculated.
Similar approach is used for calculating (W/L) for M6.

4. Phase Margin > 60°:

$$gm_{20}/2\pi C_L = Fnd$$

This relation is obtained by using,

$$PM = 90^0 - \tan^{-1}(Fugf/Fnd).....\mathbf{1}$$

C_L is given, so Fnd is obtained from the relation **1**. Therefore gm_20 is obtained. Similiarly for gm_19 is obtained.

Designing of M19 and M20

Designing for Slew Rate.

$$I20 = Iss * (1 + (C_L/C_C))$$

and gm20. Therefore, (W/L) of M19 and M20 is calculated.

M7 and M8, M17 and M18 are designed to carry a larger current than Iss and assuming a value of Vdsat as same as M19 and M20.

Designing of the other Mosfets:

Designing of M15, M16, M9, M10 is done by assuming current Iss/2 and the Vdsat across them.

The remaining transistors M11, M12, M13, M14 is based on designing of remaining transistors which have already been designed and considering there current to be Iss/4 in normal operating region.

***So, we got the following results from our calculations*:**
For these calculations we assumed the value of bias currents(Iss) to be <u>24 uA</u>.

Here we changed the value of C_{C1} and C_{C2} to,

$$C_{c1} = 2pF$$

$$C_{C2} = 2pF$$

Here are the initial calculated sizes of the transistor:

Transistor	**Width (um)**	**Length (um)**
M1	32	1u
M2	32	1u
M3	141.176	1u
M4	141.176	1u
M5	0.640	1u
M6	3.064	1u
M7	11.294	1u
M8	11.294	1u
M9	2.001	1u
M10	2.001	1u
M11	0.628	1u
M12	0.142	1u
M13	0.142	1u
M14	0.628	1u
M15	0.5	1u
M16	0.5	1u
M17	4	1u
M18	4	1u
M19	480	0.71u
M20	160	0.71u

The bias currents of the transistors are:

Transistor	Current (uA)
M1	12
M2	12
M3	12
M4	12
M5	24
M6	24
M7	24
M8	24
M9	12
M10	12
M11	6
M12	6
M13	6
M14	6
M15	12
M16	12
M17	24
M18	24
M19	27
M20	27

The bias voltages of the transistors are:

Bias Voltages	Value(V)
Vbp	0.9
Vbn	0.9
Vb1	0.71
Vb2	0.9998
Vb3	0.1799
Vb4	1.5299

2.2 Reiterating to achieve target specification

Now, as we kept the above data in the model the desired result was not obtained. The reason behind this might because of the approximations we took during the calculations as well as the parasitic we ignored. So, we followed the following:

1. If we wanted to increase the unity gain frequency of the op-amp we increased the gm of Mosfets M1 and M2.
2. If we wanted to increase the slew rate the we increased the Iss or I bias.
3. If the gain was to be increased then we increased the W/L of the transistors M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17 and M18.
4. If we wanted to increase the phase margin, we increased the W/L of transistors M19 and M20.
5. The circuit gave good gain for certain ratio of the W/L of M19 and M20 for second stage.

6. Now as **Lambda** is inversely proportional to Length so in order to increase the **Rout** we decreased the L of the Mosfets.

2.3 Schematic

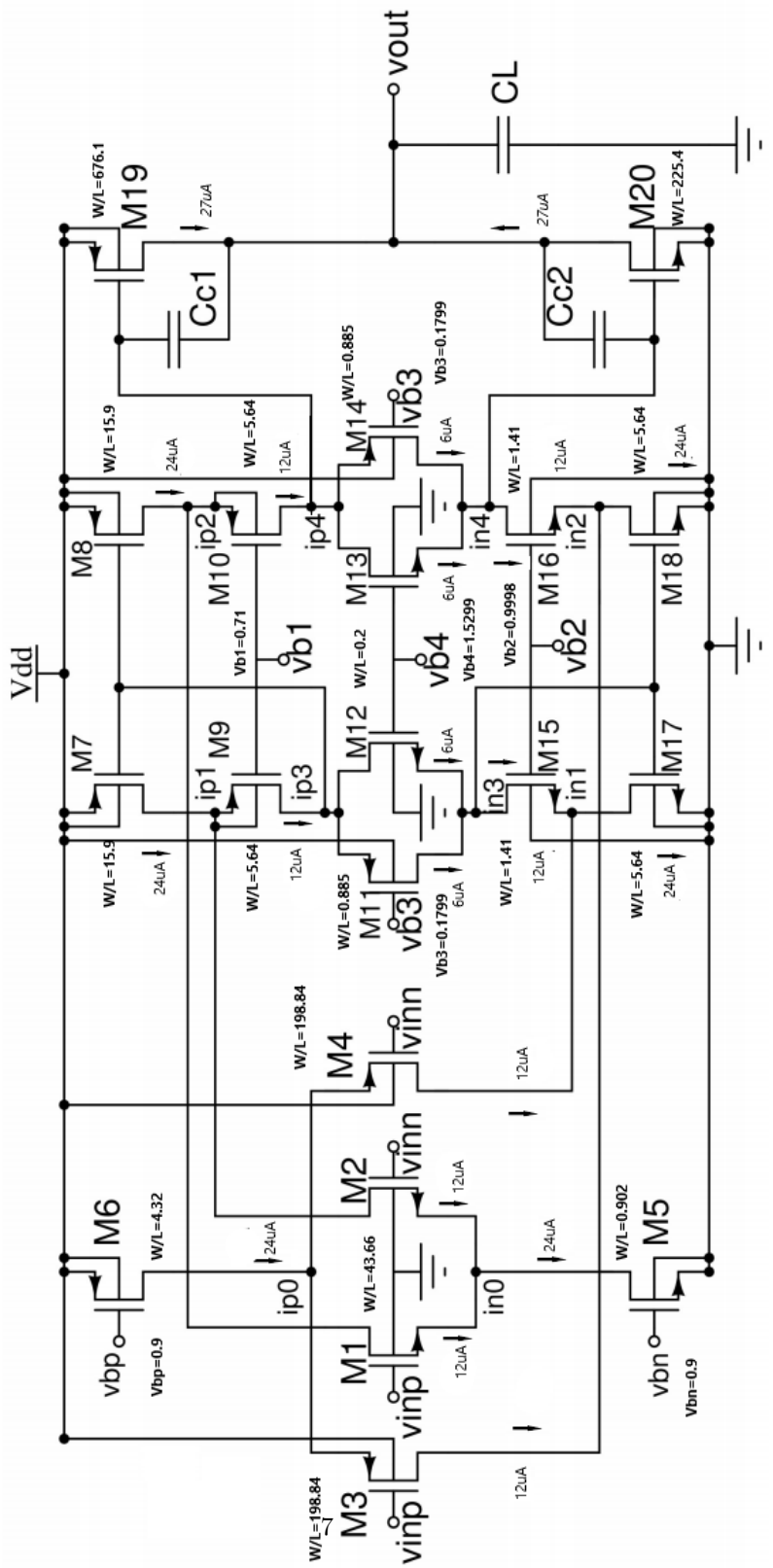

Figure 1: OP-AMP circuit.

These are the actual final values of the sizes of transistors:

Transistor	Width (um)	Length (um)
M1	31	0.71u
M2	31	0.71u
M3	141.176	0.71u
M4	141.176	0.71u
M5	0.640	0.71u
M6	3.064	0.71u
M7	11.294	0.71u
M8	11.294	0.71u
M9	4.002	0.71u
M10	4.002	0.71u
M11	0.628	0.71u
M12	0.142	0.71u
M13	0.142	0.71u
M14	0.628	0.71u
M15	1	0.71u
M16	1	0.71u
M17	4	0.71u
M18	4	0.71u
M19	480	0.71u
M20	160	0.71u

3 Reference Generator Circuit Design

3.1 Schematic

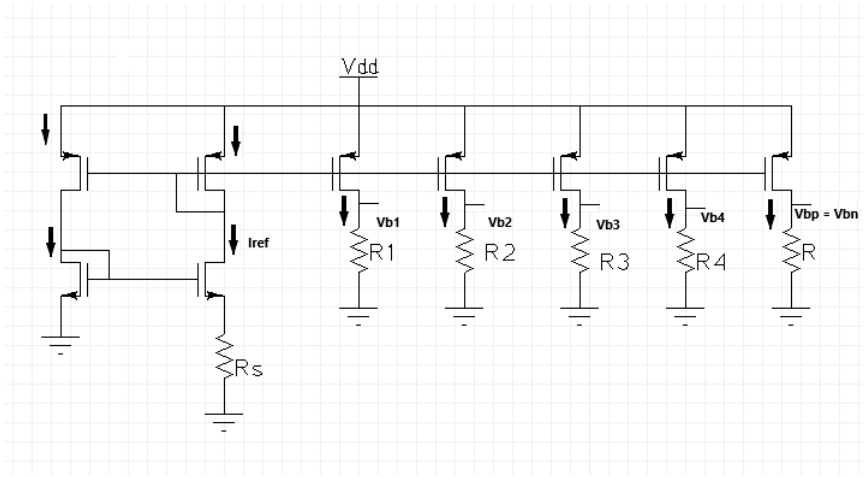

Figure 2: Reference Generator circuit.

3.2 Design procedure

Now below we will give the design procedure for the reference generator:

1. First we generate a reference current using the current mirror model at the leftmost in the circuit diagram of the reference generator circuit. By selecting a suitable value of Rs and fixing the other parameters.

$$I_{ref} = \frac{2}{\mu_n C_{ox} \frac{W}{L} R_s^2} (1 - \frac{1}{\sqrt{k}})^2$$

2. Now connecting the gate of the PMOS together to mirror the current and keeping the sizes of all the PMOS same, this is also done for the NMOS.

3. Now from the calulated bias voltages and the reference current we calculate the resistances required for all the bias voltages.

4. Here in our case we kept the Vbn = Vbp. So we derived only on source for them.

3.3 Data about reference generator

:

Transistor	**Width (um)**	**Length (um)**
M21	0.0876	2u
M22	0.7884	2u
M23	0.4366	2u
M24	0.4366	2u
M25	4.366	2u
M26	4.366	2u
M27	4.336	2u
M28	4.366	2u
M29	4.366	2u

Resistor	**Value (KOhms)**
Rs	252
R	89.282
R1	69.972
R2	99.58
R3	17.33
R4	165.5

4 DC Simulation

4.1 Schematic

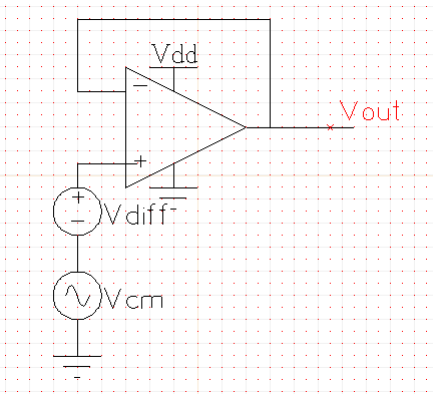

Figure 3: Circuit for DC analysis.

4.2 DC operating points

```
No. of Data Rows : 1
is1 = 9.574779e-06
@m2[id] = 9.574779e-06
@m3[id] = 9.717710e-06
@m4[id] = 9.717710e-06
@m5[id] = 1.914955e-05
@m6[id] = 1.943541e-05
@m7[id] = 1.481527e-05
@m8[id] = 1.481527e-05
@m9[id] = 5.240486e-06
@m10[id] = 5.240486e-06
@m11[id] = 2.777204e-06
@m12[id] = 2.463283e-06
@m13[id] = 2.463283e-06
@m14[id] = 2.777204e-06
@m15[id] = 5.240484e-06
@m16[id] = 5.240484e-06
@m17[id] = 1.495819e-05
@m18[id] = 1.495819e-05
@m19[id] = 6.673731e-04
@m20[id] = 6.673731e-04
v(ip0) = 1.458303e+00
v(ip1) = 1.365362e+00
v(ip2) = 1.365362e+00
v(ip3) = 1.150147e+00
v(ip4) = 1.150147e+00
v(in1) = 2.956170e-01
v(in2) = 2.956170e-01
v(in3) = 5.847786e-01
v(in4) = 5.847786e-01
v(vout) = 1.063083e+00
ngspice 3 ->
```

opamp_dcanalysis.cir

Figure 4: DC Operating points.

5 AC Simulation

5.1 Schematic

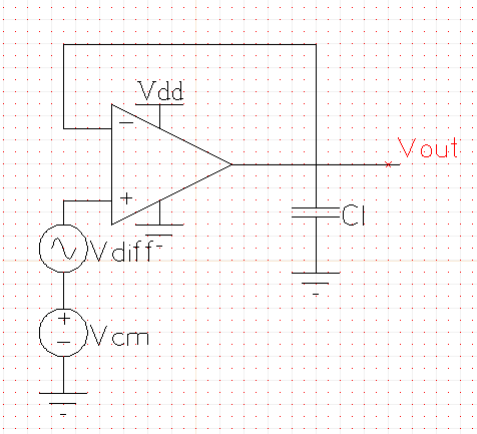

Figure 5: Circuit for AC analysis.

5.2 AC plots

5.2.1 AC Magnitude Plot

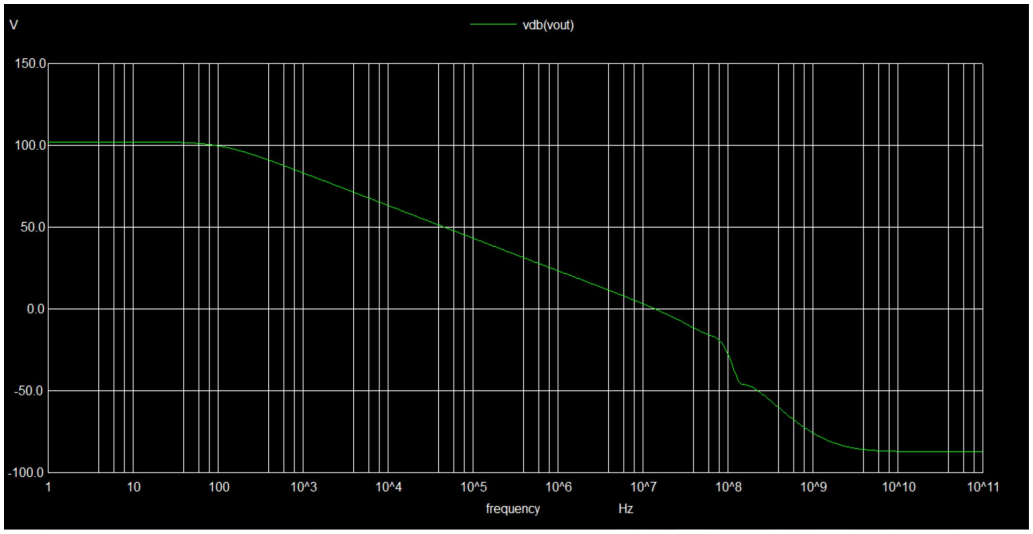

Figure 6: Magnitude plot for AC analysis.

5.2.2 AC Pole Zero Plot

The simulated poles are :

Figure 7: Pole Zero plot for AC analysis.

The calculated Poles and Zeros of the circuit are: The calculated poles are :

1. P1 = $5.895 * 10^3$ Hz
2. P2 = $91.732 * 10^3$ Hz

The calculated zeros are :

1. Z1 = $540 * 10^6$ Hz

5.2.3 AC Phase Plot

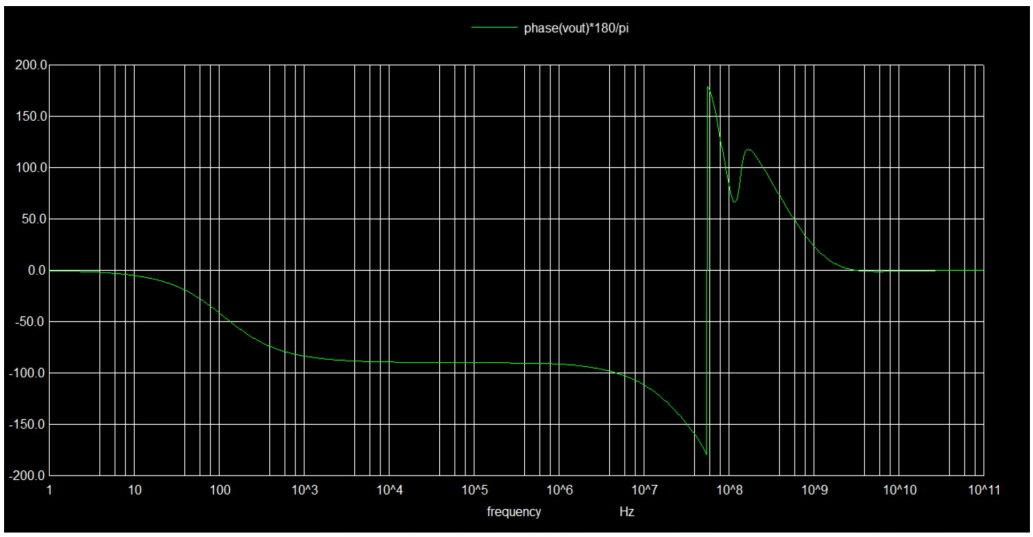

Figure 8: Phase plot for AC analysis.

5.2.4 AC Phase Margin

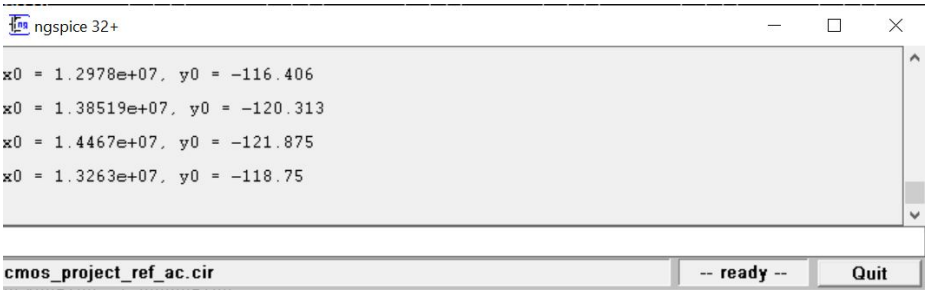

Figure 9: Phase Margin for AC analysis.

From here we can see that,For the ***Unity Gain Frequency*** of **13.15 MHz** we get the

$$\textbf{\textit{Phase Margin}} \ = 62^0$$

.

5.2.5 Roll Of Factor

Here in order to calculate the **Roll Of Factor** we find the slope from the half of the Unity Gain Frequency to the Unity Gain Frequency, which came out to be

$$\textbf{Roll of} \ = -9.626 * 10^7$$

Which is also interpreted as approx **-160 db/dec**.

6 Slew Rate Simulation

6.1 Schematic

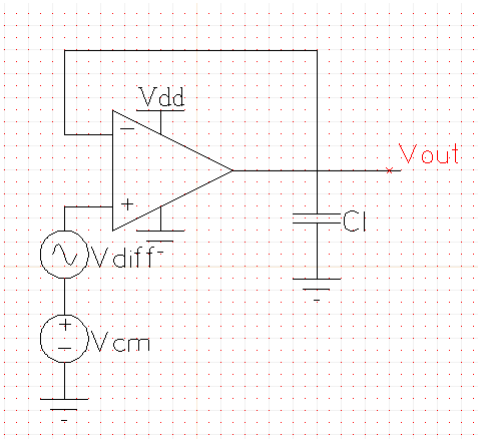

Figure 10: Circuit for Slew Rate Analysis.

6.2 Simulation

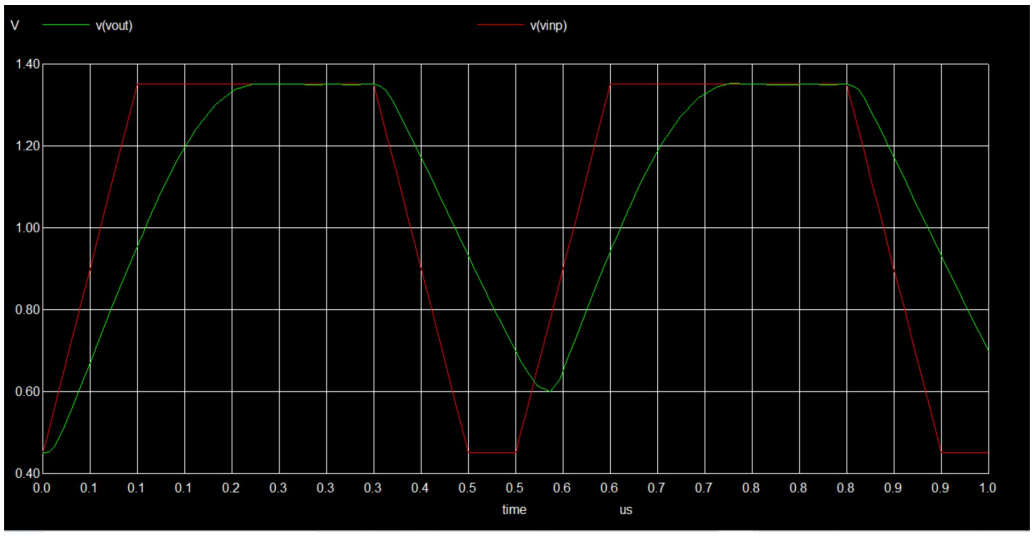

Figure 11: Simulation for Slew Rate Analysis.

6.3 Slew Rate

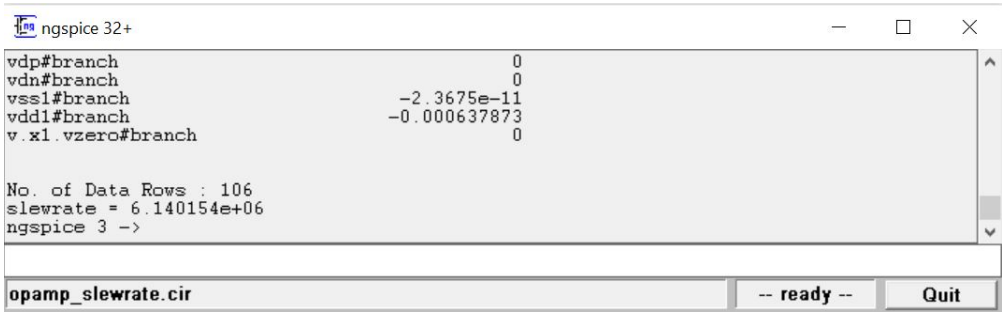

Figure 12: Slew Rate Analysis.

7 Transient Simulation

7.1 Schematic

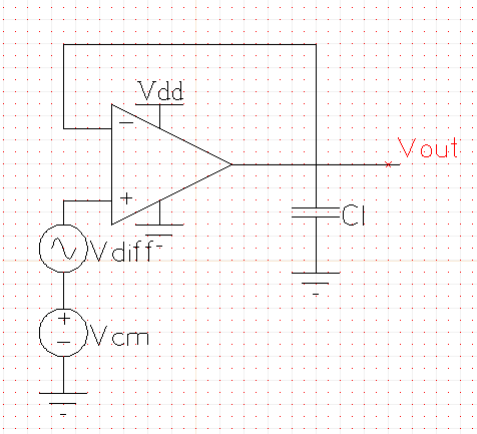

Figure 13: Circuit for Transient analysis.

7.2 Simulation

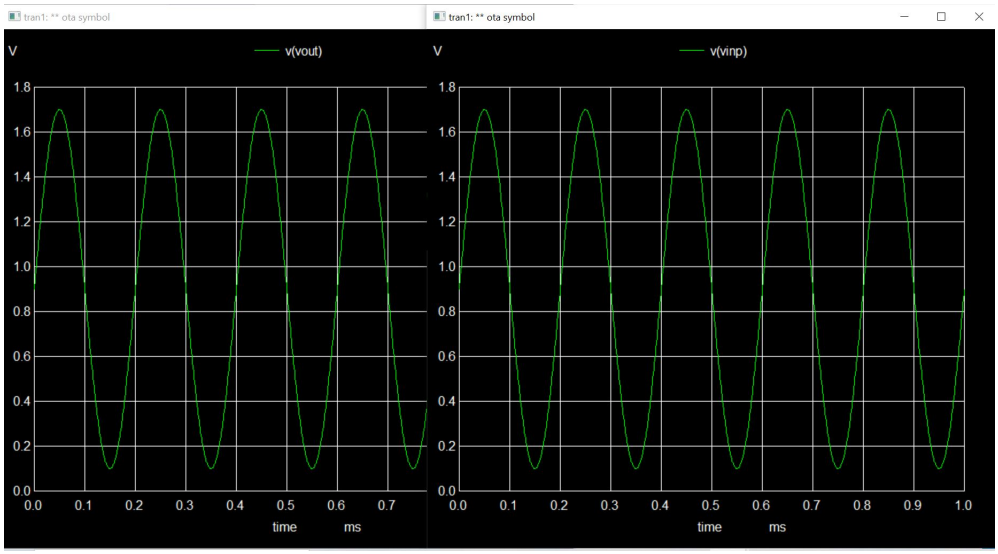

Figure 14: Transient simulation for maximum and minimum voltage swing.

8 Common-mode (CM) DC Simulation

8.1 Schematic

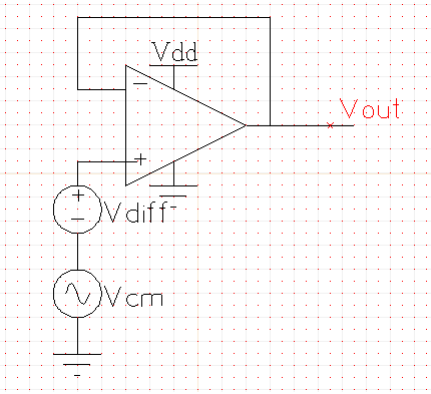

Figure 15: Circuit for DC analysis.

8.2 Simulation

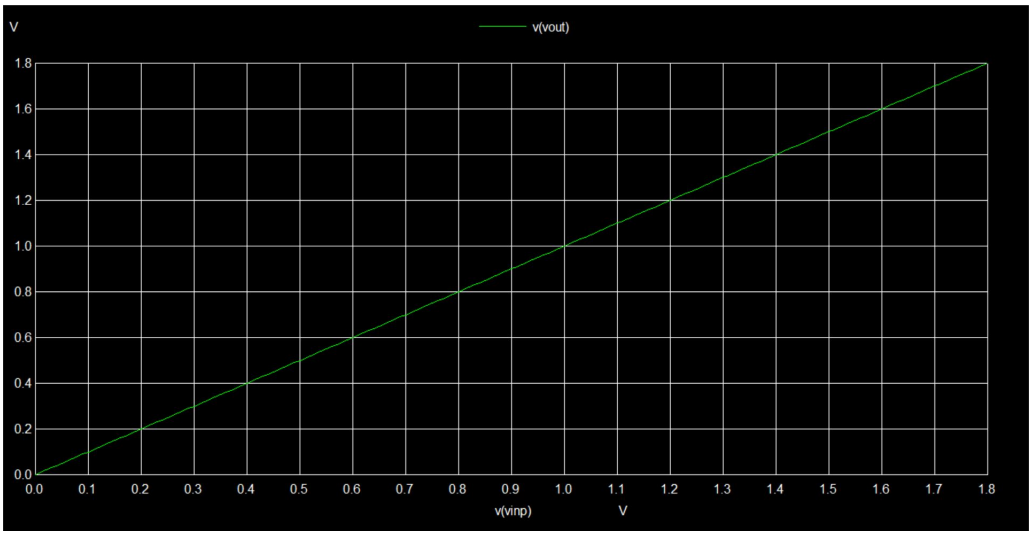

Figure 16: DC sweep analysis.

8.3 Non-Lineraity of op-amp

In our circuit the **Op-amp created has the functionality from 47 mV to 1764 mV** at the output voltage range. So, for the given values of common mode voltage we get no non-lineraity.

1. For the Vcm = 100 mV we get zero non-linearity.
2. For the Vcm = 900 mV we get zero non-linearity.

3. For the Vcm = 1600 mV we get zero non-linearity.

Hence we found the maximum and the minimum slope of the analysis:

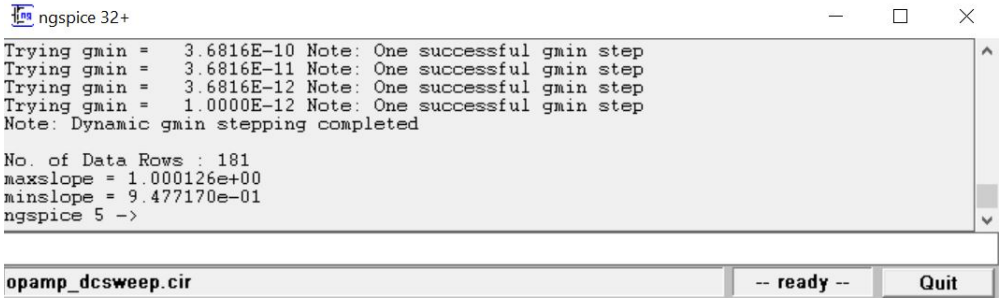

Figure 17: Slope of DC sweep analysis.

9 Power Consumption :

Total power consumption is:

$$Power = V_{dd}(I_{M6} + I_{M7} + I_{M8} + I_{M19})$$

$$Power = 1.8 * (19.43 + 14.82 + 14.82 + 667.37) * 10^{-6}$$

So, the total power consumption is,

$$\textbf{Power consumption} = 1.2895 * 10^{-3} W$$

10 Result

So, the model gave the following specifications:

Parameters	**Values**
Open loop small signal low-frequency voltage gain	102
Unity Gain Bandwidth	13.15 MHz
Input Common Mode voltage range	0.35 mV to 1.76 V
Output voltage range	47 mV to 1764 mV
Phase Margin	62^0
Slew rate	$6.14 * 10^6$

11 Work Contribution

Question Number	Ajinkya.S.Raghuwanshi	Siddharth Jain
1.1	✓	
1.2		✓
1.3		✓
1.4		✓
2.1	✓	
2.2	✓	
2.3		✓
3.1	✓	
3.2		✓
3.3		✓
4.1	✓	
4.2	✓	
4.3		✓
4.4		✓
5.1		✓
5.2	✓	
6.1	✓	
6.2		✓
7.1	✓	
7.2		✓
7.3	✓	
7.4		✓

List of Figures