Chapter 5

Bipolar Junction Transistors

Dr. Henry Ohize

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Electronics: Principles, Concepts and Practices

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Intro

Transistors and Categories

1. A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power.
2. It is a fundamental building block of modern electronic devices and circuits.
3. It is a three-terminal device and is categorized as shown in Fig. 1.

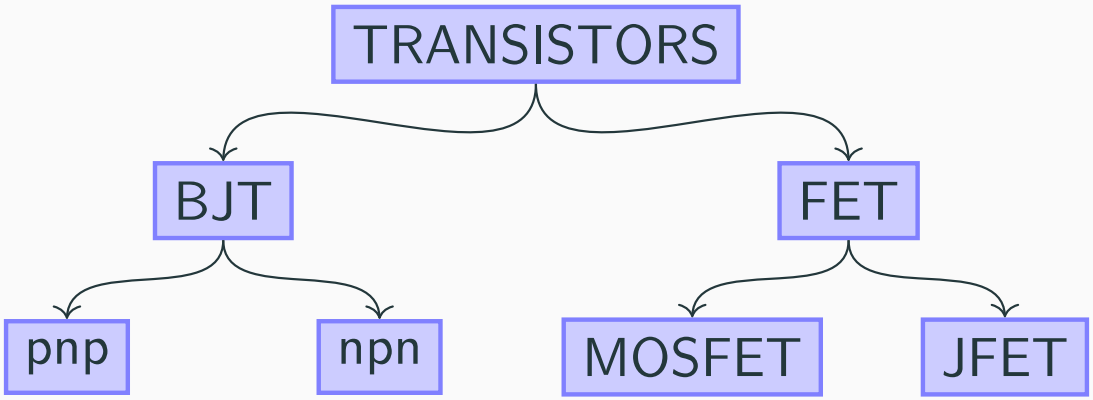


Figure 1: Transistors and the classifications

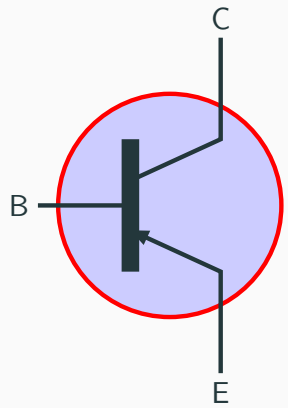
BJT Symbols

BJT Symbols

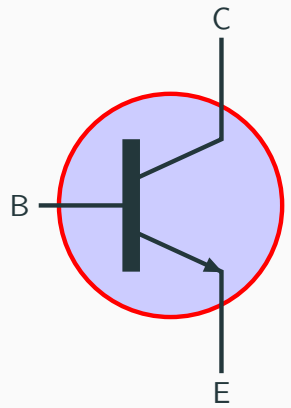
BJT stands for Bipolar Junction Transistor. The two types of BJTs are npn and pnp.

The term "bipolar" refers to the fact that current conduction in this transistor occurs through both holes and electrons.

Figure 2 shows the circuit symbols for the pnp transistor and the npn transistor.



(a) pnp circuit symbol



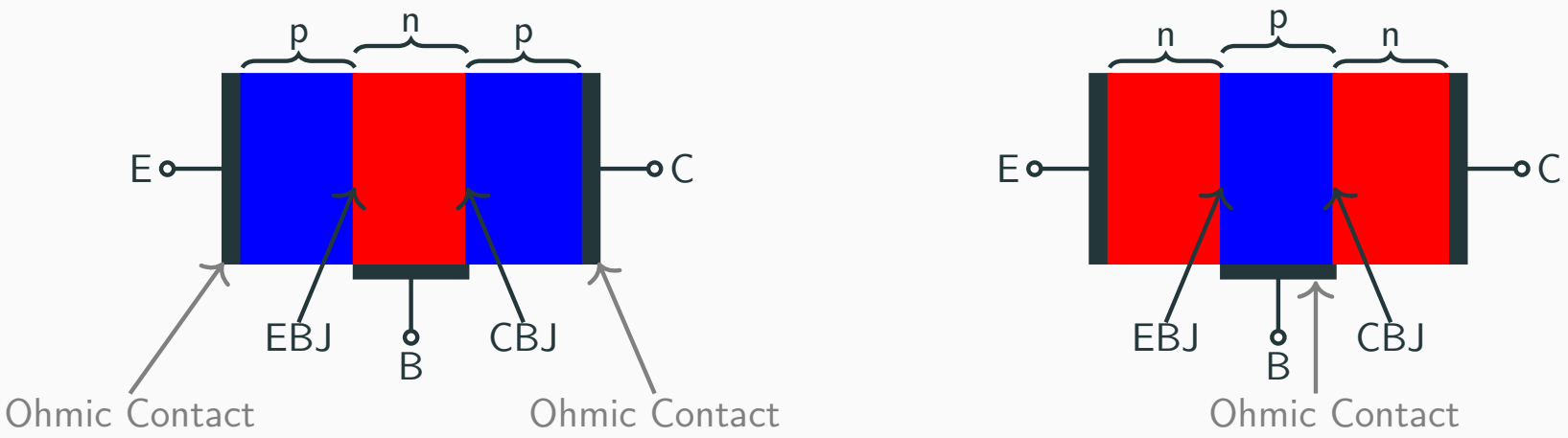
(b) npn circuit symbol

Figure 2: Circuit symbol of BJTS

BJT Construction

BJT Construction

The Bipolar Junction Transistor (BJT) is a three-terminal and two-junction device. Figure 3 illustrates the construction of both pnp and npn transistors.



(a) pnp transistor construction

(b) npn transistor construction

Figure 3: Transistor construction

BJT Operation

BJT Operation

Understanding BJT's operation is crucial for designing and analyzing electronic circuits effectively.

Depending on the biasing applied to the transistor junctions (EBJ & CBJ), three different modes of operation can be achieved.

1. Active Mode: Base- Emitter junction is forward and Base-Collector junction is reverse biased.
2. Saturation Mode: Both junctions are forward biased.
3. Cutoff Mode: Both junctions are reverse biased.

We shall illustrate the operation of the BJT using the active mode biasing. In the active mode, the BJT operates as an amplifier and it is the most common mode of operation.

See Fig. 4. For the npn transistor, the forward-biased junction that injects electrons into the center p region is called the emitter-base junction.

The reverse-biased junction that collects the injected electrons is called the collector-base junction.

The extra doped n^+ region, which serves as the source of injected electrons, is called the emitter.

The n-region into which the electrons are swept by the reverse-biased junction is called the collector.

The center p region is called the base.

The collector current consists of two components: the majority electron current from the emitter, denoted as I_{Cn} and the minority electron current from the base, typically referred to as I_{CO}, which represents the reverse leakage current when the emitter terminal is open.

The mathematical implication of Figure 4

$$I_C = I_{Cn} + I_{CO} \tag{1}$$

However, the collector current is largely the diffusion component I_{Cn} from the emitter whose magnitude is proportional to

$$I_{Cn} = I_S \exp^{\frac{V_{BE}}{V_T}} \tag{2}$$

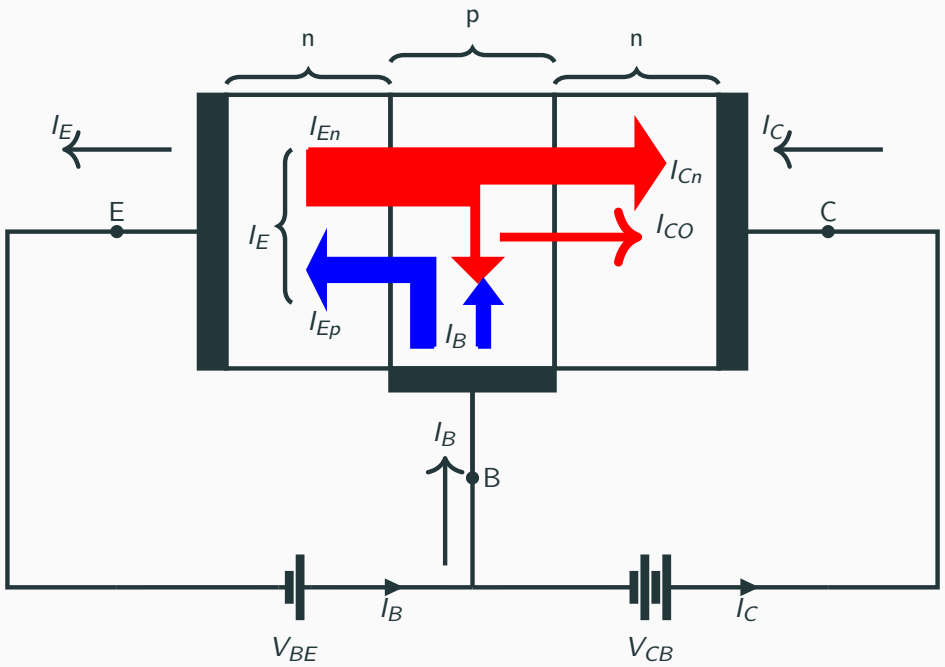


Figure 4: Operation of BJT

BJT Configuration and Device Characteristics

BJT Configuration and Device Characteristics

In typical two-port networks, there is a pair of terminals designated as the input port and another pair designated as the output port. However, in the case of a three-terminal device, it means that one of the terminals must be common to both the input and output ports. This common terminal determines the configuration of the device. The possible configurations are

1. Common-base
2. Common-emitter, and
3. Common-collector.

Common-base Configuration

Figure 5 illustrates the common-base (CB) configuration of an npn transistor.

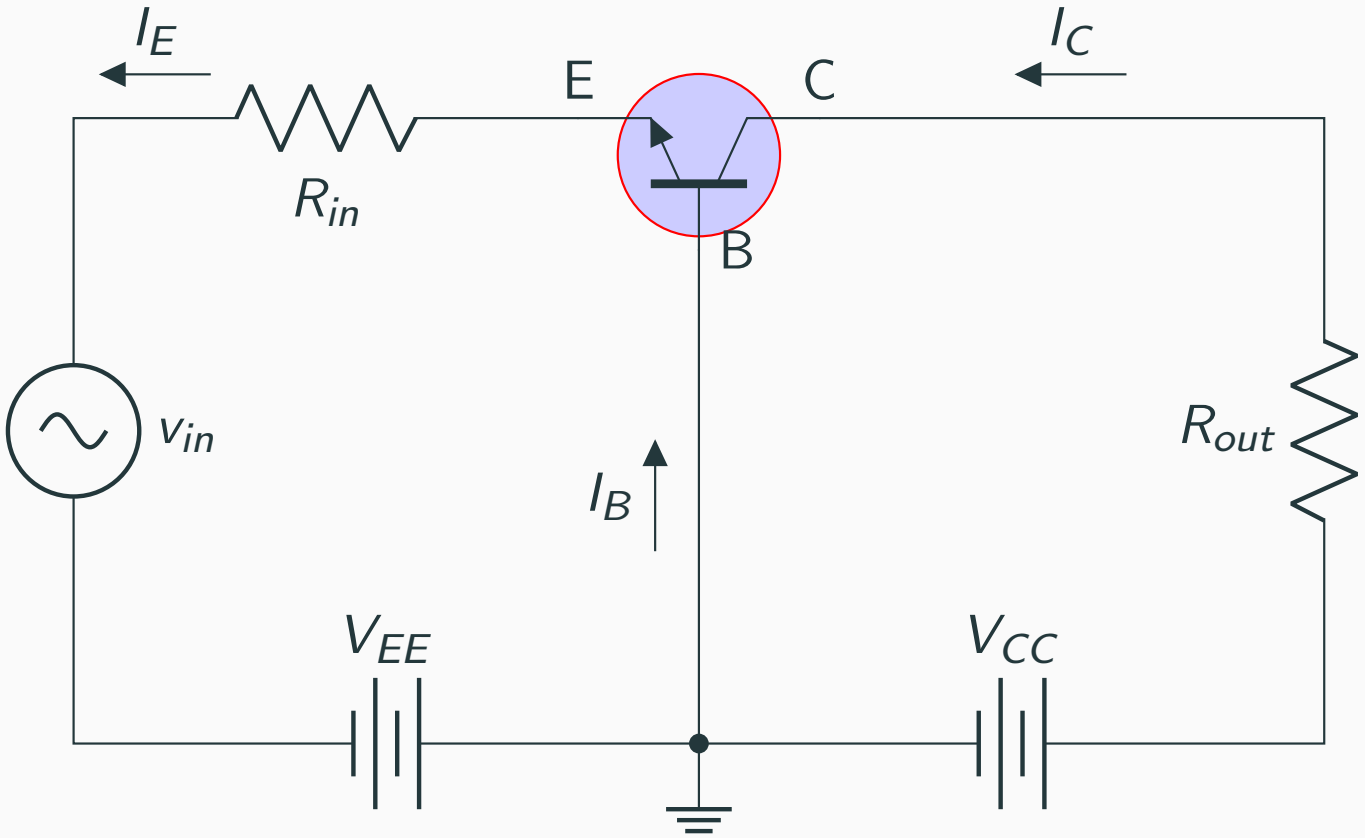
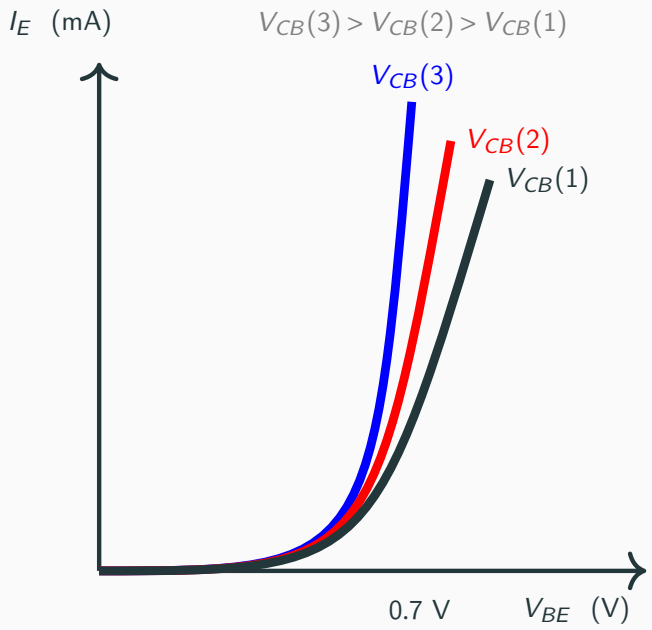


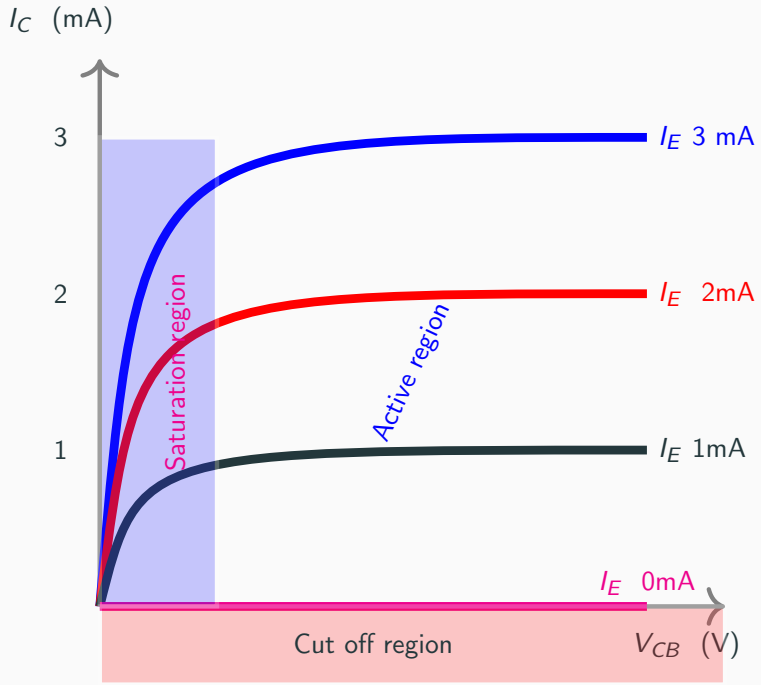
Figure 5: An npn common-base configuration

Common-base Characteristics

Fig. 5 depicts the common-base (CB) configuration input and output characteristics.



(a) Input characteristics of CB configuration



(b) Output characteristics of CB configuration

Figure 6: The characteristics of CB configuration

Common-emitter Configuration

Fig. 7 illustrates the common-emitter (CE) configuration, which is commonly used in amplifier circuits.

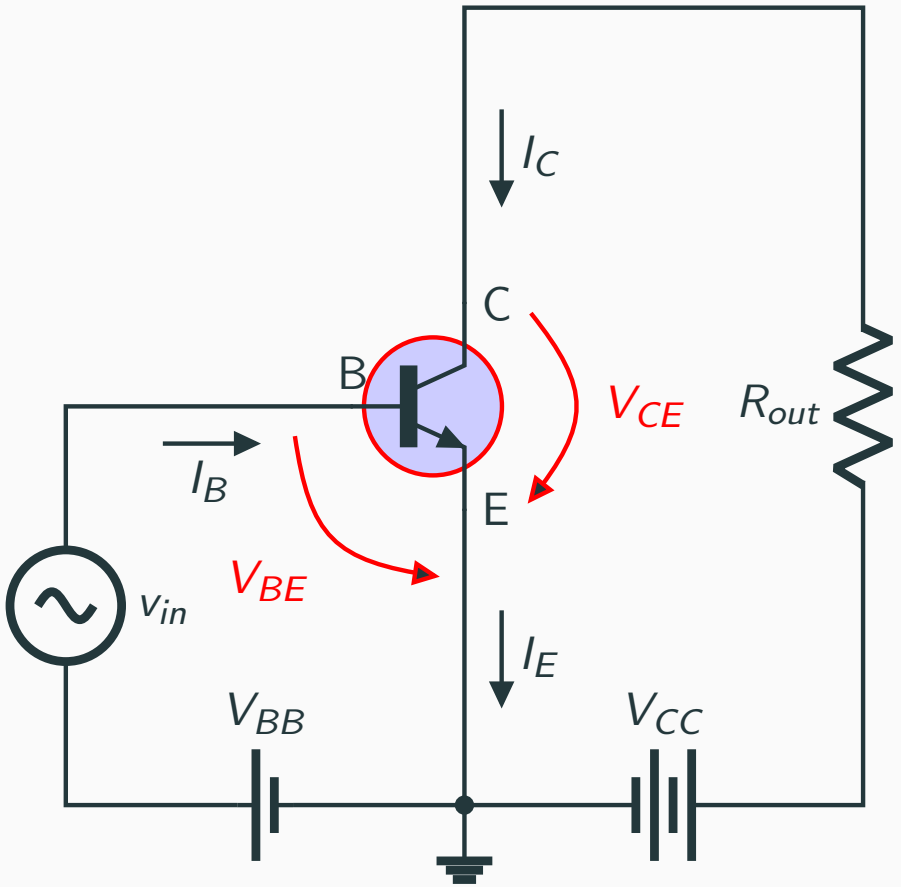
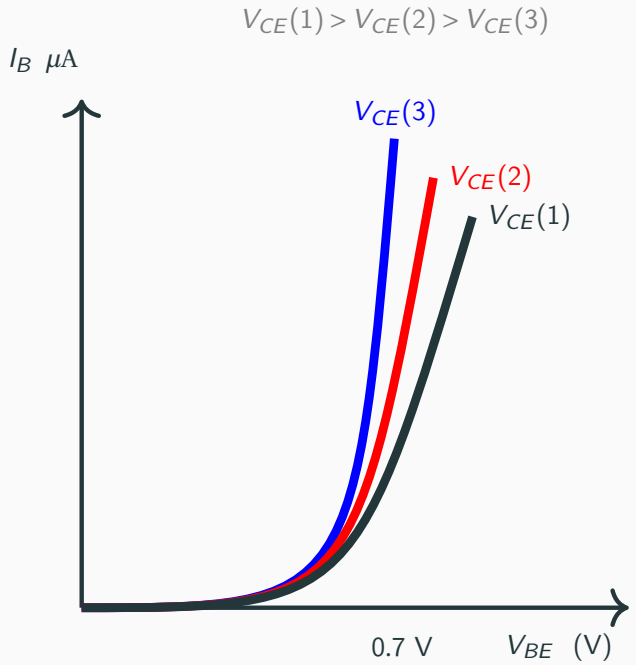


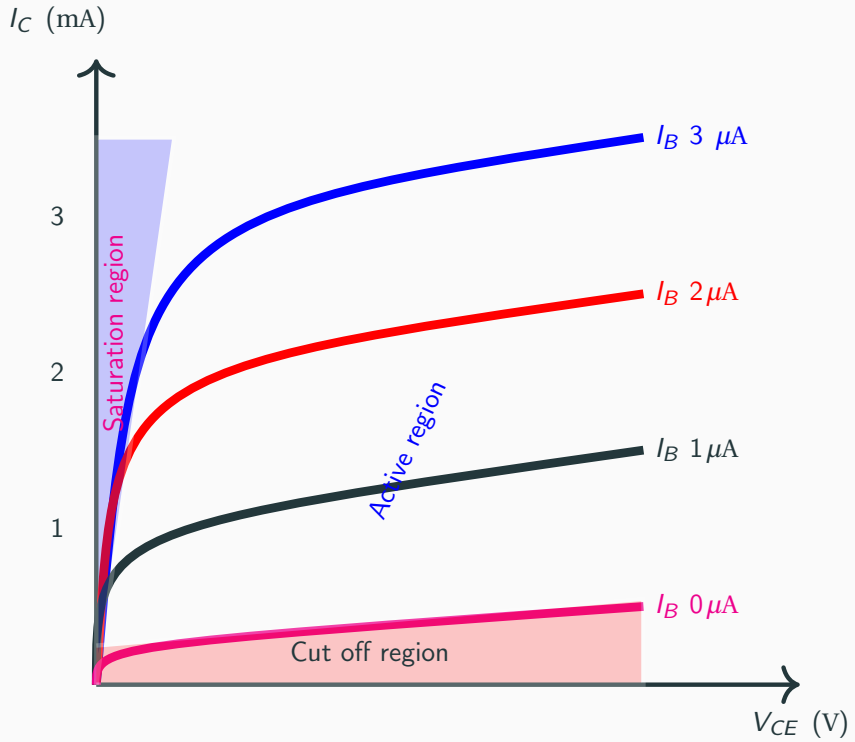
Figure 7: An npn common-emitter configuration

Common-emitter Characteristics

Fig. 8 depicts the common-emitter (CE) configuration input and output characteristics.



(a) Input characteristics of CE configuration



(b) Output characteristics of CE configuration

Figure 8: The characteristics of common-emitter configuration

Common-collector Configuration

Fig. 9 illustrates the common-collector (CC) configuration, also known as the grounded collector configuration, emitter follower, or voltage follower.

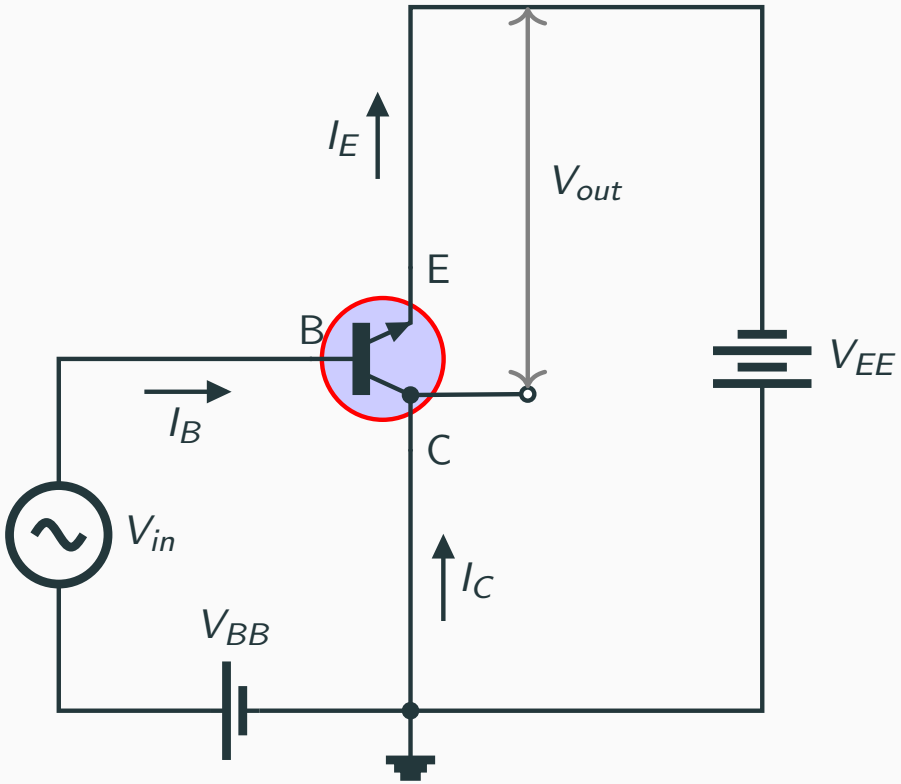
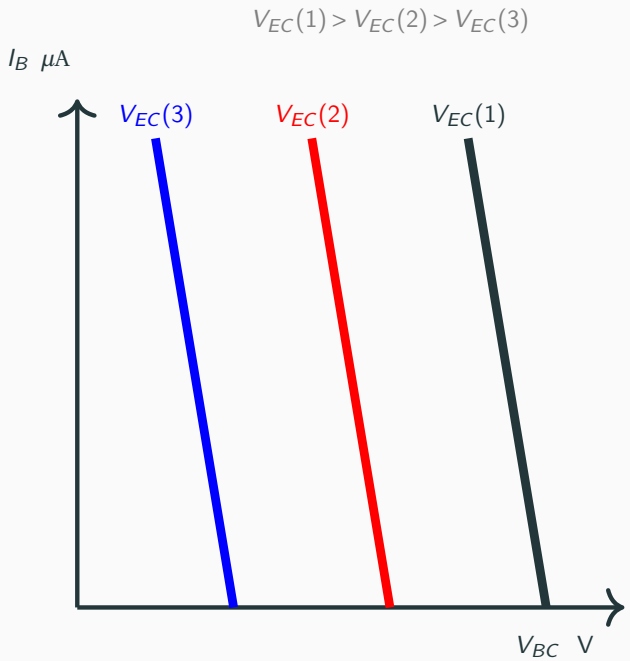


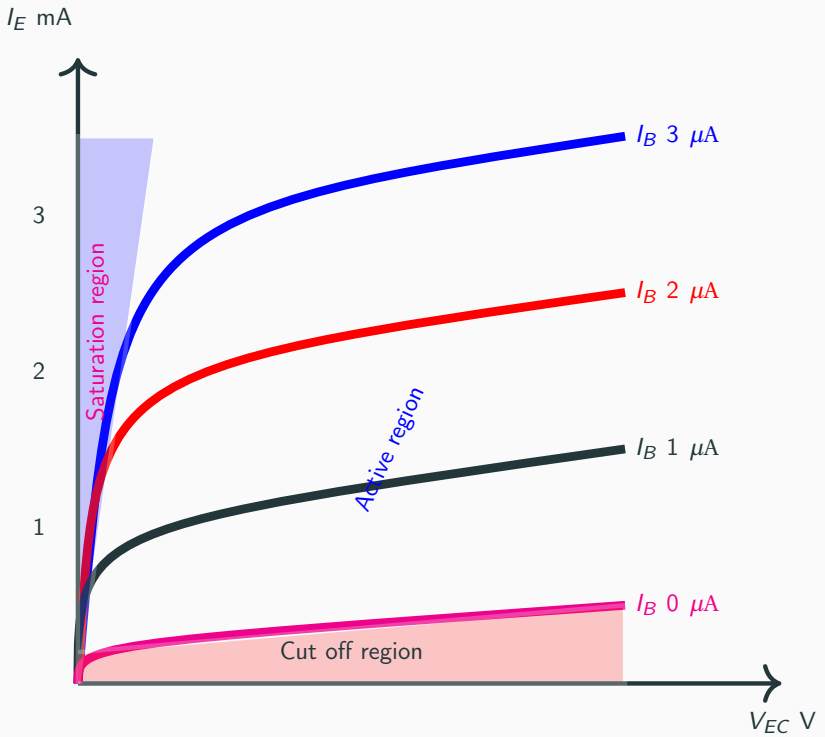
Figure 9: An npn common-collector configuration

Common-collector Characteristics

Fig. 10 depicts the common-collector (CB) configuration input and output characteristics.



(a) Input characteristics of CC configuration



(b) Output characteristics of CC configuration

Figure 10: The characteristics of CC configuration

Operating Point and Limit of Operation

Transistor's Operating Point

Fig. 11 illustrates the determination of the operating point using load line.

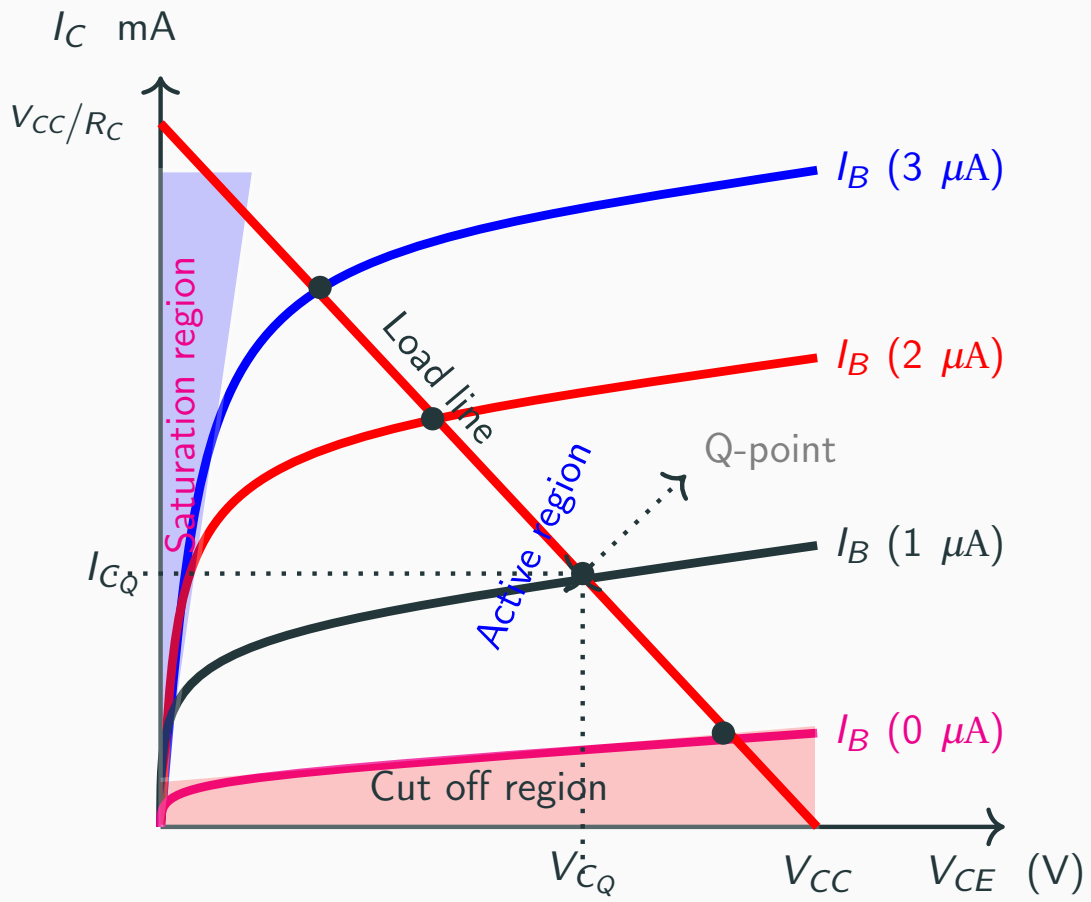


Figure 11: Determining Q-point using DC load line

For signal amplification, circuit biasing aims to set the operating point away from cutoff, saturation, and the edge of the operating limit (maximum power dissipation). Fig. 12 illustrates this.

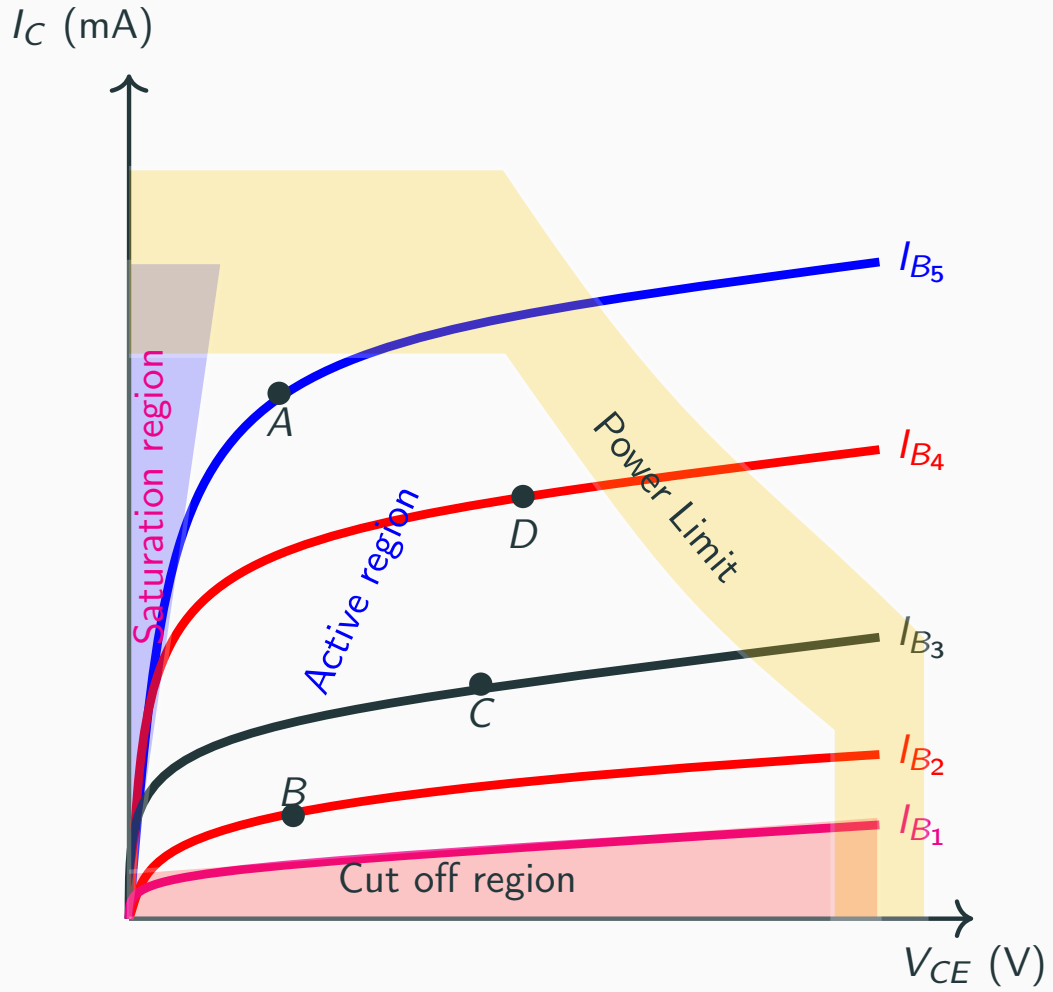


Figure 12: Biasing a BJT for desired operating regions

Circuit Biasing for Signal Amplification

Circuit Biasing for Signal Amplification

Here we shall discuss four common biasing circuit for biasing the transistor to operate in the active region for signal amplification.

1. Fixed-bias circuit;
2. Emitter-stabilized bias circuit;
3. Voltage-divider bias circuit; and
4. Collector-feedback bias circuit.

These network configurations are connected to ensure

1. The base–emitter junction is forward-biased; and
2. The base–collector junction is reverse-biased and within the limit of the maximum rating of the device.

Fixed-bias circuit

Apply KVL to the input loop to obtain

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} \tag{3}$$

Similarly, applying KVL to the output loop

$$V_{CE_Q} = V_{CC} - I_{C_Q} R_C \tag{4}$$

The output current can be obtained from the base current in Equation (3)

$$I_{C_Q} = \beta I_{B_Q} \tag{5}$$

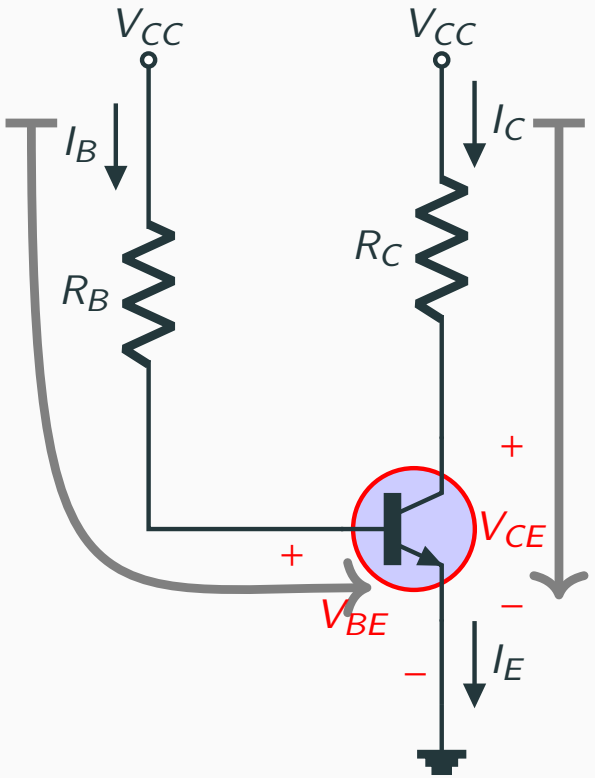


Figure 13: Fixed-bias circuit

Emitter-stabilized bias circuit

Apply KVL to the input loop to obtain

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \tag{6}$$

Similarly, applying KVL to the output loop

$$V_{CE_Q} = V_{CC} - I_C (R_C + R_E) \tag{7}$$

The output current can be obtained from the base current in Equation (6)

$$I_{C_Q} = \beta I_{B_Q} \tag{8}$$

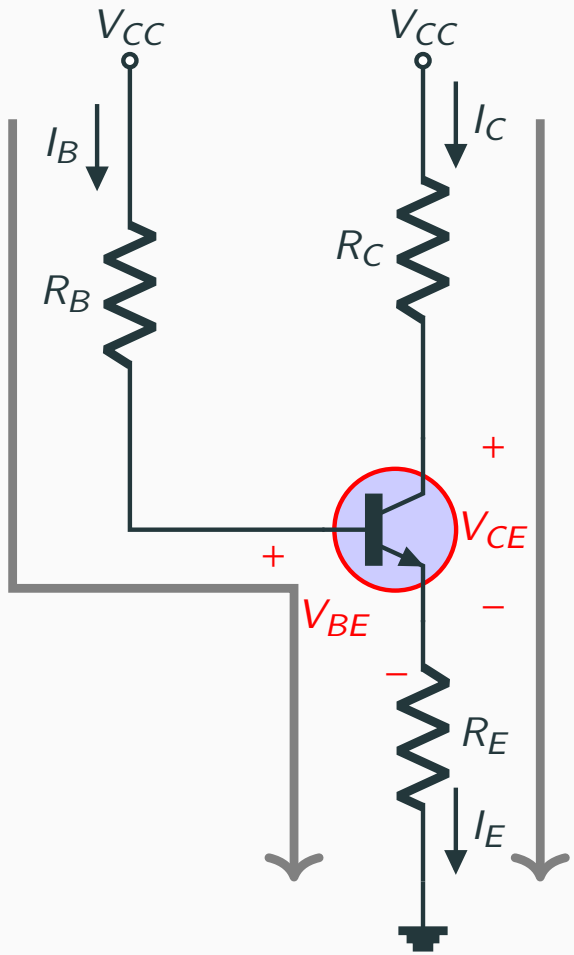


Figure 14: Emitter-stabilized bias circuit

Voltage-divider bias circuit

Fig. 15 is the voltage-divider bias circuit.
There are two approaches to determining the operating points of the voltage-divider bias network:

1. The Thévenin method, which can be applied to any voltage-divider bias configuration.
2. The approximate method, which can only be used when specific conditions are met.

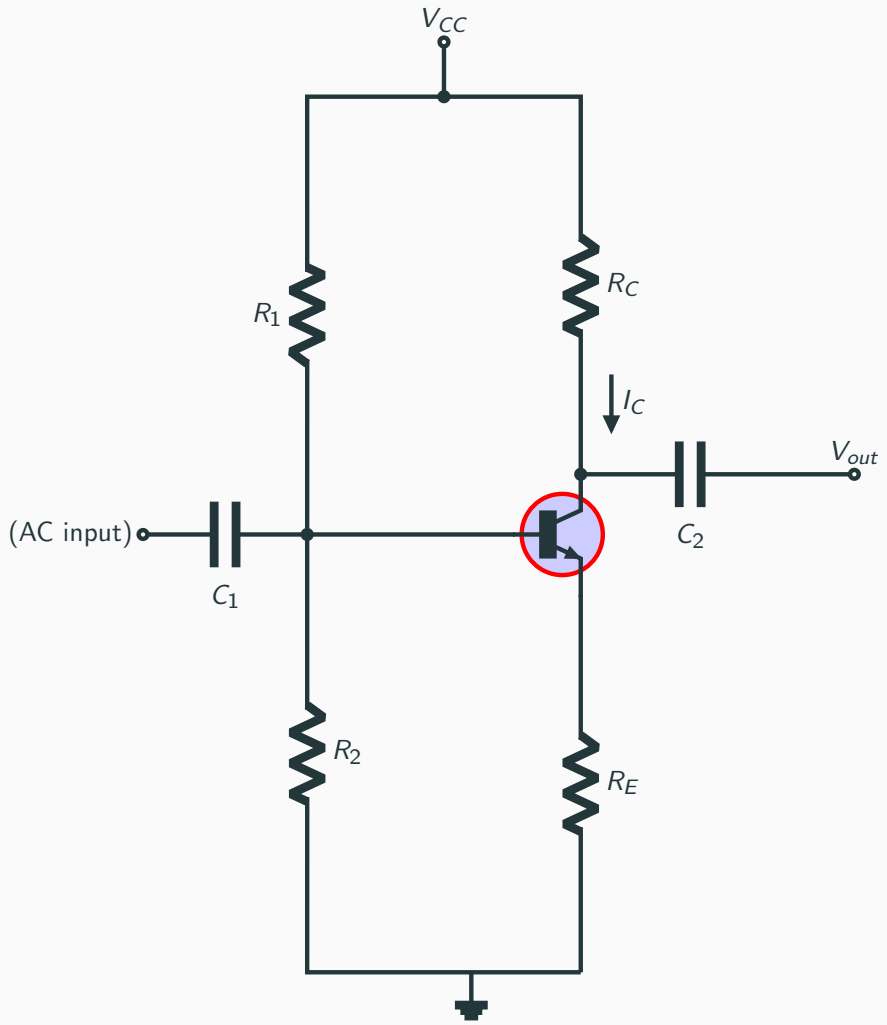


Figure 15: The voltage-divider bias circuit

Thévenin method

In this method, the voltage-divider circuit is redrawn using the Thévenin technique. Fig. 16 represents the Thévenin equivalent circuit.
Apply KVL to Théveninized circuit to obtain

$$I_{B_Q} = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \qquad (9)$$

Similarly, applying KVL to the output loop of Figure 15.

$$V_{CE_Q} = V_{CC} - I_{C_Q}(R_C + R_E) \qquad (10)$$

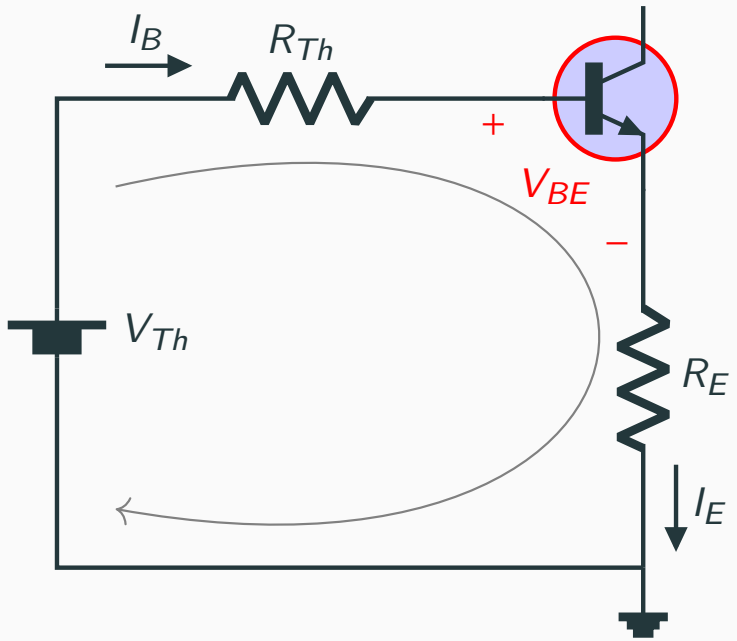


Figure 16: The Thévenin equivalent circuit

Approximation method

This method relies on the assumption that $(\beta+1)R_E >> R_2$. Thus, I_B is negligible. The network equations become:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \quad (11)$$

$$V_E = V_B - V_{BE} \quad (12)$$

$$I_E = \frac{V_E}{R_E} \quad (13)$$

$$I_C \approx I_E \quad (14)$$

From the output loop we can obtain

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (15)$$

Fig. 17 illustrates the approximation method.

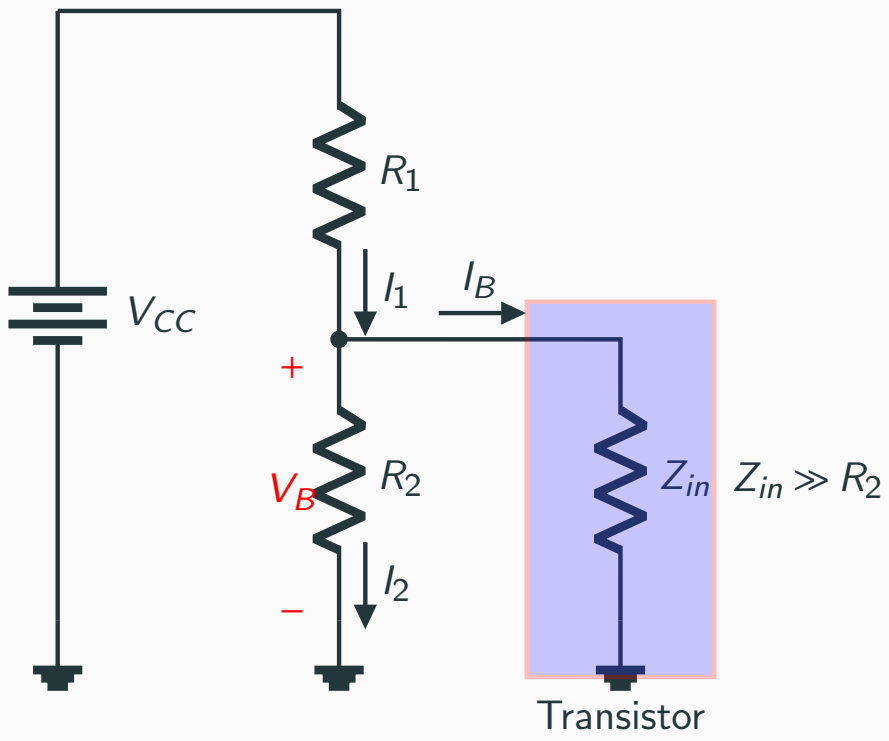


Figure 17: Approximation method

Collector-feedback bias circuit

Fig. 18 is the collector feedback circuit.
As with the previous biasing circuit, apply KVL to the base-emitter loop.
The network equations become:

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \qquad (16)$$

Applying KVL to the output loop of Fig. 18.

$$V_{CE_Q} \approx V_{CC} - I_C(R_C + R_E) \qquad (17)$$

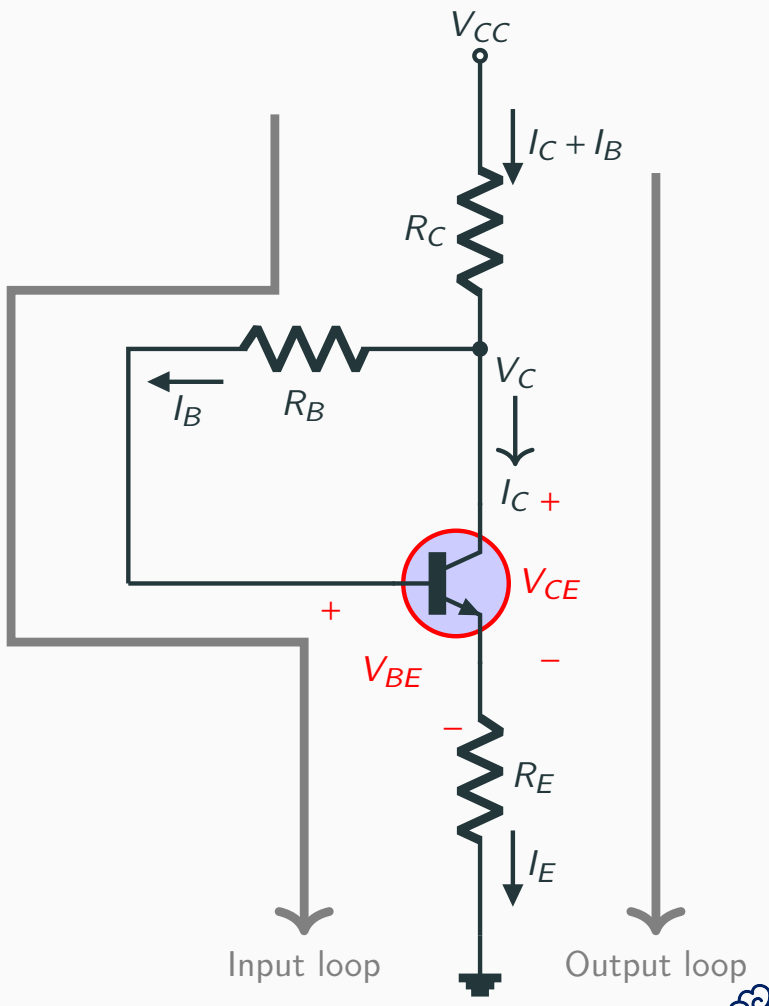


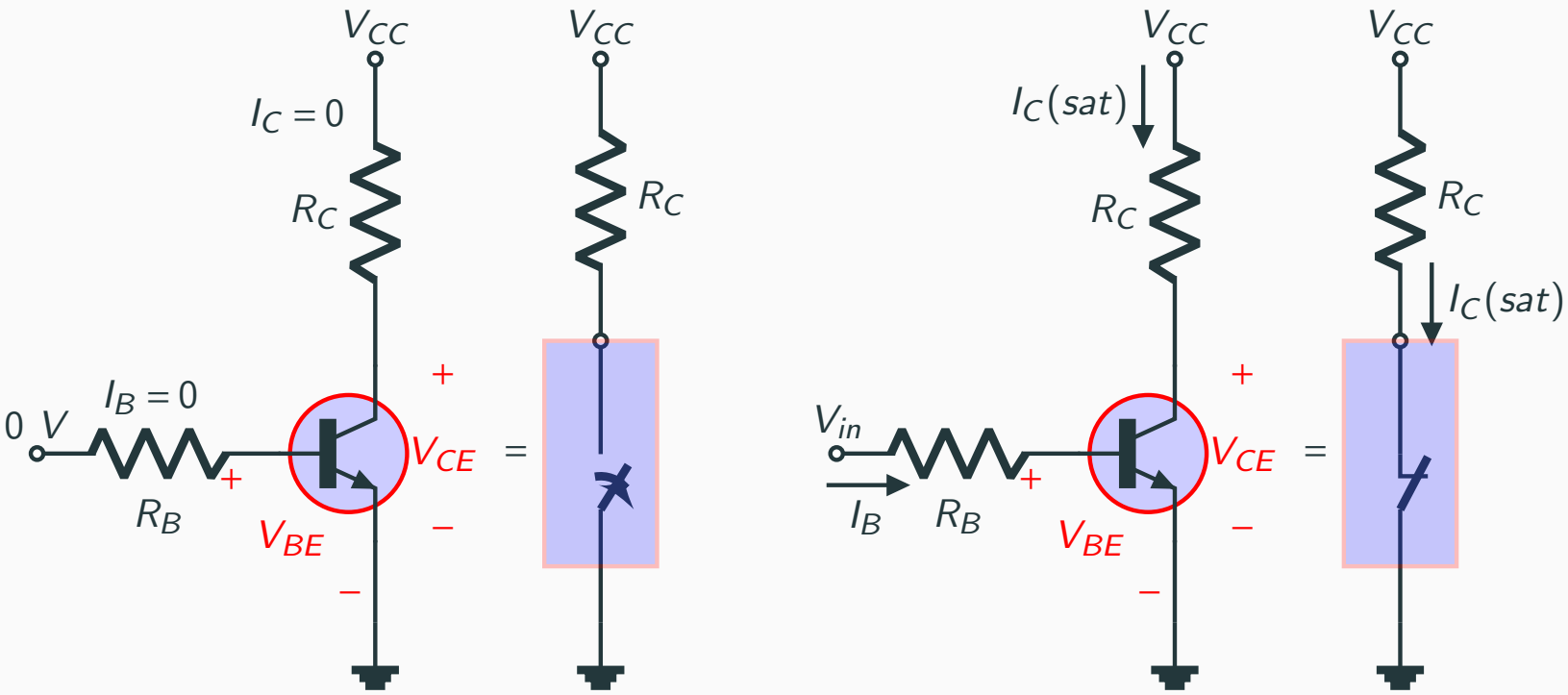
Figure 18: Collector-feedback bias circuit

Circuit Biasing for Switching

Circuit Biasing for Switching

In the cutoff region, the collector current $I_C \approx 0$.

In the saturation region, the collector-emitter voltage $V_{CE} \approx 0$.



(a) Cutoff open-circuit

(b) Saturation closed-circuit

Figure 19: Illustration of the switching action of a BJT circuit

References i

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