Electronics:
Principles, Concepts and Practices
-with LTSpice and MATLAB

Dr H. O. Ohize

Revised by Prof. Yinusa Adediran

tetfund
TERTIARY EDUCATION TRUST FUND

Electronics: Principles, Concepts and Practices

2023

ABOUT THE AUTHOR

Henry Ohiani Ohize is a Senior Lecturer in the Department of Electrical and Electronics Engineering at the Federal University of Technology, Minna, Nigeria. He obtained his doctorate degree from the University of Cape Town, South Africa, in 2017. With over 15 years of teaching experience in various universities, he has been exposed to the cultural diversity of students and their idiosyncrasies.

ABOUT THE BOOK

The new Electronics text takes a unique approach in conveying its content. It adopts a bottom-up teaching method, starting with semiconductor physics, then moving to semiconductor devices and modeling, and finally introducing circuit analysis and network design with semiconductor devices. Free lecture slides are provided for download from the web. This text avoids unnecessary theoretical baggage, focusing on fundamental understanding for effective circuit comprehension. It introduces only necessary basic mathematical concepts and is suitable for introductory-level teaching of Electronics in all institutions.

LTSpice and MATLAB are integrated into the course syllabus, allowing for self-directed learning and the exploration of "what-if" questions through simulation tasks. This approach supports the development and application of intuition, which is crucial in an engineering career. Graphical outputs are obtained from simulations to emphasize mathematical derivations and assumptions.

Overall, this text provides a comprehensive and practical approach to teaching Electronics, enabling students to build a solid foundation in the subject while incorporating simulation tools for enhanced learning.

Electronics

Principles, Concepts and Practices

H. O. Ohize

OHIZE DRAFT007

OHIZE DRAFT007

Copyright © 2022 Goro Akechi

PUBLISHED BY PUBLISHER
ISBN:979-978-781-068-2
BOOK-WEBSITE.COM

Licensed under the Creative Commons Attribution-NonCommercial 4.0 License (the "License"). You may not use this file except in compliance with the License. You may obtain a copy of the License at https://creativecommons.org/licenses/by-nc-sa/4.0. Unless required by applicable law or agreed to in writing, software distributed under the License is distributed on an "AS IS" BASIS, WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied. See the License for the specific language governing permissions and limitations under the License.

First printing, March 2022

Dedication

To all the students who have fueled my inspiration.

OHIZE DRAFT007

INTENTIONALLY LEFT BLANK.

OHIZE DRAFT007

Preface

The field of Electronics already has numerous textbooks, prompting the question of why another one is necessary. In reality, authors often write books because they identify gaps in existing works and believe they can present the content in a more effective manner. This book is a response to such a need. It offers a unique approach to conveying Electronics concepts through the use of circuit simulations, setting it apart from other textbooks in terms of content and presentation style.

The book *Electronics: Principles, Concepts and Practices* follows a bottom-up approach to teaching Electronics, beginning with an introduction to semiconductor physics, followed by semiconductor devices and modeling, circuit analysis, circuit design with semiconductor devices, and concluding with an introduction to trends in Electronics. It is divided into four parts: Part I, Part II, Part III, and Part IV. The fundamental idea behind this book is to address a wide range of topics in a simplified manner, emphasizing the interactions between physics, devices, and circuits in modern Electronics. In addition, free lecture slides are made available for download.

This book intentionally avoids delving into unnecessary theoretical baggage, such as Fermi statistics, effective mass theory, differential equations, Laplace transform, complex conjugate, poles and zeros, and more. Instead, it focuses on building the fundamental concepts required for a thorough understanding of circuits, introducing only the necessary basic mathematical concepts. This approach makes the book highly suitable for introductory-level teaching of Electronics in all institutions.

The text integrates LTSpice and MATLAB into the course syllabus for Electronics, allowing for self-directed learning and reaping the benefits of learning through mistakes. Simulation tasks are included at the end of each part to reinforce the concepts learned in preceding chapters. These tasks are designed to challenge students without trivializing the development or application of intuition, which is crucial for an engineering career. Students are encouraged to explore "what-if" scenarios in the simulation tasks, while graphical outputs further enhance their understanding of mathematical derivations and assumptions.

In conclusion, this book fills the gaps identified in existing Electronics textbooks by offering a unique approach that utilizes circuit simulations. Its structure, emphasis on fundamentals, and integration of simulation tools make it a valuable resource for introductory-level teaching. By focusing on practical comprehension and providing opportunities for self-directed learning, this book aims to equip students with a solid foundation in Electronics.

OHZE DRAFT 007

INTENTIONALLY LEFT BLANK.

OHIZE DRAFT007

Acknowledgments

My appreciation goes first to God Almighty for the gift of life. He has been my help, and His grace has sustained me thus far. Avo Nda!

I am greatly indebted to Professor Yinusa Adediran for his comprehensive review of the book. He gave his all, and I appreciate his thorough review. I must also extend this gratitude to Prof. Emmanuel Ohize for the meticulous editing and review work throughout the entire writing phase.

Special thanks to Engr. Prof. Babatunde Adegboye, Engr. Prof. Jonathan Kolo, Prof. M.N. Nwohu, Engr. Prof. Jacob Tsado, and Engr Dr Lanre Olatomiwa, for their leadership and unwavering support. My gratitude goes to Engr. Prof. Elizabeth Onwuka and Engr. Prof. Olayemi Mikail Olaniyi, the Dean and the Deputy Dean respectively, of the School of Electrical Engineering and Technology of Federal University of Technology, Minna, Nigeria. By extension, this appreciation goes to all my colleagues, the staff of the Department of Electrical and Electronics Engineering, and the entire staff of the School of Electrical Engineering and Technology of Federal University of Technology, Minna. Thank you all for your encouragement and support.

I want to express a big thank you to the following people for their invaluable support: Engr Dr Ambafi James; Engr Dr Dauda Suleiman Umar; Engr Dr Nathaniel Salawu; Assoc. Prof. Abraham Usman; Engr. Dr Eustace Manayi Dogo; Engr Prof. Musa Aibinu; Assoc. Prof. James Agajo; Assoc. Prof. Caroline Alenoghena; Engr Dr Adeiza Onumanyi; Engr Dr Opeyemi Osanaiye; Engr Dr Habeeb Bello-Salawu; Engr Dr Buhari Ugbede Umar; Engr Dr. Salihu Bala; Engr Prof. Adamu M. Zungeru; Engr Dr. Abdullahi Daniyan; Engr Dr. Habibu Hussaini; Engr Prof. Abdulkareem Saka; Assoc. Prof. Adeyemi Abel Ajibesin; Prof. Mqhele Dlodlo; Engr Tade Durojaiye; Mr Ekundayo Ayeni; Mr Hafeez Ochepa and Mr. Musbau Dahiru.

I extend my gratitude to all my students over the years, particularly those I taught while writing this book. Organizing the text in this simple manner did not just happen by magic but through your lenses. You all have unknowingly helped me organize and clarify the material; you have tactfully pointed out mistakes and fueled my inspiration. This book is for you and those who follow in your footsteps.

For the production and editing work, I wish to thank the entire team at the University Academic Publishing Centre (APC), Federal University of Technology, Minna. Worthy of special mention are Engr Dr Abubakar Sadiq Ahmad and the Director (APU), Prof Abdulsalam Kovo. For the cover art, I express my gratitude to Mr Martins Adeiza Ibrahim.

Special thanks to the Management of Federal University of Technology, Minna, and the Tertiary Education Trust Fund (TETFund) for their logistic and production support.

Finally, I say a very special thank you to my family for their unwavering support during the writing of this book: my lovely wife, Comfort Ohize; our children (Oiza Favour, Onize Adora, and Otaru Filbert); my dear parents, Professor and Mrs Emmanuel Ohize; my beloved sister and her husband, Mr and Mrs Collins Abu, and my fantastic brothers and their spouses, Dr and Dr(Mrs) Victor Ohize and Dr and Mrs Stephen Ohize.

OHIZE DRAFT COPY

INTENTIONALLY LEFT BLANK.

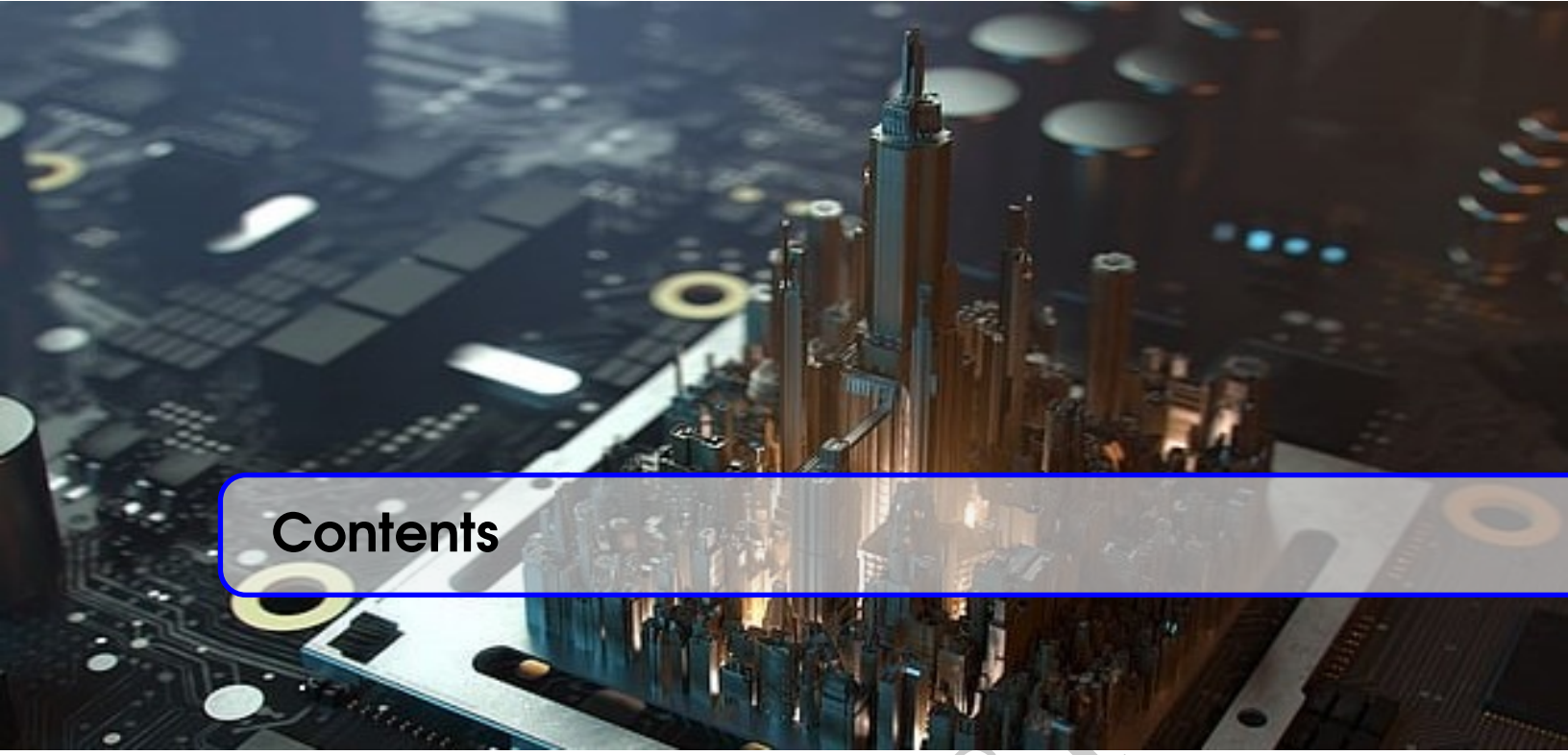
OHIZE DRAFT007

Foreword

foreword by

OHIZE DRAFT007

OHIZE DRAFT007



Contents

QHIZE DRAFT

OHIZE DRAFT007

OHZE DRAFT007

CHZE DRAFT007

OHIZE DRAFT007

OHZE DRAFT 007

FREEZE DRAFT007

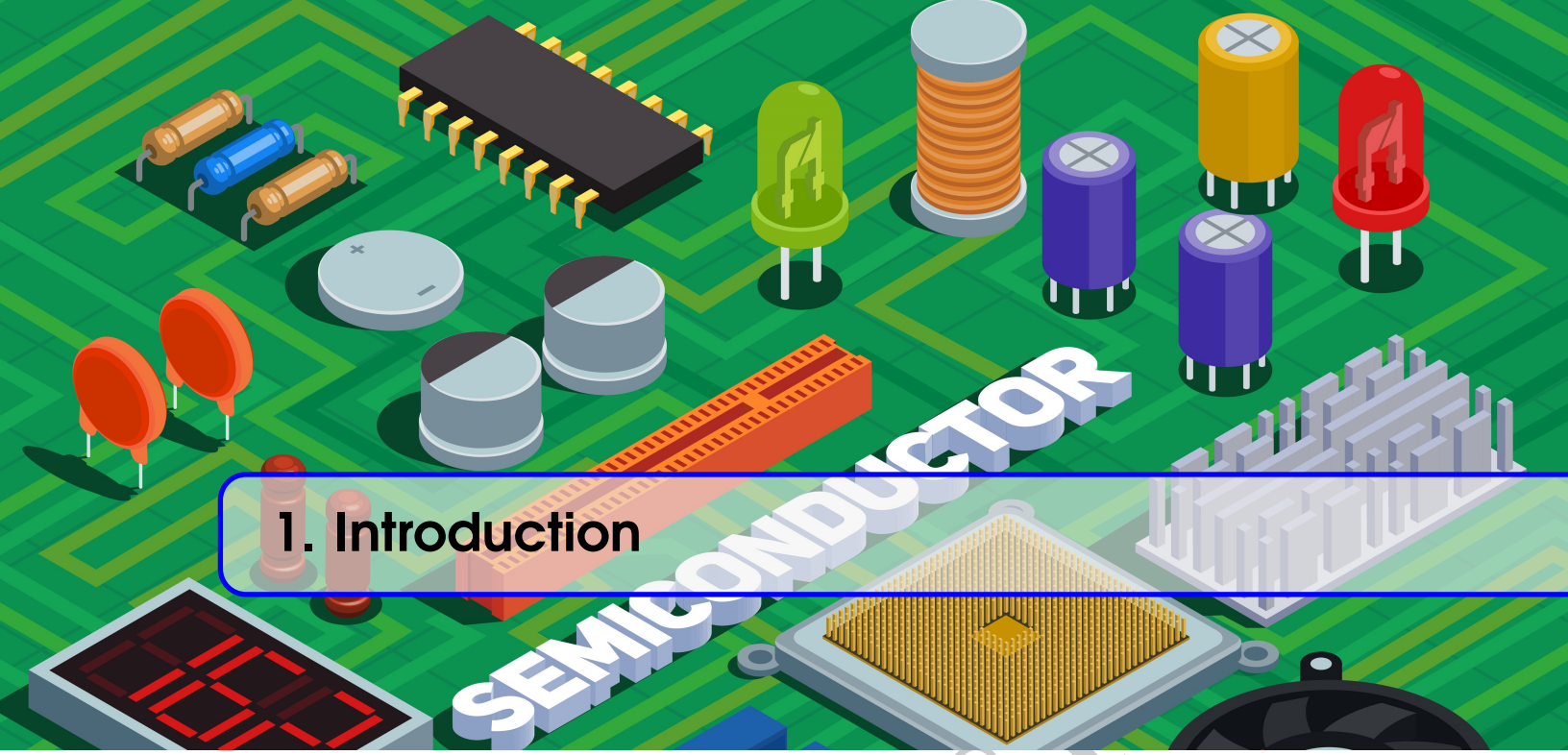
CHZE DRAFT007

OHIZE DRAFT007

OHIZE DRAFT007

Part One

OHIZE DRAFT007



1. Introduction

1.1 Electronics

There is a saying that the best place to start a story is at the very beginning. The question then arises: where does the tale of modern electronics truly begin? We may disagree on the precise starting point, but it can be argued that the story of modern electronics finds its origins in our understanding of the atom.

Indeed, understanding the atom is a crucial starting point when delving into the narrative of modern electronics. The study of atoms and their behavior provides the foundation for comprehending the behavior of materials and their electrical properties. The advent of electronics would not have been possible without a deep understanding of the atom and its structure.

The story of the atom began in the early 20th century with groundbreaking discoveries in the field of quantum mechanics. Scientists such as Max Planck, Albert Einstein, Niels Bohr, and Erwin Schrödinger made significant contributions to our understanding of the atom's structure and behavior. One of the key insights was the realization that atoms consist of a central nucleus, which contains protons and neutrons, surrounded by electrons in orbitals or energy levels. The arrangement of electrons in these energy levels determines the chemical and electrical properties of the atom.

So, while the tale of modern electronics encompasses various aspects and milestones, its true beginning can be traced back to the understanding of atoms and the behavior of materials. From there, the journey progressed through the exploration and utilization of semiconductors, paving the way for the remarkable advancements we witness in the field of Electronics today.

1.2 The Atom

Atom

The atom is the smallest unit of matter that retains the complete property of an element. Atoms are made up of three basic particles, namely: protons, electrons and neutrons.

The atom is the smallest unit of matter that retains the complete property of an element. Atoms are made up of three basic particles, namely: protons, electrons and neutrons. Figure 1.1 shows a

OHZE DRAFT

two-dimension basic structure of an atom. The nucleus (centre) of the atom contains the protons (positively charged) and the neutrons (no charge).

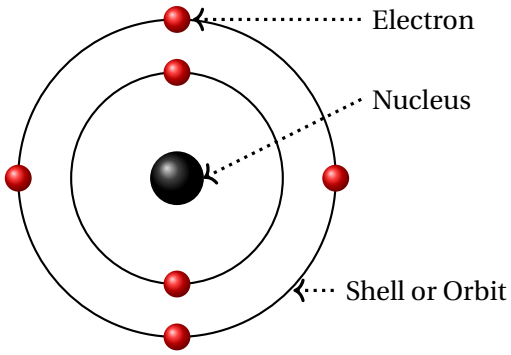


Figure 1.1: Bohr's atomic model

The outer region of the atom consists of electrons in orbits. Electrons are negatively charged. The outermost orbit can only have a maximum of 8 electrons which are known as valence electrons. The understanding that the valence electrons determine the physical, chemical and, most essentially, the electrical properties of materials is crucial to our electronics discussion.

As a quick rule, one can determine the electrical behaviour of materials from the number of valence electrons as follows:

- When the number of valence electrons is less than 4, the material is usually a metal and an electrical conductor. Examples are sodium, magnesium and aluminium which have 1, 2 and 3 valence electrons respectively;
- When the number of valence electrons is greater than 4, the material is usually a non-metal and an electrical insulator. Examples are nitrogen, sulphur and neon which have 5, 6 and 8 valence electrons respectively; and
- When the number of valence electrons equal 4, the material has both metal and non-metal properties and is usually a semiconductor. Examples are carbon, silicon and germanium.

1.3 Bohr's Atomic Model

The adopted atomic model as proposed by Bohr in 1913, was a modification of the Rutherford model of 1911. By using Planck's Quantum theory , Bohr assumptions may be paraphrased in simple terms as follows:

1. The atom has a massive positively charged nucleus consisting of protons and neutrons orbited by negatively charged electrons;
2. The electrons move round the nucleus in circular orbits that have a discrete size and energy and are balanced to do so due to the centrifugal force of pull between the nucleus and electrons;
3. Electrons revolve around their discrete permitted orbits and do not radiate out electromagnetic energy unless when forced or excited from the permitted orbits; and
4. If E_1 and E_2 are the energies corresponding to two orbits before and after a transition, then the frequency f of the emitted photon is

$$E_2 - E_1 = \Delta E = \hbar f \tag{1.1}$$

where $\hbar$ is the Plank's constant and $E_2 > E_1$.

OHIZE DRAFT 007

Exercise

Exercise 1.1 Explain the classification of electrical materials ■

Problem

Problem 1.1 A metal has 6.5×10^{28} conduction electrons per m^3. Find the relaxation time of the conduction electrons if the metal has resistivity of 1.43×10^{-8} Ωm.

Problem 1.2 Calculate the mobility of the electrons in copper obeying classical laws, given that the density of copper is 8.92×10^3 kg/m^3, resistivity of copper is 1.73×10^{-8} Ωm, atomic weight of copper is 63.5 and Avogadro's number is 6.02×10^{26} /kmol.

[*Hint*: Number of free electron concentration per cm^3; $n = \dfrac{a \times b \times c}{w}$; where '$a$' is number of free electron per atom, 'b' is the Avogadro's number, 'c' is the density of copper and 'w' is the atomic weight]

Problem 1.3 A voltage is applied to a conductor with charged particle density of 10^{28} m^{-3} so that a drift velocity of 1.5×10^{-2} m/s is attained by the particle. Given that the cross-sectional area of the material is 1.5 cm^2 and $q = 1.6 \times 10^{-19}$ C, calculate the current magnitude.

Problem 1.4 A cuboid metal strip has the following dimensions:

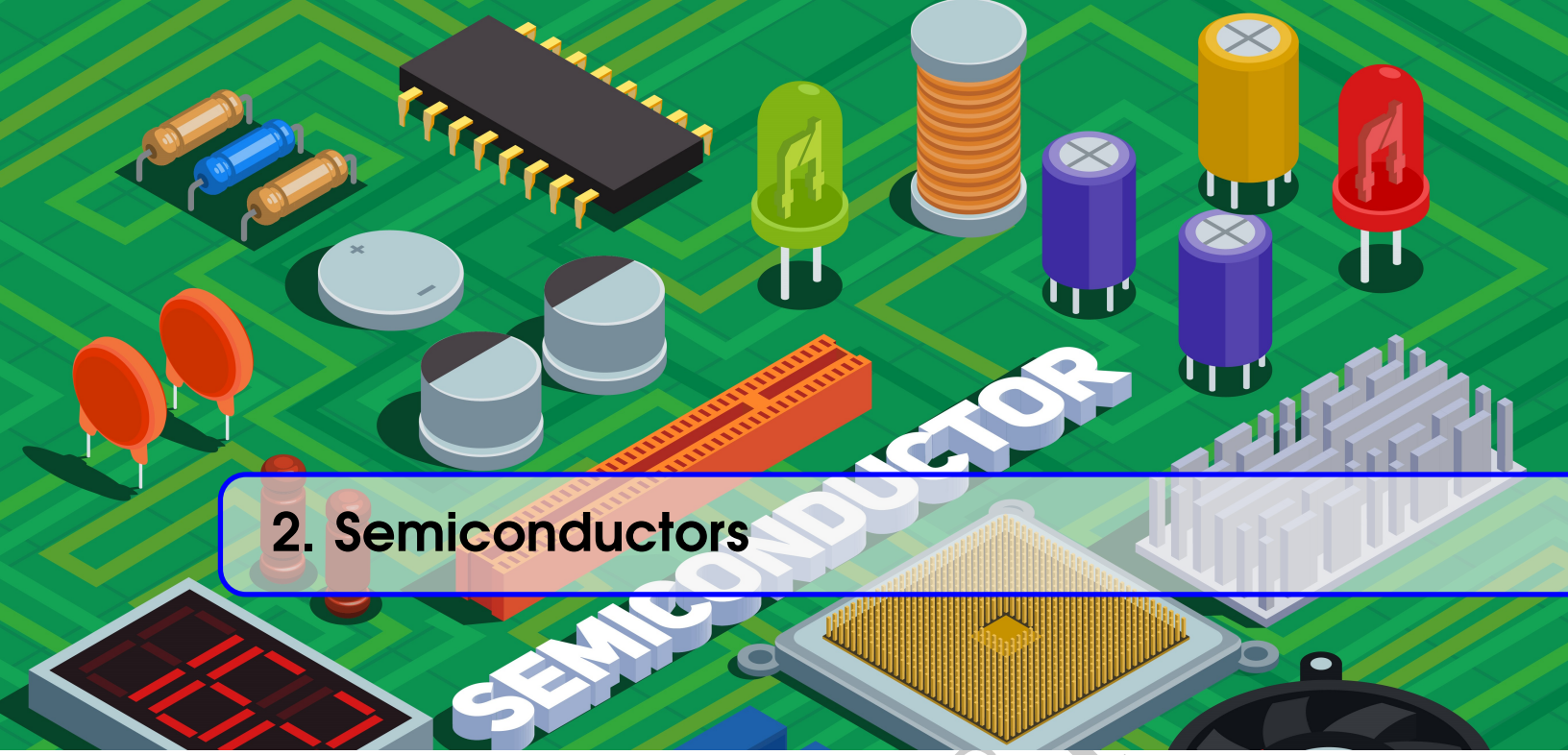
$$x = 10 \text{ cm} \qquad y = 0.5 \text{ cm} \qquad z = 0.2 \text{ cm}$$

Determine the ratio of resistances R_x, R_y, and R_z between the respective pairs of opposite faces.

Problem 1.5 When a current of 2 A flows for 3 micro-seconds in a copper wire, estimate the number of electrons crossing the cross-section of the wire.

Problem 1.6 A cube of a material of side 1 cm has a resistance of 0.001 Ω between its opposite faces. If the same volume of the material has a length of 8 cm and a uniform cross-section, what will be the resistance of this length?

OHIZE DRAFT 007



2. Semiconductors

2.1 Modeling Concept in Electronics

The entire text aims to familiarize students with the operation of semiconductors and their applications, emphasizing the importance of modeling. The approach taken is to introduce students to the physics of semiconductors and the inner workings of semiconductor devices, providing them with insights that are valuable for understanding new semiconductor technologies. As a result, the text serves as a foundation for studying Electronics.

In general, an engineer's task involves designing and implementing accurate models with minimal limitations and complexity. Design criteria often require assumptions and trade-offs, posing a dilemma for engineers who want accuracy and simplicity. This dilemma leads to the existence of various design models, such as small-signal and large-signal models. Models offer valuable insights into the performance of devices and circuits.

In Chapter 1, Section 1.7, we derived the expression for terminal voltage V across a conductor and current I through a conductor of resistance R. We obtained Ohm's law as $V = IR$ from both the field perspective and classical physics. When dealing with hardware circuits, we tend to approach our circuit problems using this model with the hope that the distinction between our ideal and real models becomes less distinctive. It is important to recognize that $V = IR$ is just a model. For example, if we increase the temperature of a conductor, its resistance value (R) will change (resistivity is temperature-dependent), and at high current levels, the relationship between voltage and current is no longer linear due to internal heating and vibration. The key point here is that while developing models, it is crucial to be aware of their limitations.

To illustrate the concept of modeling and their limitation, let us consider the models of the earth. Before the round earth model was widely accepted, there were competing models, such as the flat earth model. The Columbus' round earth model was based on a more advanced understanding of the solar system compared to the earlier flat earth model. Today, we know that the flat earth model is incorrect. However, if we only need to work within limited space or a small square area, the flat earth model would be sufficient, as in the design of a stadium. This flat earth model can be analogous to the small-signal model. On the other hand, if we are interested in long-distance travel across the earth, the round earth model is more appropriate, and the flat earth model becomes significantly inaccurate.

OHIZE DRAFT

and Group VI. For a concise overview of selected compound semiconductors, refer to Table 2.1

Table 2.1: **Some compound semiconductors**

Materials	Chemical Symbol	Group	Information
Gallium arsenide	GaAs	III and V	Gallium arsenide (GaAs) is a widely used semiconductor, ranking second only to silicon. GaAs-based devices are known for their high electron mobility, allowing them to operate at frequencies up to hundreds of GHz. However, GaAs has some limitations. It is a brittle material and has a lower hole mobility compared to silicon, which makes it unsuitable for applications like p-type CMOS transistors. Additionally, the fabrication process for GaAs is relatively challenging, leading to higher costs for GaAs devices. It is worth noting that GaAs has a band gap of 1.4 eV, which is an important characteristic for its electronic properties.
Silicon carbide	SiC	IV	Silicon carbide (SiC) is commonly employed in power devices due to its lower losses and ability to operate at higher temperatures compared to silicon-based devices. SiC has a remarkable breakdown capability, approximately ten times higher than that of silicon. In the past, SiC was utilized in the production of early yellow and blue LEDs. It possesses a band gap of 3.0 eV, which is a significant factor determining its electronic properties.
Gallium Nitride	GaN	III and V	Gallium nitride (GaN) is gaining popularity in the field of microwave transistors, particularly in applications that require high temperatures and power levels. It is also finding use in certain microwave integrated circuits (ICs). GaN presents challenges in achieving p-type doping, but it demonstrates relatively good resistance to ionizing radiation. Additionally, GaN has been successfully utilized in the production of blue LEDs. It possesses a band gap of 3.4 eV, which is an important characteristic for its electronic properties.
Gallium phosphide	GaP	III and V	Gallium phosphide (GaP), has found numerous applications in LED technology. In the past, it was widely used in low to medium brightness LEDs, capable of producing various colors depending on the addition of different dopants. Pure Gallium phosphide emits green light, but when doped with nitrogen, it emits yellow-green light. On the other hand, doping it with Zinc Oxide results in red light emission.
Cadmium sulphide	CdS	II and VI	Cadmium sulphide is an inorganic compound with a red-black solid appearance, categorized as an n-type semiconductor. The growing demand for cadmium sulphide in semiconductors and electronics is due to its malleability and ductility properties. It is used in photo-resistors and also solar cells. It has a band gap of 2.42 eV and electron and hole mobility of about 350 cm^2/Vs and 40 cm^2/Vs, respectively.
Lead sulphide	PbS	IV and VI	Lead sulfide (PbS) possesses a band gap of 0.37 eV. This relatively small band gap makes PbS sensitive to infrared light and valuable in various applications, particularly in infrared detectors and sensors. PbS demonstrates favorable properties with hole mobility and electron mobility in the range of $10-1000$ cm^2/Vs and $1-100$ cm^2/Vs, respectively. The specific values can vary depending on factors such as doping, temperature, and crystal structure.

OHIZE DRAFT

2.4.2.1 Donors (n-type)

By replacing one of the silicon atoms in the diamond lattice of Figure 2.3 with an atom from group V, like phosphorus or arsenic, an extra electron is introduced into the lattice structure. This additional electron is not involved in the covalent bonding between atoms, as illustrated in Figure 2.4. The dopant atom, such as arsenic, now carries one extra positive charge on its nucleus (As^+) compared to silicon due to the ionization process. This is because the extra electron of arsenic is ionized into the conduction band, leaving the arsenic atom's nucleus with more positive charge (protons) than electrons, thus resulting in the designation of the arsenic atom in its ionized form as As^+. Despite this, the overall charge of the arsenic atom remains neutral, but the focus is on the extra electron that has been introduced into the crystal structure from the ionization of the dopant atom.

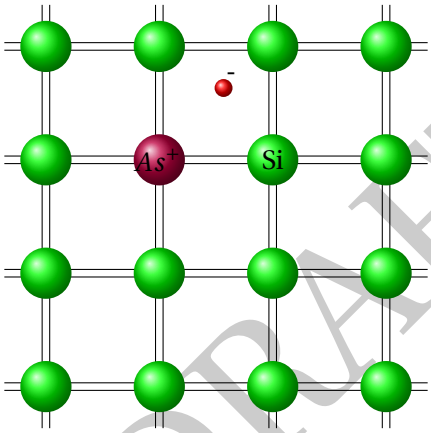


Figure 2.4: n-type: Introduction of group V dopant

The dopant from group V is known as a donor and the resulting extrinsic material is referred to as n-type. The extra electron lies just some 50 meV below the conduction band as shown in Figure 2.5. If some external stimuli above 50 meV are applied to the extrinsic semiconductor, the extra electron, on gaining 50 meV jumps to the conduction band and free to move about the crystal along with the other conduction electrons. This excitation and jump into the conduction band is termed ionization and the donor atom, such as arsenic, becomes positively charged (A^+). The concentration of these ionized atoms is denoted as N_d^+. The energy required to excite the donor electron is referred to as the donor ionization energy (E_d). Donors of interest are those with low ionization energy such that if N_d is the concentration of donor atom at room temperature, then the density of ionized donor atom N_d^+ will be entirely or almost equal to N_d.

Ionization and Ionization Energy

Ionization refers to the process of removing an electron from its orbital around an atom, to a point where it is no longer associated with the atom. The energy required for this process is known as ionization energy. During ionization, electrically neutral atoms can be transformed into electrically charged atoms by gaining or losing electrons.

It is important for readers to observe the distinction between intrinsic and extrinsic silicon. In intrinsic silicon, both mobile holes and electrons are generated. On the other hand, in the case of extrinsic silicon, specifically in the n-type scenario, a mobile electron is generated while the positive charge related to the dopant remains fixed and immobile.

UNDER DRAFT007

2.7.1 Diffusion

Diffusion is the net motion of charge carriers in response to a concentration gradient. It occurs when charged particles move from regions of higher concentration to regions of lower concentration. In semiconductors, diffusion plays a crucial role in the transport of carriers and is responsible for various device behaviors.

Diffusion

Diffusion is the net motion of carriers in a density or concentration gradient. This concentration gradient results in particle flow. In semiconductors, the charged particles move from an area with a higher concentration to an area with a lower concentration.

To mathematically represent diffusion, let us consider a semiconductor divided into slabs normal to the x direction, with each slab having a width of Δx (see Figure 2.9). Within each slab, there are particles of a specific species m with a concentration denoted as C_m. The concentration C_m varies with position, so that at any point x, the concentration is given by $C_m(x)$.

Let us focus on a slab centered around x, which contains particles with a concentration of $\Delta x C_m(x)$ per unit area. Over time, a fraction a of these particles will diffuse to the neighboring slab at $x+\Delta x$, resulting in a flow of particles with a concentration of $a\Delta x C_m(x)$ to the right. Similarly, in the slab centered at $x+\Delta x$, the same fraction a of particles will move to the left toward the slab at x. It is important to note that we assume random and independent motion. Therefore, the net flux

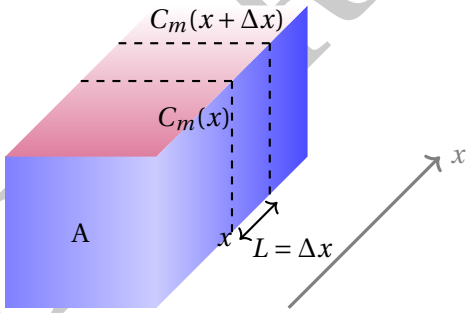


Figure 2.9: Modeling diffusion concept

density, denoted as F_m, is given by the difference in flow between the two slabs:

$$F_m = a\Delta x\,[C_m(x) - C_m(x+\Delta x)] \tag{2.37}$$

Applying Taylor's series expansion to the second term in the expression of Equation (2.37), we have

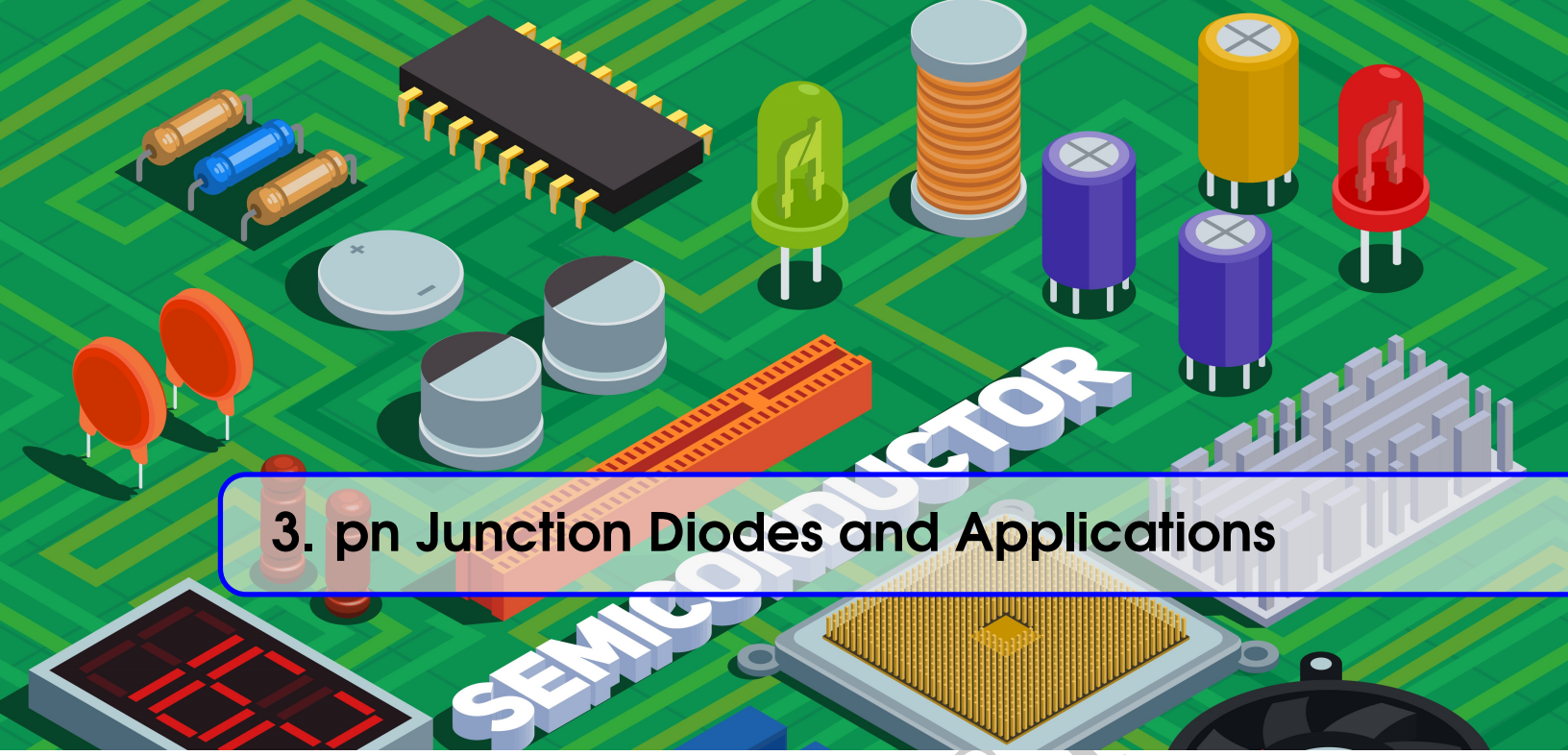
$$C_m(x+\Delta x) \approx C_m(x) + \Delta x \frac{\partial C_m}{\partial x} \tag{2.38}$$

Substituting Equation (2.38) into Equation (2.37) yields

$$F_m = -a(\Delta x)^2 \frac{\partial C_m}{\partial x} \tag{2.39}$$

$$F_m = -D_m \frac{\partial C_m}{\partial x} \tag{2.40}$$

OHIZ DRAFT



3. pn Junction Diodes and Applications

3.1 Introduction

In this chapter, the student is introduced to an important semiconductor device, the **pn junction diode**. First, we shall discuss the pn junction in thermal equilibrium. The next step is to force this junction out of equilibrium by applying a voltage called biasing. Thereafter, the different equivalent circuits that model a diode in circuit analysis will be introduced. We shall conclude by studying some applications of this simple pn junction device.

3.2 pn Junction at Equilibrium

pn Junction

In the extrinsic material of interest, a doping variation in which the semiconductor changes over a relatively short distance from a p-type to an n-type is known as pn junction. In other words, the p-type material is brought in close contact with the n-type material.

Figure 3.1 displays two profiles of a p-n junction: the step or abrupt p-n junction (depicted in Figure 3.1(a)) and the linearly-graded p-n junction (illustrated in Figure 3.1(b)). In this text, we shall base our discussions primarily on the step p-n junction being the ideal state.

The electrostatic potentials on the n-side ϕ_n and on the p-side ϕ_p region are written respectively as

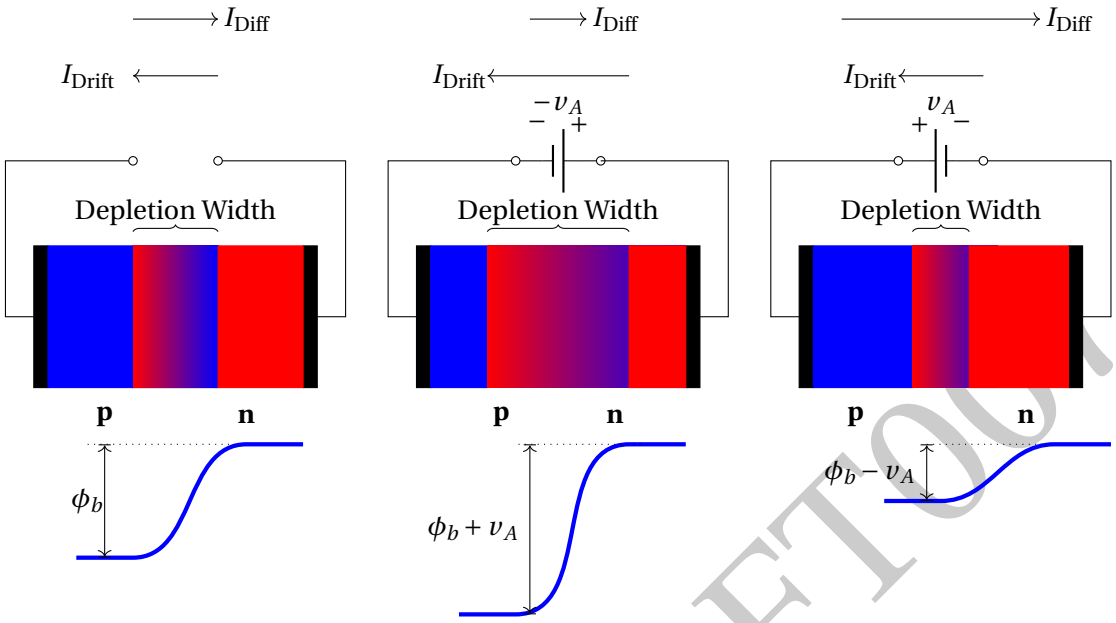
$$\phi_n = V_{TH} \ln \frac{N_{Dn}}{n_i} \tag{3.1}$$

$$\phi_p = -V_{TH} \ln \frac{N_{Ap}}{n_i} \tag{3.2}$$

where V_{TH} is the thermal voltage expressed as

$$V_{TH} = \frac{kT}{q} \tag{3.3}$$

OHL DRAFT



(a) Open-circuit (b) Reverse-bias (c) Forward-bias

Figure 3.3: Barrier potential, ϕ_b across the pn junction for $\pm v_A$

material is represented by L_n. We can approximate the widths w_p and w_n as approximately equal to L_n and L_p, respectively. This essentially means that w_p and w_n represent the average distance that minority carriers (holes in the n-type material and electrons in the p-type material) can diffuse into a region dominated by majority carriers before undergoing recombination.

▪ **Example 3.1** Consider a pn junction in equilibrium at room temperature ($T = 300$ K) for which the doping concentrations are $N_{A\text{p}} = 10^{18}$ cm^{-3} and $N_{D\text{n}} = 10^{16}$ cm^{-3} and the cross-sectional area $A = 10^{-4}$ cm^2. Using $n_i = 1.5 \times 10^{10}$ cm^{-3}. Calculate the following:

(a) concentrations, p_p, n_{p0}, n_n, p_{p0};
(b) built in potential ϕ_b;
(c) width of the depletion layer w;
(d) depletion width on the n and p side; and
(e) charge stored in the depletion junction Q_j.

Solution

Given:

$$N_{A\text{p}} = 10^{18}\ \text{cm}^{-3}, \qquad N_{D\text{n}} = 10^{16}\ \text{cm}^{-3}, \qquad n_i = 1.5 \times 10^{10}\ \text{cm}^{-3},$$
$$A = 10^{-4}\ \text{cm}^2, \qquad \varepsilon_0 = 8.85 \times 10^{-14}\ \text{F/cm}$$

(a) The concentrations are obtained as
  (i) majority carrier in the doped p-type material is given as

$$p_p \approx N_{A\text{p}} = 10^{18}\ \text{cm}^{-3}$$

OHZE DRAFT 08

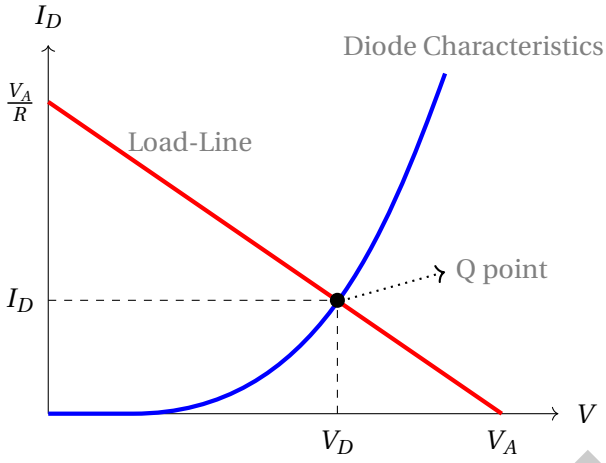


Figure 3.11: Analysis using the exponential model

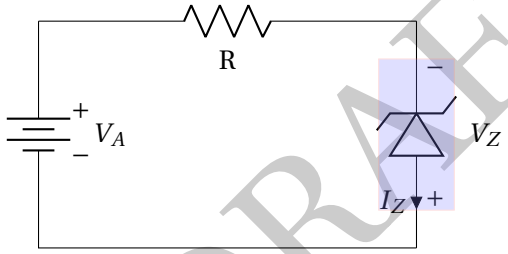
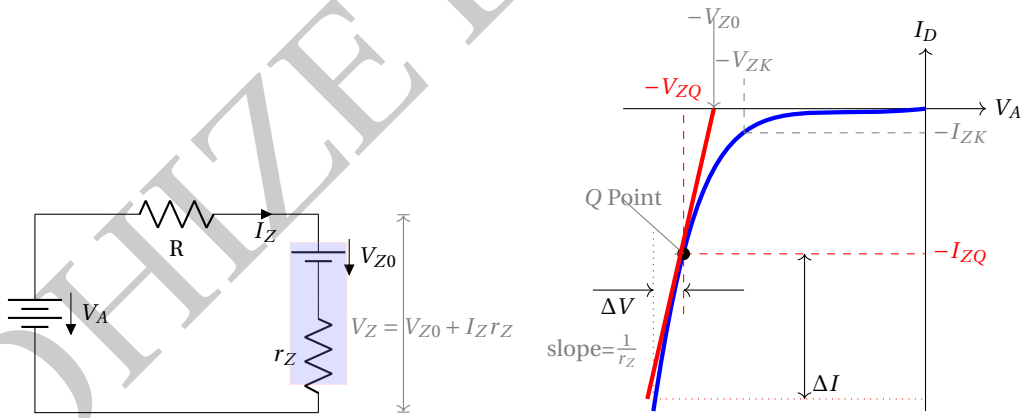


Figure 3.12: A simple zener diode circuit



(a) Zener diode equivalent circuit

(b) Zener diode *i-v* characteristics

Figure 3.13: Zener diode

The zener region of operation can be approximated as

$$V_{ZQ} = V_{Z0} + I_Z r_Z \tag{3.23}$$

where V_{Z0} denotes the point at which the straight line of the slope intersects the voltage axis in Figure 3.13(b). In circuit analysis, it is safe to approximate this point of intersection on the voltage

OHIZE DRAFT007

3.6.1.2 Full-wave rectification

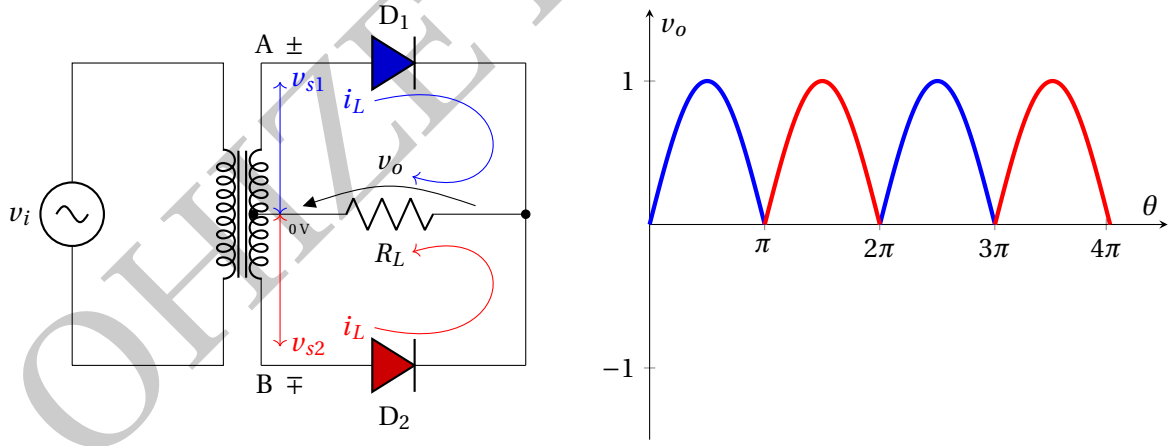
Full-wave rectification, often referred to as full-wave rectification, is a technique used to convert alternating current (AC) into direct current (DC) with continuous current flowing through the load regardless of the polarity of the input signal. Unlike half-wave rectification, where only half of the input AC signal is utilized, full-wave rectification ensures that the current flows through the load for both halves of the input signal. This is achieved through a special circuit arrangement that allows the current to always flow in the same direction through the load. As a result, the output waveform has a higher average value and provides smoother DC power compared to half-wave rectification. There are two commonly used circuits for full-wave rectification, namely:

1. Centre-tapped transformer; and
2. Bridge Rectifier.

Full-wave rectification with centre-tapped transformer

In Figure 3.38(a), we can see a transformer's secondary winding that is centre-tapped. Note that in centre tapped arrangement, the centre wire is adjusted in such a way that it falls in the exact middle point of the secondary winding so that the wire is exactly at zero volts of the AC signal. This means that there are two voltages across the two halves of the secondary winding (v_{S1} and v_{S2}), each with an opposite polarity. The magnitude of these voltages is half of the secondary output of the transformer.

During the positive half-cycle of the input AC signal, terminal A is positive and terminal B is negative while the centre tap is grounded. Hence, the diode D_1 conducts while D_2 is reverse-biased. This allows the current to flow through D_1, the load R_L, and to the centre-tap. Similarly, during the negative half-cycle, terminal B become positive and terminal A becomes negative while the centre tap is grounded. Hence, D_2 conducts while D_1 is reverse-biased. As a result, the current flows through D_2, the load R_L, and to the centre-tap.



(a) Centre-tapped transformer rectifier

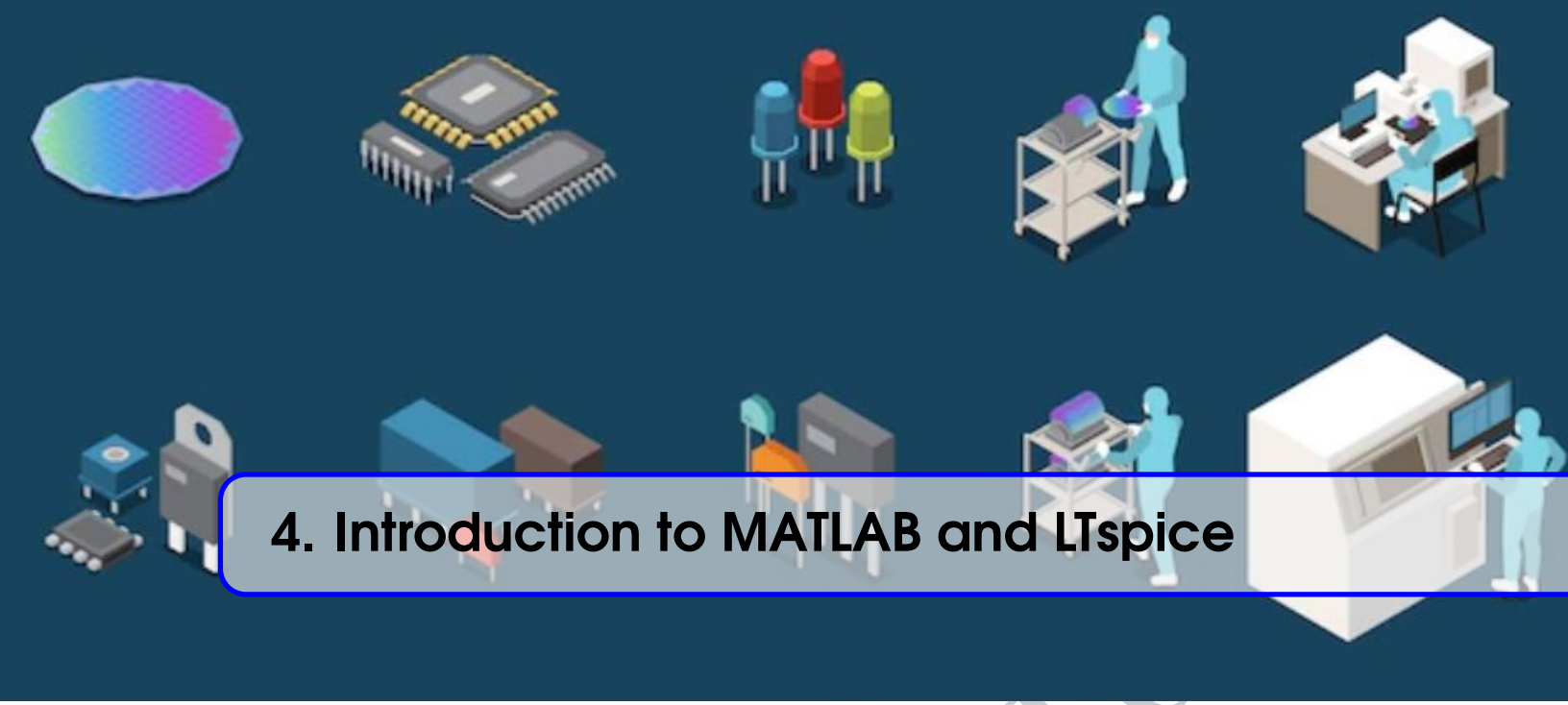
(b) Output signal

Figure 3.38: Full-wave centre-tapped rectification

It is important to note that the current through the load flows in the same direction for both the positive and negative halves of the input AC signal. This leads to full-wave rectification, where the current flows continuously through the load, providing a more efficient conversion of AC to DC.

Additionally, it is worth mentioning that the output frequency of the full-wave rectified signal is twice the input frequency. While the input signal completes its cycle in the interval from 0 to 2π,

OHZE DRAFT007



4. Introduction to MATLAB and LTspice

OHZE DRAFT

4.1 Introduction

The call for innovation and creativity is growing and students must not limit learning experience to just experiments and exploration within physical laboratory. We have therefore integrated LTspice and MATLAB within the course curriculum for electronics in a manner that supports self-directed learning plus the benefits of zero-cost while making mistakes! Engineers working at the cutting-edge often use state-of-the-art design and simulation tools in their work. This is worthwhile even if it means dealing with a few bugs, small annoyances, and less than optimal documentation.

Two of the state-of-the-art simulation tools introduced in this chapter are analytic tools employed for design and demonstration purposes, each with its unique advantage. LTspice offers good graphical user interface (GUI) while only showing device characterisation of a given network while MATLAB interfaces the students with the mathematical details that define the device characterisation. It means with MATLAB one must understand the underlying physics of the network to be able to code its outcome. But not to worry, the task here takes into consideration the very likelihood that you may be a first-time user of the analytical tools discussed here.

We have employed both MATLAB and LTspice to support the learning of semiconductor technology. This does not refute the need for practical or laboratory demonstration. In fact, this is to complement the challenges of setting up laboratory while noting that LTspice is an open source software and MATLAB is readily available in all higher institutions of learning. As a student being trained for the state-of-the-art industrial experience, you should approach the tasks or projects in this chapter in a conservative way and carry out your assignment as early as possible. You should also seek help if you find any difficulties; after all, Engineering is about team work.

The concept presented in parts is to have experiments undertaken using LTspice and the results obtained are analysed using MATLAB. The goal is to introduce the young Engineering students to both the semiconductor devices and the analytical tools. The Experimental Concept is shown in Figure 4.1.

4.2 LTspice

The projects use the LTSpice simulation software. The LTSpice installation and user guide may be seen in Section 4.2.1. LTspice is a circuit simulator based on the SPICE simulator and available as a

```
ND = input('Input the n-side doping concentration (in cm^-3), ND = ');
T = 300; % Temperature (K)

% Compute hole mobility using equation 4.5
NAref = 2.35e17;
upmin = 54.3;
up0 = 406.9;
ap = 0.88;
up = upmin + up0 ./ (1 + (ND ./ NAref) .^ ap); % Equation 4.5

% I-V Calculation
VA = linspace(-1, 0.2);
DP = k * T * up; % Equation 4.4
LP = sqrt(DP .* taup); % Equation 4.3
I0 = q * A * (DP ./ LP) .* (ni ^ 2 ./ ND); % Equation 4.2
I = I0.' * (exp(VA ./ (k * T)) - 1); % Equation 3.16

% Plotting Results
close;
plot(VA, I);
grid on;
ymin = -2 * I0(1);
ymax = 5 * I0(1);
axis([-1, 0.2, ymin, ymax]);
xlabel('VA (volts)');
ylabel('I (amps)');

% Adding axis and key
xx = [-1 0.2];
yx = [0 0];
xy = [0 0];
yy = [ymin, ymax];
hold on;
plot(xx, yx, '-w', xy, yy, '-w');

j = length(ND);
for i = 1:j
    yput = (0.70 - 0.06 * i) * ymax;
    yk(i, 1) = yput;
    yk(i, 2) = yput;
    text(-0.68, (0.69 - 0.06 * i) * ymax, ['ND=', num2str(ND(i)), '/cm^3']);
end

xk = [-0.8 -0.7];
plot(xk, yk);
text(-0.74, 0.75 * ymax, 'Si 300K');
hold off;
```

©HIZE DRAFT007

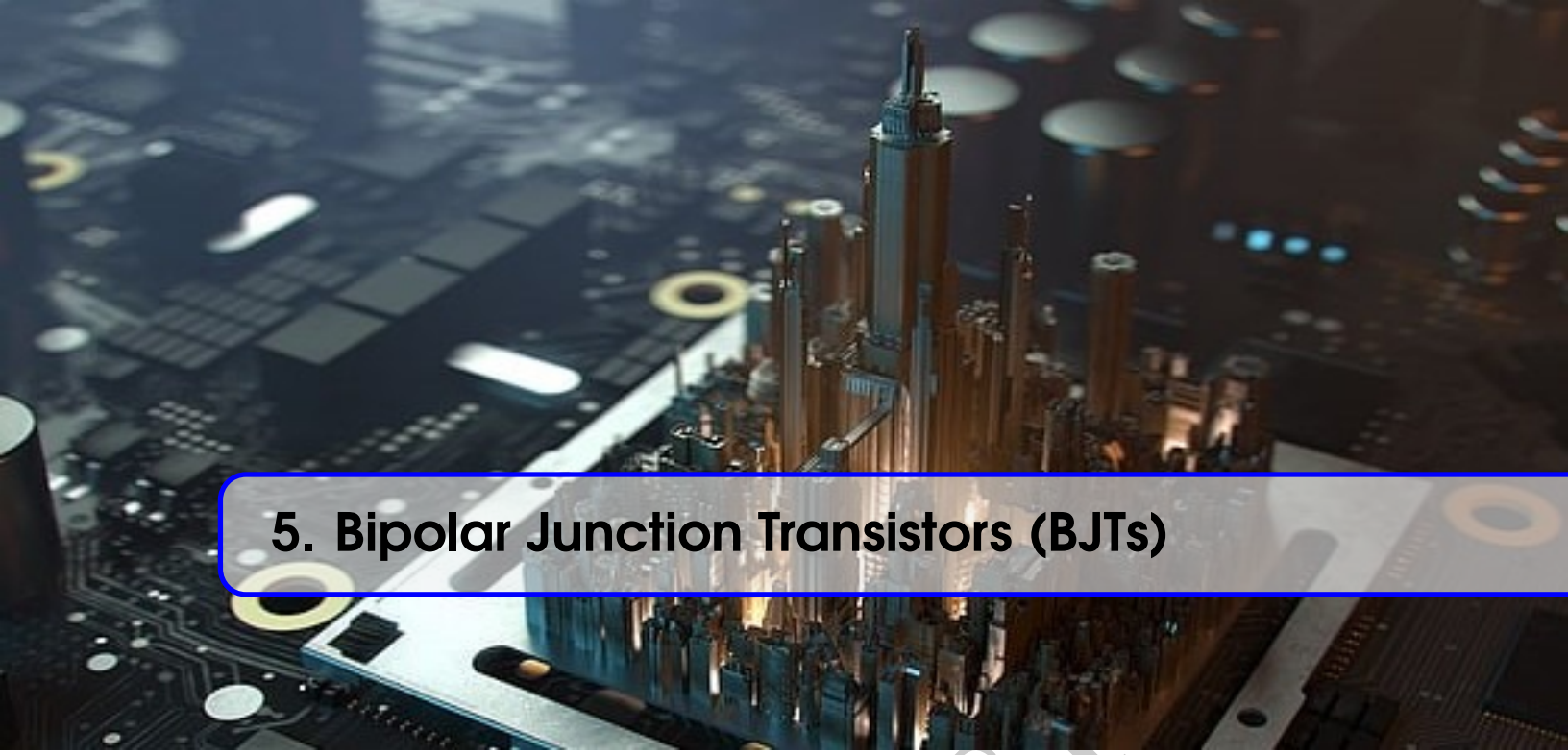
Please copy and paste the MATLAB code provided above and explore how the diode characteristics vary as a function of the semiconductor doping. The program is designed to handle multiple doping inputs. When prompted, enclose your input in square brackets and type the desired doping values in response to the N_D prompt.

Make sure you have MATLAB installed to run this code. The program will calculate the ideal diode current-voltage characteristics and plot the results. The doping concentrations will be displayed as a key on the graph.

Please note that you may encounter typos or errors on your path, so it is important to debug

II

Part Two



5. Bipolar Junction Transistors (BJTs)

5.1 Introduction

This chapter introduces the three-terminal device known as the transistor. The transistor is an extension of the two-terminal pn junction device discussed in Chapter 3. These three-terminal devices, the transistors, are significantly more beneficial as they have applications in signal amplification, switching circuits, digital logic, and memory circuits. Transistors have enormous implications for the electronics industry, considering that the average Intel Core *i7* processor contains about 2.2 billion transistors!

The three-terminal device is generally classified into two broad categories: the Bipolar Junction Transistor (BJT) and the Unipolar Junction Transistor or Field Effect Transistor (FET). Figure 5.1 shows the classification. However, this chapter will discuss the BJT, while the FET will be covered in Chapter 6. There are two types of BJT: pnp and npn. The invention of the BJT in 1948 at the Bell Telephone Laboratory ushered in an era of solid-state circuits. Today, BJTs are part of integrated circuits that can contain several million transistors on a single chip. The term "bipolar" refers to the fact that current conduction in this transistor occurs through both holes and electrons.

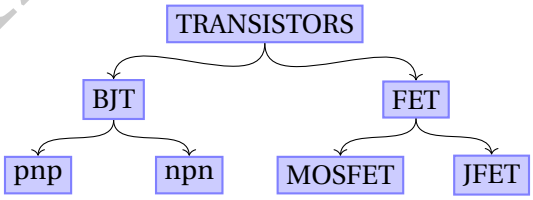


Figure 5.1: Transistors and the classifications

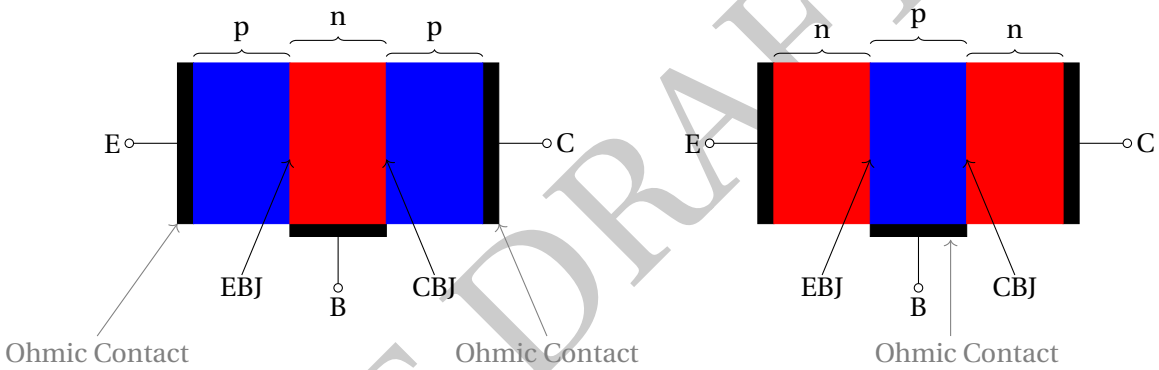
5.2 Construction

The Bipolar Junction Transistor (BJT) is a three-terminal and two-junction device. Figure 5.2 illustrates the construction of both pnp and npn transistors. In the pnp transistor, two p-type materials are sandwiched by an n-type material, forming the structure. Conversely, the npn transistor consists of two n-type materials sandwiching a p-type material.

OHIZE DRAFT

This arrangement of materials creates two pn junctions within the transistor. With reference to Figure 5.2(a), the junction to the left, known as the base-emitter junction, is formed between the n-type material and one of the p-type regions. The outer junction (to your right), referred to as the collector-base junction, is formed between the other p-type region and the n-type material. Similarly, for the npn transistor in Figure 5.2(b) the junction to the left, known as the base-emitter junction, is formed between the p-type material and one of the n-type regions. The outer junction (to your right), referred to as the collector-base junction, is likewise formed between the other n-type region and the p-type material. These two junctions play crucial roles in the operation of the BJT and enable its amplification capabilities.

The pnp and npn configurations of the BJT allow for different types of current flow within the transistor. In the pnp transistor, the current is carried by holes, which are the majority carriers in the p-type regions. In contrast, in the npn transistor, the current is carried by electrons, which are the majority carriers in the n-type regions. By controlling the flow of these charge carriers through the base region, the BJT can effectively amplify and control electrical signals.[1]



(a) pnp transistor construction

(b) npn transistor construction

Figure 5.2: Transistor construction

Figure 5.2 shows the three terminals of the BJT, which are the Emitter (E), Base (B), and Collector (C). The terminals are connected to substrate through ohmic contacts. Also indicated in the figure are two important pn junctions within the BJT: the Emitter-Base junction (EBJ) and the Collector-Base junction (CBJ).

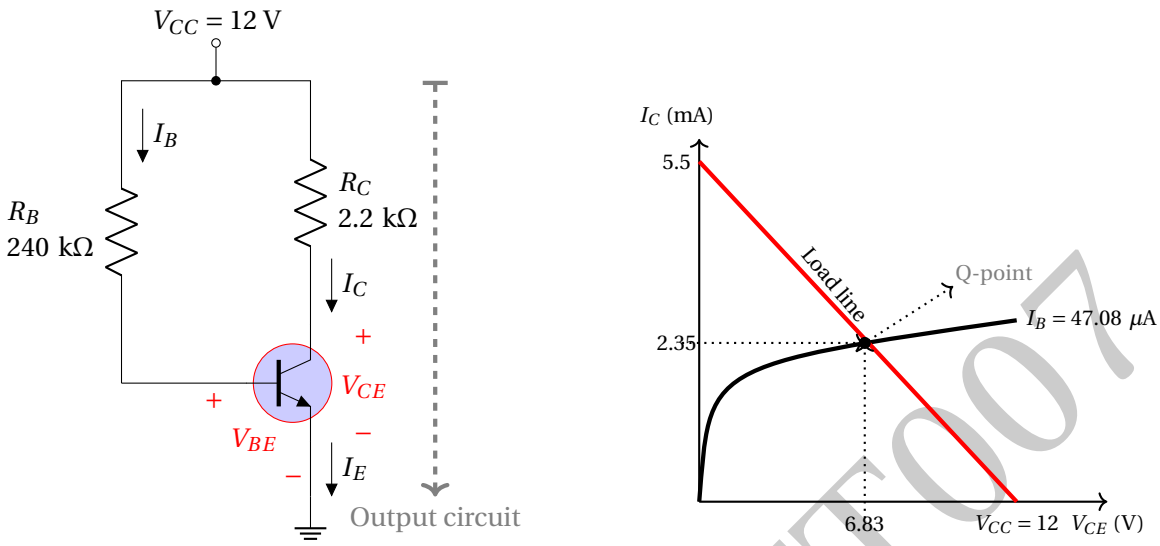
These junctions play a crucial role in the operation of the transistor. By applying appropriate biasing to these junctions, different regions of operation can be achieved. The three main regions of operation are the **Active region**, **Cutoff region**, and **Saturation region**.

Active or linear region

In this region, the base-emitter junction is forward-biased and the collector-base junction is reverse-biased. This is the normal transistor operation mode for amplification, and is characterized by the transistor current gain value, beta (β).

[1] The doped regions in the diagram is not drawn to scale

OHIZE DRAFT007



(a) Fixed-bias circuit indicating current and voltage

(b) Determining operating point

Figure 5.14: Plot of load line superimposed on output characteristic curve for Example 5.2

Please note that solving this problem requires prior familiarity with the device's output characteristic curve, against which the load line is positioned. In a usual scenario, the quiescent base current, denoted as I_{B_Q}, is provided, rendering the graphical approach unnecessary. With this value, you can compute the quiescent collector current, designated as I_{C_Q}, using a given DC current gain, β. Following this, the quiescent collector-emitter voltage, denoted as V_{CE_Q}, can be ascertained through the network's output equation.

Limit of Operation

The limit of operation refers to the maximum allowable power dissipation in a transistor. This limit is determined by factors such as the junction temperature and the ambient temperature. As electrical power is consumed within the transistor, the junction temperature increases. If the power dissipation exceeds the maximum allowed rating, the junction temperature can rise to a point where the device burns out. Therefore, the maximum allowed power dissipation represents the amount of power consumption that can be safely handled by the transistor without causing damage.

The correct biasing of a transistor is of utmost importance for its proper operation. Biasing establishes the DC operating point, also known as the quiescent or quiet point, where the transistor is ready to receive an AC signal. It is crucial to set the biasing correctly to avoid signal distortion, such as signal clipping, which occurs when the AC signal swings into the cutoff or saturation regions.

The ideal quiescent point for a voltage or current amplifier lies at the center of the DC static or load line. Figure 5.15 illustrates different biasing points, denoted as A, B, C, and D. Biasing points too close to saturation (point A) or cutoff (point B) are undesirable as they can lead to distortion. Similarly, a biasing point close to the maximum power rating (point D) is also undesirable.

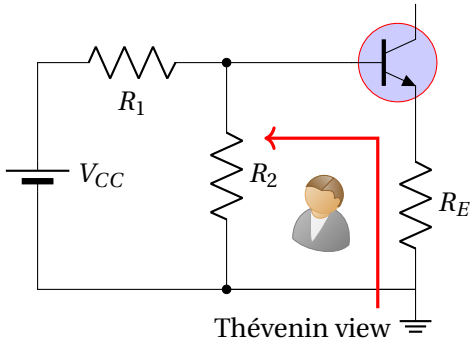
For signal amplification, circuit biasing aims to set the operating point away from cutoff, saturation, and the edge of the operating limit (maximum power dissipation). The desirable quiescent point is around location C. This allows the small signal AC to swing comfortably around the quies-

DRAFT007

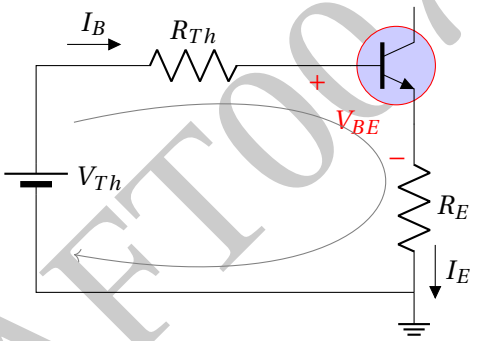
Thévenin method

In this method, the voltage-divider circuit is redrawn using the Thévenin technique. Figure 5.23(a) illustrates the redrawn circuit for conceptualization, while Figure 5.23(b) represents the Thévenin equivalent circuit.

Definition 5.1 — Thévenin's Theorem. Any linear circuit containing more than one voltage source and resistor can be replaced by just one single voltage source designated as V_{Th} in series with a single resistor R_{Th}.



(a) Redrawn input network



(b) The Thévenin equivalent circuit

Figure 5.23: Thévenin's technique for the voltage-divider bias circuit

To draw the equivalent Thévenin circuit, let us observe the network shown in Figure 5.23(a) from the right side. Generally, to find Thévenin resistance, you need to deactivate all the independent sources in the circuit (voltage sources become short circuits, and current sources become open circuits). Then, we calculate the equivalent resistance as seen from the load terminals. For the circuit of interest in Figure 5.23(a), the Thévenin resistance is given as R_{Th}.

$$R_{Th} = R_1 \parallel R_2 \tag{5.32}$$

or

$$R_{Th} = \frac{R_1 \times R_2}{R_1 + R_2}. \tag{5.33}$$

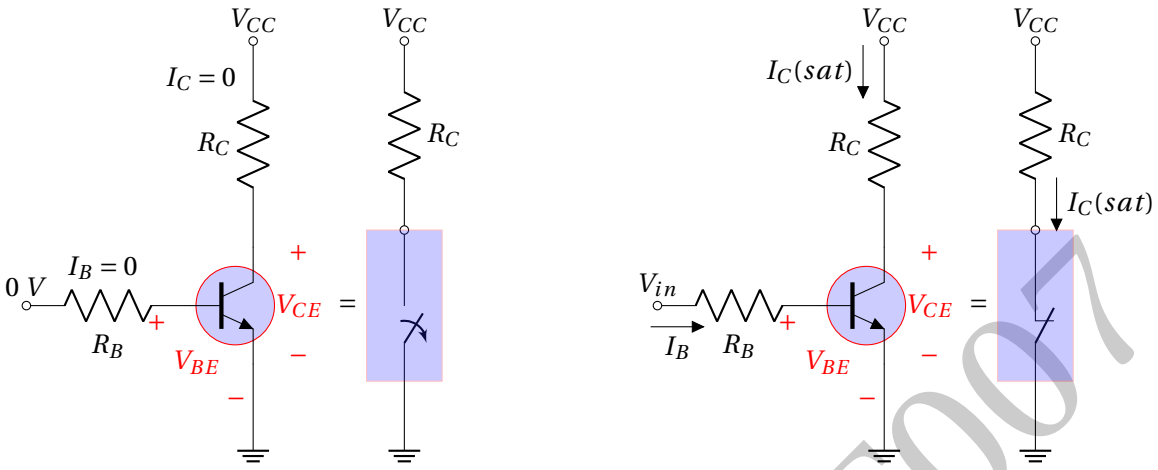
To find the Thévenin voltage, we look into the circuit from the load terminal, which in our case is the transistor network. Disconnect the load and calculate the voltage across the open circuit. We now have two resistors R_1 and R_2 in series so that the Thévenin voltage is obtained using the voltage-divider rule as

$$V_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{5.34}$$

Finally, we create the Thévenin equivalent circuit, which consists of a single voltage source (V_{Th}) in series with a single resistor (R_{Th}). The complete Thévenin's equivalent circuit is then depicted in Figure 5.23(b). The redrawn circuit now represents our base-emitter or input loop. By applying KVL, we can obtain the following equation:

$$0 = V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E \tag{5.35}$$

QHIZE DRAFT007



(a) Cutoff open-circuit

(b) Saturation closed-circuit

Figure 5.41: Illustration of the switching action of a BJT circuit

Table 5.3: **Node Voltages for Cutoff and Saturation Regions**

Biasing method	**Cutoff**	**Saturation**
fixed-bias	$V_{CE} = V_{CC}\|_{I_C=0}$	$I_C = \frac{V_{CC}}{R_C}\|_{V_{CE}=0}$
Emitter Stabilized	$V_{CE} = V_{CC}\|_{I_C=0}$	$I_C = \frac{V_{CC}}{R_C+R_E}\|_{V_{CE}=0}$
Voltage-Divider	$V_{CE} = V_{CC}\|_{I_C=0}$	$I_C = \frac{V_{CC}}{R_C+R_E}\|_{V_{CE}=0}$
Collector-Feedback	$V_{CE} = V_{CC}\|_{I_C=0}$	$I_C = \frac{V_{CC}}{R_C+R_E}\|_{V_{CE}=0}$

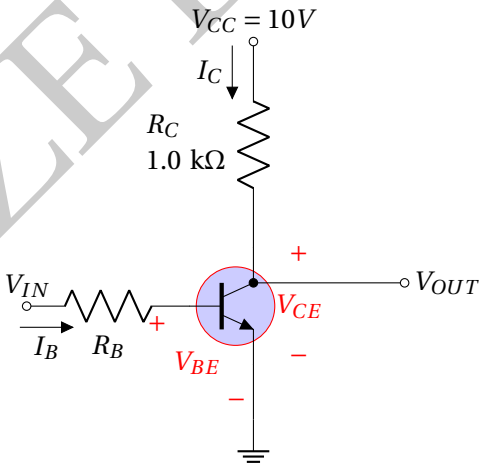


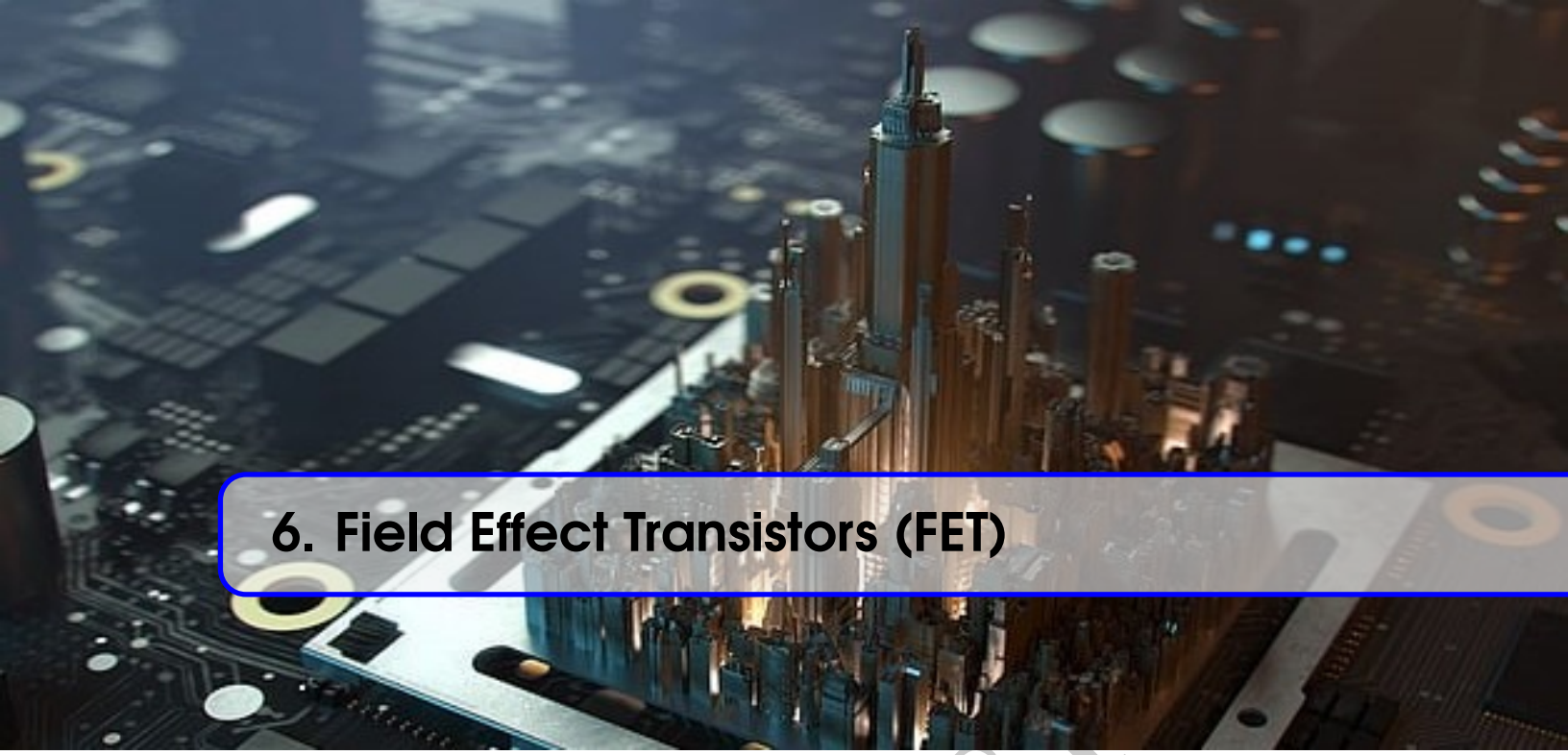
Figure 5.42: Transistor switching circuit for Example 5.13

(a) What is the value of V_{CE} when the input voltage V_{in} is 0 V?
(b) What is the minimum value of I_B required to saturate the transistor if β is 200?
(c) Find the maximum value of R_B when the input voltage V_{in} is 5 V.

Solution

(a) When $V_{in} = 0$ V, the transistor is in the cutoff region. This occurs when the collector-emitter

OHIZE DRAFT007



6. Field Effect Transistors (FET)

6.1 Introduction

In the previous chapter, we learned about the BJT, a three-terminal device where the output is controlled by applying a potential to a specific terminal. In the BJT, we saw that the potential applied to the base, called V_{BE}, creates the current I_B. This applied potential affects the barrier potential. Another way to control the barrier potential in a transistor is by using field plates, which modulate the barrier potential through induced charges on adjacent electrodes. This technique gives rise to Field Effect Transistors (FETs), which have a high input impedance and eliminate the need for control current. Consequently, FET is voltage controlled device while BJT is current controlled.[1]

There are different classifications of FETs, but we will only consider the categories shown in Figure 6.1. Similar to the base terminal in the BJT, the control terminal in the FET is called the **Gate**. The terminals corresponding to the emitter and collector in the BJT are now referred to as the **Source** and **Drain** in the FET, respectively. It is important to understand that in a FET, current flows between the source and the drain primarily through the drift phenomenon. Conversely, in BJT, current conduction occurs through both the drift and diffusion phenomena. The BJT is called bipolar because it involves both holes and electrons in current flow, while the FET is unipolar because current flows only through the majority carrier. FETs are smaller and easier to fabricate compared to BJTs, which is why they are widely used in electronic devices, particularly in the design of integrated circuits (ICs).

6.2 JFET

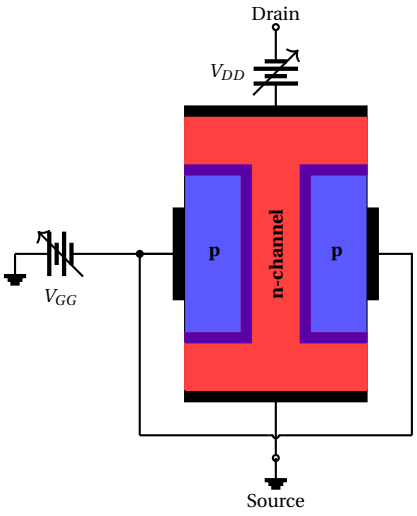
The Junction Field Effect Transistor (JFET) became widely used in the 1960s. It is a three-terminal device that conducts current through either electrons or holes, depending on whether it is an n-channel or p-channel JFET. In the n-channel type, current is carried by electrons, while in the p-channel type, it is carried solely by holes. These are known as unipolar Transistors. The circuit symbols for the n-channel and p-channel JFETs are shown in Figure 6.2. Notice that the arrow points inward for the n-channel device, indicating the conventional direction of current flow for I_G. In contrast, for the p-channel device, the arrow points outward, indicating the direction of I_G.

[1] Control current in the BJT is the base current I_B. In the FET, the equivalent is the gate current I_G, which is zero. Therefore, FET control does not involve current modulation.

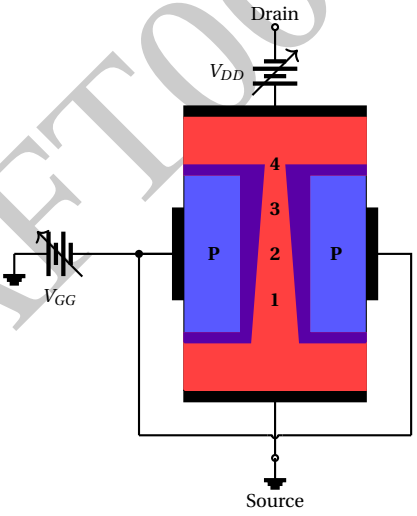
OHZE DRAFT

positive voltage, as shown in Figure 6.5(b), a current I_D starts to flow into the drain through the non-depleted n-channel between the pn junctions. As we further increase V_{DD} above a few tenths of a volt, the device enters an interesting phase of operation.

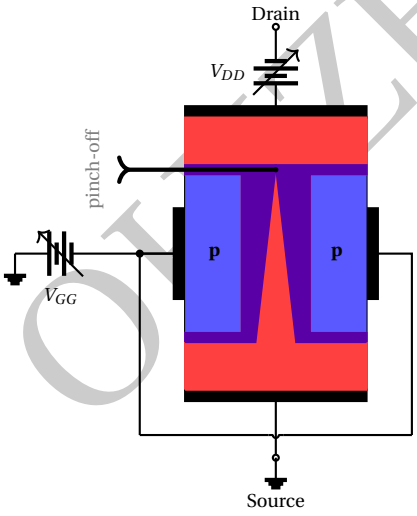
To understand this phase, let us consider the progressive increase in voltage from the grounded source to the applied V_{DD} in Figure 6.5(b). Assume a voltage of $V_{DD} = 5$ V being applied at the drain, the potential progressively takes on values of 1 V, 2 V, 3 V, and 4 V along the channel from the source to the drain, as indicated in Figure 6.5(b). Meanwhile, the gate (p-type side) is at zero volts, creating a varying reverse bias between the channel and the gate, similar to a pn junction. This situation is depicted in Figure 6.5(c). As the reverse bias potential increases along the channel, the depletion widths widen towards the drain, leading to a narrower channel.



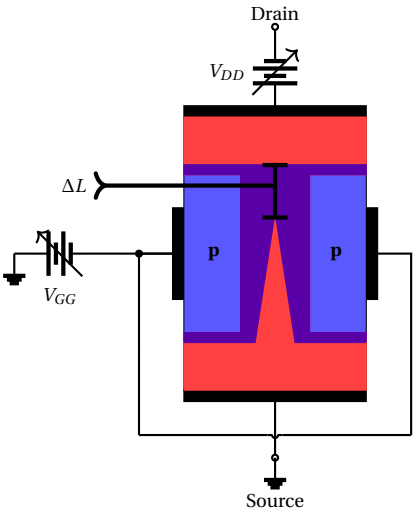
(a) $V_G = 0$ V and $V_{DD} = 0$ V



(b) $V_G = 0$ V and $V_{DD} > 0$ V



(c) $V_{GG} = 0$ V and $V_{DD} = V_{Dsat}$



(d) $V_{GG} = 0$ V and post pitch-off at $V_{DD} > V_{Dsat}$

Figure 6.5: A depiction of JFET operation

This effect is reflected in the output characteristic curve shown in Figure 6.6. It can be observed

OLIZE DRAFT007

But we know from the device equation that $I_D = I_S$ so that $V_{R_S} = I_D R_S$

$$\therefore V_{GS} = -I_D R_S \tag{6.12}$$

Note that in this scenario, V_{GS} is a function of the drain current, and its magnitude varies. It is not fixed as in the case of the fixed-bias configuration. Substituting Equation (6.12) into Equation (6.5), we obtain:

$$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_P}\right)^2 \tag{6.13}$$

Now let us consider, the output loop by apply KVL to obtain.

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \tag{6.14}$$

Rearranging the expression and substituting $I_S = I_D$, we may now write

$$V_{DS} = V_{DD} - I_D (R_S + R_D) \tag{6.15}$$

A graphical approach can also be obtained for the self-bias configuration by finding the interception between the transfer equation and the network equation as shown in Figure 6.14 where the network equation is the load-line whose slope is $-1/R_S$.

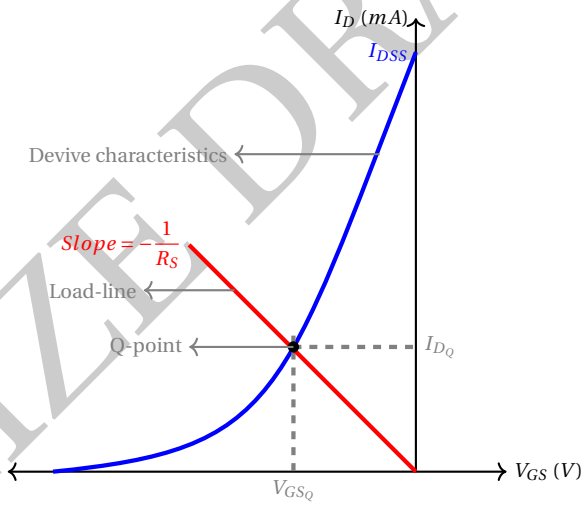


Figure 6.14: Graphical solution for self-bias network

6.2.6.3 Voltage-divider biasing

Figure 6.15(a) illustrates the voltage-divider biasing configuration. To obtain the DC equivalent circuit shown in Figure 6.15(b), we apply the rules for drawing the DC equivalent circuit as presented in section 6.2.6.1. It is important to note that, unlike the control current (I_B) of BJTs, the gate current I_G is negligible, which means $I_G = 0$ mA. As a result, resistors R_1 and R_2 will be in series, while V_G represents the voltage across R_2. Therefore, we can apply the voltage-divider rule to determine:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{6.16}$$

OHIZE DRAFT007

thus the device equation to be graphed is

$$I_D = 0.56 \text{ mA/V}^2 (V_{GS} - 4 \text{ V})^2$$

From the graph in Figure 6.35 we see that the Q point is

$$V_{GS_Q} = 8.5 \text{ V} \qquad I_{D_Q} = 11.3 \text{ mA}$$

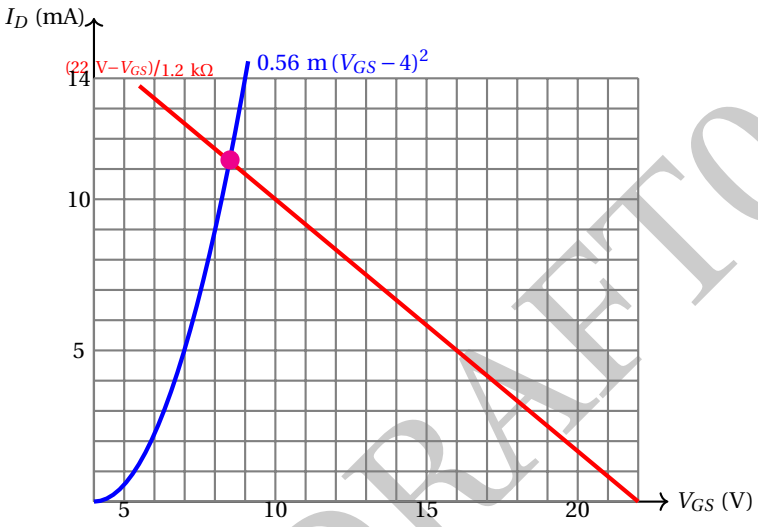


Figure 6.35: Graphical solution to Example 6.7

(b) Applying KVL to the output loop and solving for V_{DS} gives

$$V_{DS_Q} = V_{DD} - I_{D_Q}(R_D + R_S)$$
$$V_{DS} = 22 - 8.5 \text{ mA}(1.2 \text{ k}\Omega + 0.51 \text{ k}\Omega)$$
$$= 7.5 \text{ V}$$

(c) V_D is

$$V_D = V_{DS} + I_D R_S$$
$$V_D = 7.5 \text{ V} + 8.5 \text{ mA} \times 0.51 \text{ k}\Omega$$
$$= 11.83 \text{ V}$$

(d) V_S is

$$V_S = I_D R_S$$
$$V_S = 8.5 \text{ mA} \times 0.51 \text{ k}\Omega$$
$$= 4.34 \text{ V}$$

■

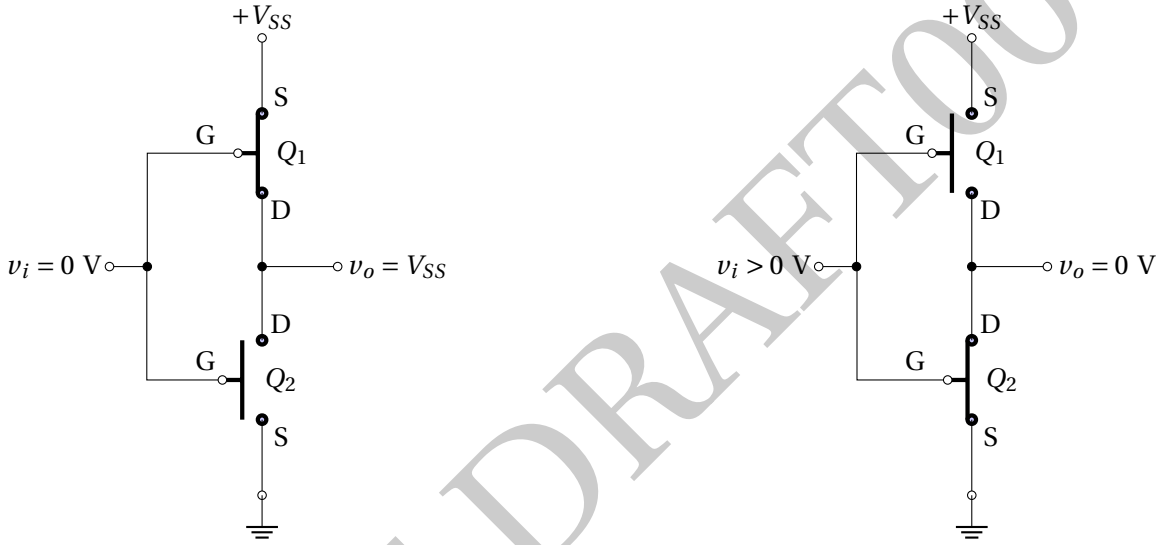
■ **Example 6.8** For the EMOSFET voltage-divider network shown in Figure 6.36, determine the following:

OHIZE DRAFT007

The gate-to-source voltage is negative ($-V_{SS}$). Hence, Q_1 will conduct, if we consider the conduction condition $V_{GS} > -V_{GS_{th}}$. Conversely, given that the source terminal is grounded for Q_2, the gate-to-source voltage (V_{GS}) for the n-channel is:

$$\begin{aligned} V_{GS} &= V_{GG} - V_{SS} \\ &= 0V - 0V \\ &= 0V \end{aligned}$$

Therefore, Q_2 is in the off-state and acts as an open circuit, allowing the entire supply voltage (V_{SS}) to be coupled to the output.



(a) CMOSFET when input signal is low

(b) CMOSFET when input signal is high

Figure 6.45: Operational Illustration of CMOS

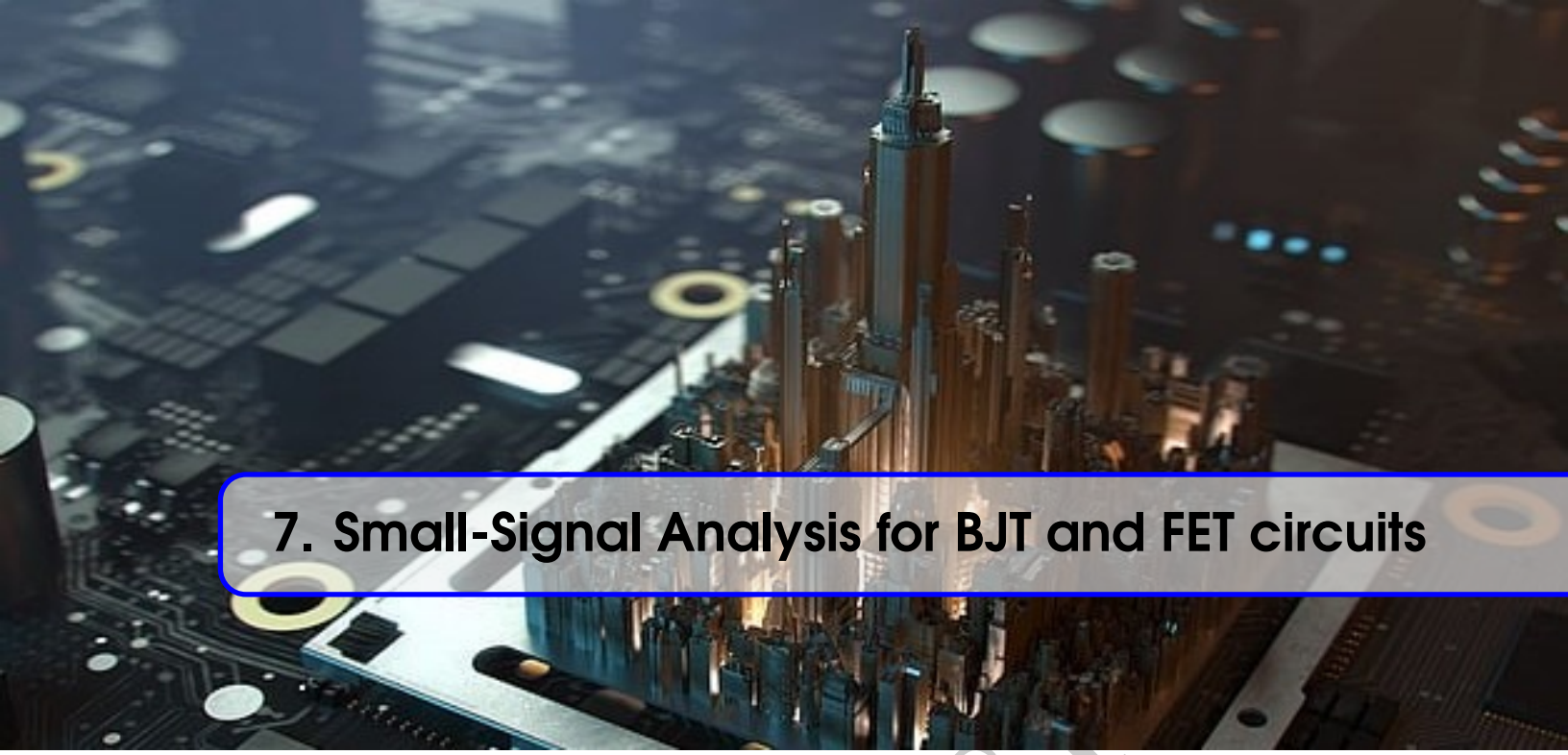
(b) When the input signal is high:
Now, let us consider when a signal is applied to the gate terminal, such as V_{GG} = 5V (see Figure 6.45(b)). In this case, the p-channel MOSFET (Q_1) is biased off (open circuit), while the n-channel MOSFET (Q_2) is biased on (short circuit). As a result, Q_2 becomes a closed circuit with zero resistance, ensuring that the output is connected to ground with a voltage of zero volts. For better illustration, let us assume a supply voltage of V_{SS} = 5V. The gate voltage (V_{GS}) for the p-channel Q_1 is:

$$\begin{aligned} V_{GS} &= V_{GG} - V_{SS} \\ &= 5\text{ V} - 5\text{ V} \\ &= 0\text{ V} \end{aligned}$$

Therefore, Q_1 is not conducting and acts as an open circuit. Hence, the gate voltage (V_{GS}) for the n-channel Q_2 is:

$$\begin{aligned} V_{GS} &= V_{GG} - V_{SS} \\ V_{GS} &= 5\text{ V} - 0\text{ V} \\ &= 5\text{ V} \end{aligned}$$

CHIZE DRAFT007



7. Small-Signal Analysis for BJT and FET circuits

7.1 Introduction

In the previous section, we introduced transistors and discussed their biasing methods for operation in specific regions. We mentioned that BJTs need to be biased in the active region for signal amplification, while FETs require biasing in the saturation region. Now, our focus is on examining the AC signal response of our biased transistor circuit, which refers to when an AC signal is applied to the transistor. We will use the term "small-signal analysis" to describe this process, as it considers the magnitude of the input signal relative to the device characteristics.

In small-signal analysis, we limit the AC signal to a relatively small percentage of the transistor amplifier's operational range to avoid signal distortion. This is commonly observed in antennas and microphones, where the AC signal variation around the quiescent point is relatively small. In this chapter, you will learn about the appropriate models to represent transistors and how to simplify the amplifier circuit for AC signal analysis. By using the AC equivalent circuit and the transistor's parameters, students will be able to predict the behavior of any given transistor amplifier circuit.

To start, let us get acquainted with the notations used in this chapter. We will employ uppercase letters with uppercase subscripts, like I_C, to denote DC components. Conversely, lowercase letters with lowercase subscripts, such as i_c, will be used for AC quantities

7.2 Important Metrics in AC Analysis

The important metrics in the AC domain for a two-port network[1] are the:

- Input impedance;
- Output impedance;
- Voltage gain;
- Current gain;
- Power gain; and
- Phase shift.

[1] We shall give insight into two-port network in the next section.

OHIZE DRAFT

7.2.1 Input impedance

Input impedance

Input impedance, denoted as Z_i, is a crucial parameter in amplifiers that indicates how much load or resistance the amplifier presents to the signal source when the signal source is connected to the amplifier's input. It is like the "friendliness" of the amplifier towards the signal source.
When we connect a signal source with a voltage v_i across the amplifier's input, it results in a certain current i_i, as shown in Figure 7.1(a). The input impedance Z_i can be calculated using the following equation:

$$Z_i = \frac{|\, v_i \,|}{|\, i_i \,|} \tag{7.1}$$

Let us take a look at Figure 7.2, the voltage v_i that reaches the amplifier's input is determined by the source voltage v_s minus the voltage drop $i_i R_S$ within the signal source due to the current i_i, as described in Equation (7.2).

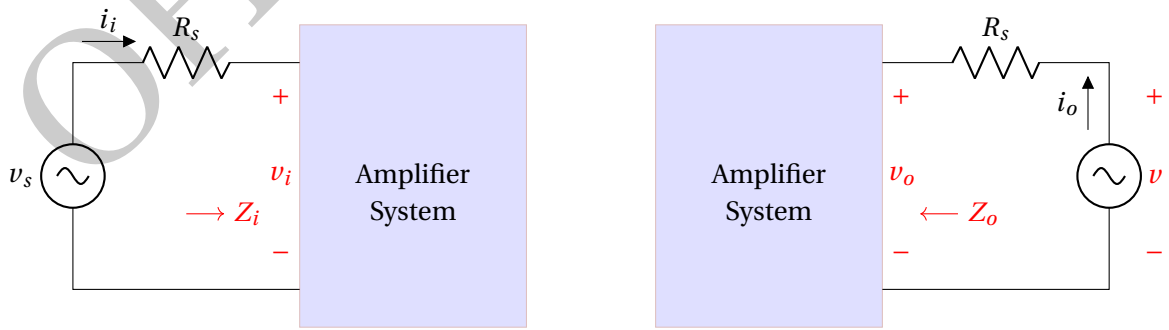
$$v_i = v_s - i_i R_S \tag{7.2}$$

If the amplifier's input impedance Z_i is too low (much smaller than the source's internal resistance R_S), it will impact the signal source given that the current in the circuit i_i is

$$i_i = \frac{v_s}{R_S + Z_i}. \tag{7.3}$$

The current in the circuit will be larger, causing more voltage drop $i_i R_S$ across the signal source. This means less voltage will be delivered to the amplifier, resulting in a weaker signal. Conversely, if the input impedance approaches infinity (extremely high), the current (i_i) becomes smaller, leading to a smaller voltage drop ($i_i R_S$) in the signal source. As a result, the load voltage (v_i) delivered to the amplifier is larger. This shows that higher input impedance is desirable for effective signal transfer.

R Note: Higher input impedance is beneficial as it presents a lighter load to the signal source, allowing for more efficient signal transfer. On the contrary, lower input impedance means the amplifier draws more current from the source, potentially affecting the source's performance.



(a) Determination of Z_i (b) Determination of Z_o

Figure 7.1: Determination of input and output impedance

OHZE DRAFT

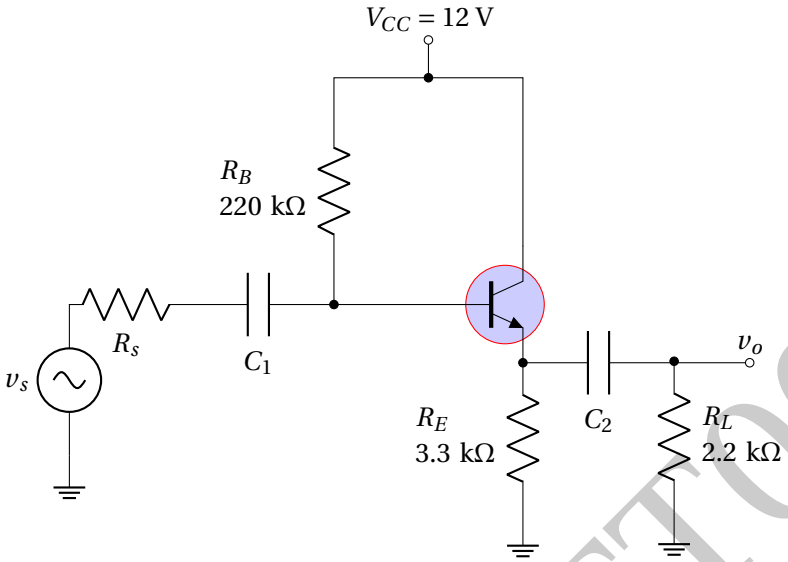


Figure 7.43: Amplifier circuit for Example 7.15

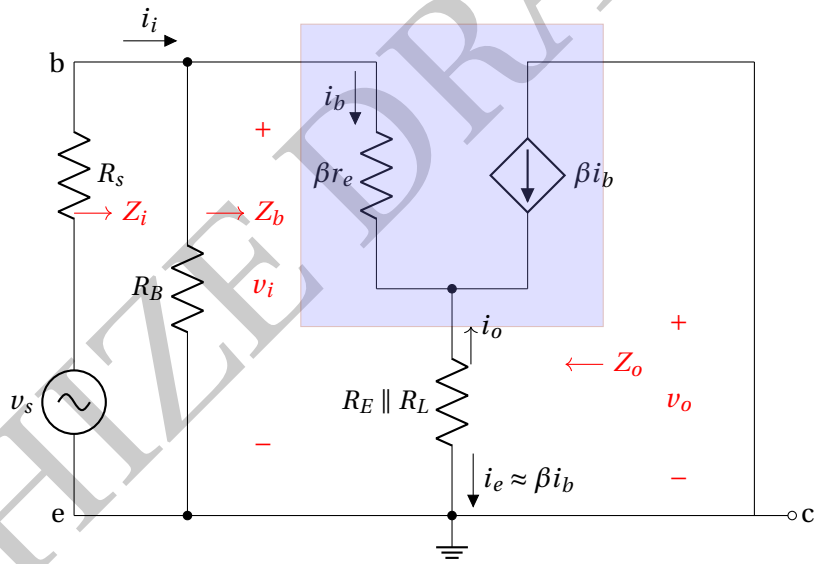


Figure 7.44: AC r_e circuit for Example 7.15

(a) The input impedance can be shown by similar derivation as with the emitter un-bypassed, CE, emitter biased configuration in Example 7.10.

$$Z_i = R_B \parallel Z_b$$

OHIZE DRAFT007

parameter, and the subscript 's' indicates that it is related to the common-source connection.

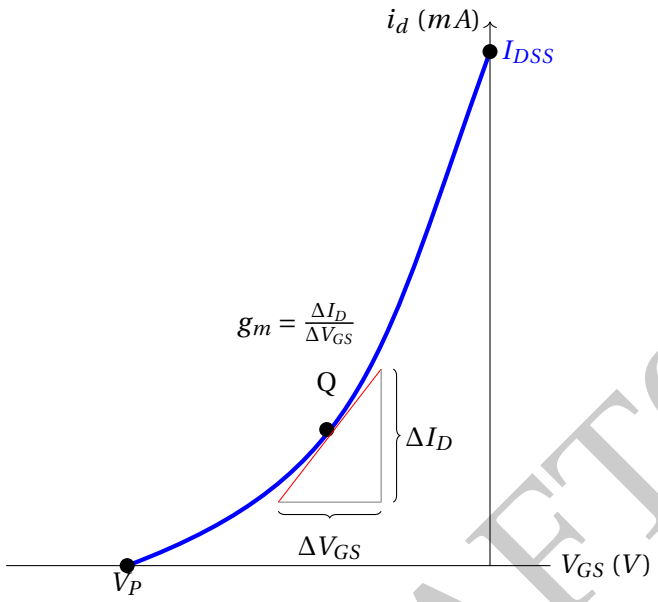


Figure 7.47: Definition of g_m using transfer characteristic

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{7.63}$$

The transconductance parameter (g_m) plays a crucial role in the FET transistor model, as depicted in the transistor equivalent circuit shown in Figure 7.46. There are two approaches to obtain g_m: a graphical approach (Figure 7.47) or a mathematical approach, which will be used here. From the non-linear curve in Figure 7.47, the transconductance (g_m) will vary along the curve. However, we can observe that the slope becomes steeper as we approach the top of the i_d axis or as v_{gs} approaches zero and beyond, entering the enhancement mode for DMOSFETs. The mathematical approach involves taking the derivative of the function I_D, derived from Shockley's equation, with respect to V_{GS} at the specified Q-point. This can be expressed as:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right] \tag{7.64}$$

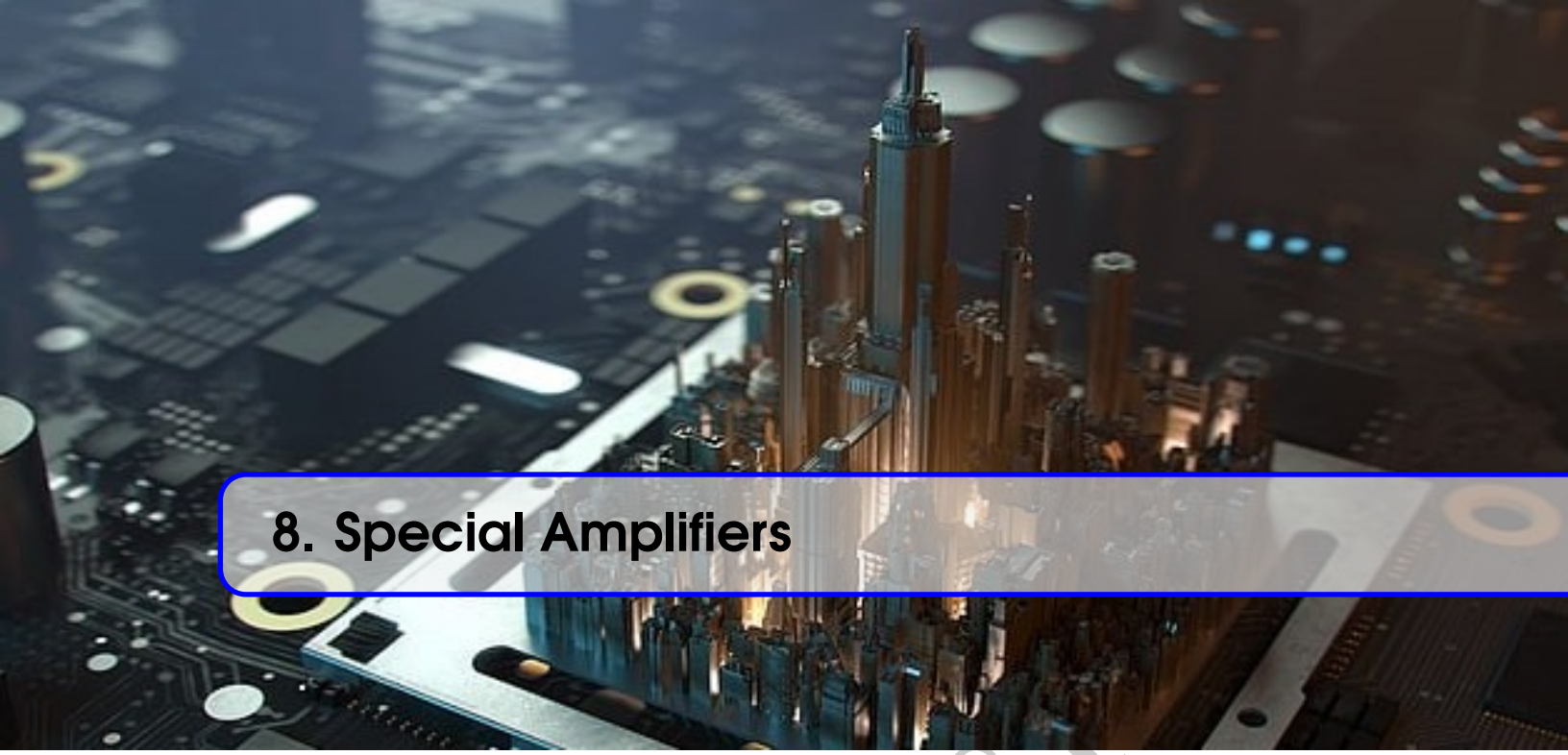
By evaluating the derivative, we obtain the expression shown in Equation (7.65). Note that $|V_P|$ represents the magnitude of V_P, disregarding polarity.

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \tag{7.65}$$

We can calculate the value of g_m at $V_{GS} = 0$ V, which corresponds to the maximum value of g_m for a JFET. In this case, Equation (7.65) simplifies to:

$$g_{m_0} = \frac{2I_{DSS}}{|V_P|} \tag{7.66}$$

OHIZE DRAFT007



8. Special Amplifiers

8.1 Introduction

In the earlier Chapters (5, 6, and 7), we learned about the basic ideas and rules behind BJT (Bipolar Junction Transistor) and FET (Field Effect Transistor) amplifiers. Now, we are going to build on that understanding and go deeper into the topic by talking about how amplifiers are classified. After that, we will look at three special kinds of amplifiers: multistage amplifiers, differential amplifiers, and power amplifiers.

8.2 Classification of Amplifiers

The classification of amplifiers does not follow a single set of rules, and different sources in the literature have adopted diverse taxonomies based on their specific objectives. In this chapter, we will examine various classifications that have been proposed, taking into account different considerations in the literature.

The classification of amplifiers can be based on several factors, including their operating conditions, circuit configurations, frequency ranges, and applications. By understanding these classifications, we can gain valuable insights into the characteristics and functionality of different types of amplifiers.

It is important to note that these classifications are not mutually exclusive, and an amplifier may fall into multiple categories depending on its design and specifications. The choice of classification depends on the specific context and the purpose for which the classification is being used.

In the subsequent sections of this chapter, we will delve deeper into each classification, exploring the characteristics, advantages, and applications of amplifiers within each category. This comprehensive examination will provide a broader understanding of the different types of amplifiers and their diverse uses in various fields of electronics and communication.

8.2.1 Based on the number of stages

In amplifier classification based on the number of stages, there are two categories: single-stage amplifiers and multi-stage amplifiers.

(a) **Single-stage Amplifier:** A single-stage amplifier consists of only one transistor and provides a single stage of signal amplification. The circuits discussed in the previous chapters are

OHZE DRAFT

are more efficient than class A amplifiers but introduce some crossover distortion.

(c) **Class C Amplifier:** A class C power amplifier operates for less than half a cycle, less than 180°, of the input AC signal. The output current flows for a fraction of the input signal cycle. Class C amplifiers are highly efficient but introduce significant distortion and are typically used in applications where fidelity is not critical, such as RF power amplification.

(d) **Class AB Amplifier:** A class AB power amplifier combines characteristics of class A and class B amplifiers. It operates over slightly more than half a cycle of the input AC signal. Class AB amplifiers provide improved efficiency compared to class A amplifiers while reducing crossover distortion.

It is worth noting that the realm of amplifier design does not stop at class AB. Within this category, other amplifier classes like Class D, Class E, Class F, and Class G emerge. Each of these classes introduces unique design principles and operating modes that suit particular applications. For instance, Class D amplifiers use pulse-width modulation to achieve high efficiency, making them ideal for audio applications. Class E amplifiers are commonly used in radio frequency circuits due to their high efficiency and low distortion. Class F and Class G amplifiers optimize efficiency further, often at the cost of increased complexity, making them suitable for specific high-power scenarios. In essence, the different amplifier classes within this category offer engineers a diverse toolbox to choose from, allowing them to tailor their amplifier designs to meet the specific requirements of a wide range of applications.

8.3 Multistage Amplifier

Two or more amplifiers can be connected to improve signal gain, frequency response, or for other special purposes. Figure 8.1 illustrates a multistage amplifier. The most common types of connections are the cascaded and cascode arrangements, where the output of one amplifier drives the input of the next. While discrete multi-stage amplifiers are not as common as they once were, understanding the operation of a discrete multi-stage amplifier helps gain insights into the interactions between circuits when they are connected together.

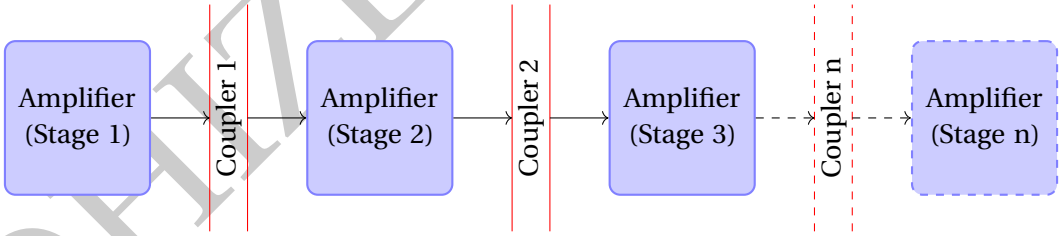


Figure 8.1: Multiple stage amplifiers

8.3.1 Cascade connection

Each amplifier (transistor) in a cascade arrangement is called a stage. The main purpose of a multi-stage arrangement is to increase the overall voltage gain. Ideally, the overall voltage gain of a cascaded amplifier with n stages is the product of the individual voltage gains, or it can be calculated as the sum of the decibel gains of the individual stages. Mathematically, this can be expressed as:

$$A_V = A_{V1} \times A_{V2} \times A_{V3} \ldots A_{Vn} \tag{8.1}$$

$$A_{V\ \mathrm{dB}} = 20\log_{10} A_{V1} + 20\log_{10} A_{V2} + 20\log_{10} A_{V3} + \cdots + 20\log_{10} A_{Vn} \tag{8.2}$$

OHIZE DRAFT 007

Common-Mode Rejection Ratio (CMRR)

The CMRR is the ratio of the differential voltage gain $A_{V_{DM}}$ to the the common-mode voltage gain $A_{V_{CM}}$ and it is given mathematically as

$$CMRR = \frac{A_{V_{DM}}}{A_{V_{CM}}} \tag{8.3}$$

In dB scale, the CMRR is

$$CMRR_{dB} = 20 \log \frac{A_{V_{DM}}}{A_{V_{CM}}} \tag{8.4}$$

For a good design, the CMRR should be high.

Input bias current

Input bias current refers to a DC parameter of the differential amplifier, which represents the average of the two base currents. It can be calculated by taking the sum of the base currents, I_{B_1} and I_{B_2}, and dividing it by two. Mathematically, it can be expressed as:

$$I_{in_{bias}} = \frac{I_{B_1} + I_{B_2}}{2} \tag{8.5}$$

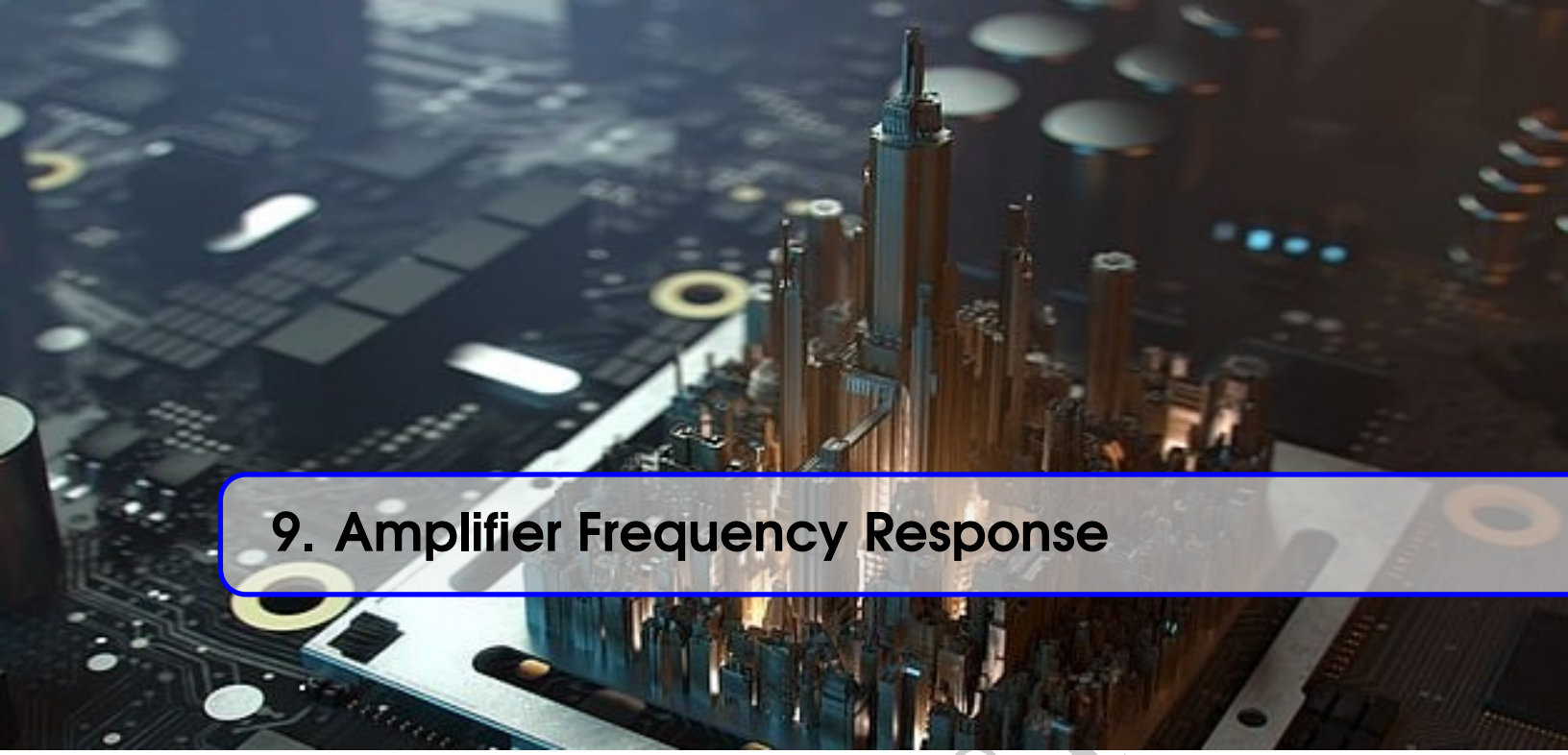
The input bias current is an important parameter to consider in the design and operation of the differential amplifier. It helps determine the operating point and the biasing requirements for the input stage of the amplifier.

Input offset voltage

Input offset voltage is a DC parameter that arises due to the mismatch in the electrical characteristics of the two transistors in a differential amplifier. This mismatch can result in a differential voltage even when the input is grounded, meaning there is a non-zero voltage difference between the two input terminals.

The input offset voltage can cause an undesired offset in the output signal of the differential amplifier, which can lead to errors in certain applications. It is important to minimize the input offset voltage to ensure accurate and precise operation of the amplifier.

To mitigate the effects of input offset voltage, techniques such as offset voltage compensation or trimming may be employed. These techniques aim to minimize or eliminate the differential voltage when the input is grounded, ensuring better overall performance of the differential amplifier.



9. Amplifier Frequency Response

9.1 Introduction

Up until now, we have focused on various aspects of amplifiers without considering the impact of signal frequencies. Some of you might have wondered why this topic has been overlooked. The reason is simple: we wanted to lay a foundation by emphasizing certain concepts first. In our previous discussions, we assumed that capacitive elements, such as coupling capacitors and bypass capacitors, acted as short circuits, while the internal transistor capacitors acted as open circuits. This assumption holds true within a specific frequency range called the amplifier's mid-range frequency. However, below and above this range, the capacitive reactances start to have an effect. In this chapter, we will explore the relationship between voltage gain, phase shift, and frequency. Understanding this concept is crucial for designing amplifiers that provide uniform amplification across all signal frequencies within the signal spectrum of interest, thus avoiding distortion.

9.2 Frequency Response Fundamentals

Before delving into the impact of signal frequency, let us discuss some fundamental concepts that will enhance our understanding of how frequency affects the performance of an amplifier. These concepts form the basis of our discussions in this chapter.

9.2.1 The Decibel

Decibel

The decibel (dB) is a unit used to express the ratio between the output and input of field quantities like voltage or power. It serves as an auxiliary unit and is dimensionless since it represents a ratio. However, when a fixed reference value is used, the decibel can also function as a pseudo unit or level, such as the decibel Watt (dBW). The decibel is commonly used to measure the gain of active devices like amplifiers or the loss in passive devices acting as attenuators, such as the length of a cable.

The decibel (dB) is a logarithmic unit used to measure gain, typically in voltage or power. It is one-tenth of the bel, which is the base unit. The bel represents the logarithm to the base 10 of

OHZE DRAFT

$$A_v(jf) = \frac{1}{1 - j\left(\frac{f_C}{f}\right)} \tag{9.15}$$

In Equation (9.15), $f_c = \dfrac{1}{2\pi RC}$, and the frequency f_c is known as the cutoff frequency. To express the complex function of Equation (9.15) in magnitude and phase, we have:

$$A_v(jf) = |A_v| \angle\phi = \frac{1}{\sqrt{1 + \left(\frac{f_c}{f}\right)^2}} \angle \tan^{-1}\left(\frac{f_c}{f}\right) \tag{9.16}$$

Equation (9.16) can also be expressed in decibels (dB) as:

$$G_{\text{VdB}} = 20\log_{10} | A_V | \tag{9.17}$$

$$G_{\text{VdB}} = -20\log_{10}\sqrt{1 + \left(\frac{f_c}{f}\right)^2} \tag{9.18}$$

$$G_{\text{VdB}} = -20\log_{10}\left[1 + \left(\frac{f_c}{f}\right)^2\right]^{1/2} \tag{9.19}$$

$$G_{\text{VdB}} = -20 \times \left(\frac{1}{2}\right)\log_{10}\left[1 + \left(\frac{f_c}{f}\right)^2\right] \tag{9.20}$$

$$G_{\text{VdB}} = -10\log_{10}\left[1 + \left(\frac{f_c}{f}\right)^2\right] \tag{9.21}$$

■ **Example 9.7** Given a lead network with a lower break frequency of 40 Hz, we want to determine the gain and phase values at 10 Hz.

Solution

First, let us set up the values:

$f_c = 40$ Hz, $\qquad\qquad$ $f = 10$ Hz.

Now, we can calculate the gain in decibels:

$$G_{\text{VdB}} = -10\log_{10}\left[1 + \left(\frac{f_c}{f}\right)^2\right]$$

$$G_{\text{VdB}} = -10\log_{10}\left[1 + \left(\frac{40 \text{ Hz}}{10 \text{ Hz}}\right)^2\right]$$

$$= -12.3 \text{ dB}$$

This means that at a frequency of 10 Hz, the gain is 12.3 dB lower than the mid-band gain.

Next, let us calculate the phase angle:

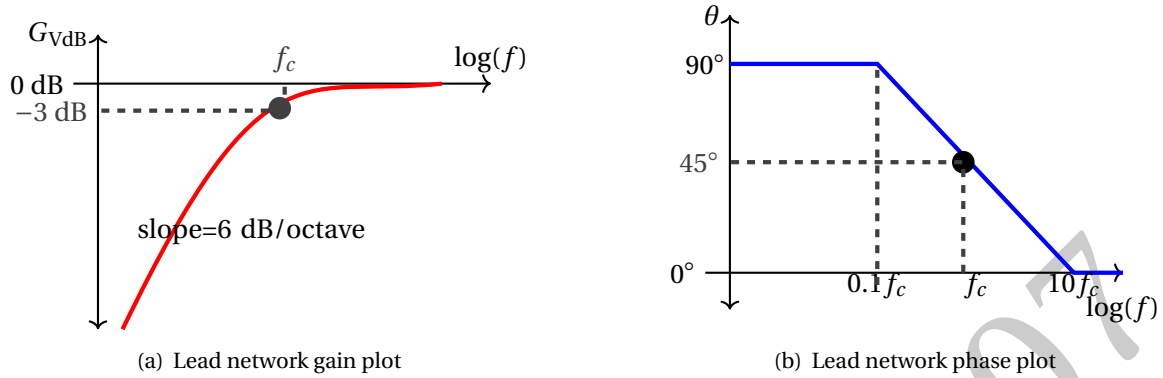
$$\phi = \tan^{-1}\frac{f_c}{f}$$

$$\phi = \tan^{-1}\frac{40 \text{ Hz}}{10 \text{ Hz}}$$

$$\phi = 75.96^\circ$$

In summary, at a frequency of 10 Hz, the gain is −12.3 dB and the phase angle is 75.96°. ■

OHIZE DRAFT007



(a) Lead network gain plot

(b) Lead network phase plot

Figure 9.4: Lead network frequency response

Figure 9.5 illustrates a typical Bode gain plot for an RC-coupled amplifier. The plot shows the normalized gain against frequency. The maximum gain occurs within the frequency range between the upper cutoff frequency (f_H) and the lower cutoff frequency (f_L), known as the mid-range. Any gain value below the mid-range or reference level of 0 dB is expressed as a negative dB value. The critical frequencies f_L and f_H are determined by the lead and lag networks formed by the amplifier, respectively.

Figure 9.5: A typical Gain versus Frequency or Bode gain plot

The Bode plot in Figure 9.5 has three frequency regions of interest:

1. The low-frequency region below the lower cutoff frequency f_L,
2. The mid-band region between the lower and upper cutoff frequencies, and
3. The high-frequency region above the upper cutoff frequency f_H.

In the low-frequency region, the drop in gain is primarily caused by the increase in reactance of the series capacitor in the lead or high-pass filter network (see Figure 9.2). This increasing reactance becomes significant at lower frequencies. In BJTs, the coupling or bypass capacitors C_B, C_C, and C_E contribute to the loss in gain. For FETs, the source coupling capacitor C_S is the main reactive element causing loss in gain. These coupling or bypass capacitors form a high-pass filter network.

In the mid-band region, where the frequencies are within the mid-range, there is no reduction

OHIZE DRAFT007

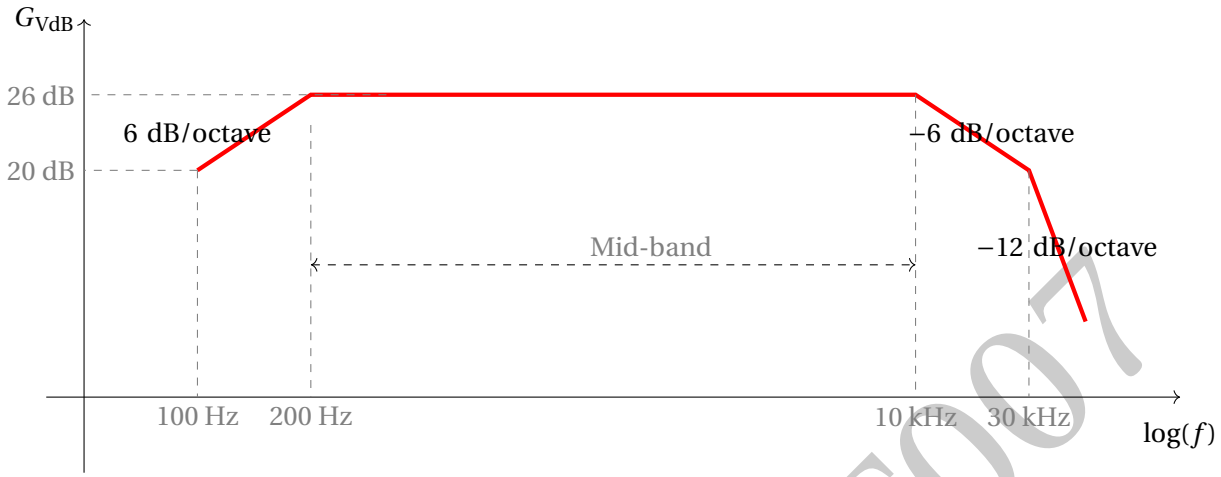


Figure 9.6: Bode magnitude sketch for Example 9.8

steps and considering the dominant networks, we can accurately sketch the Bode plot, which provides an approximate representation of the amplifier's frequency response. ■

9.3.3 Bandwidth

Bandwidth refers to the range of frequencies in which a circuit operates with linear signal amplification. It is defined as the range between the upper and lower cutoff frequencies on the frequency response curve (Figure 9.5). The bandwidth represents the desired range for minimal signal attenuation and is often referred to as the mid-band range for a typical band-pass filter. Mathematically, the bandwidth is calculated as:

$$BW = f_H - f_L \tag{9.25}$$

For a DC coupled amplifier without a lead network, the lower cutoff frequency (F_L) is 0 Hz. In this case, the bandwidth simplifies to:

$$BW = f_H \tag{9.26}$$

In summary, the bandwidth represents the frequency range over which the circuit operates linearly and is determined by the difference between the upper and lower cutoff frequencies.

9.4 Frequency Response of BJT and FET Amplifiers

Up until now, our focus has been on understanding the relationship between frequency of operation and amplifier's gain. We will now specifically delve into the frequency response analysis of BJT and FET networks.

9.4.1 Frequency Response of BJT Amplifier

In Figure 9.7, you can see a common-emitter amplifier that is capacitively coupled. We will use this voltage-divider bias network setup to explain our frequency analysis. As mentioned before, all the network capacitors—C_1, C_2, C_3, and C_L—play a role in setting up the critical frequency. Additionally,

OHIZE DRAFT007

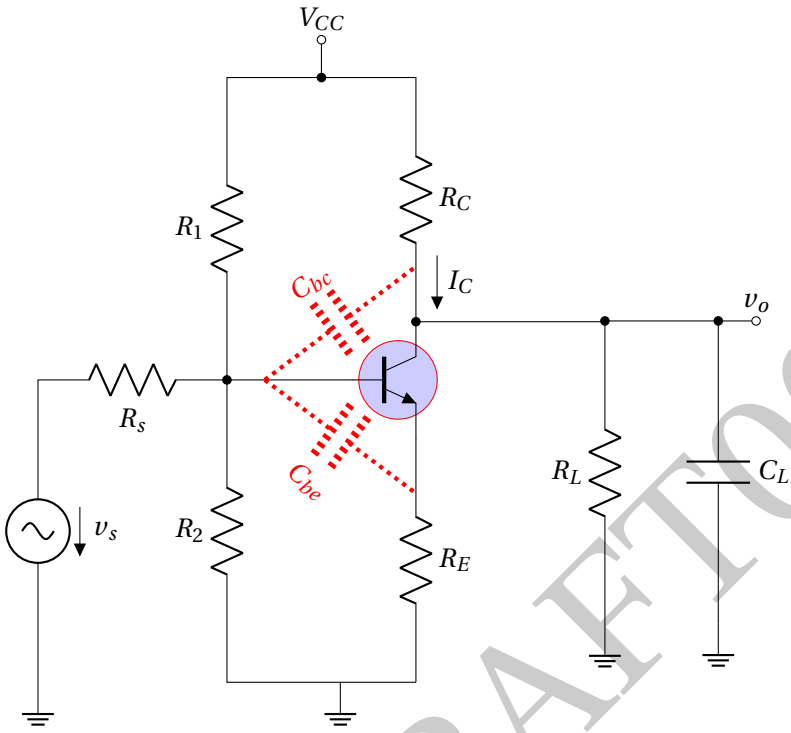


Figure 9.9: High frequency equivalent circuit for CE amplifier

9.4.1.3 Miller's Theorem

Miller's theorem is a valuable tool for analyzing amplifiers that incorporate a feedback element. It simplifies the high-frequency response analysis by allowing us to divide the effective impedance of the feedback element between the input and output terminals.

Miller's Theorem

Miller's theorem states that if an impedance is connected between the input and output nodes of an amplifier, with a reference node present, then this impedance can be replaced by two separate impedances. One impedance is connected between the input and the reference node, while the other impedance is connected between the output and the reference node.

Miller's theorem provides a useful technique for breaking down complex amplifier circuits and simplifying their analysis by redistributing the impedance of the feedback element. Figure 9.10 serves as an illustration of Miller's theorem. In this setup, the feedback capacitor C_f (Figure 9.10(a)) affects both the input and output terminals of the amplifier. Consequently, we can determine the corresponding effective values known as the Miller input capacitor $C_{\text{in}_{\text{Miller}}}$ and the Miller output capacitor $C_{\text{out}_{\text{Miller}}}$, both attributed to C_f. These Miller capacitors can be calculated using the following formulas:

$$C_{\text{in}_{\text{Miller}}} = C_f\,(|\,A_v\,|+1) \tag{9.36}$$

$$C_{\text{out}_{\text{Miller}}} = C_f\left(\frac{|\,A_v\,|+1}{|\,A_v\,|}\right) \tag{9.37}$$

ONLINE DRAFT007

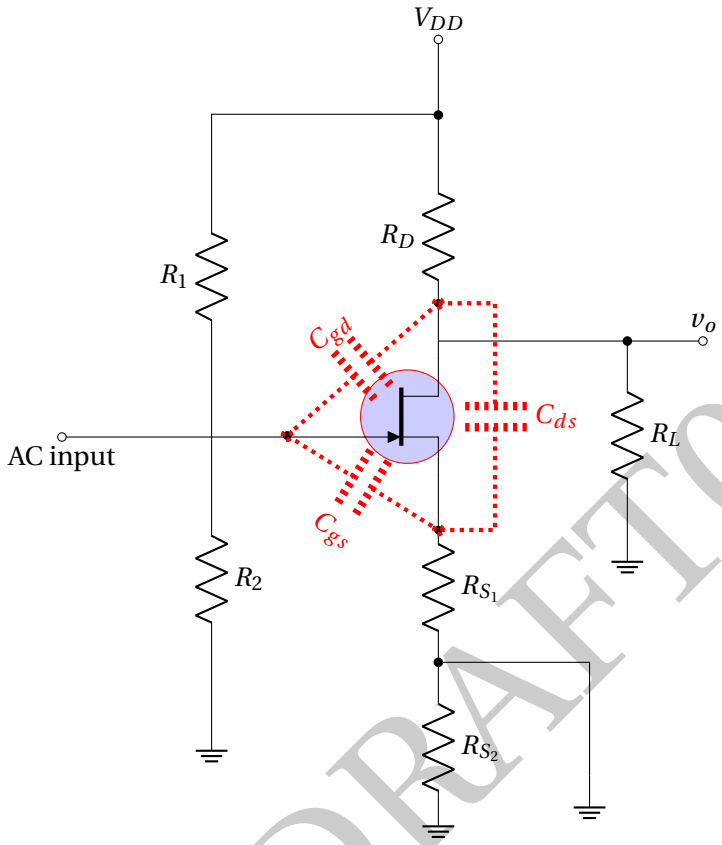


Figure 9.17: High frequency equivalent circuit for CS

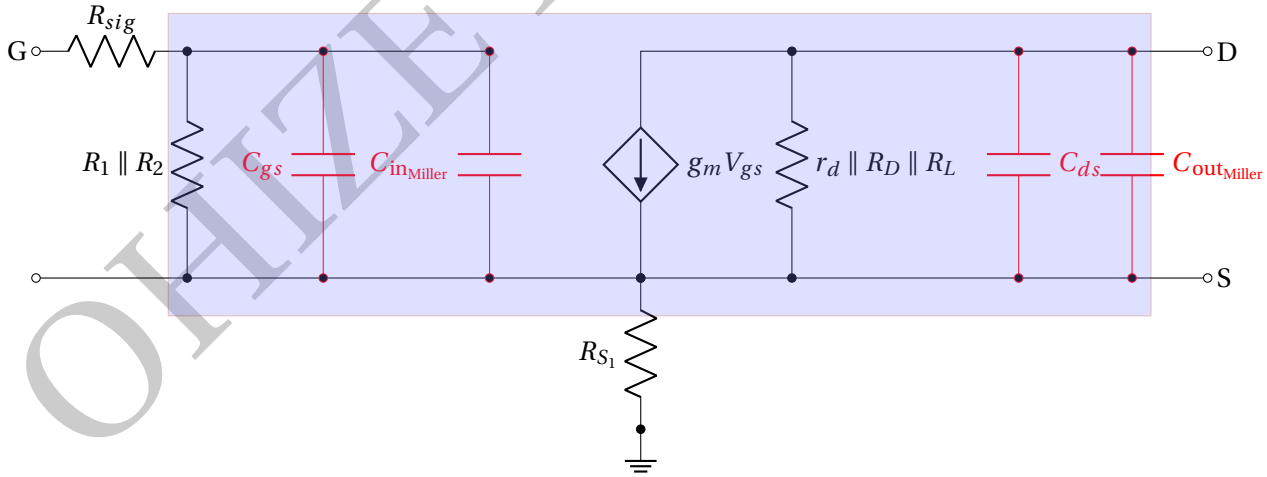


Figure 9.18: High frequency model of FET

at the input terminal, denoted as $C_{\text{in}_{\text{Miller}}}$, and the other seen at the output terminal, denoted as $C_{\text{out}_{\text{Miller}}}$. At high frequencies, the FET AC equivalent circuit is depicted in Figure 9.18.

Upon examining the manufacturer's data sheets, you may not find the specific labels C_{gs}, C_{gd}, and C_{ds} for the device capacitors. Instead, the data sheets provide values for the equivalent input

OHIZE DRAFT007

10. Simulation Part II

10.1 Introduction

This Chapter is to test the students' understanding of the concept delivered in part II of this text. Here we shall demonstrate the concepts covered in Chapter 5 through Chapter 9 by way of design and simulation Task. At this point we expect that the students have a basic level understanding of LTSpice and MATLAB while opened to learn more on the simulators when performing the Task. It is encouraged that the student revise MATLAB and LTSpice tutorial in Chapter 4.

10.2 Plotting BJT Characteristic Curves using EM's Model

Task 1

Use the Ebers-Moll equations and subsidiary relationships described in Chapter 5 (Section 5.4), construct a MATLAB program that calculates and plots the input and output characteristics of a pnp BJT operated in both the common-base and the common-emitter configurations. Students must submit the codes along with a report on the equation derivations and a tabulation of the simulation parameters or values.

10.3 Determining the Q-point of FET

Coding Example

Here is a MATLAB code that determines the Q-point for the voltage-divider network of Example **??**. It is a graphical solution that involves plotting the load line on the transfer curve and finding their intersection.

```
clc; clear all; close all; % Clear workspace and command window
% FET Q-Point Calculation (Graphical Method with Voltage-Divider Network)

% Define FET parameters
Vdd = 12;          % Supply voltage (V)
Idss = 10e-3;       % Drain current at Vgs = 0 (A)
Vp = -6;           % Pinch-off voltage (V)
```

OHTZE DRAFT

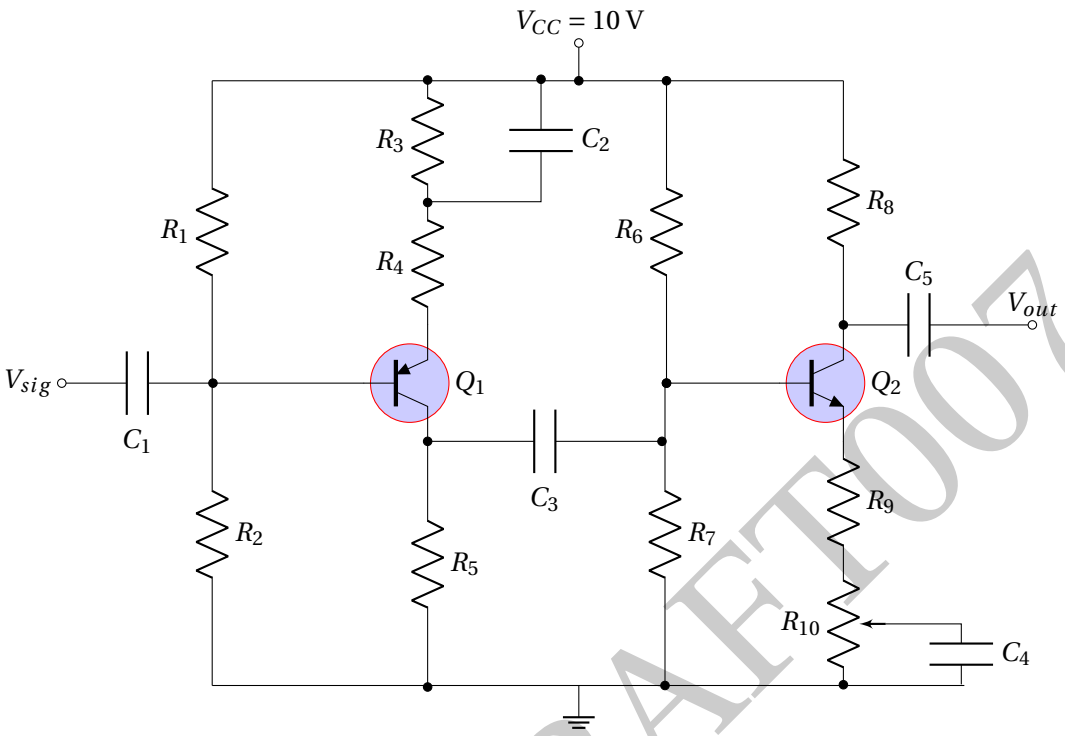


Figure 10.7: Audio pre-amplifier for Task 10

guesses about resistor values.

Stage Q_1 design

(a) For the Q_1 stage, follow a similar process as with Q_2 outlined above, but with a few changes to determine the values of resistors and capacitors specific to this stage.
(b) Simulate this stage to verify that you have chosen reasonable values.
(c) Once you have completed the design and simulation, submit your results. Your efforts in making intelligent guesses and achieving the desired circuit performance will be duly acknowledged and rewarded by the assigned tutor.

10.8 FET Amplifier Design

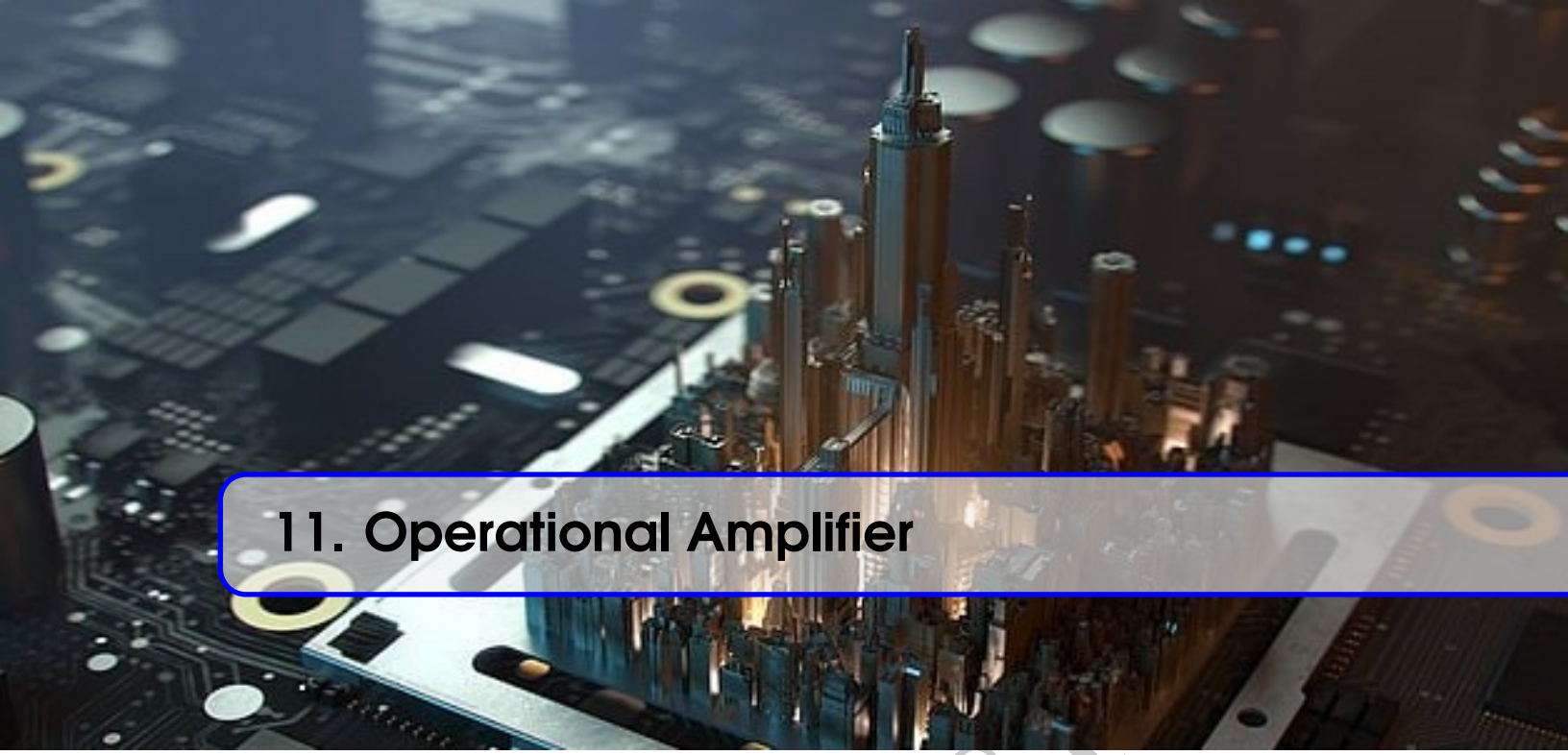
Task 11

You will connect the circuit shown in Figure 10.8 to enhance your understanding of the DC operating point or Q-point of a FET. The specific transistor to be used in this circuit is the IRF150.

(a) You will perform a DC sweep analysis for the circuit. Unlike the nested SWEEP used for the BJT in Task 3, this time you will plot only one graph. The simulation will vary the values of V_{GG} while keeping V_{DD} fixed.
(b) I will leave the selection of the range for V_{GG} to you. To set up the simulation, click on the "Simulate" tab, select "Edit Simulation," and choose "DC Sweep." Then, click on the "1st source" tab and enter the start, stop, and increment values for V_{GG}. Make sure to select the sweep type as linear.
(c) Click the "Run" button on the simulation tab and ensure that the trace value is set to I_D.

OHZE DRAFT007

Part Three



11. Operational Amplifier

11.1 Introduction

We have now reached a point where we can delve into the exploration of a versatile electronic component known as the Operational Amplifier, or Op-Amp for short. In Part II of this text, we covered the fundamental concepts and terminology of amplifiers. In this chapter, our focus will be on this essential circuit component that holds universal importance in electronics: the Operational Amplifier.

Operational Amplifier

An Operational Amplifier is a two-input directly coupled multistage differential amplifier with high voltage gain and high input impedance designed to perform mathematical operations.

The Operational Amplifier, or Op-Amp, has been widely used for many decades. It serves as a fundamental building block in electronic circuits, encompassing the differential amplifier, voltage amplifier, and, in certain cases, the class B push-pull amplifier at the output stage. While Figure 11.1 depicts the basic internal arrangement of an Op-Amp, an in-depth discussion of its internal circuit elements falls outside the scope of this book. Instead, we will treat the Op-Amp as a black box and present models that accurately represent its behavior within an electrical circuit in the following section.

In Chapter 8, we discussed the differential amplifier and its various input/output configurations. It is important to note that the Op-Amp is essentially a differential amplifier, employing a differential input and a single-ended output. The circuit symbol representing the Op-Amp and its corresponding pins are shown in Figure 11.2. Pin 1 and pin 2 serve as the two input terminals. Pin 1 is the inverting input, indicated by a negative sign, while pin 2 is the non-inverting input, denoted by a positive sign. Pin 3 represents the output terminal, referenced to ground. Pins 4 and 5 are the DC power supply pins. Typically, pin 4 is connected to the positive voltage V_{CC}, while pin 5 is connected to the negative voltage V_{EE}. It is worth noting that practical Op-Amps may have additional pins for specific purposes, such as terminals for frequency compensation and offset nulling.

OHZ DRAFT

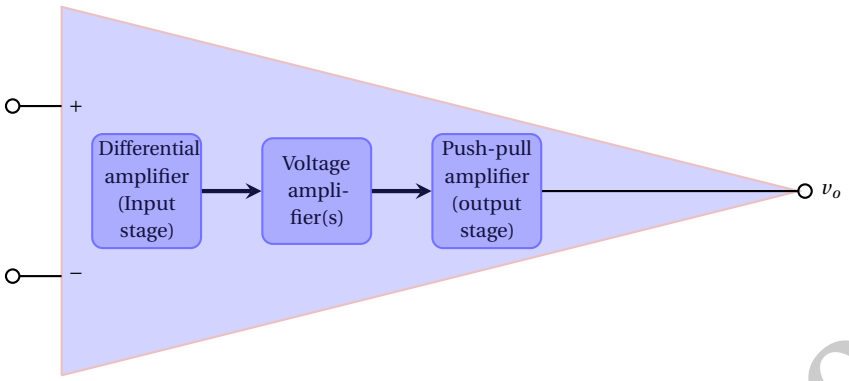


Figure 11.1: Basic building block of the Op-Amp

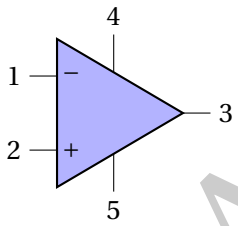


Figure 11.2: Circuit symbol of the Op-Amp

11.2 Modeling an Op-Amp

In engineering applications, we model systems based on our understanding of their behavioral characteristics and expected functions. As we defined earlier, an Op-Amp can be considered as a differential amplifier with a single-ended output. This means that the output is equal to the difference between the two inputs, v_1 and v_2, multiplied by a gain factor A_V. This relationship is illustrated by the functional block diagram shown in Figure 11.3.

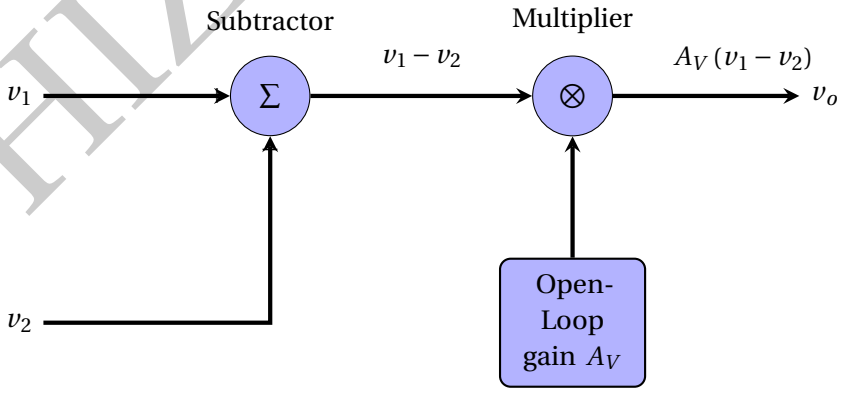


Figure 11.3: Functional block diagram of an Op-Amp

In a more rigorous mathematical sense, the relationship can be expressed as:

$$v_o = A_V(v_1 - v_2) \tag{11.1}$$

OHIZE DRAFT007

resulting in a reduced distortion range. The reduction in gain is known as the "sacrifice factor," which is the difference between the closed-loop gain and the open-loop gain.

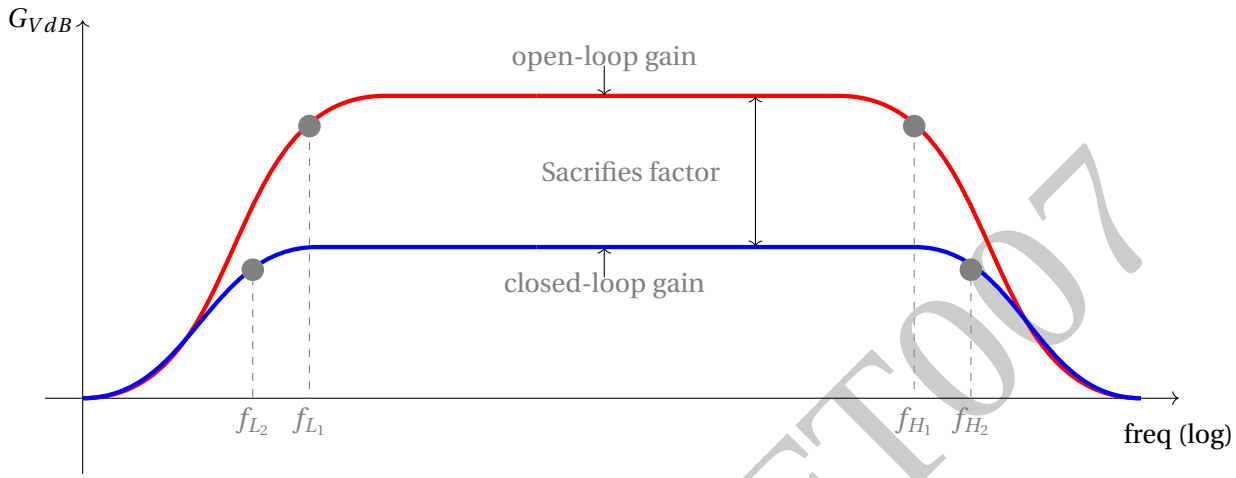
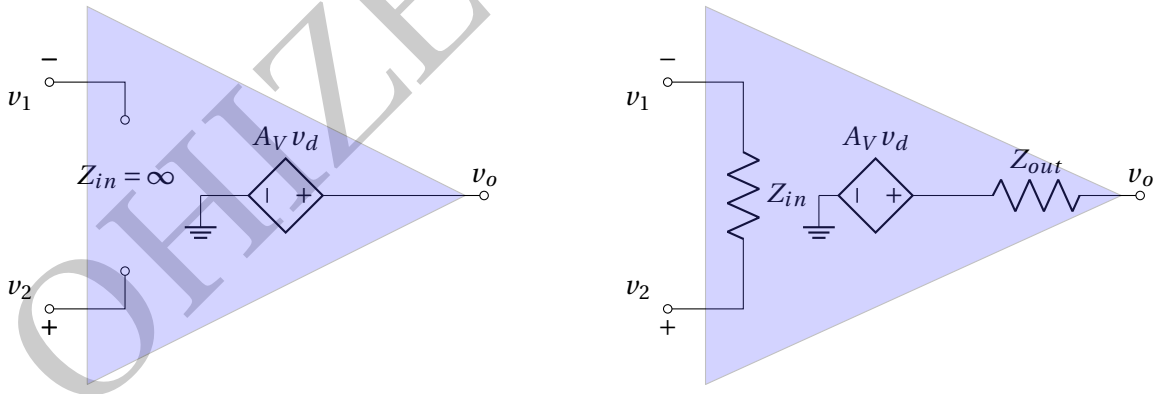


Figure 11.9: Gain Vs frequency response with and without feedback

11.6 Ideal Op-Amp Characteristics

The Op-Amp representation is shown in Figure 11.10. In Figure 11.10(a), we have the ideal Op-Amp, and in Figure 11.10(b), we have the practical Op-Amp for comparison. Understanding the ideal Op-Amp is crucial for our circuit analysis. By assuming an ideal Op-Amp, we can simplify the analysis process and obtain results that are close to those of a practical Op-Amp, without the need for complex mathematical calculations.



(a) Ideal Op-Amp

(b) Practical Op-Amp

Figure 11.10: Basic Op-Amp representation

We can summarize the key points about the practical Op-Amp based on our discussion so far:

(i) The Op-Amp circuit with feedback operates by maintaining a small differential voltage v_d (that is, $v_2 - v_1$) at its inputs to control the Op-Amp's large internal/open-loop gain.

(ii) The Op-Amp with feedback regulates its own differential voltage by adjusting its output voltage v_o, whose fraction is fed back to the input through the feedback loop.

OHIZE DRAFT007

12. Oscillators

12.1 Introduction

In this chapter, we will explore the fascinating world of oscillators. Oscillators are essential electronic devices widely used in various applications, including ultrasonic and radio frequency systems. They play a crucial role in generating different types of signals, such as sine waves, square waves, sawtooth waves, and triangular waves, which are vital in communication systems, control systems, computers, and more. But what exactly is an oscillator in the context of electronics?

Oscillator

An oscillator is a circuit that generates a repetitive, alternating signal waveform without any applied input signal. It achieves this by converting the direct current (DC) flow from a DC source into an alternating waveform of a specific frequency determined by the oscillator's circuit components.

Oscillators find widespread use in various applications, including quartz watches, audio systems, video systems (such as in radio and television), and other communication devices. They are also employed in computers to generate clock pulses for microprocessors and microcontrollers. Additionally, oscillators play a role in alarms, buzzers, metal detectors, stun guns, inverters, and more.

Throughout this chapter, we will introduce the principles of oscillator operation, explore feedback arrangements that sustain oscillation, and examine different practical oscillator circuits. A typical oscillator consists of an oscillatory unit and an amplifier with a feedback arrangement. While we have already discussed amplifiers, we will now delve into oscillatory circuits to further expand our understanding.

12.2 Oscillatory Circuit

A circuit that can generate electrical oscillations of a desired frequency is known as an oscillatory circuit. There are different types of oscillatory circuits, but two common ones are the LC oscillator and the crystal oscillator. Let us take a closer look at these circuits.

If this crystal is used in an oscillator, the frequency of oscillations will lie between 796 kHz and 797 kHz. ∎

In conclusion, it is important to understand that the oscillatory circuits discussed so far are not capable of sustaining oscillation on their own. In other words, while we defined an oscillator as a continuous and repetitive signal generator without an external input, the circuits we discussed require external energy to keep the cycle of charging and discharging the inductor and capacitor going. Energy is lost through the circuit wiring and electromagnetic radiation, resulting in a damping effect on the generated signal.

To achieve a constant amplitude or undamped oscillation, we need to introduce the concept of sustained oscillation and a frequency-selective feedback network. This theory explains how to maintain oscillation over time and control the frequency of the generated signal.

12.3 Theory of Oscillation

Oscillators consist of two main parts: an amplifier with an open-loop gain A_v and a frequency-selective positive feedback network, as shown in Figure 12.3. In an actual oscillator circuit, no input signal is present, but an input signal v_i is used here to explain the principle of operation. Unlike the negative feedback loop discussed in Chapter 11, the feedback signal βv_o is summed with a positive sign, known as positive feedback.

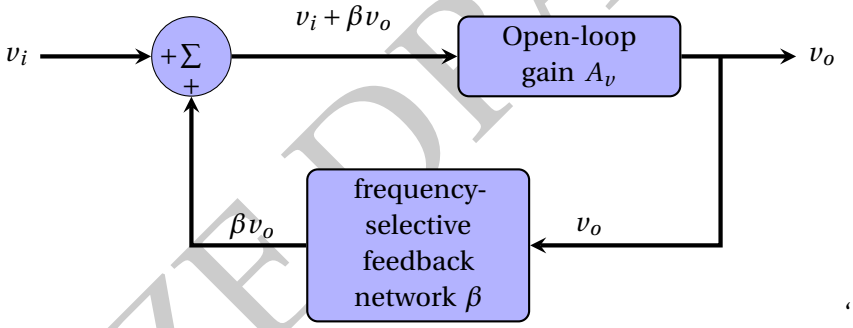


Figure 12.3: Feedback system in oscillator

The closed-loop phasor gain, obtained from Figure 12.3, is given by

$$A_{v_C}(s) = \frac{A_v(s)}{1 - A_v(s)\beta(s)} \tag{12.7}$$

The closed-loop gain represents the ratio of output to input. When the denominator of Equation (12.7) is zero, the closed-loop gain becomes infinity, even without any input. In other words, when $A(s)\beta(s) = 1$, the closed-loop gain is infinite. By replacing s with its frequency domain representation, we can rewrite Equation (12.7) as

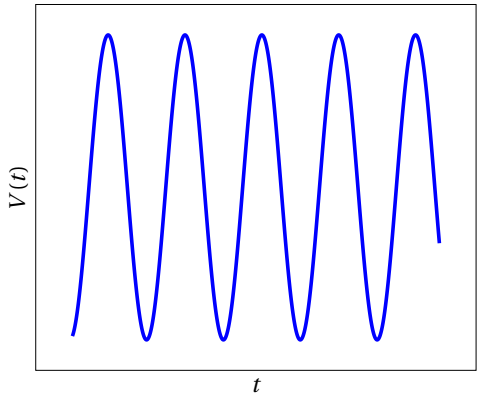
$$A_{v_C}(j\omega) = \frac{A_v(j\omega)}{1 - A_v(j\omega)\beta(j\omega)} \tag{12.8}$$

The condition for infinite gain is again expressed as

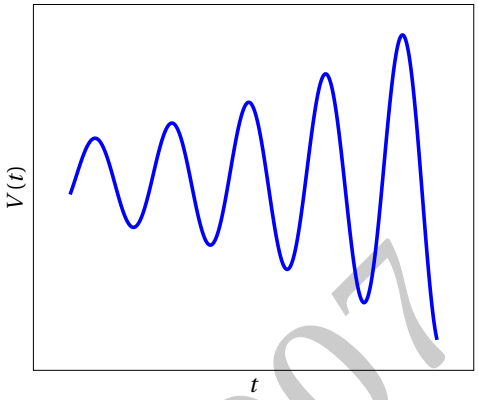
$$1 - A_v(j\omega)\beta(j\omega) = 0 \tag{12.9}$$

$$\therefore A_v(j\omega)\beta(j\omega) = 1 \tag{12.10}$$

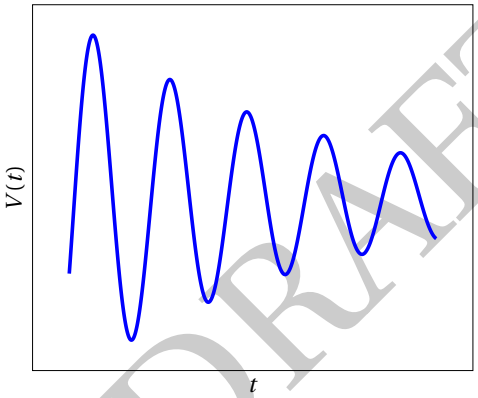
QHIZE DRAFT007



(a) Feedback loop gain $A_v(s)\beta = 1$



(b) Feedback loop gain $A_v(s)\beta > 1$



(c) Feedback loop gain $A_v(s)\beta < 1$

Figure 12.4: Effect of feedback loop gain

12.5 Sinusoidal oscillators

The basic structure of sinusoidal oscillators, also known as harmonic oscillators, consists of an amplifier (such as Op-Amps, BJTs, or FETs) connected in a positive feedback loop arrangement with a frequency-selective network. These oscillators generate sinusoidal waveforms. In the following subsections, we will discuss the following examples of sinusoidal oscillators:

(a) Wien bridge oscillator
(b) Phase-shift oscillator
(c) Twin-T oscillator
(d) Colpitts oscillator
(e) Hartley oscillator
(f) Armstrong oscillator
(g) Tuned oscillator

Each of these oscillators has its unique implementations and applications, and we will explore them in detail.

OHIZE DRAFT007

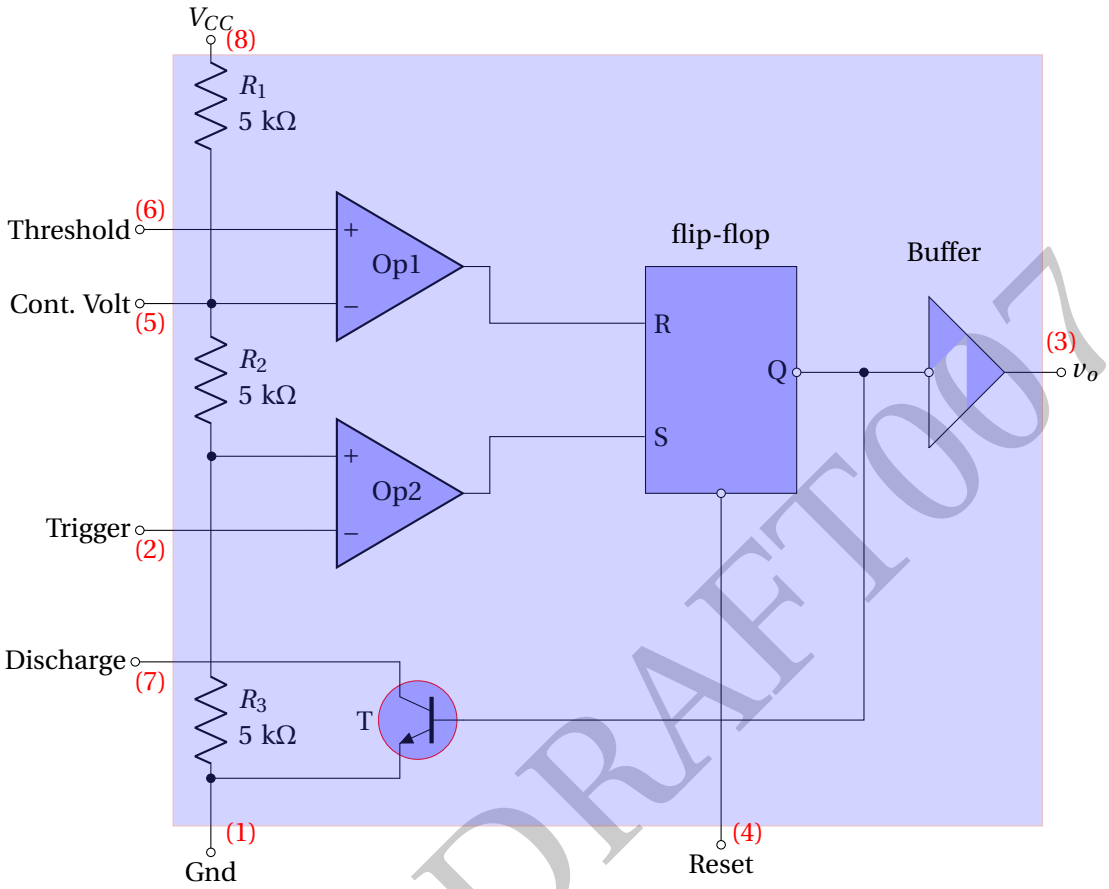


Figure 12.20: 555 timer showing internal circuitry

timing circuit.

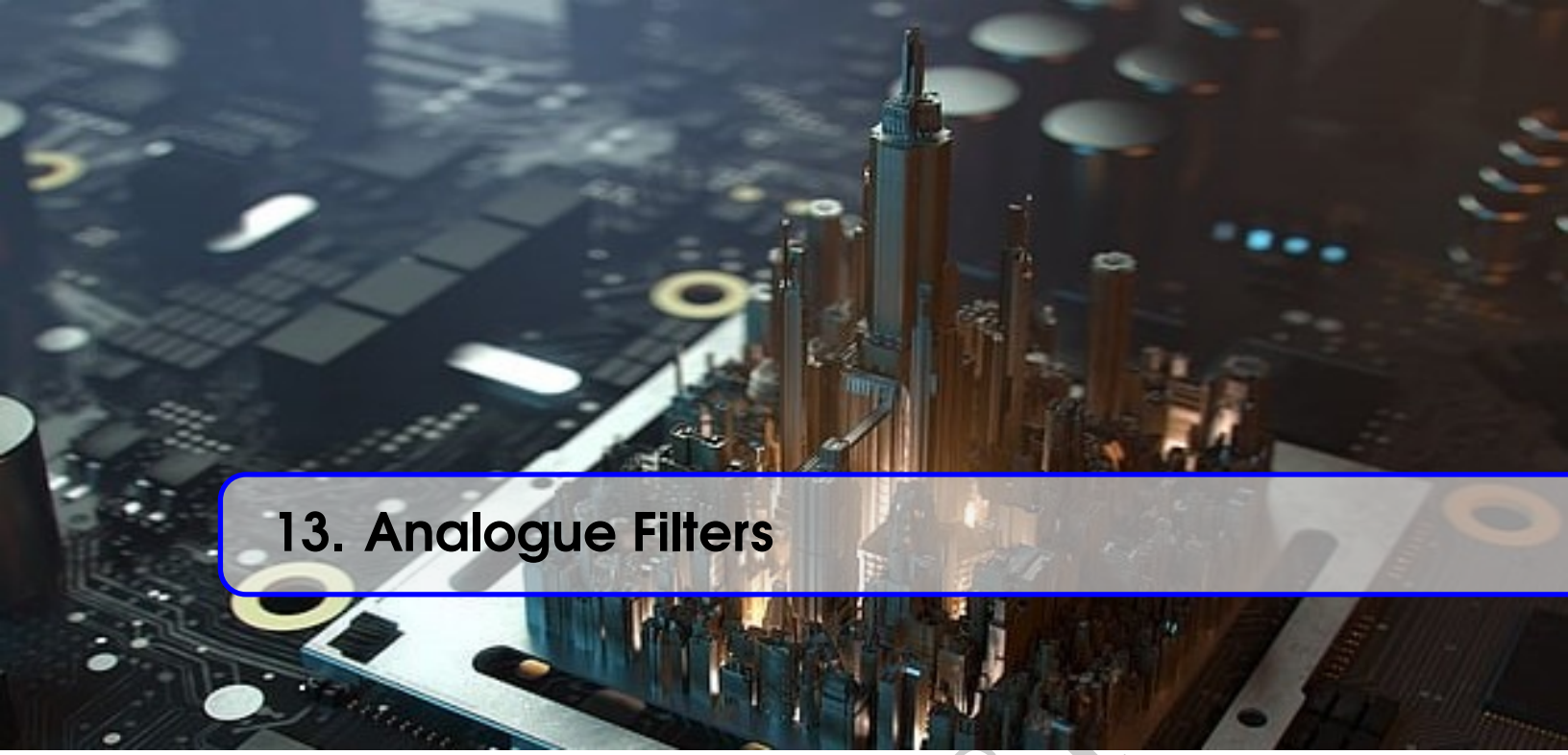
12.7.2 Astable Multivibrator using 555 timer

One of the versatile applications of the 555 timer is the free-running astable multivibrator. Although it can also be configured to function in the bistable or monostable mode, we shall only discuss the circuit connection for astable mode as shown in Figure 12.21. The external components R_1, R_2 and C_1 form the timing circuit as well as the frequency-determining components. The capacitor, C_2 is a decoupling capacitor. The Threshold pin 6 and the Trigger pin 2 are connected in the astable mode as shown in Figure 12.21.

In the astable mode, the Threshold pin 6 and Trigger pin 2 are connected as depicted in Figure 12.21. The principle of operation involves the charging and discharging of the external timing capacitor C_1. When the circuit is powered, the capacitor begins to charge through resistors R_1 and R_2. The charging process is shown by the green dotted line. The Trigger pin 2 affects the two internal Op-Amps because the Threshold pin and Trigger pin are connected together. Figure 12.20 indicates that the Threshold pin is linked to the non-inverting terminal of Op-Amp Op1, while the Trigger pin is connected to the inverting terminal of Op-Amp Op2.

When the voltage across capacitor C_1 (connected to trigger pin 2, see Figure 12.21) is less than the reference voltage $^1/_3V_{CC}$, the internal Comparator Op2 goes high while Op1 remains low. This

QHIZE DRAFT007



13. Analogue Filters

13.1 Introduction

In this chapter, we will discuss the concept of analogue filters. Filters are essential components in electronics used in communication systems, instrumentation systems, and various other applications.

The focus of this chapter is to introduce you to the design of analogue filters. This field of engineering has a complete design theory with numerous texts dedicated to filter theories. analogue filter design covers a wide range of topics, from specifications to the actual implementation of working circuits. While we won't delve deeply into the underlying mathematics, such as Laplace transforms, poles and zeros, and transfer functions, we will mention them. They are useful for describing filter effects and examining design stability.

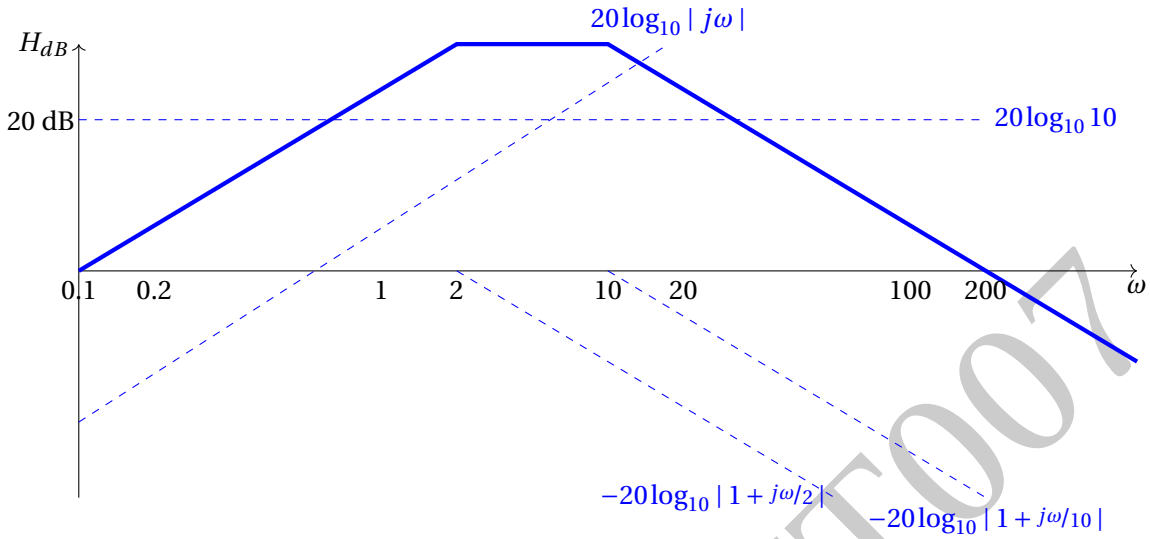
The main goal of this chapter is to provide you with a basic understanding of the filter design process and the ability to analyze existing analogue filter designs. It is important to note that despite the increasing use of digital signal processing, analogue filters are still necessary. This is because most systems need to interface with the analogue world. At a minimum, this interface requires an amplifier and an analogue filter.

Filters

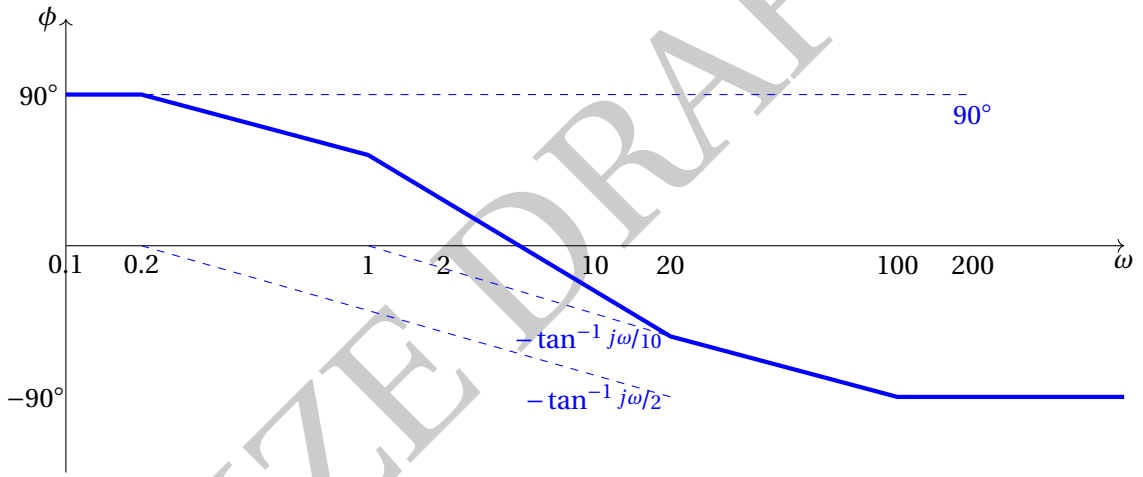
Filters are networks that process signals in a frequency-dependent manner. They consist of frequency-selective elements such as inductors, capacitors, resistors and sometimes, amplifier circuits.

The basic concept of a filter can be understood by examining the frequency-dependent nature of capacitors' and inductors' impedance. Consider a voltage divider network with a reactive element. As the frequency changes, the reactive impedance value changes, affecting the voltage divider ratio. This leads to a frequency-dependent change in the input/output transfer function, known as the frequency response.

FREEDRAFT



(a) Magnitude Bode plot



(b) Phase Bode plot

Figure 13.9: Bode plot for Example 13.3

Express the relationship in standard terms by multiplying both numerator and denominator terms by $1/4$ and $1/100$ (note the square term in the pole term $(j\omega+10)$) to obtain

$$H(j\omega) = \frac{0.125\,j\omega}{(1+j\omega/4)\,(1+j\omega/10)^2}$$

$$H(j\omega) = \frac{j\omega}{8\,(1+j\omega/4)\,(1+j\omega/10)^2}$$

we now have four terms for our straight line approximation plot: a denominator gain constant, a zero at the origin, one simple pole and another simple pole of order 2. Expressed in magnitude as

$$H_{dB} = 20\log_{10}|j\omega| - 20\log_{10}8 - 20\log_{10}|1+j\omega/4| - 40\log_{10}|1+j\omega/10|$$

OHIZE DRAFT007

and expressed in phase as

$$\phi = 90^\circ - 0^\circ - \tan^{-1} j\omega/2 - 2 \times \tan^{-1} j\omega/10$$

■

Exercise 13.1 Complete Example 13.4 by sketching the Bode plots using the approximation approach discussed thus far. ■

13.3 Filter Specifications

In this section, we will discuss the characteristics and important parameters of filters. First, let us review the concept of an ideal filter. An ideal filter has a frequency response that is unity (or at a fixed gain) within a specific range of frequencies called the pass-band, and it attenuates or rejects all other frequencies in a region called the stop-band. The frequency at which the response transitions from the pass-band to the stop-band, or vice versa, is known as the cutoff frequency (ω_c).

In some cases, filters may have additional cutoff frequencies, such as the lower cutoff frequency (ω_L) or the higher cutoff frequency (ω_H) for band-pass or notch filters. These specifications define the frequency range of interest for the filter. Figure 13.10 illustrates the idealized filter responses for different filter types, that is, low-pass, high-pass, band-pass, and band-stop filters. We will discuss each of these filter types in detail in the following sections.

However, in real-world filters, the frequency response is not as ideal as depicted in Figure 13.10. Figure 13.11 shows a typical response for a high-pass filter, which demonstrates that the transition between the pass-band and the stop-band is not instantaneous. The response curve exhibits certain characteristics that can be specified using key parameters. Figure 13.11 also highlights these parameters for the amplitude response of the filter.

Before selecting a filter, it is essential to understand how filters are specified.

Cutoff frequency

The cutoff frequency (ω_c) is the frequency at which the filter response transitions from the pass-band to the stop-band in a low-pass filter or from the stop-band to the pass-band in a high-pass filter (see Figure 13.11). It is also referred to as the corner frequency. The cutoff frequency is important for specifying the range where the pass-band ends in a low-pass filter or starts in a high-pass filter. It is also the frequency at which the output signal power is half the power of the input signal, resulting in a 3 dB drop in gain. This 3 dB drop represents a one-half power ratio decrease (equivalent to $10\log(0.5)$ dB), hence it is used as the reference for defining the cutoff frequency.

Stop-band

The stop-band, also known as the reject band, is the range of frequencies where a filter attenuates the signals above a specified level (see Figure 13.11). In an ideal filter, the magnitude of the signal is zero within the stop-band.

ZED DRAFT 00

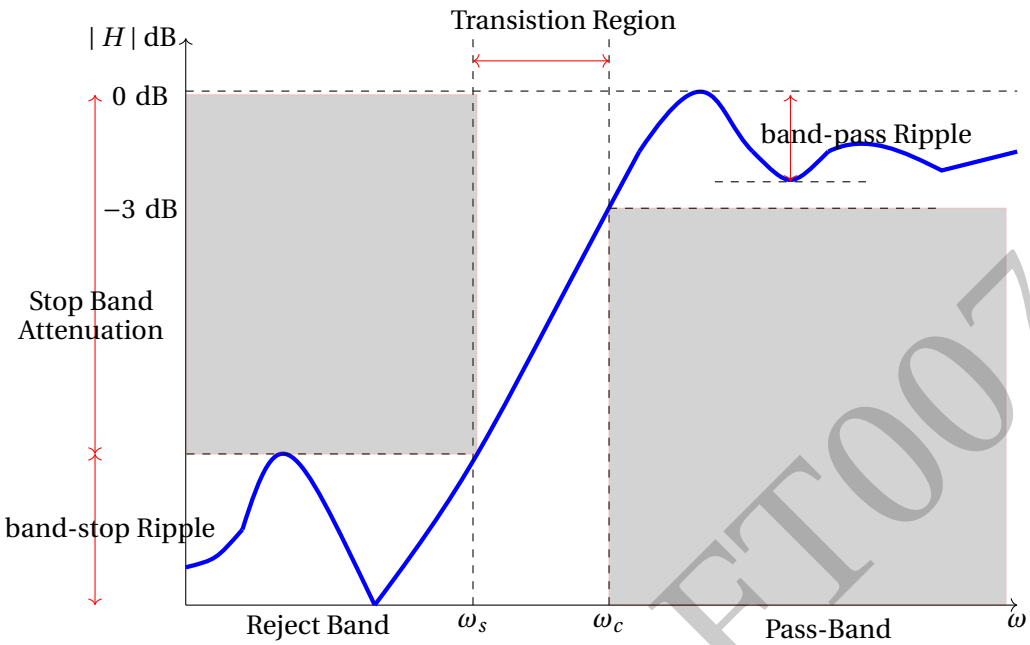


Figure 13.11: Typical high-pass filter response

OHM DRAFT007

Steepness of filter

The steepness of a filter determines the extent of the transition region between the pass-band and the stop-band. It is related to the realistic response of the filter. Steepness is characterized by the slope of the transition region, as shown in Figure 13.11. It can also be defined as the ratio of the stop-band frequency (ω_s) to the cutoff frequency (ω_c). Steepness, also known as selectivity factor, is determined by the filter order or the number of poles in the transfer function.

Bandwidth

The bandwidth represents the range of frequencies that a filter allows to pass. In cases where a filter acts as both a high-pass and a low-pass filter, passing or rejecting only a specific range of frequencies, two cutoff frequencies are defined. The higher frequency is denoted as ω_H, and the lower frequency is denoted as ω_L. The bandwidth is then calculated as the difference between these two frequencies:

$$BW = \omega_H - \omega_L \tag{13.19}$$

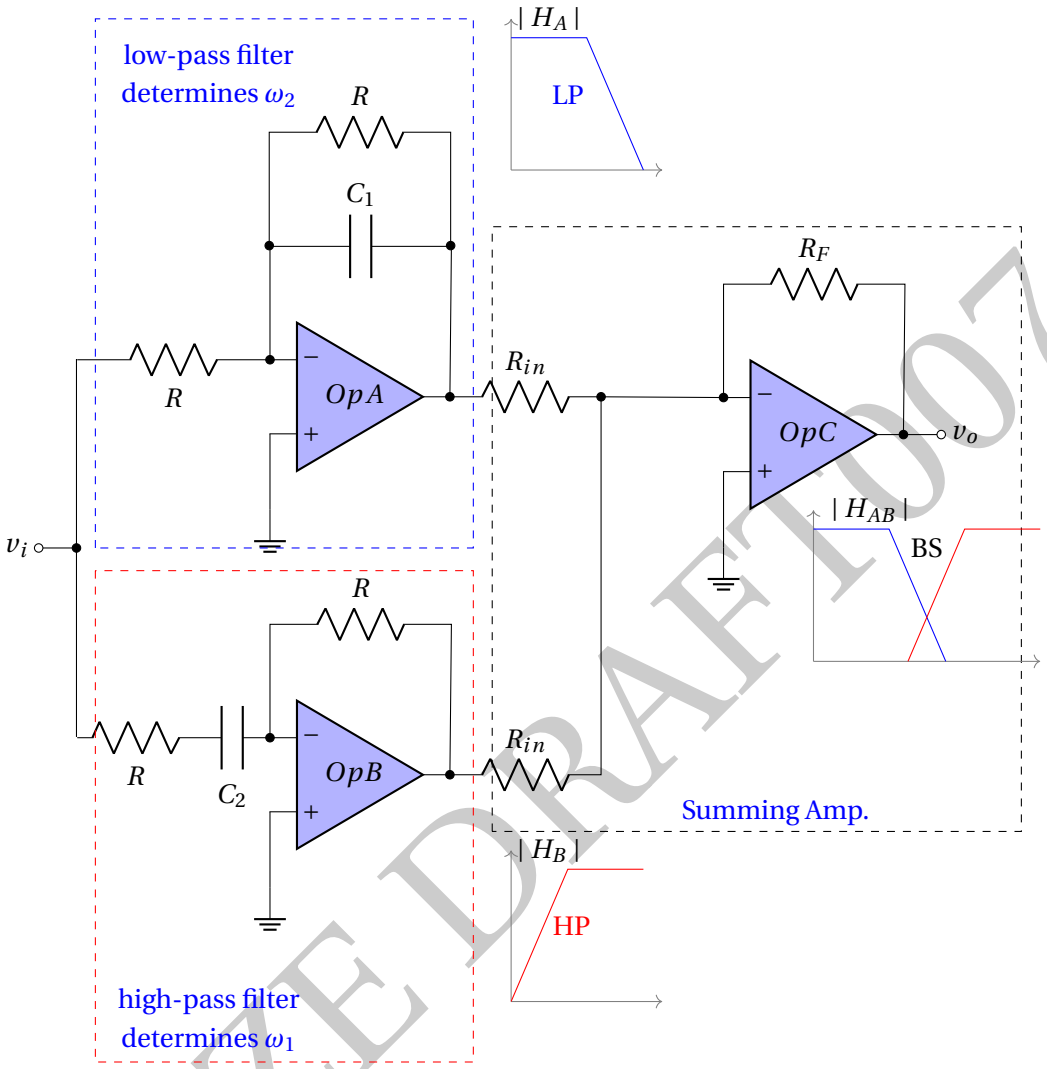


Figure 13.34: First-order active band-stop filter

OHIZE DRAFT 007

■ **Example 13.9** Design a low-pass filter with a DC gain of 5 and a corner frequency of 1 kHz.

Solution

A low-pass filter with a gain requires the use of an active filter design. Consequently, we use the circuit of an active low-pass filter as shown in Figure 13.31. It is an inverting amplifier whose gain at the low-pass region is defined as

$$H(0) = -\frac{R_F}{R_{in}} = 5.$$

The cut-off frequency for the active filter is determined by the feedback capacitor and resistor, given as

$$\begin{aligned}\omega_c &= 2\pi f_c \\ &= 2\pi \times 1000 = \frac{1}{R_F C_F}.\end{aligned}$$

14. Simulation Part III

14.1 Introduction

In this chapter, we will conclude by applying the concepts learned from Chapter 11 to Chapter 13. The purpose of this chapter is to assess the students' understanding of the material covered in Part III of the text. We will demonstrate these concepts through design and simulation tasks. At this point, it is expected that students have a basic understanding of LTSpice and MATLAB, and they should be open to learning more about these simulators as they perform the tasks. We encourage students to refer to the MATLAB and LTSpice tutorials provided in Chapter 4 for further guidance.

14.2 Basic Operation of Op-Amp Circuit

14.2.1 Inverting Amplifier

Task 1:Inverting amplifier

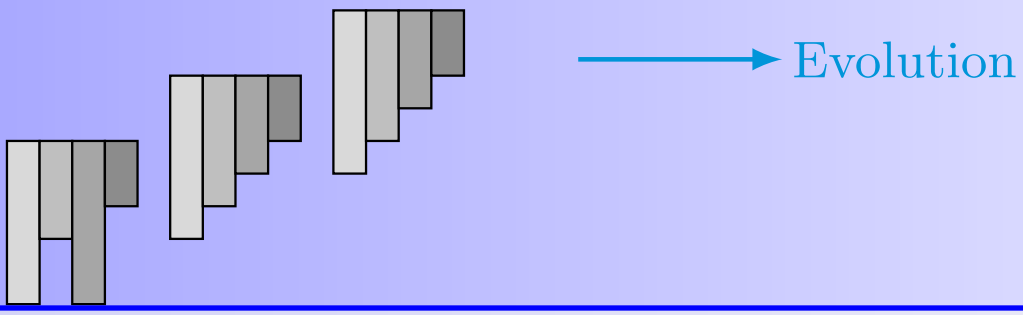
The simple inverting amplifier circuit will be connected as depicted in Figure 14.1 using LTSpice, and we will observe the behavior of the circuit.

(a) Build the circuit in LTSpice using the Op-Amp OP27 from the Op-Amp folder in the LTSpice components. The input should have a peak-to-peak amplitude of 400 mV, which means a peak amplitude of 200 mV, a frequency of 1 kHz, and no DC offset. Make sure that the two DC supplies are negative and positive, and ensure that the inverting and non-inverting inputs are not switched.
(b) Run a transient simulation of this circuit and determine the gain of the circuit.
(c) What does the equation for this type of circuit predict for its behavior? Calculate the actual gain of the circuit.
(d) Is the actual gain close to the gain predicted by the inverting amplifier's equation?
(e) Run a transient simulation of the circuit with a much higher input amplitude. At approximately what input amplitude does the Op-Amp saturate?
(f) What does the equation predict for the behavior in this case? Does the circuit display the output as expected? What happened?
(g) What is the magnitude of the output of the circuit when it saturates?

This experiment aims to familiarize students with the operation and limitations of Op-Amp

OHZE DRAFT

IV Trends in Electronics



15. Trends in Electronics: Exploring the Frontier of Nanoelectronics

15.1 Introduction

We conclude this book by exploring the future of electronics and the emerging trends in nanoelectronics. While microelectronics has been the main focus so far, we will now shift our attention to nanoelectronics. This field involves manipulating matter at the nanoscale and has the potential to bring about revolutionary advancements and applications. Embracing nanoelectronics opens the door to smaller, faster, and more efficient electronic devices, marking a new era in technology. In this chapter, we will discuss current trends, challenges, and future prospects in nanoelectronics, providing a comprehensive overview of this exciting field.

Electronics has played a vital role in transforming society and driving technological advancements. It encompasses the study, design, and development of devices and systems that manipulate and control the flow of electrons for information processing and communication. The rapid evolution of electronics has led to numerous innovations, including integrated circuits and smartphones, which have revolutionized various industries and improved our daily lives.

Advancements in electronics have enabled devices to become smaller, more functional, and higher performing. This progress has had a significant impact on fields such as healthcare, transportation, energy, and communication. Smaller, more powerful, and energy-efficient electronic devices have paved the way for groundbreaking applications that were once considered science fiction.

Nanoelectronics is a specialized branch of electronics that focuses on manipulating and controlling matter at the nanoscale. It exploits the unique properties exhibited by materials and structures at this scale to create innovative electronic devices and systems. By harnessing nanotechnology, researchers have the potential to revolutionize electronics by achieving advancements that were previously unattainable.

15.2 Foundations of Nanoelectronics

Our exploration of the world of electronics and its ever-shrinking sizes takes us back to 1946, when the Electronic Numerical Integrator and Computer (ENIAC), the first digital computer, was built. It was massive, occupying an entire room, weighing 30 tons, and consuming 200 kilowatts of power. Over the next 60 years, the journey of miniaturization revolutionized the electronics industry with

OPEN DRAFT

matrix material, leading to enhanced mechanical, electrical, or thermal characteristics.

(vii) Nanofibers: These are extremely thin fibers with diameters in the nanoscale range. They possess high surface area and unique properties, making them useful in filtration, tissue engineering, and protective coatings.

(viii) Nanoporous Materials: These materials have a porous structure at the nanoscale, providing a large surface area and unique adsorption properties. They find applications in catalysis, gas storage, and water purification.

These examples represent just a fraction of the wide variety of nanomaterials that exist, each with its own unique properties and potential applications.

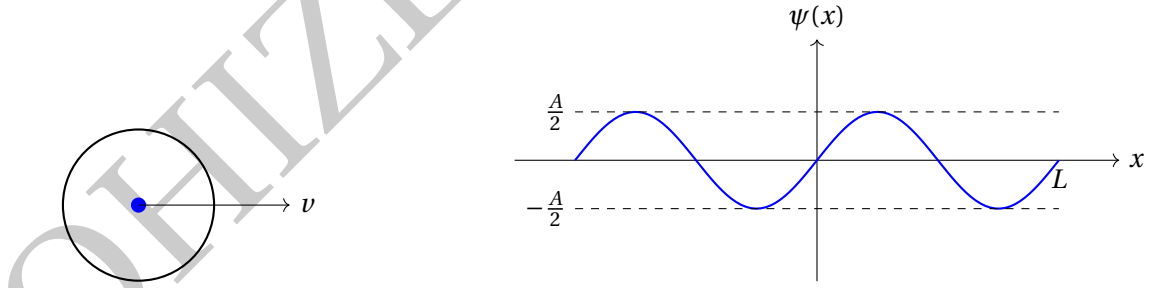
15.2.2 Quantum mechanics and its significance

Quantum mechanics is a scientific theory that explains the behavior of very tiny particles, like atoms and electrons. It tells us that these particles can act like both particles and waves simultaneously know as the duality principle.

In the quantum world, particles have wave-like properties, similar to ocean waves or sound waves. They can spread out, interfere with each other, and show patterns like peaks and troughs. This behavior is crucial at the microscopic level, where particles can be in multiple places at once or jump between energy levels without going through all the states in between. Figure 15.1 is an illustration of particles in both classical and quantum physics. The classical physics illustration (see Figure 15.1(a)) shows a point-like particle with a definite velocity, while the quantum physics illustration (see Figure 15.1(b)) represents the particle as a wave function, with the dashed lines indicating the probability density. Mathematically the wave is defined by the function $\psi(x)$ given as

$$\psi(x) = A\sin(kx+\phi) \tag{15.1}$$

where A is the amplitude, k is the wave number, x is the position of the particle, and ϕ is the phase constant. The square of the absolute value of the wave function, $|\psi(x)|^2$, gives the probability density of finding the particle at position x.



(a) Particle in classical physics

(b) Particle in Quantum physics

Figure 15.1: Subatomic particle representation in classical and quantum physics

Unlike our everyday experiences in the macroscopic world, where things behave predictably like solid objects, the rules of classical physics do not apply at the atomic and subatomic scale. Quantum mechanics is needed to explain these phenomena.

In summary, quantum mechanics describes the behavior of tiny particles, showing both particle-like and wave-like characteristics. Understanding these principles is essential for the design and operation of nanoelectronic devices, enabling the development of faster, more sensitive, and energy-efficient systems.

OHIZE DRAFT007

16. Transistor: Evolving Perspective

16.1 Introduction

The invention of the transistor stands as one of the most significant milestones of the 20th century, revolutionizing the world of electronics and playing a crucial role in the advent of the digital age. Designed to amplify electrical signals and control their flow, transistors have undergone substantial evolution over time. As their channel lengths reached as low as 100 nanometers, microelectronics progressed into the realm of nanoelectronics, with nanotransistors becoming an integral part of the nanotechnology revolution. Today, the relentless march of progress indicates that transistor channel lengths will continue to shrink further, potentially reaching scales as small as 10 nanometers. This naturally raises the question: Just how tiny can we push the boundaries of transistor technology?

As transistors reached the nanometer scale, the overall characteristics measured at their terminals did not change significantly. Otherwise, they would no longer be recognizable as "transistors." However, what did undergo a profound change is the internal physics that governs how charge carriers move from the source (S) to the drain (D) within a transistor. Figure 16.1 provides a cross-sectional view of a Field-Effect Transistor (FET) with an illustration of the shrinking dimensions of the channel. As the channel dimensions reduce, the classical physics, which we relied upon to comprehend larger transistors, can no longer explain the relationship between the channel length and resistance in these minuscule devices. Specifically, as the length decreases, the diffusion or drift flow model, which we used previously, gives way to the ballistic flow model.

For example, one might expect that the resistance would continuously decrease and eventually become zero as the channel length diminishes. However, this is not the case in nanoscale transistors. Similarly, one could anticipate that the small channel would overheat and fail due to heat dissipation, but interestingly, such issues do not manifest themselves. These intriguing observations challenge our prior understanding and beckon us to embrace a new paradigm that can explain these phenomena as the channel enters the nanoscale dimension. The key concept that explains these characteristic behaviors is the phenomenon of ballistic electron flow.

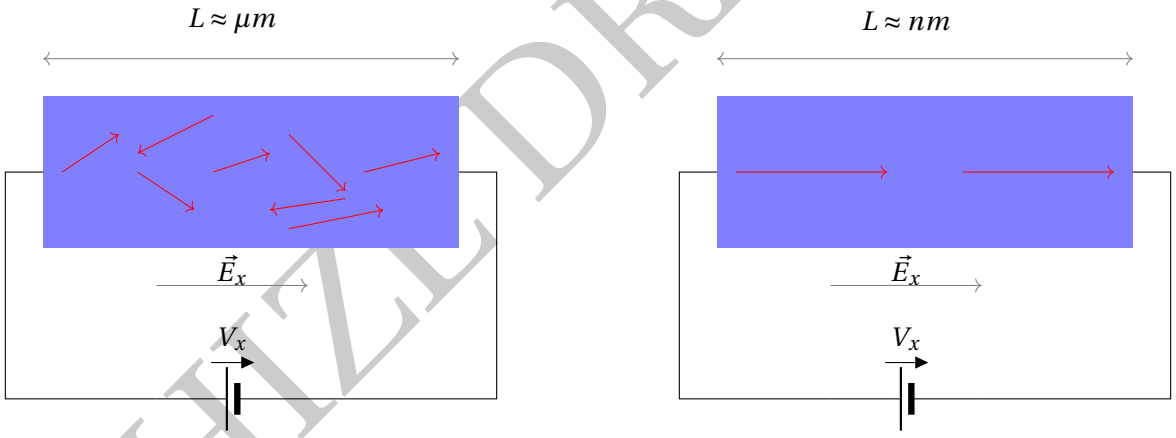
In this chapter, we will embark on a journey to explore the intricate world of electronic transport in nanoscale transistors and witness the intriguing transition from the familiar drift and diffusion phenomena to the fascinating realm of ballistic transport. We will delve into the electron flow model and discuss the crucial concept of conductance.

QUIZ DRAF

scattering events become comparable to the transistor dimensions, leading to the breakdown of the classical drift model. For instance, in Carbon nanotube transistors, the incredibly small one-dimensional band structure suppresses backscattering and allows for near-ballistic operation. However, the diffusion regime describes the movement of electrons due to concentration gradients. Electrons tend to move from regions of high electron density to regions of lower density, much like the behavior of particles diffusing in a fluid. Diffusion currents become significant when the transistor dimensions are large enough to support substantial concentration gradients. However, as transistors scale down to the nanoscale, the distances between regions of varying concentration become shorter, making diffusion less dominant.

As a result, it becomes crucial to comprehend the concept of ballistic operation in the context of the shrinking channel size. In the conventional view, the motion of electrons through a solid is considered "diffusive," where electrons take a random walk from the source to the drain, traveling in various directions before experiencing scattering events (see Figure 16.2(a)). The mean free path, which is the average distance an electron travels before scattering, is typically less than a micrometer in common semiconductors and varies with temperature and material properties.

However, in our shrinking nanoelectronic devices, electrons exhibit "ballistic" flow (see Figure 16.2(b)). This means that electrons move through the channel without scattering, similar to bullets flying through the channel. The device channel's length is now shorter than the mean free path, allowing electrons to traverse it without significant scattering events and losing energy only to heat in the contacts.



(a) Diffusive flow (b) Ballistic flow

Figure 16.2: Illustration of flow mechanisms in semiconductors

Understanding the transition from classical physics to quantum physics and the shift from drift and diffusion flow to ballistic flow provides us with invaluable insights into the behavior of nanoscale transistors. It paves the way for harnessing quantum effects to create innovative and efficient transistor designs that push the boundaries of technology even further.

16.4 Energy Band Perspective of Electron Flow in FET

In order to understand the operation of a Field Effect Transistor (FET), we can utilize the energy band diagrams. These diagrams show the variation of energy levels along the length of the FET from the source to the drain. Let us explore these energy band diagrams step by step.

OHIZL DRAFT007

Bibliography

Books

[1] Chales K. Alexander and Matthew N. O Sadiku. *Fundamentals of Electric Circuits*. 4th edition. Volume 1. 1. USA: McGraw-Hill, Jan. 2008, page 905.

[2] Agarwal Anant and Jeffrey M. Lang. *Foundations of Analog and Digital Electronic Circuits*. 7th edition. Volume 1. 1. USA: Morgan Kaufmann, Oct. 2021, page 592.

[3] Darren Ashby. *Electrical Engineering 101: Everything You Should Have Learned in School ... but Probably Did not*. 3rd edition. Volume 1. 1. USA: Newnes, Sept. 2011, page 304.

[4] John Okyere Attia. *PSPICE and MATLAB for Electronics: An Integrated Approach (VLSI Circuits)*. 1st edition. Volume 1. 1. USA: CRC Press, June 2002, page 360.

[5] John Okyere Attia. *Electronics and Circuit Analysis Using MATLAB*. 2nd edition. Volume 1. 1. USA: CRC Press, June 2004, page 288.

[6] Cabe Satalic Atwell. *Essential 555 IC: Design, Configure, and Create Clever Circuits*. 1st edition. Volume 1. 1. USA: Pragmatic Bookshelf, June 2021, page 106.

[7] Jacob Baker, Harry W. Li, and David E. Boyce. *CMOS Circuit Design, Layout, and Simulation*. 3rd edition. Volume 1. 1. USA: Wiley-IEEE Press, Aug. 1997, page 902.

[8] John Bird. *Birds Electrical and Electronic Principles and Technology*. 7th edition. Volume 1. 1. USA: Routledge, Aug. 2005, page 984.

[9] Robert L. Boylestad and Louis Nashelsky. *Electronic Devices and Circuit Theory*. 11th edition. Volume 1. 1. USA: Pearson, Jan. 2008, page 990.

[10] David Buchla. *Lab Manual for Electronics Fundamentals and Electronic Circuits Fundamentals: Devices and Applications*. 8th edition. Volume 1. 1. USA: Pearson, Sept. 2009, page 416.

[11] Bob Dobkin and Jim Williams. *Analog Circuit Design: A Tutorial Guide to Applications and Solutions*. 1st edition. Volume 1. 1. USA: Newnes, Sept. 2011, page 722.

[12] James Fiore. *Operational Amplifiers and Linear Integrated Circuits: Laboratory Manual*. 1st edition. Volume 1. 1. USA: Independently published, May 2022, page 130.

[13] James M. Fiore. *Operational Amplifiers and Linear Integrated Circuits: Theory and Application*. 7th edition. Volume 1. 1. USA: Independently published, Mar. 2016, page 589.

[14] James M. Fiore. *Semiconductor Devices: Theory and Application*. 7th edition. Volume 1. 1. USA: Independently published, May 2017, page 485.

[15] James M. Fiore. *AC Electrical Circuit Analysis: A Practical Approach*. 7th edition. Volume 1. 1. USA: Independently published, Apr. 2020, page 422.

[16] Thomas Floyd, David Buchla, and Steven Wetterling. *Electronic Devices (Conventional Current Version)*. 10th edition. Volume 1. 1. UK: Pearson, Jan. 2018, page 976.

[17] Clifton G. Fonstad. *Microelectronics Devices and Circuits*. 3rd edition. Volume 1. 1. USA: McGraw-Hill College, Jan. 1994, page 640.

OHZEDRAFT007

[18] M. Mims III Forrest. *Timer, Op Amp, and Optoelectronic Circuits and Projects*. 1st edition. Volume 1. 1. USA: Master Publishing, Inc, Feb. 2004, page 106.

[19] Karl Goser. *Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices*. 9th edition. Volume 1. 1. Germany: Springer, Aug. 2019, page 285.

[20] Holger T. Grahn. *Introduction to Semiconductor Physics*. 7th edition. Volume 1. 1. USA: World Scientific Publishing Company, Apr. 1999, page 984.

[21] David J. Griffiths and Darrell F. Schroeter. *Introduction to Quantum Mechanics*. 3rd edition. Volume 1. 1. UK: Cambridge University Press, Aug. 2018, page 508.

[22] Paul Horowitz and Winfield Hill. *The Art of Electronics*. 3rd edition. Volume 1. 1. USA: Cambridge University Press, Apr. 2015, page 1220.

[23] Eklas Hossain. *MATLAB and Simulink Crash Course for Engineers*. 1st edition. Volume 1. 1. USA: Springer, Sept. 2022, page 288.

[24] Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. 4th edition. Volume 5. 1. USA: Addison-Wesley, Jan. 1988, page 224.

[25] Safa O. Kasap. *Principles of Electronic Materials and Devices*. 4th edition. Volume 1. 1. USA: McGraw-Hill, July 2017, page 992.

[26] Anupama B. Kaul. *Microelectronics to Nanoelectronics, Materials, Devices and Manufacturability*. 9th edition. Volume 3. 1. USA: CRC Press, Aug. 2012, page 464.

[27] Ashok Kumar, A. Kalaiarasi, and Uma Y. Maheswari. *Power Electronics with MATLAB*. 1st edition. Volume 1. 1. USA: Newnes, Nov. 2017, page 544.

[28] Clive Maxfield and John Bird. *Electrical Engineering: Know It All (Newnes Know It All)*. 1st edition. Volume 1. 1. USA: McGrall Hill Education, Aug. 2008, page 2007.

[29] V. K. Mehta and Rohit Mehta. *Principles of Electronics*. 11th edition. Volume 1. 1. New Delhi, India: S. Chand and Company, Dec. 2016, page 780.

[30] Jacob Millman and Christos C. Halkias. *Integrated Electronics: Analog and Digital Circuits and Systems*. 11th edition. Volume 1. 1. USA: McGraw-Hill, Jan. 1972, page 911.

[31] Alexei Nazarov et al. *Semiconductor-On-Insulator Materials for Nanoelectronics Applications (Engineering Materials)*. 2011th edition. Volume 1. 1. UK: Springer, Mar. 2011, page 794.

[32] Donald Neamen. *Microelectronics Circuit Analysis and Design*. 3rd edition. Volume 1. 1. USA: McGraw-Hill, Feb. 2006, page 1392.

[33] Donald Neamen. *Semiconductor Physics And Devices: Basic Principles*. 4th edition. Volume 1. 1. USA: McGraw-Hill, Jan. 2011, page 784.

[34] U.S. Naval Personnel. *Basic Electricity*. Illustrated edition. Volume 1. 1. USA: McGraw-Hill, Mar. 2002, page 504.

[35] Robert F. Pierret. *Semiconductor Device Fundamentals*. 2nd edition. Volume 1. 1. USA: Addison Wesley, Apr. 1996, page 816.

[36] Robert F. Pierret. *Advance Semiconductor Fundamentals*. 2nd edition. Volume 1. 1. USA: Pearson, Aug. 2002, page 240.

[37] A. T. Rajamanickam and G. Gowrisankar. *LABORATORY MANUAL: BASIC ELECTRONICS PRACTICALS*. 1st edition. Volume 1. 1. USA: LAP LAMBERT Academic Publishing, Nov. 2022, page 52.

OHZE DRAFT007

[38] Muhammad H. Rashid. *Microelectronics: Circuit Analysis and Design*. 4th edition. Volume 1. 1. USA: McGraw-Hill, July 2017, page 992.

[39] Behzad Razavi. *Fundamentals of Microelectronics*. 11th edition. Volume 1. 1. Loss Angele, USA: John Wiley and Sons, Jan. 2006, page 928.

[40] Gordon J. Ritchie. *Transistor Circuit Techniques: Discrete and integrated*. 3rd edition. Volume 1. 1. USA: CRC Press, May 2003, page 240.

[41] Paul Scherz and Simon Monk. *Practical Electronics for Inventors*. 4th edition. Volume 1. 1. USA: McGraw-Hill, Mar. 2016, page 1056.

[42] Charles A. Schuller. *Electronics: Principles and Apllication*. 9th edition. Volume 3. 1. Nigeria: McGraw-Hill Education, Jan. 2018, page 624.

[43] Mitchel E. Schultz. *Grobs Basic Electronics*. 13th edition. Volume 1. 1. USA: McGrall Hill Education, Mar. 2020, page 1262.

[44] Adel S Sendra et al. *Microelectronic Circuits*. 8th edition. Volume 1. 1. USA: Oxford University Press, Nov. 2019, page 1296.

[45] Benjamin Spahic. *Electrical engineering without prior knowledge: Understand the basics within 7 days (Become an Engineer Without Prior Knowledge)*. 7th edition. Volume 1. 1. USA: Independently published, Oct. 2020, page 163.

[46] James Squire and Julie Phillips Brown. *Programming for Electrical Engineers: MATLAB and Spice*. 1st edition. Volume 1. 1. USA: Academic Press, Sept. 2020, page 288.

[47] Neil Storey. *Electronics A Systems Approach*. 6th edition. Volume 1. 1. UK: Pearson, Prentice Hall, July 2017, page 864.

[48] Ben G. Streetman and Sanjay Kumar Banerjee. *Solid State Electronic Devices*. 11th edition. Volume 1. 1. USA: Pearson, Jan. 2008, page 990.

[49] Simon M. Sze, Yiming Li, and Kwok K. Ng. *Physics of Semiconductor Devices*. 4th edition. Volume 1. 1. UK: Wiley, Mar. 2021, page 944.

[50] B. L. Theraja and A. K. Theraja. *A Textbook of Electrical Technology*. 11th edition. Volume 1. 1. India: S. Chand and Company, July 2008, page 2782.

[51] Marc Thompson. *Intuitive Analog Circuit Design*. 2nd edition. Volume 1. 1. USA: Newnes, Dec. 2013, page 722.

[52] Bill Wilson. *Introduction to Physical Electronics*. 4th edition. Volume 1. 1. USA: Orange Grove Texts Plus, Sept. 2009, page 263.

[53] Won Y. Yang et al. *Electronic Circuits with MATLAB, PSpice, and Smith Chart*. 1st edition. Volume 1. 1. USA: Wiley, Dec. 2019, page 859.

[54] Adamu Murtala Zungeru and James Garba Ambafi. *Handbook of Laboratory Experiments in Electrical and Electronics*. 8th edition. Volume 3. 1. Nigeria: CreateSpace Independent Publishing Platform, Mar. 2014, page 114.

Articles

[55] Caroline Omoanatse Alenoghena et al. “Telemedicine: A survey of Telecommunication Technologies, Developments, and Challenges”. In: *Journal of Sensor and Actuator Networks* 12.2 (2023), page 20.

OHZE DRAFT007

[56] MP Anantram, Mark S Lundstrom, and Dmitri E Nikonov. “Modeling of nanoscale devices”. In: *Proceedings of the IEEE* 96.9 (2008), pages 1511–1550.

[57] A Baron, D Szewieczek, and R Nowosielski. “Selected manufacturing techniques of nanomaterials”. In: *Journal of Achievements in Materials and Manufacturing Engineering* 20.1-2 (2007), pages 83–86.

[58] Shekhar Borkar. “Design challenges of technology scaling”. In: *IEEE micro* 19.4 (1999), pages 23–29.

[59] Sergey B Brichkin and Vladimir F Razumov. “Colloidal quantum dots: synthesis, properties and applications”. In: *Russian Chemical Reviews* 85.12 (2016), page 1297.

[60] V Chandrakala, Valmiki Aruna, and Gangadhara Angajala. “Review on metal nanoparticles as nanocarriers: Current challenges and perspectives in drug delivery systems”. In: *Emergent Materials* 5.6 (2022), pages 1593–1615.

[61] V Chandrakala, Valmiki Aruna, and Gangadhara Angajala. “Review on metal nanoparticles as nanocarriers: Current challenges and perspectives in drug delivery systems”. In: *Emergent Materials* 5.6 (2022), pages 1593–1615.

[62] Philip G Collins et al. “Nanotube nanodevice”. In: *Science* 278.5335 (1997), pages 100–102.

[63] Jose Maria De Teresa. “Nanofabrication: Nanolithography techniques and their applications”. In: (2020).

[64] Fatma Hadef. “An introduction to nanomaterials”. In: *Environmental Nanotechnology: Volume 1* (2018), pages 1–58.

[65] KD Hirschman et al. “Silicon-based visible light-emitting devices integrated into microelectronic circuits”. In: *Nature* 384.6607 (1996), pages 338–341.

[66] Jing Huang, Mariam Momenzadeh, and Fabrizio Lombardi. “An overview of nanoscale devices and circuits”. In: *IEEE design & test of computers* 24.4 (2007), pages 304–311.

[67] Wilhelm TS Huck. “Self-assembly meets nanofabrication: recent developments in microcontact printing and dip-pen nanolithography”. In: *Angewandte Chemie International Edition* 46.16 (2007), pages 2754–2757.

[68] Gerald J Iafrate and MA Stroscio. “Application of quantum-based devices: Trends and challenges”. In: *IEEE Transactions on Electron Devices* 43.10 (1996), pages 1621–1625.

[69] Adrian M Ionescu and Heike Riel. “Tunnel field-effect transistors as energy-efficient electronic switches”. In: *nature* 479.7373 (2011), pages 329–337.

[70] S Karmakar et al. “Nano-electronics and spintronics with nanoparticles”. In: 292.1 (2011), page 012002.

[71] Wei Lu, Ping Xie, and Charles M Lieber. “Nanowire transistor performance limits and applications”. In: *IEEE transactions on Electron Devices* 55.11 (2008), pages 2859–2876.

[72] Wei Lu, Ping Xie, and Charles M Lieber. “Nanowire transistor performance limits and applications”. In: *IEEE transactions on Electron Devices* 55.11 (2008), pages 2859–2876.

[73] Loutfy H Madkour and Loutfy H Madkour. “Introduction to nanotechnology (NT) and nanomaterials (NMs)”. In: *Nanoelectronic Materials: Fundamentals and Applications* (2019), pages 1–47.

OHZE DRAFT007

[74] Loutfy H. Madkour. “Introduction to Nanotechnology (NT) and Nanomaterials (NMs)”. In: *Nanoelectronic Materials: Fundamentals and Applications* (2019), pages 1–47. DOI: 10.1007/978-3-030-21621-4_1. URL: https://doi.org/10.1007/978-3-030-21621-4_1.

[75] Grigorii N Makarov. “Laser applications in nanotechnology: nanofabrication using laser ablation and laser nanolithography”. In: *Physics-Uspekhi* 56.7 (2013), page 643.

[76] Gordon E Moore. “Cramming more components onto integrated circuits”. In: *Proceedings of the IEEE* 86.1 (1998), pages 82–85.

[77] Gordon E Moore. “Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff.” In: *IEEE solid-state circuits society newsletter* 11.3 (2006), pages 33–35.

[78] Konstantin S Novoselov et al. “A roadmap for graphene”. In: *nature* 490.7419 (2012), pages 192–200.

[79] Suphiya Parveen, Ranjita Misra, and Sanjeeb K Sahoo. “Nanoparticles: a boon to drug delivery, therapeutics, diagnostics and imaging”. In: *Nanomedicine: Nanotechnology, Biology and Medicine* 8.2 (2012), pages 147–166.

[80] Branimir Radisavljevic et al. “Single-layer MoS2 transistors”. In: *Nature nanotechnology* 6.3 (2011), pages 147–150.

[81] A. Rahman et al. “Theory of ballistic nanotransistors”. In: *IEEE Transactions on Electron Devices* 50.9 (2003), pages 1853–1864. DOI: 10.1109/TED.2003.815366.

[82] CNR Rao and AK Cheetham. “Science and technology of nanomaterials: current status and future prospects”. In: *Journal of Materials Chemistry* 11.12 (2001), pages 2887–2894.

[83] Farhang Shadman. “Environmental challenges in nanoelectronics manufacturing”. In: *Current Opinion in Chemical Engineering* 1.3 (2012), pages 258–268.

[84] Mani Vaidyanathan. “Electronics From the Bottom Up: Strategies for Teaching Nanoelectronics at the Undergraduate Level”. In: *IEEE Transactions on Education* 54.1 (2011), pages 77–86. DOI: 10.1109/TE.2010.2043845.

[85] Anxin Wang et al. “Role of surface charge and oxidative stress in cytotoxicity and genotoxicity of graphene oxide towards human lung fibroblast cells”. In: *Journal of Applied Toxicology* 33.10 (2013), pages 1156–1164.

OHZE DRAFT007

OHIZE DRAFT007

Index

QHIZE DRAFT 007

OHIZE DRAFT007

OHZE DRAFT007