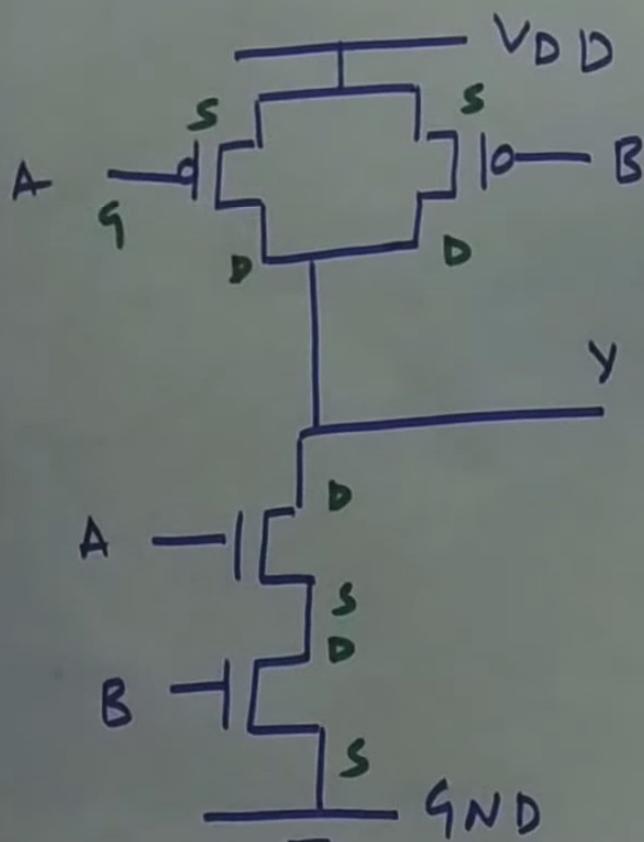


• → series

+ → series

$$Y = \overline{A \cdot B} \quad \underline{\text{CMOS}}$$

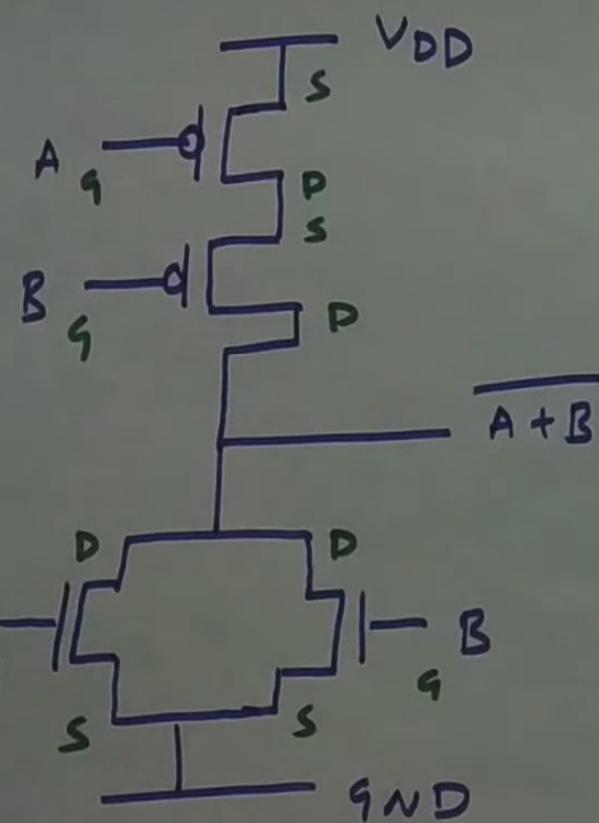


STICK DIAGRAM

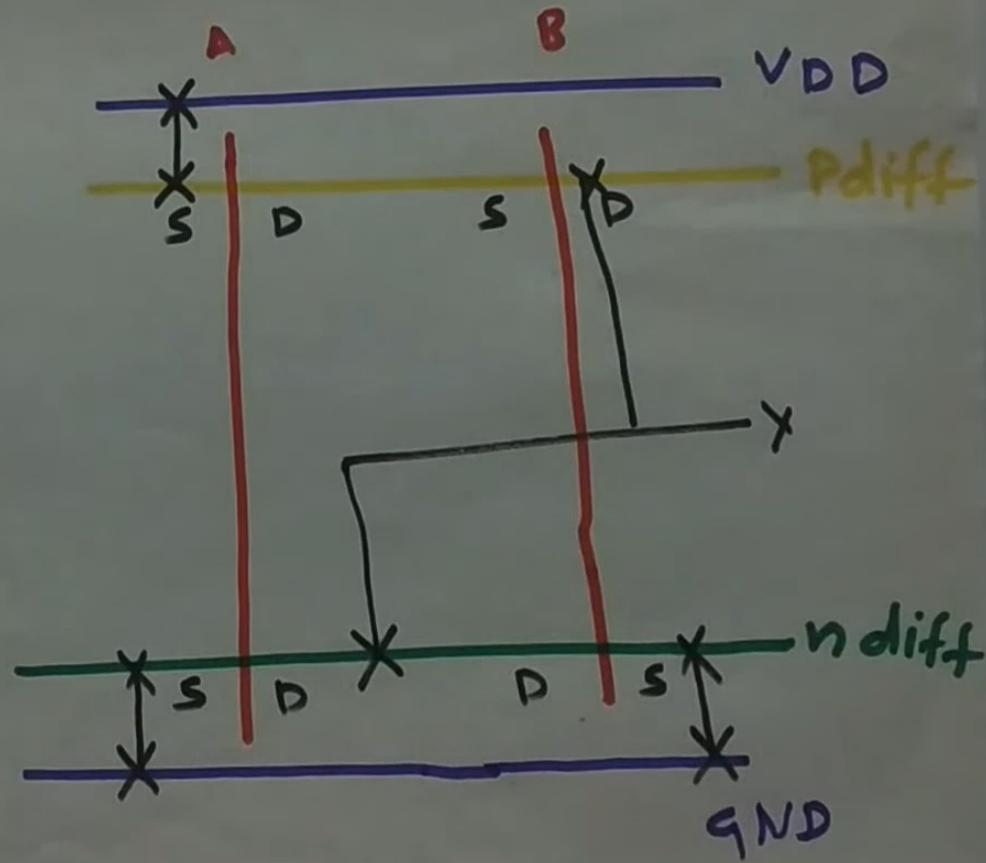


How to draw Stick diagrams ?(VLSI)| simplified| With Examples

C MOS



STICK DIAGRAM



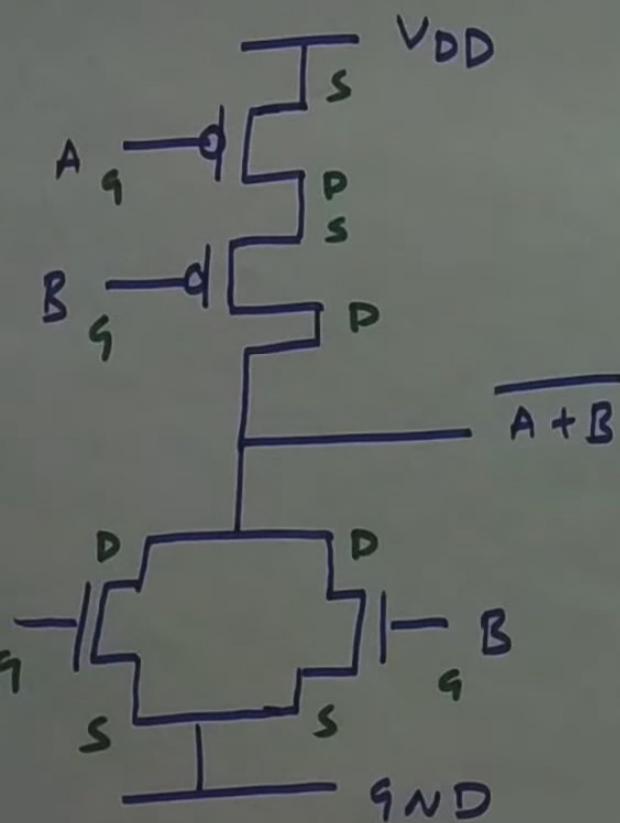
8:33 / 12:57



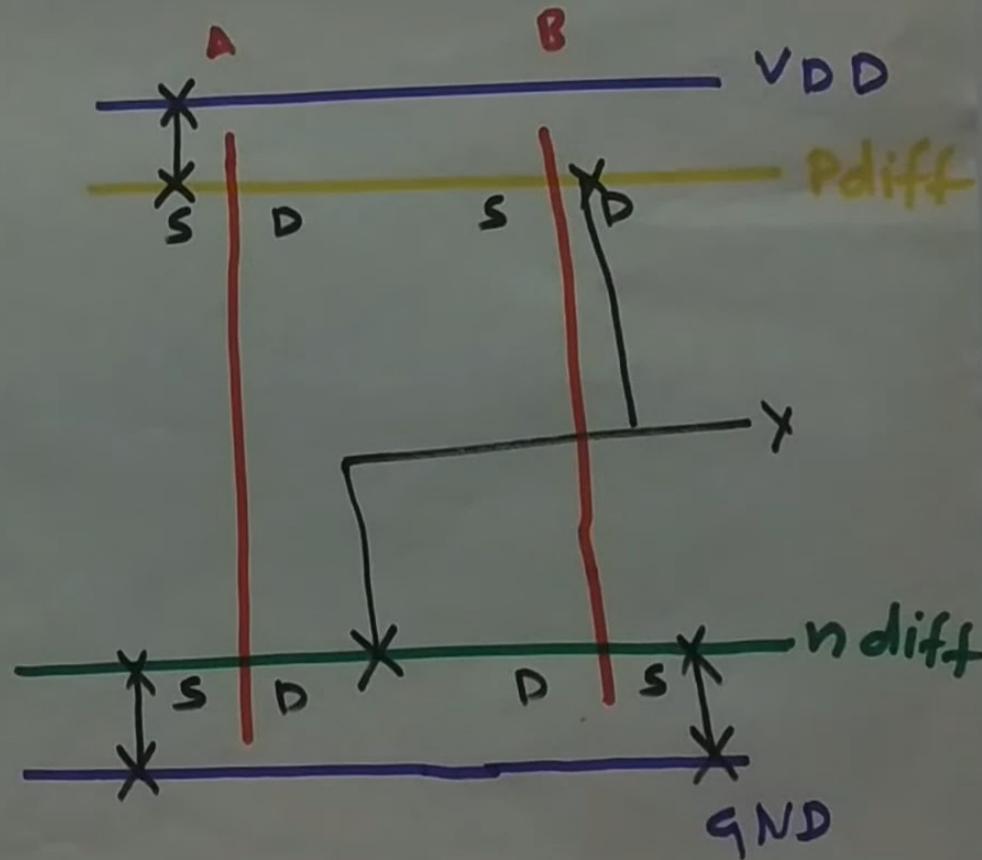
How to draw Stick diagrams ?(VLSI)| simplified| With Examples

C MOS

$A + B$



STICK DIAGRAM

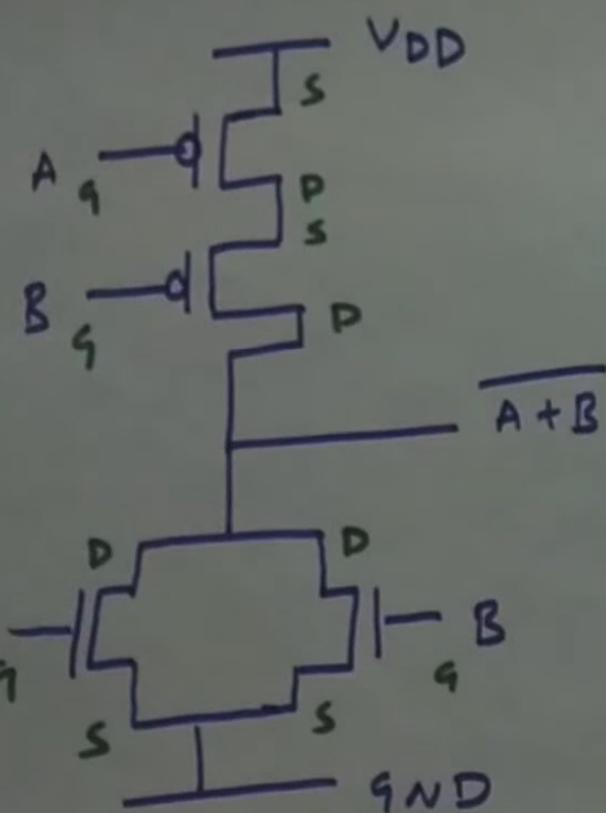


8:35 / 12:57

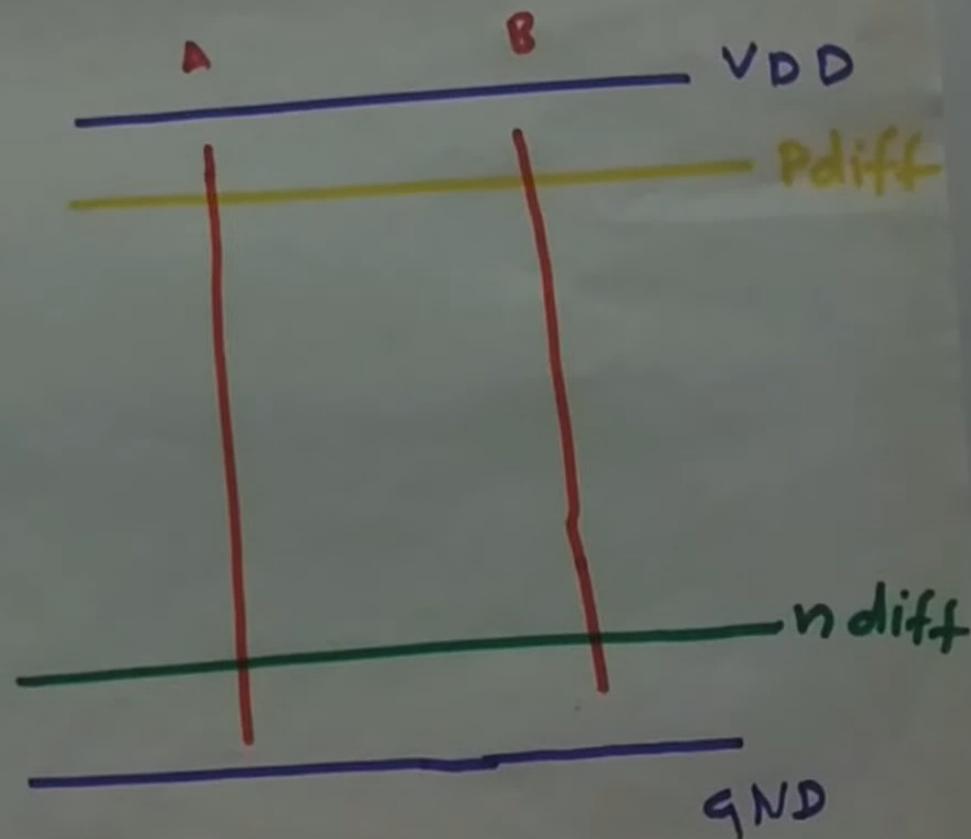


$\overline{A+B}$

CMOS



STICK DIAGRAM

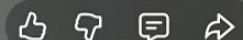
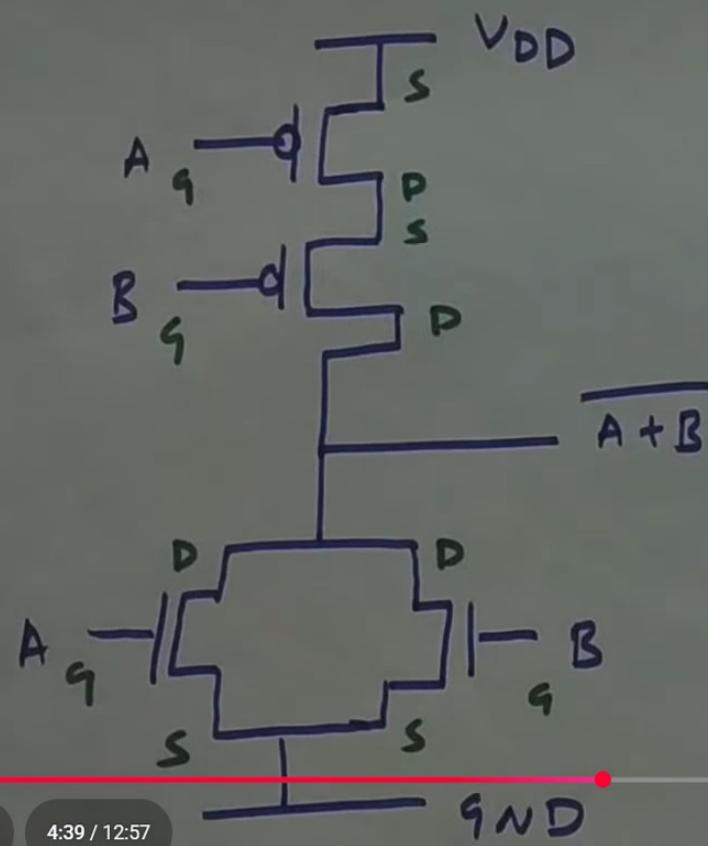


How to draw Stick diagrams ?(VLSI)| simplified| With Examples

$$Y = \overline{A+B}$$

CMOS

STICK DIAGRAM

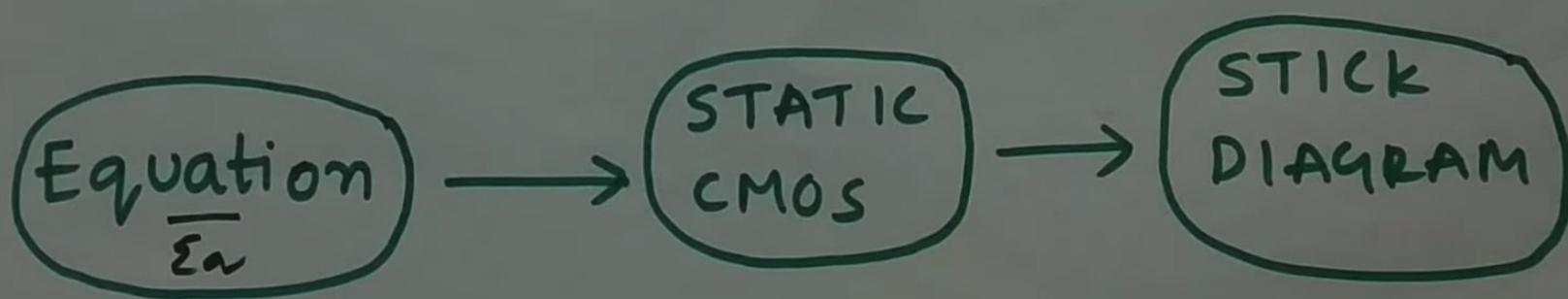


4:39 / 12:57



STICK DIAGRAMS

STICK DIAGRAMS are means of capturing topography and layer information using simple diagrams.



NMOS : + → Parallel
· → Series

PMOS • → Parallel
+ → Series

λ Rules

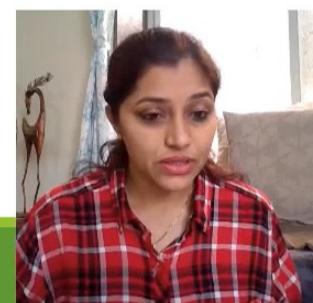
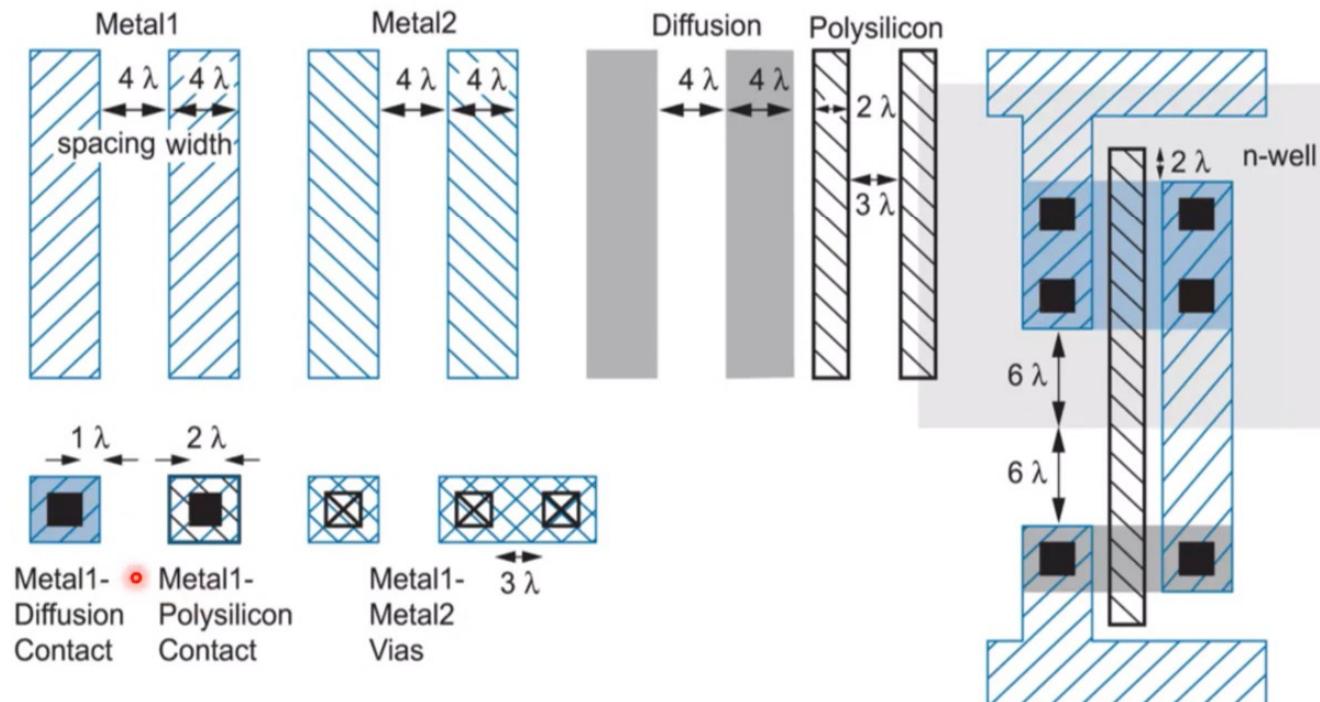


Image: CMOS VLSI Design by Weste, Harries and Banerjee

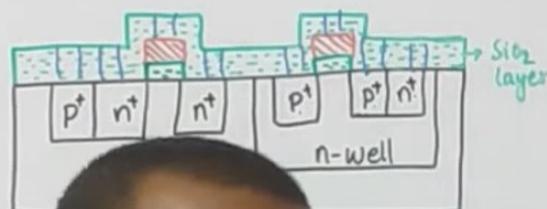
What are Lambda Rules?

- ❑ VLSI (Very Large Scale Integration) involves designing complex circuits on a chip.
- ❑ Layout design is a crucial step where circuit elements are placed and interconnected.
- ❑ Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- ❑ Need to define transistors, interconnection— Transistor widths (for performance)
- ❑ Spacing, interconnect widths, to reduce defects, satisfy power requirements
- ❑ Contacts (between poly or active and metal), and vias (between metal layers)
- ❑ Wells and their contacts (to power or ground)
- ❑ Lambda (λ) is a unit of measurement used in VLSI design.
- ❑ Express rules in terms of $\lambda = L/2$
- ❑ E.g. $\lambda = 45$ nm in 90 nm process



CMOSFABRICATION

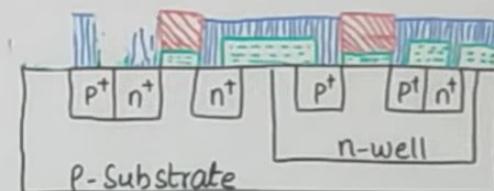
Step 12: Now grown thick oxide On the top & etch oxide where contact cuts are needed



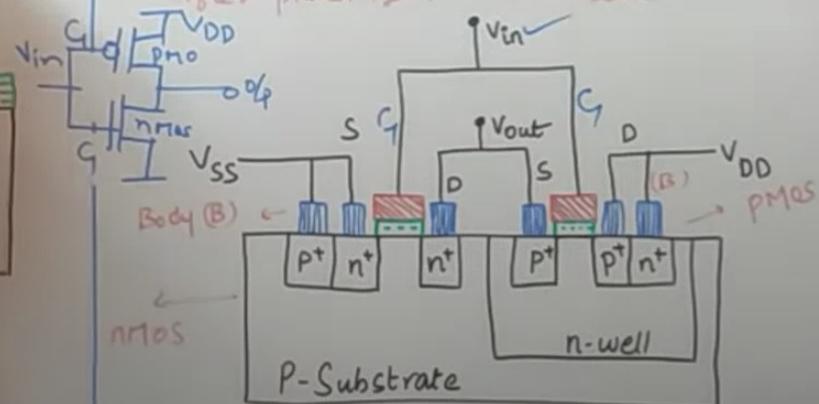
Step 13: place contact where contact cuts are made



Step 14: Now place aluminium (copper) metal whole wafer & pattern to remove excess metal

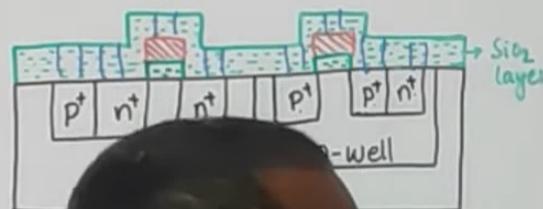


Step 15: finally remove the excess metal and SiO_2 and connect metal Contact through wires
After planarization we have



CMOSFABRICATION

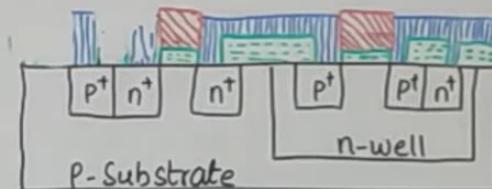
Step 12: Now grown thick oxide On the top & etch oxide where contact cuts are needed



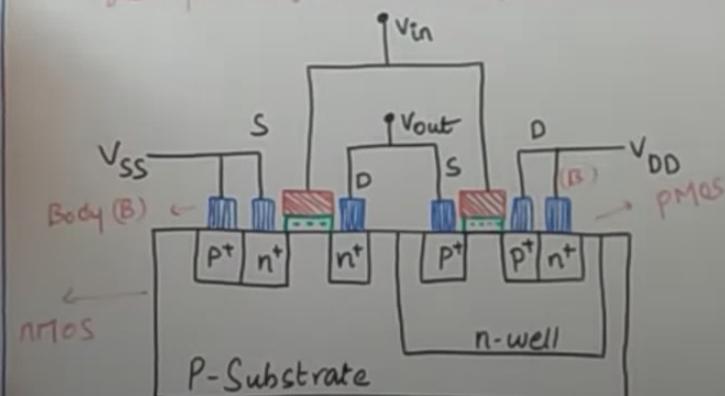
Step 13: place contact



Step 14: Now place aluminium (copper) metal whole wafer & pattern to remove excess metal

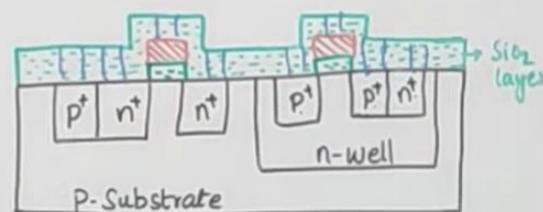


Step 15: finally remove the excess metal and SiO₂ and connect metal Contact through wires
After planarization we have

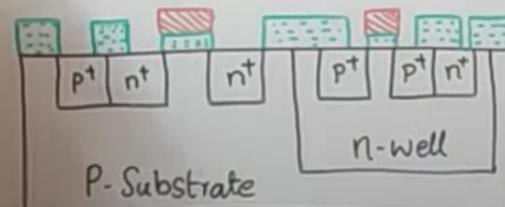


CMOSFABRICATION

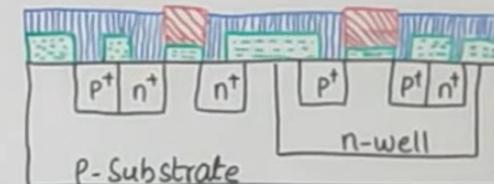
Step 12: Now grown thick oxide On the top & etch oxide where contact cuts are needed



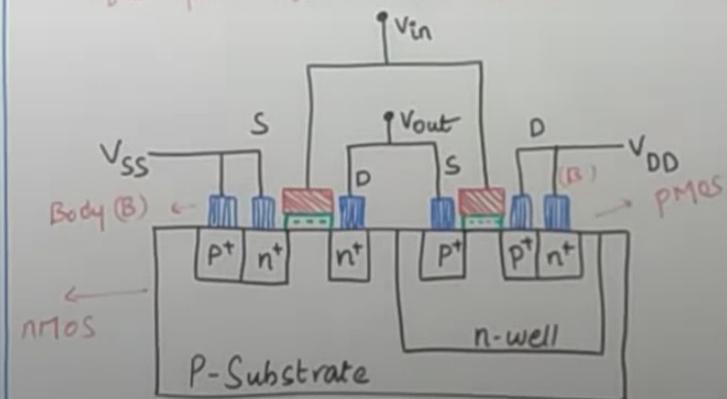
Step 13: Remove oxide where contact cuts are needed



Step 14: Now place aluminium (copper) metal over whole wafer & pattern to remove excess metal



Step 15: finally remove the excess metal and SiO_2 and connect metal Contact through wires
After planarization we have



N- Well Process

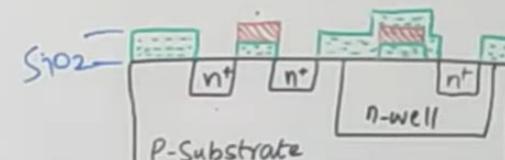
Step 7: After removing photoresist grown, thick Oxide and photoresist on it. Expose the photoresist to UV light using mask to define n⁺ regions.



Step 8: Remove photoresist then remove thick SiO₂ under it

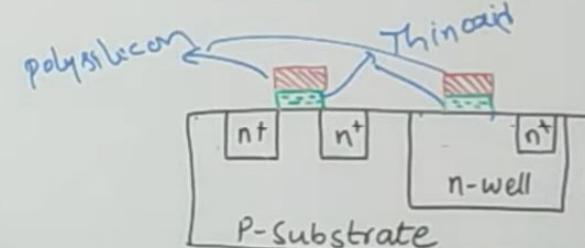
equivalent impurity

to form back the source.

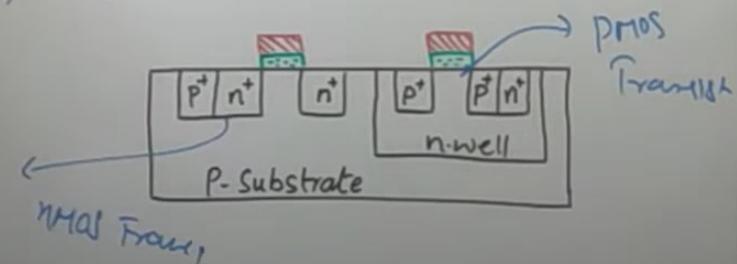
CMOS FABRICATION

Step 10:

Now remove SiO₂ to complete Pattern of n⁺ regions

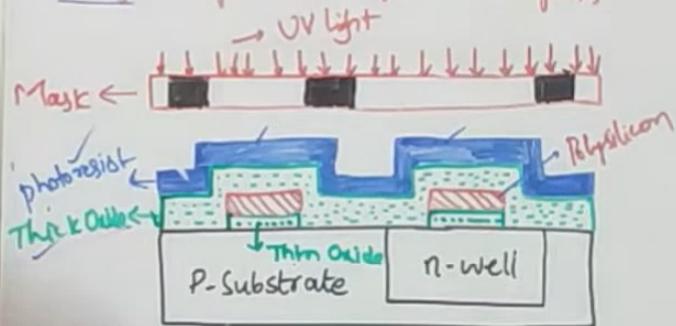


Step 11: Similarly we can form p⁺ diffusion regions for PMOS Source and drain & Substrate contact.

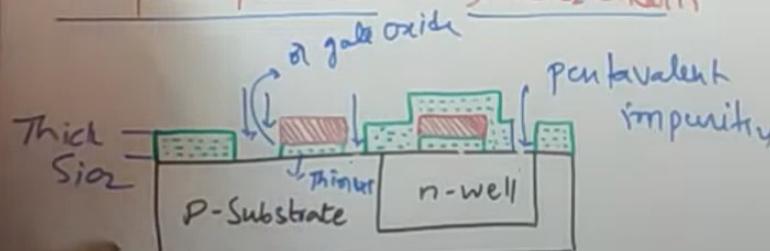


CMOS FABRICATIONN- Well Process

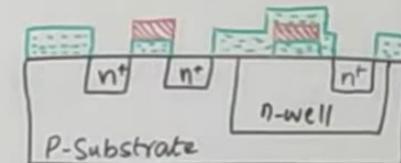
Step 7:- After removing photoresist grown, thick Oxide and photoresist on it. Expose the photoresist to UV light using mask to define n⁺ regions.



Step 8:- Remove the exposed photoresist then remove unexposed photoresist and thick SiO₂ under it

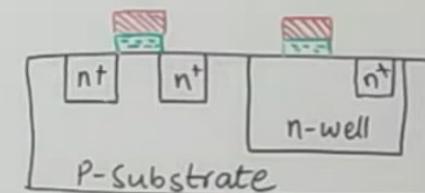


Here N-diffusion Process used to form regions where gate oxide will block the impurities. Called Self-Aligned Process.

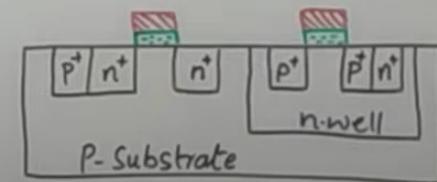


Step 10:-

Now remove SiO₂ to complete Pattern of n⁺ regions

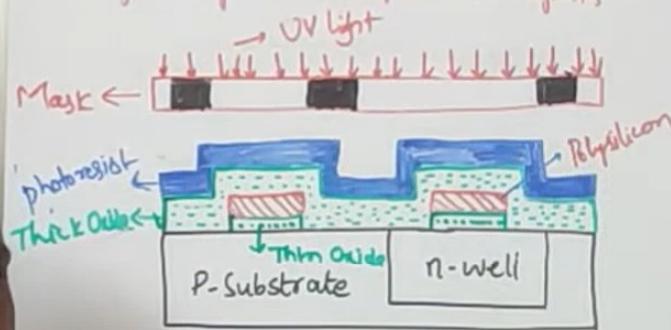


Step 11:- Similarly we can form p+ diffusion regions for PMOS Source and drain & Substrate contact.

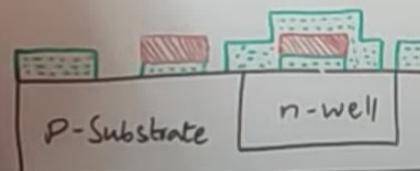


N- Well Process

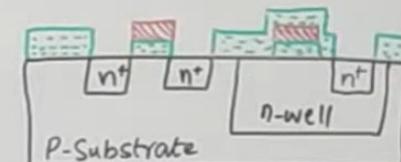
Step 7: After removing photoresist grown, thick Oxide and photoresist on it. Expose the photoresist to UV light using mask to define n⁺ regions.



Step 8: Remove the exposed photoresist then remove unexposed photoresist and thick SiO₂ under it

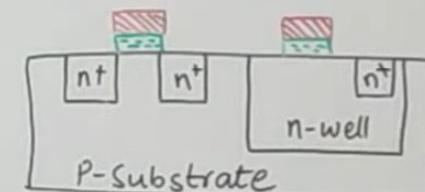


Step 9: Here N-diffusion Process used to form n⁺ regions here gate oxide will block the dopants Called Self-Aligned Process.

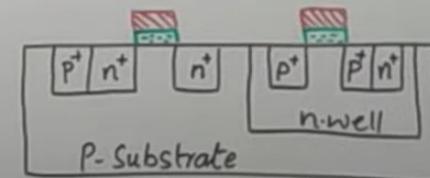
CMOS FABRICATION

Step 10:

Now remove SiO₂ to complete Pattern of n⁺ regions

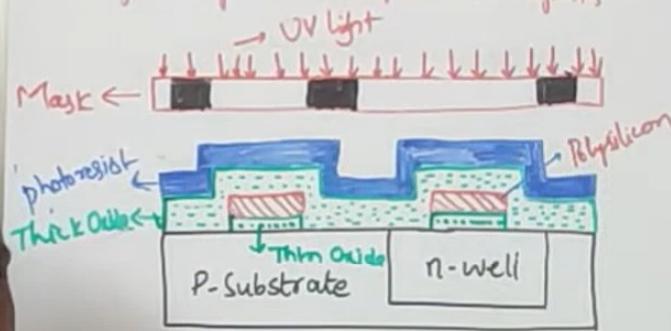


Step 11: Similarly we can form p⁺ diffusion regions for PMOS Source and drain & Substrate contact.

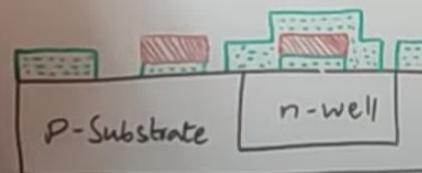


N- Well Process

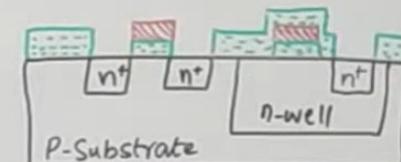
Step 7: After removing photoresist grown, thick Oxide and photoresist on it. Expose the photoresist to UV light using mask to define n⁺ regions.



Step 8: Remove the exposed photoresist then remove unexposed photoresist and thick SiO₂ under it

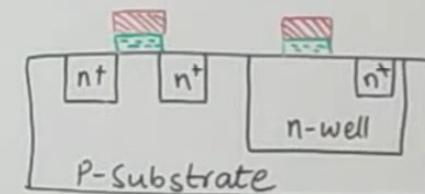


Step 9: Here N-diffusion Process used to form n⁺ regions here gate oxide will block the dopants Called Self-Aligned Process.

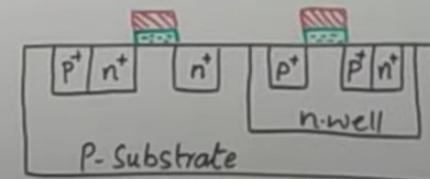
CMOS FABRICATION

Step 10:

Now remove SiO₂ to complete Pattern of n⁺ regions



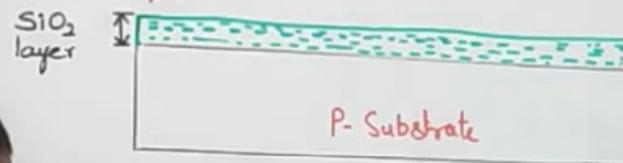
Step 11: Similarly we can form p⁺ diffusion regions for PMOS Source and drain & Substrate contact.



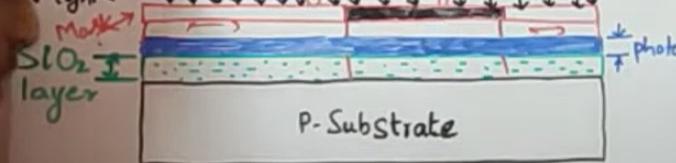
CMOSFABRICATION

- We have different methods of CMOS Fabrication
1. n-Well Process
 2. P-Well Process
 3. Twin-Tub Process
 4. Silicon on Insulator Process

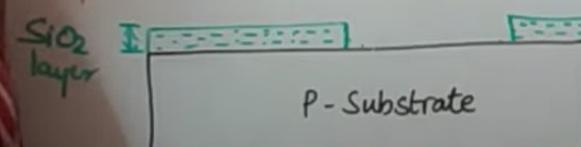
Step 1: Consider a Silicon Wafer and grown SiO_2 layer by heating at 900 to 1200°C with H_2O & O_2 in oxidation furnace.



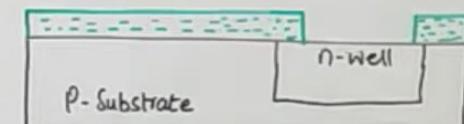
Step 2: Grown the photoresist layer on top of SiO_2 and Expose to UV light through n-Well mask



Step 3: Remove the unexposed photoresist and SiO_2 under it using Hydro Fluoric Acid then Strip off Exposed Photoresist

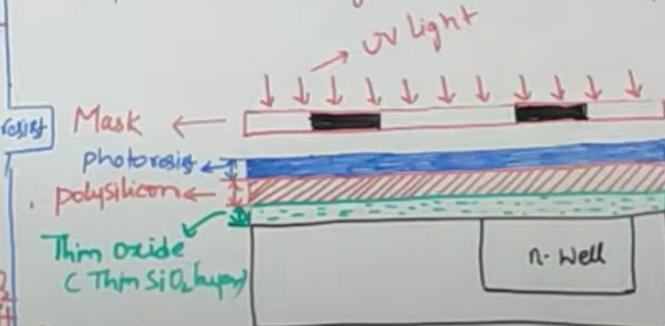


Step 4: n-Well is formed by diffusion & ion implantation by introducing pentavalent impurities

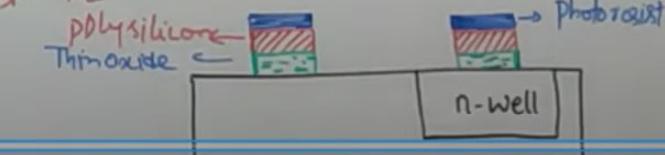


Step 5: Remove the SiO_2 layer, deposit thin oxide & polysilicon above it by chemical Vapour deposition (CVD)

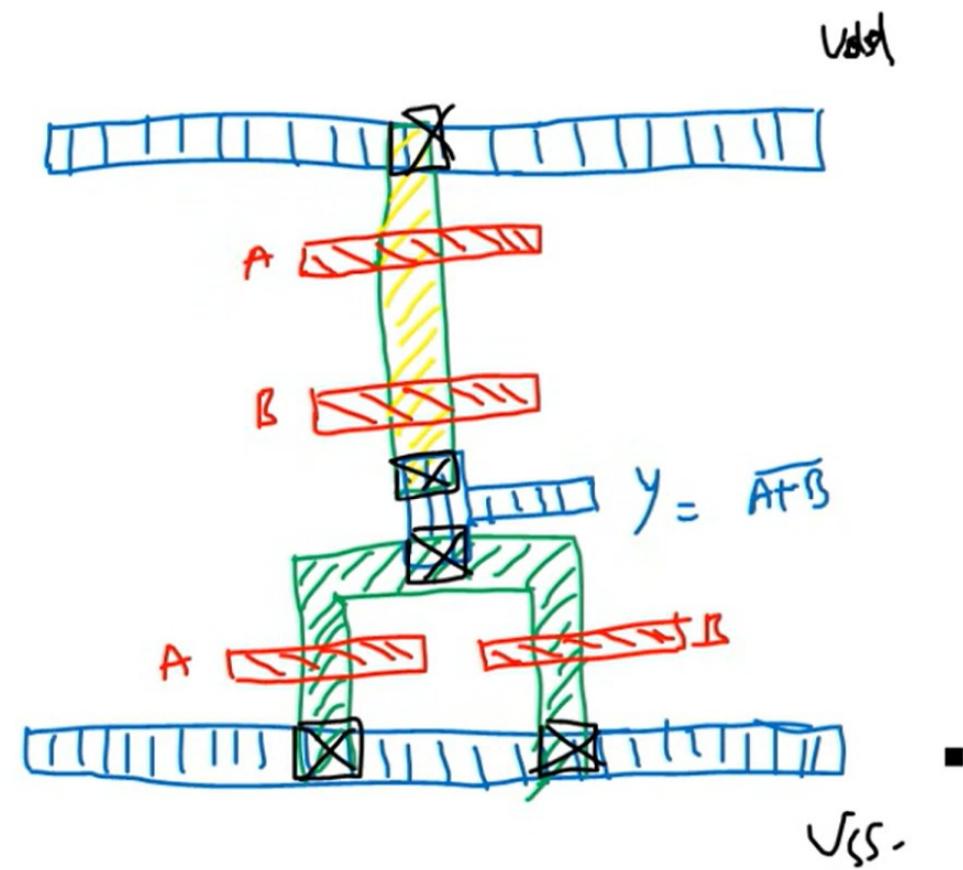
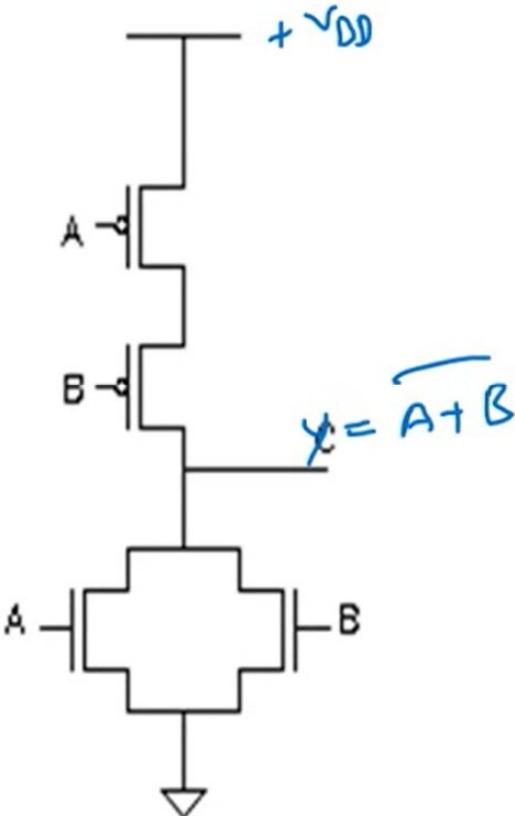
Grown a photoresist layer above polysilicon and then expose it to UV light for the formation of gates



Step 6: Now remove the exposed photoresist, polysilicon & SiO_2 under it



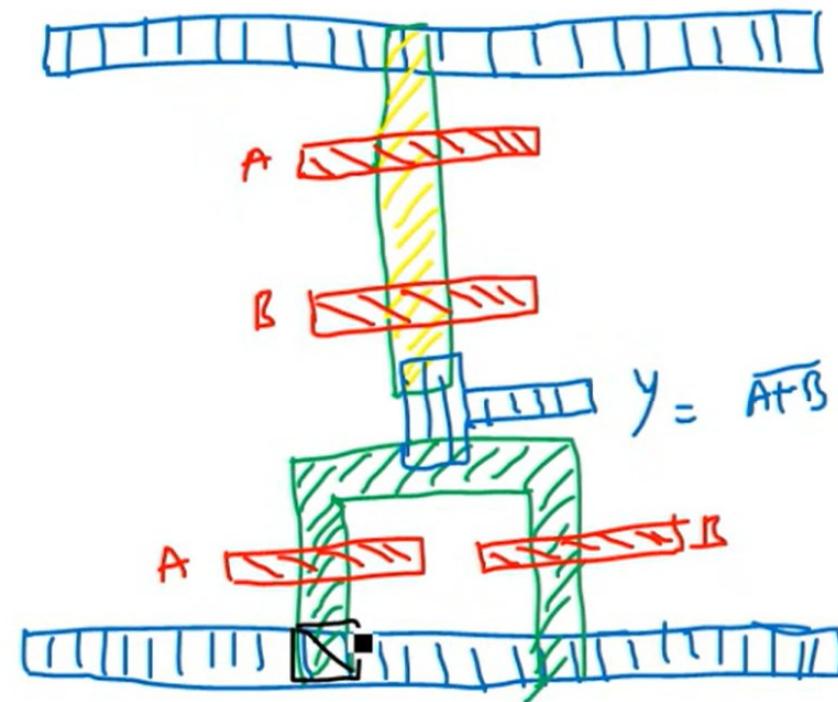
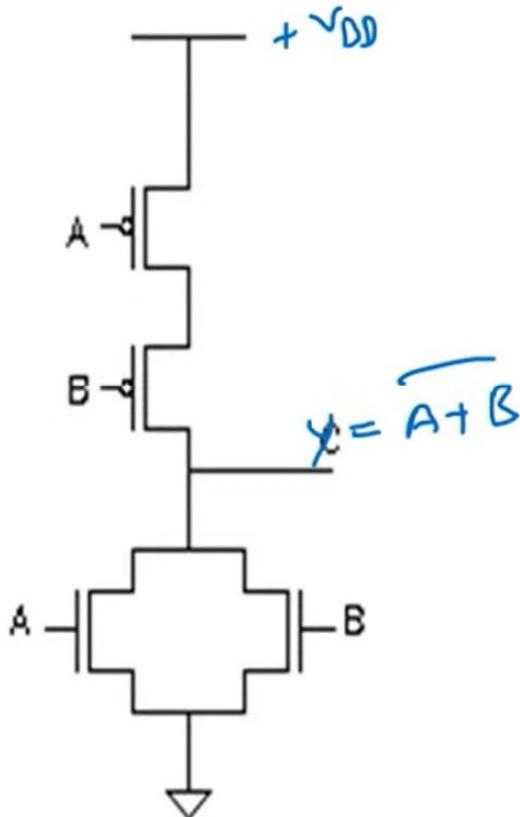
2-input NOR gate



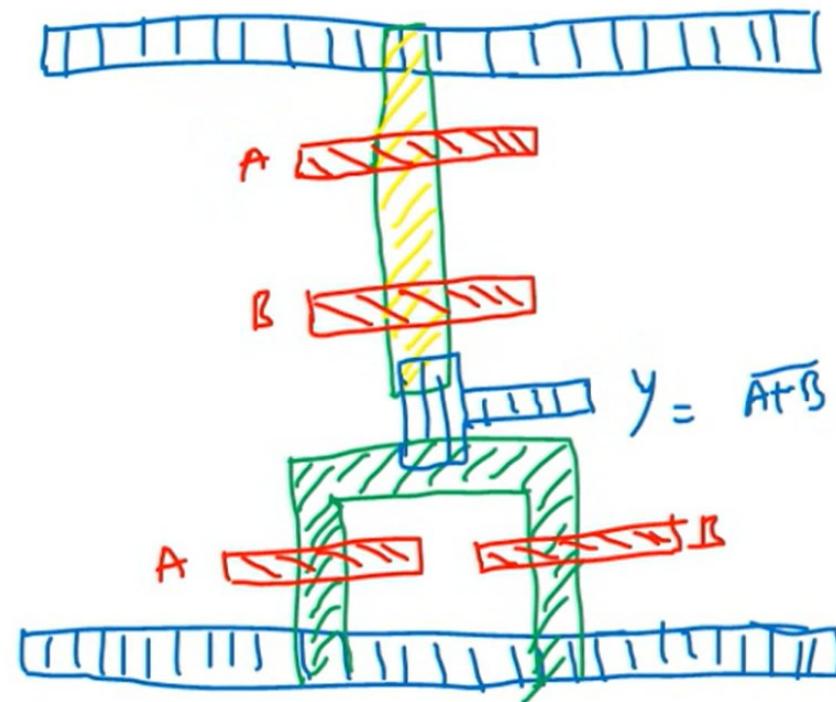
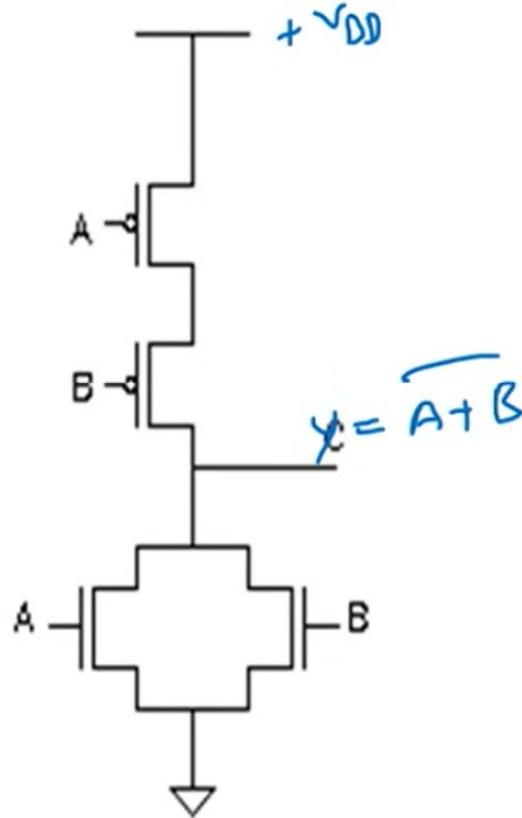
11:27 / 11:33 (11:31)



2-input NOR gate

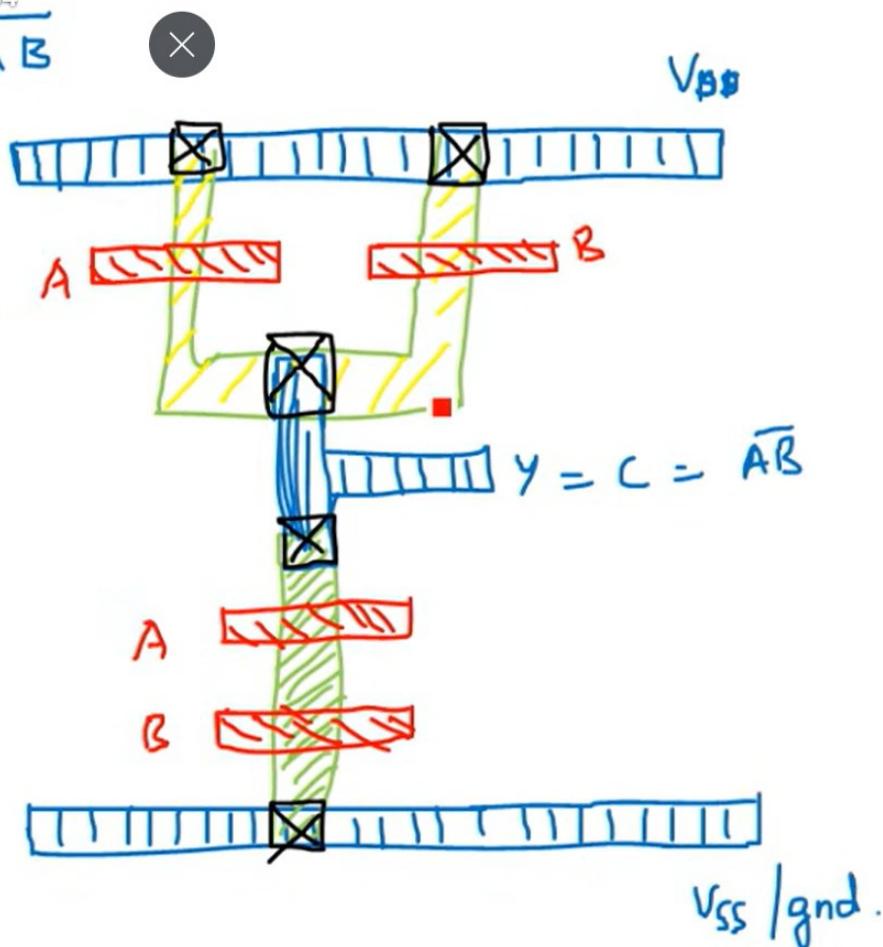
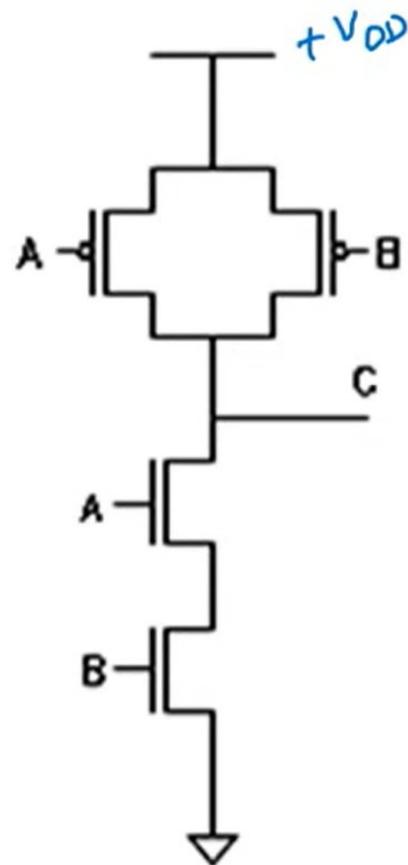


2-input NOR gate



2-input NAND gate

$$C = \overline{A} \overline{B}$$

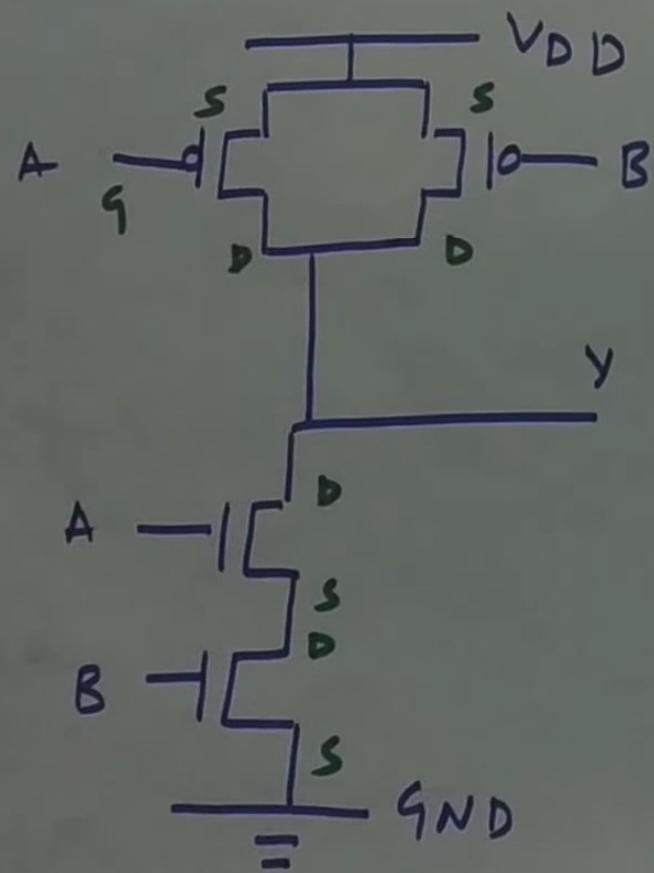


6:51 / 11:33 (11:31)

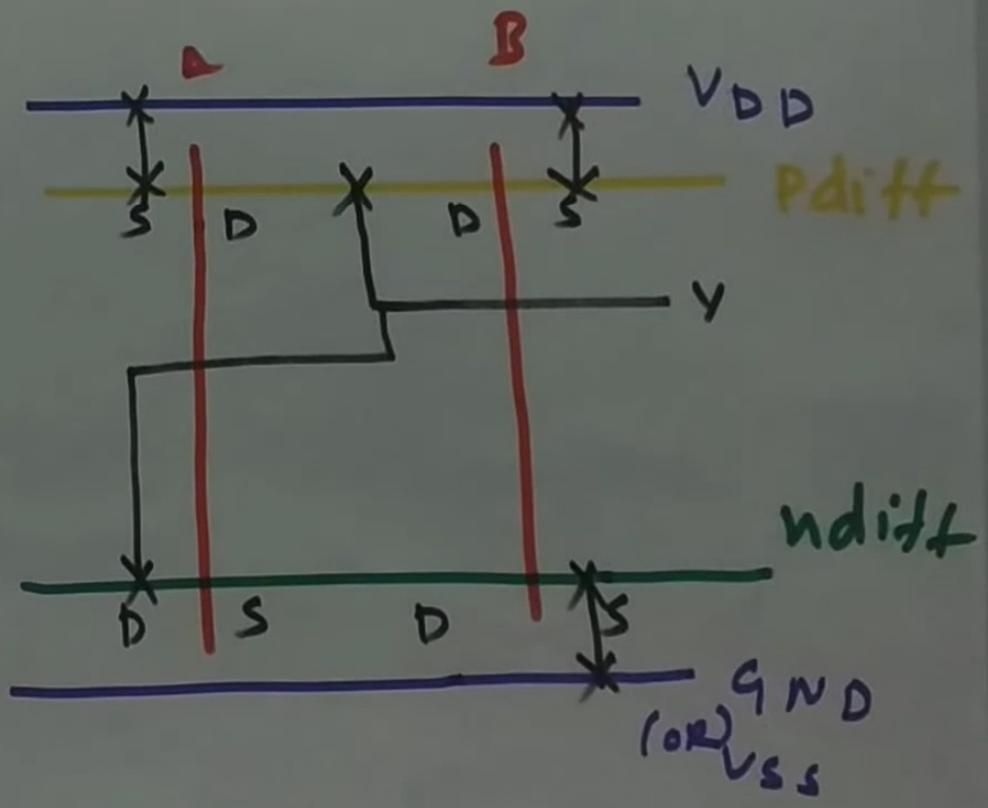


$$= \overline{A} \cdot B$$

CMOS

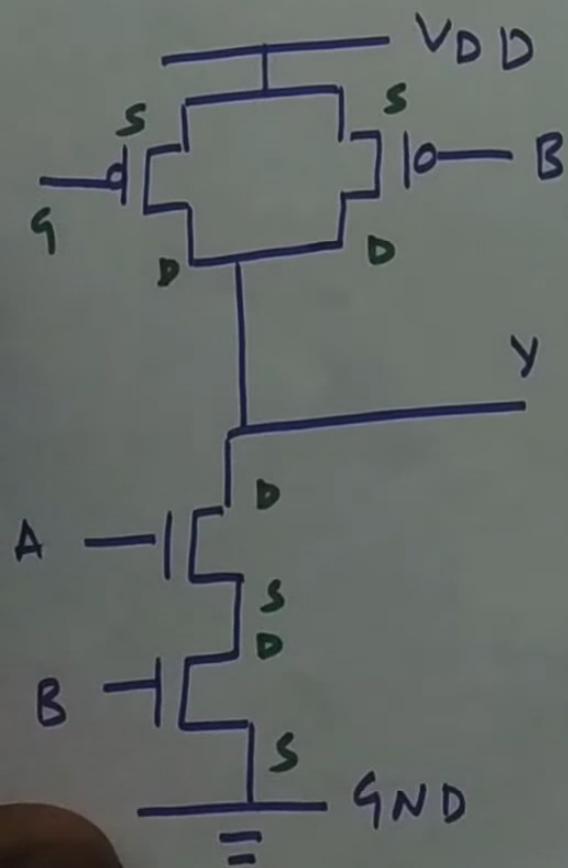


STICK DIAGRAM

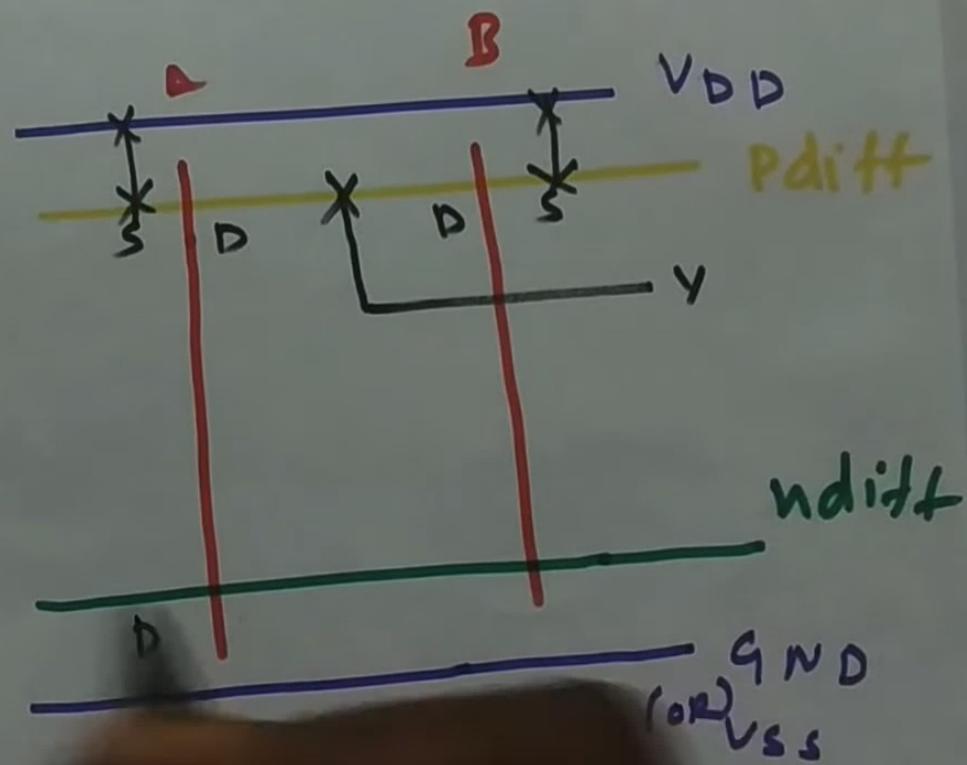


\bar{B}

CMOS

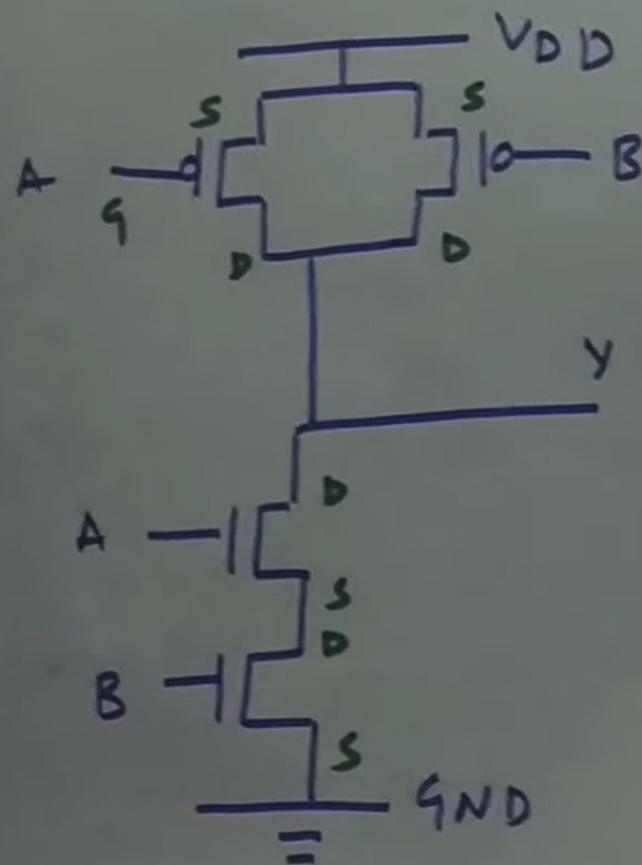


STAGE DIFFERENTIAL



$$y = \overline{A \cdot B}$$

CMOS



STICK DIAGRAM

