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To cite this article: Mohammad Javad Mirshojaeian Hosseini *et al* 2022 *Neuromorph. Comput. Eng.* **2** 034009

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OPEN ACCESS

RECEIVED
31 March 2022REVISED
13 July 2022ACCEPTED FOR PUBLICATION
21 July 2022PUBLISHED
2 September 2022

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An organic synaptic circuit: toward flexible and biocompatible organic neuromorphic processing

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mfaezipo@purdue.edu, giacomo@ini.uzh.ch and robertnawrocki@purdue.edu**Keywords:** spiking neuromorphics, organic neuromorphics, flexible organic synaptic circuit, differential-pair integrator synapse, biologically plausible time constant

Abstract

In the nervous system synapses play a critical role in computation. In neuromorphic systems, biologically inspired hardware implementations of spiking neural networks, electronic synaptic circuits pass signals between silicon neurons by integrating pre-synaptic voltage pulses and converting them into post-synaptic currents, which are scaled by the synaptic weight parameter. The overwhelming majority of neuromorphic systems are implemented using inorganic, mainly silicon, technology. As such, they are physically rigid, require expensive fabrication equipment and high fabrication temperatures, are limited to small-area fabrication, and are difficult to interface with biological tissue. Organic electronics are based on electronic properties of carbon-based molecules and polymers and offer benefits including physical flexibility, low cost, low temperature, and large-area fabrication, as well as biocompatibility, all unavailable to inorganic electronics. Here, we demonstrate an organic differential-pair integrator synaptic circuit, a biologically realistic synapse model, implemented using physically flexible complementary organic electronics. The synapse is shown to convert input voltage spikes into output current traces with biologically realistic time scales. We characterize circuit's responses based on various synaptic parameters, including gain and weighting voltages, time-constant, synaptic capacitance, and circuit response due to inputs of different frequencies. Time constants comparable to those of biological synapses and the neurons are critical in processing real-world sensory signals such as speech, or bio-signals measured from the body. For processing even slower signals, e.g., on behavioral time scales, we demonstrate time constants in excess of two seconds, while biologically plausible time constants are achieved by deploying smaller synaptic capacitors. We measure the circuit synaptic response to input voltage spikes and present the circuit response properties using custom-made circuit simulations, which are in good agreement with the measured behavior.

1. Introduction

The neuromorphic engineering field was pioneered by Carver Mead in the early 90s [1]. Neuromorphic electronic systems aim to apply biologically inspired principles to develop neural computing systems with applications including sensory signal perception and processing, autonomous robotics, or brain-machine interfaces [2, 3]. Recently, the term 'neuromorphic' has been used to refer to artificial intelligence sensory processing systems *emulated in hardware* with full custom spiking neural network chips, rather than being *simulated in software* using conventional computers and neural network software simulation environments, such as Emergent or Matlab [4, 5].

Neuromorphic systems are based on densely interconnected individual units called neurons, consisting of multiple *synapses* and a single *soma* [6]. A synapse receives the incoming voltage pulse and weights, or scales,

it via the so-called synaptic weight, which is adjusted during training. The function of a soma is to sum all of the weighted input signals and, once a threshold value has been exceeded, produce a voltage pulse (a spike) in output.

Conventional, so-called von Neumann, computing is based on macro separation of information and information processing, thus it is serial, deterministic, synchronous, power hungry (mainly because of data movement), and explicitly programmed [7]. In contrast, neuromorphic systems are analog, parallel, nondeterministic, event-driven, low power (mainly because of in-memory computing architectures), and programmed by learning, with the information stored and programmed at the same site (at the synapse) [8].

The majority of current neuromorphic systems are large multi-neuron implementations, either based on conventional hardware emulating neuronal functions, such as the University of Manchester's SpiNNaker [9], or on custom-made neuromorphic hardware. The latter approach has attracted more attention in both academia, for instance the Institute of Neuroinformatics' ROLLS and DYNAPs or Stanford's BrainDrop [10–12], and recently industry, including IBM's TrueNorth, Intel's Loihi, and Qualcomm's NPU [13–15].

Memristors, or memristive devices, devices that can change their resistive state in a non-volatile way, have received a great deal of attention due to their ability to emulate synaptic weighting [16, 17]. Memristors have been proposed or implemented with spiking and non-spiking neurons, including dedicated and memristive cross-bar arrays [18–20].

The overwhelming majority of neuromorphic, including memristive, systems are implemented using inorganic materials. While their advantages include high-speed operation, small device variability, and high reproducibility, their main disadvantages include physical rigidity, biological incompatibility, expensive fabrication equipment, and high fabrication temperature. *Organic electronics*, electronics based on organic (carbon-based) materials, including polymers, offer physical flexibility, biocompatibility, large-area circuits, and low-cost and low-temperature fabrication, such as spin, spray, blade casting, roll-to-roll and ink-jet printing, and laminating [21–24].

The majority of organic neuromorphic systems aim to emulate a single aspect of neuromorphic computing: the synapse. With organic bi- and multistate memories exhibiting memristive behavior, demonstrated as early as the 1970s [25–27], recent interest has resulted in two- and three-terminal memristive synapses, utilizing electronic [28–30] and ionic transport of such devices [31–33].

Biological synapses can be accurately described by a set of nonlinear differential equations [34–36]. While CMOS circuits lose all state information if power is removed, memristive devices can store their state in a non-volatile manner. Bistable, multistate, and continuously variable, two- and three-terminal memristive devices, made from inorganic and organic materials, exhibiting neuromorphic computing with such memristive cross-bar, have already been demonstrated [37–39]. However, a major drawback of these memristive synapses is their limited tunability, and hence their ability to encode and decode complex spatio-temporal encoding associated with biological synapses. In addition, they are often implemented from materials and processes incompatible with transistor technologies, making their integration a challenge. In contrast, complex synaptic models built in electrical circuits afford a large degree of customizability and tunability, for instance, global synaptic weighting or variable time constant [35, 40]. Implementing artificial synapses and somas from the same materials and technologies eases many fabrications constraints. To the best of our knowledge, despite some organic demonstrations to date [29, 41–43], all implemented artificial synaptic circuits have relied on inorganic materials.

In our own group, we have been developing neuromorphic circuits and implementing systems using organic electronics. In contrast to other groups, we have previously demonstrated simple non-spiking neurons, fit with both synapses and somas [44, 45]. We also showed a three-neuron network performing very rudimentary classification, as well as a six-legged walking PaperBot called NUCLEOs (or Neuromorphic Computing on Laminated Electronic Organic substrate), with hybrid organic–inorganic neuromorphic circuitry used to control the robot's movement [46, 47]. However, recognizing the computational and power limitations of non-spiking neural networks, we commenced research aiming to develop spiking neural networks. To this end, we previously demonstrated an organic spiking Axon-Hillock somatic circuit, an early, simple model of an integrate-and-fire (I & F) neural soma [48].

Here, we show a type of biologically realistic spiking synaptic circuit called differential-pair integrator (DPI) synapse that is implemented using physically flexible and biologically compatible complementary organic electronics. The biocompatibility of the materials has been shown in our previously fabricated OFETs [49, 50], albeit the devices in this study are fabricated using a thicker dielectric layer and substrate. We demonstrate that, indeed, the organic synapse converts somatic voltage spikes into linearly proportional output current. We characterize the effects of synaptic parameters, including gain and weighting voltages, V_g and V_w , time constant bias, V_τ , and synaptic capacitance, C_{syn} . We also demonstrate synaptic circuit response when stimulated with input spikes of different frequencies. Synaptic time constants comparable to the time constants of the neuron's membrane potential are critical in distinguishing different temporal input spike patterns. Despite

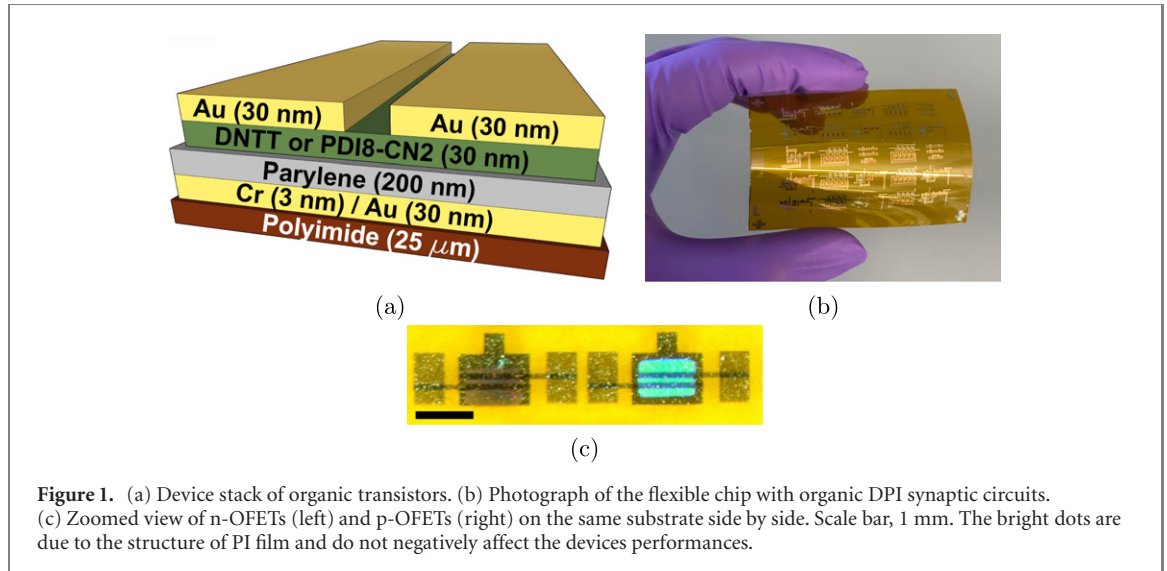


Figure 1. (a) Device stack of organic transistors. (b) Photograph of the flexible chip with organic DPI synaptic circuits. (c) Zoomed view of n-OFETs (left) and p-OFETs (right) on the same substrate side by side. Scale bar, 1 mm. The bright dots are due to the structure of PI film and do not negatively affect the devices performances.

the high operating voltage and current of the circuit that makes any biological interface impossible, the nature, or the shape, of the electrical signals of a biological synapse is compatible with the output of our circuit, and could be interfaced using additional electrical circuits to scale it up or down [51, 52]. We demonstrate that the time constant of our organic spiking synapses can reach in excess of two seconds. We also demonstrate synaptic response due to biologically realistic input voltage spikes. Finally, using custom-made circuit simulation based on transconductances of p- and n-type organic transistors, we show that the fabricated synaptic circuit is in good agreement with simulation-predicted behavior.

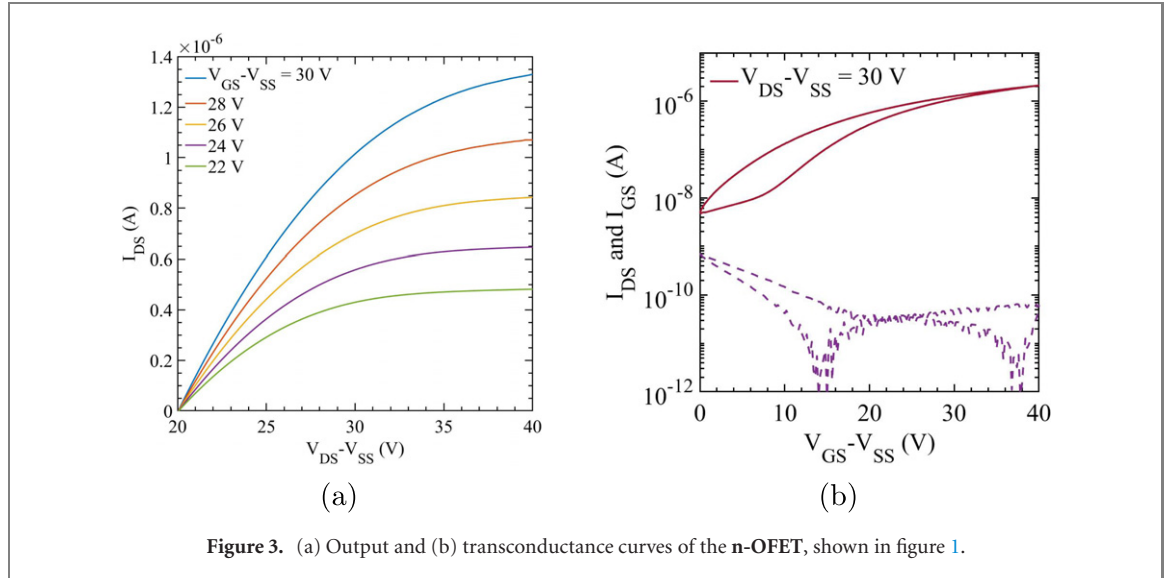
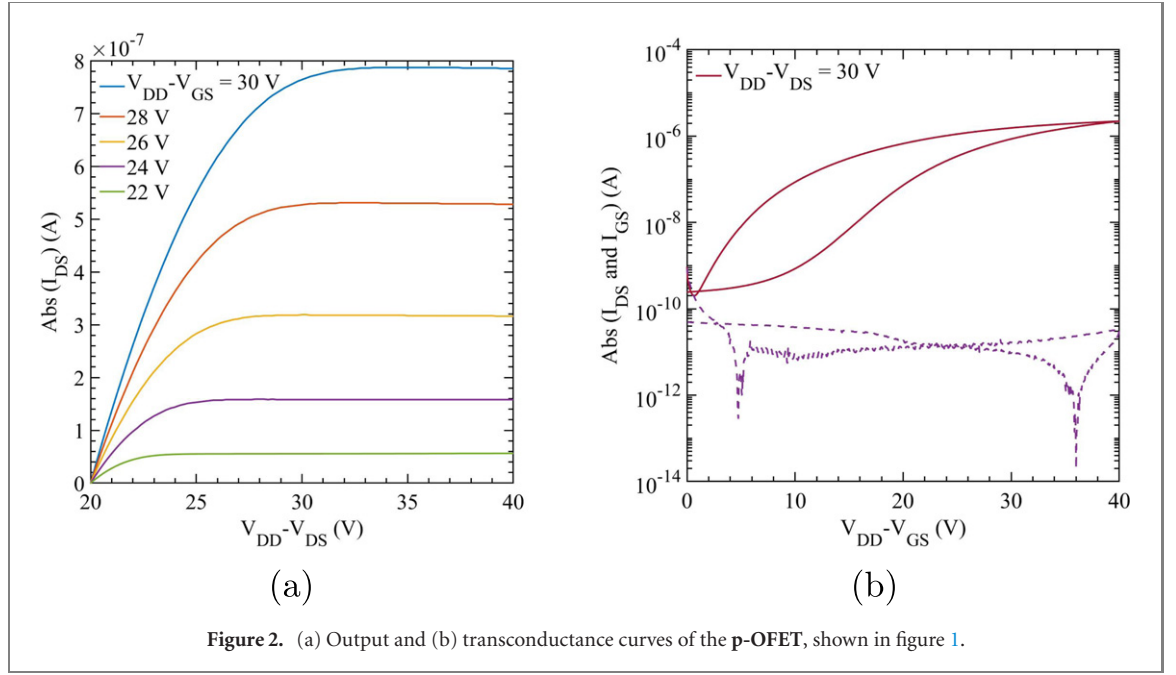
2. Materials and methods

2.1. Materials and equipment

The flexible substrates, 25 μm thick polyimide (PI) films, were purchased from DuPont. The metals—chromium (Cr), gold (Au), and silver (Ag)—were obtained from Kurt J. Lesker Company (KJLC). Parylene diX-SR was given by Specialty Coating Systems (SCS), Inc. and deposited using a SCS LabCoater 3 (PDS 2010) employing the chemical vapor deposition (CVD) process. N,N'-bis(n-octyl)-x,y, dicyanoperylene-3, 4:9, 10-bis(dicarboximide)(PDI8-CN2, also referred to as N1200), and Dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT) were deployed as the n- and p-type organic semiconductors and obtained from Polyera and Sigma-Aldrich, respectively. The source, drain, gate, and active layers were thermally deposited using a NANO 36 thermal-evaporation thin-film deposition system by KJLC. The I - V characterizations were performed using an HP 4155A semiconductor parameter analyzer. A reactive ion etching (RIE) process was deployed to clean the substrate using a Glow Research RIE system. A Thorlabs AMP100 transimpedance amplifier and a National Instrument USB-6343 data acquisition card collected the high-frequency signals with control via National Instrument LabVIEW.

2.2. Fabrication process

The synaptic circuit mainly consists of organic field-effect transistors (OFETs) with top-contact bottom-gate structures. The OFETs are the only elements implemented on the chip to expedite the fabrication process and decrease the procedure's complexity. Figure 1 demonstrates the structure of n- and p-type OFETs (n- and p-OFETs) with photographs of the flexible chip and both types of OFETs. The channel length and width are 100 μm and 1000 μm for both types of devices, respectively. The fabrication starts with cleaning the substrate through 10 min of sonication in isopropanol, followed by the RIE cleaning process for three minutes. A sandwich layer of 3 nm Cr and 30 nm Ag as the gate electrode is thermally deposited at the rate of 0.1 \AA s^{-1} and 1.5 \AA s^{-1} , respectively. Parylene dix-SR is grown using a CVD process as the gate dielectric, resulting in a 200 nm thin film. The active layers, DNTT and N1200, are deposited at the rate of 0.08 \AA s^{-1} and substrate temperatures of 60 $^{\circ}\text{C}$ and 25 $^{\circ}\text{C}$, respectively. Via holes are produced through mechanical removal of the dielectric film. The source and drain electrodes are obtained by deposition of a 30 nm thick layer of Au at the rate of 1.2 \AA s^{-1} . Finally, the 30 nm Au tracks between OFETs are thermally deposited with the same process as the source and drain electrodes. Shadow masking defines the geometry of electrodes, tracks, and active layers.

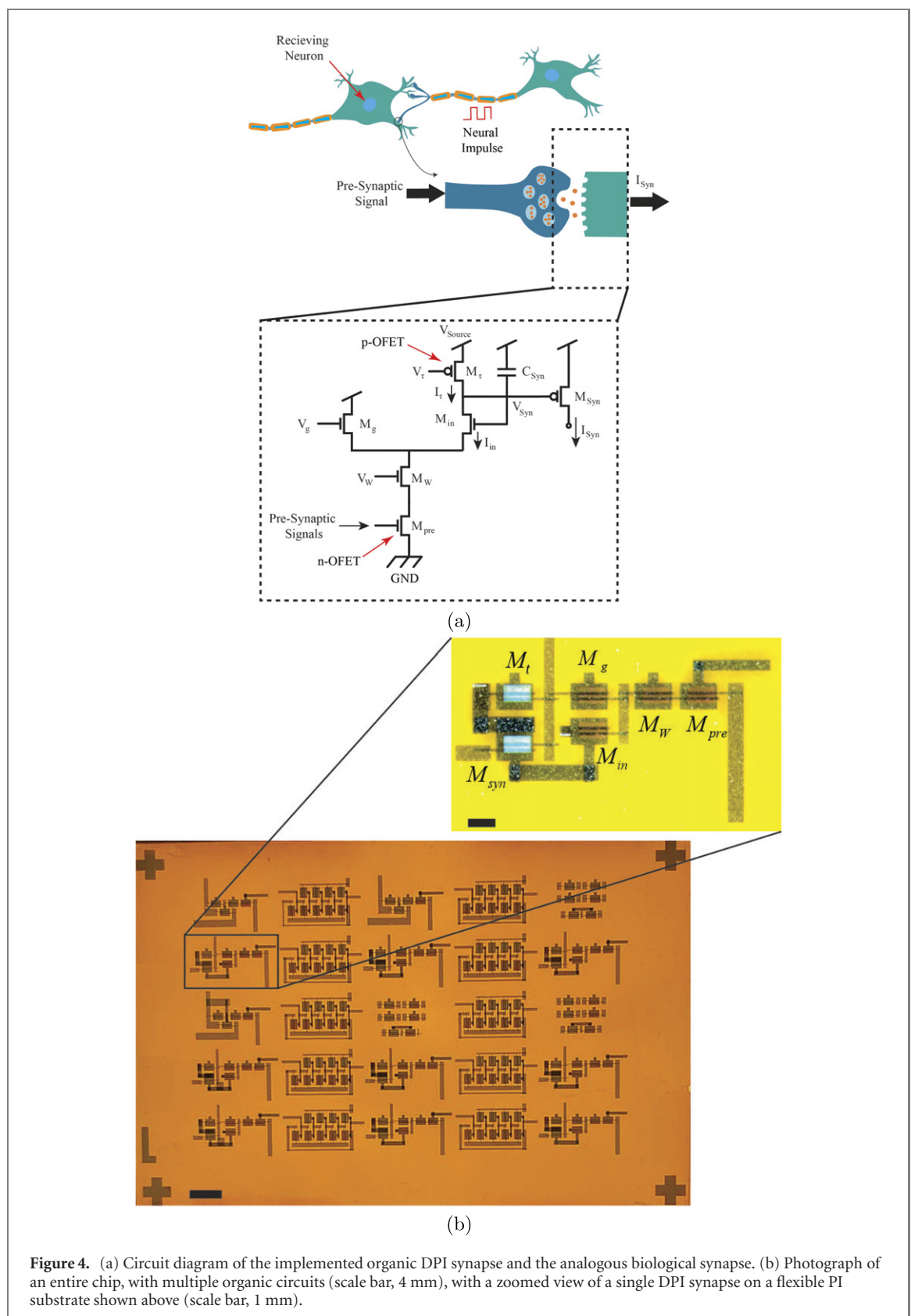


2.3. Characterization of organic transistors

The maximum and minimum voltages that are applied in the circuit characterization are $V_{DD} = 20$ V and $V_{SS} = -20$ V. The applied voltages in experiments are presented with respect to V_{DD} and V_{SS} . Figures 2 and 3 show the characterization results of representative examples of p- and n-OFETs. The carrier mobilities and threshold voltages (V_T) of p- and n-OFETs are $0.27 \text{ cm}^2 \text{ V s}^{-1}$, $V_{DD} - V_T = 18.09$ V, and $0.033 \text{ cm}^2 \text{ V s}^{-1}$, $V_T - V_{SS} = 7.92$ V, respectively. The OFF current of n-OFET (4×10^{-9} A) is larger compared with p-OFET (2×10^{-10} A), adversely affecting the operational regime of the synaptic circuit, as described later in detail.

2.4. DPI synaptic circuit

Synapses are vital for artificial and biological pulse-based neurons to transfer signals and the learning process [53]. Numerous analog synaptic circuits have been proposed to mimic the spatiotemporal behavior of a biological synapse. However, the temporal behavior of biological synapses has often been neglected [35]. Indiveri *et al* presented a current-mode synaptic circuit, including a DPI that allows the circuit to achieve the functionality of log-domain first-order low-pass filters. Additionally, the circuit has the advantage of tunable gain (V_g) independently from the time constant. The tunable gain acts globally and scales the weights of a cluster of DPI synapses afferent onto one post-synaptic neuron to implement homeostatic plasticity stabilizing mechanisms. The gain voltage forms an ensemble of strategies to control the overall stability of the network [54].



The DPI synapse offers exponential dynamics of pre- and post-synaptic currents of real synapses. More importantly, the circuit can obtain a plausible time constant with a relatively small capacitor [10, 34, 55].

Figure 4 demonstrates the schematic of the DPI synapse with the analogous biological synapse beside a photograph of the fabricated organic circuit. The DPI synaptic circuit operates in the subthreshold regime and is comprised of four n-OFETs, two p-OFETs, and a single capacitor. Assuming OFETs' subthreshold operation, DPI synaptic circuit behavior can be described as follows: the input voltage signal activates the n-type M_{pre} and

Table 1. Theoretical time constants according to equation (1) with $\kappa = 0.0379$.

C_{syn} (nF)	$V_{\text{DD}} - V_{\tau}$ (V)	I_{τ} (nA)	τ_{theo} (ms)
33	9	18.9	1152
47	9	18.9	1640
68	9	18.9	2373
47	8.9	17.8	1741
47	9.1	19.6	1581

allows the synaptic capacitor (C_{syn}) to discharge, V_{syn} decreases with a rate set by $I_{\text{in}} - I_{\tau}$, and I_{syn} increases exponentially. M_{τ} recharges C_{syn} linearly to V_{Source} by deactivating the input voltage signal, and I_{syn} decreases back to the leakage current. M_{τ} and M_{W} are subthreshold current sources in the circuit. The maximum amplitude of I_{syn} is set by three parameters: V_{W} , V_{g} , and V_{τ} . The weighing voltage (V_{W}) can be adjusted locally to implement learning and plasticity, and the gain voltage (V_{g}) is an extra degree of freedom to implement global plasticity mechanisms.

2.5. Time constant

The temporal dynamics of a pulse-based (spiking) neural network play an important role in decoding spatiotemporal patterns of spikes and learning neural codes [56]. However, modeling the temporal behavior of each synapse in a network of leaky integrate-and-firing (I & F) neurons is a resource-intensive process and needs a large area in very large-scale integration implementation [57]. Synapses in I & F neurons can identify the difference between temporal input spiking patterns only when they have a time constant close to the time constant of the membrane potential of the neurons [58].

A subthreshold DPI synaptic circuit offers a long and biologically plausible time constant (tens of milliseconds) while a small and compact capacitor is deployed. The time constant linearly depends only on synaptic capacitance and I_{τ} , as shown in equation (1) [34],

$$\tau = \frac{C_{\text{syn}} \times U_{\text{T}}}{\kappa \times I_{\tau}} \quad (1)$$

where U_{T} represents the thermal voltage, C_{syn} denotes the synaptic capacitance, I_{τ} is the current from M_{τ} , and κ is the subthreshold slope factor. The synaptic capacitances are 33 nF, 47 nF, 68 nF, with a thermal voltage of 25 mV. I_{τ} is a tunable value controlled through V_{τ} and estimated using figure 2(b). κ is an intrinsic property of field-effect transistors that is determined from the slope of the transconductance curve in the subthreshold regime. The subthreshold slope factor of OFETs is one order of magnitude smaller than MOSFETs due to slower carrier-charge mobilities. The κ value is measured at 0.0379 for p-OFETs. Table 1 summarizes the parameter values in this paper, and the theoretical time constants (τ_{theo}) are calculated according to equation (1).

The time constant can be estimated from experimental measurements and validated the theoretical values. The experimental time constant (τ_{exp}) is estimated using the measured step response of the DPI synaptic circuit fitting the data with an exponential equation. Equation (2) demonstrates the exponential relationship between the synaptic current and the time constant

$$I_{\text{syn}} = \begin{cases} a + b \times e^{-\frac{t}{\tau}} & \text{charge phase} \\ c \times e^{-\frac{t}{\tau}} & \text{discharge phase.} \end{cases} \quad (2)$$

3. Results and discussion

3.1. DPI synaptic circuit characterization

A series of experiments have been designed and implemented to validate τ_{theo} , theoretical time constant values calculated in section 2.5 and show the DPI circuit's functionalities. Sections 3.3 and 3.2 show the role of weighing (V_{W}) and gain (V_{g}) voltages in the DPI circuit, respectively. They either amplify or attenuate the output signal while not affecting the time constant. The effects of synaptic capacitance (C_{syn}) and the time-constant bias (V_{τ}) are discussed in sections 3.5 and 3.4 according to equation (1). C_{syn} and I_{τ} are linearly proportional to the time constant that has been estimated in a broader range using an extrapolation. Section 3.6 presents the i - f curves of the DPI synapse. Finally, the circuit's response to a train of simulated tonic spikes has been demonstrated in section 3.7.

To ease the analysis of circuit behavior, input voltage signal is simulated using a square wave altering between ± 20 V to turn the circuit ON and OFF. The amplitude of the input voltage signal is determined

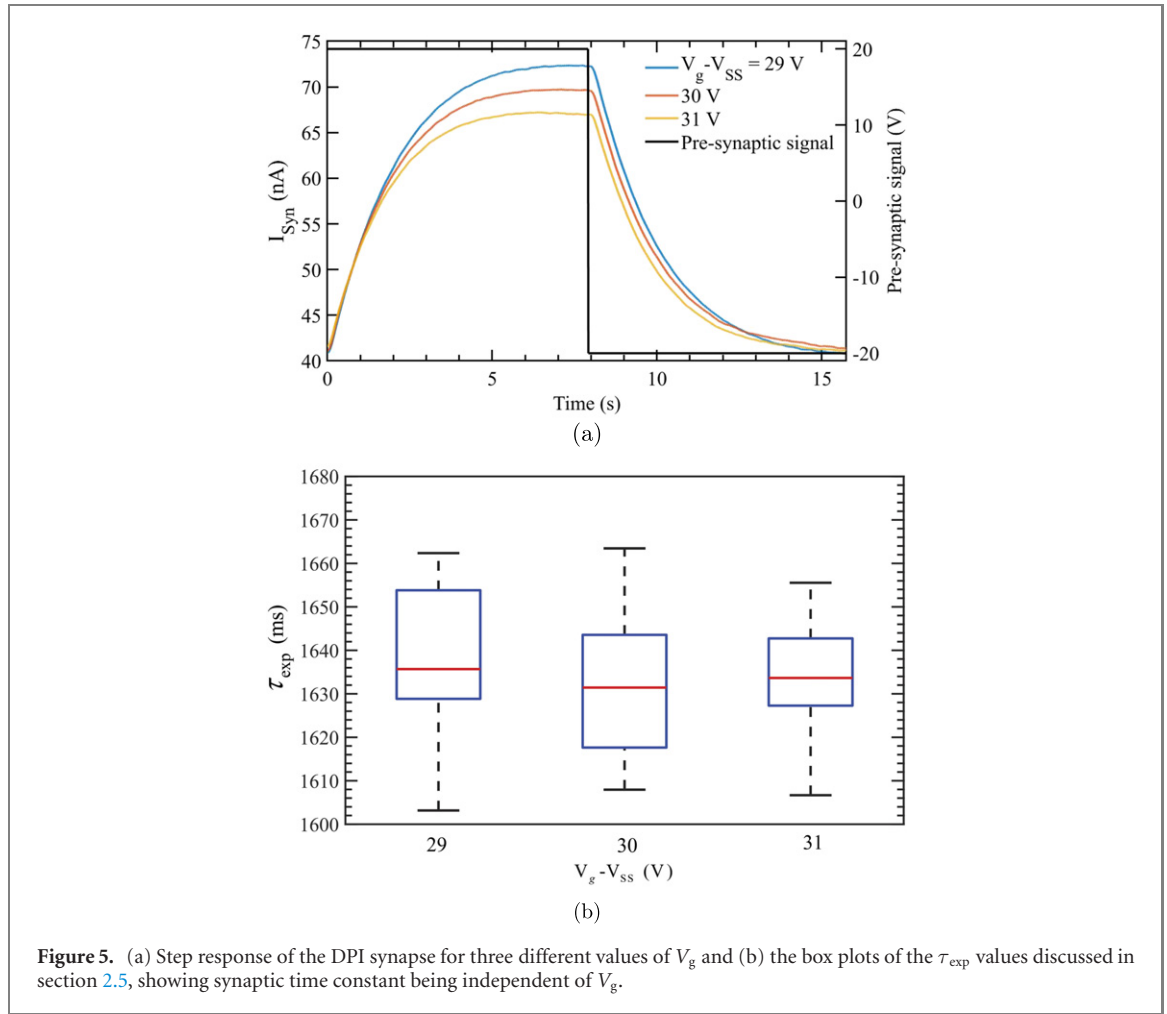


Figure 5. (a) Step response of the DPI synapse for three different values of V_g and (b) the box plots of the τ_{exp} values discussed in section 2.5, showing synaptic time constant being independent of V_g .

Table 2. Experimental parameters regarding figure 5.

C_{syn} (nF)	V_{Source} (V)	$V_{DD} - V_T$ (V)	$V_W - V_{SS}$ (V)	$V_g - V_{SS}$ (V)
47	10	9	7	29, 30, 31

Table 3. Statistical results regarding figure 5(b).

$V_g - V_{SS}$ (V)	Min (ms)	Max (ms)	Median (ms)	Mean (ms)	τ_{theo} (ms)
29	1603	1662	1633	1634	1640
30	1608	1664	1631	1632	
31	1607	1656	1637	1635	

by the n-OFET characterization results presented in figure 3(b). The period of the input signal is constant, 16 s, through sections 3.2 to 3.6. The power supply voltage (V_{Source}) is constant, 10 V, in all the experiments.

The experimental time constant is estimated for every step response of the DPI synaptic circuit; therefore, the number of steps (cycles) determines the number of time constants estimated in an experiment. Eighteen cycles have been captured for every experiment, and the results are shown through box plots.

3.2. Gain voltage

The gain voltage (V_g) is the DPI's one extra degree of freedom compared to the LDI synaptic circuit [34, 59]. V_g nonlinearly affects the amount of integrated I_{in} and, consequently, amplifies or attenuates the synaptic current. Figure 5(a) illustrates the step response of the DPI synaptic circuit with three different V_g values. The τ_{exp} values are demonstrated in figure 5(b) using box plots. Table 2 shows the experimental parameters, and table 3 summarizes the statistical data regarding figure 5(b).

According to section 2.5, the theoretical time constant is estimated to be 1640 ms for the experimental parameters shown in table 2. Figure 5(b) shows that the time constant is independent of the gain voltage;

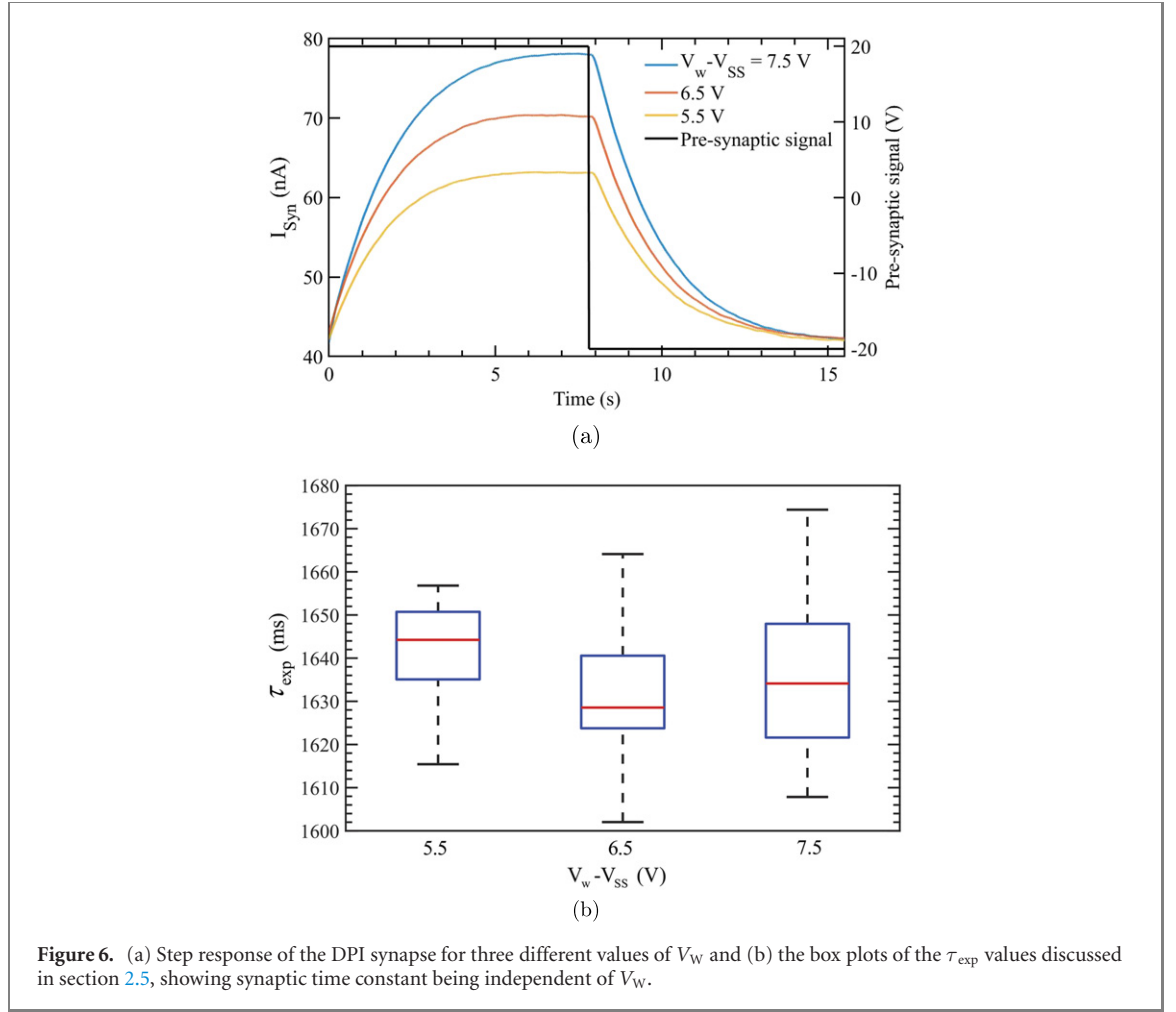


Figure 6. (a) Step response of the DPI synapse for three different values of V_W and (b) the box plots of the τ_{exp} values discussed in section 2.5, showing synaptic time constant being independent of V_W .

Table 4. Experimental parameters regarding figure 6.

C_{syn} (nF)	V_{Source} (V)	$V_{\text{DD}} - V_{\tau}$ (V)	$V_W - V_{SS}$ (V)	$V_g - V_{SS}$ (V)
47	10	9	5.5, 6.5, 7.5	30

Table 5. Statistical results regarding figure 6(b).

$V_W - V_{SS}$ (V)	Min (ms)	Max (ms)	Median (ms)	Mean (ms)	τ_{theo} (ms)
5.5	1615	1654	1637	1638	1640
6.5	1602	1664	1629	1631	
7.5	1608	1674	1636	1636	

however, the experimental results present a range of values, with the theoretical time constant between the 25th and 75th percentiles. Two factors cause this discrepancy. First, the OFET characterization results show hysteresis [60] that affects the results during data collection. Second, as previously discussed, the estimation method is intrinsically an error-prone process [59].

3.3. Weighing voltage

The weighing voltage (V_W) locally modulates the synaptic current amplitude. M_W works as a subthreshold current source, and I_W needs to be much greater than I_r to allow the DPI circuit to operate as a linear first-order filter. Figure 6(a) demonstrates the step response of the DPI synaptic circuit to three V_W values. The τ_{exp} values are shown in figure 6(b) using box plots. Table 4 shows the experimental parameters, and table 5 summarizes the statistical data regarding figure 6(b).

Figure 6(b) confirms that the weighing voltage does not affect the time constant; however, the box plots show a range of time-constant values compared with the theoretically calculated values shown in section 2.5

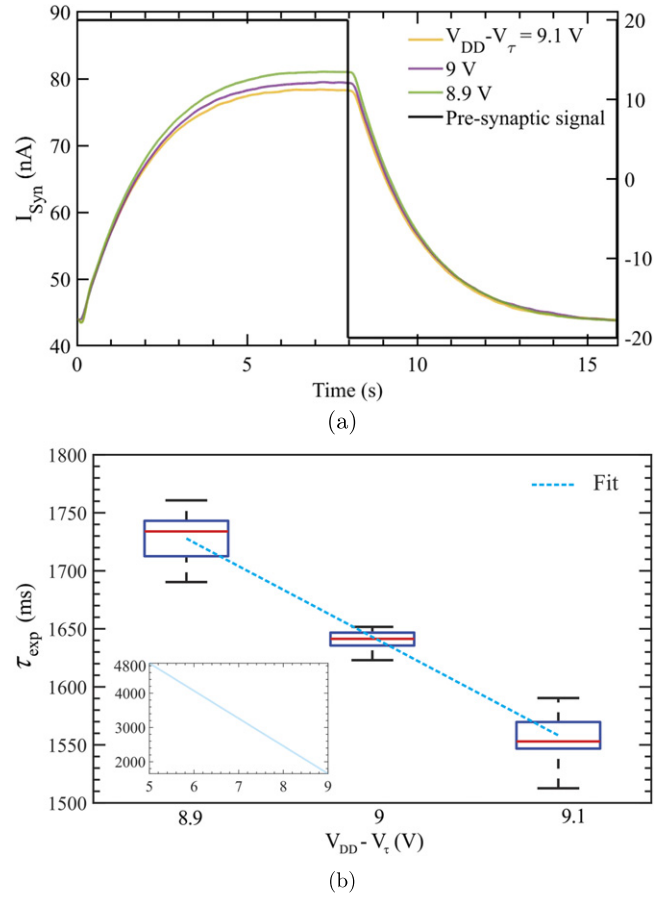


Figure 7. (a) Step response of the DPI synapse for three different values of V_{τ} and (b) the box plots of the τ_{exp} values discussed in section 2.5, showing time constant being dependent on V_{τ} . The inset indicates extrapolated values.

Table 6. Experimental parameters regarding figure 7.

C_{syn} (nF)	V_{Source} (V)	$V_{\text{DD}} - V_{\tau}$ (V)	$V_{\text{W}} - V_{\text{SS}}$ (V)	$V_{\text{g}} - V_{\text{SS}}$ (V)
47	10	8.9, 9, 9.1	7	30

Table 7. Statistical results regarding figure 7(b).

$V_{\text{DD}} - V_{\tau}$ (V)	Min (ms)	Max (ms)	Median (ms)	Mean (ms)	τ_{theo} (ms)
8.9	1690	1761	1734	1731	1741
9	1623	1652	1639	1638	1640
9.1	1513	1590	1553	1554	1581

(1640 ms). The hysteresis mechanisms and the estimation method's error are two main reasons for the discrepancy.

3.4. Time-constant bias

The time-constant bias (V_{τ}) is a parameter that allows explicit control of the circuit's time response. M_{τ} is a subthreshold current source in the DPI synaptic circuit that charges the synaptic capacitor when M_{pre} is OFF. Increasing $V_{\text{DD}} - V_{\tau}$ leads to a smaller V_{GS} of p-type M_{τ} and increases I_{τ} , consequently decreasing the time constant. Figure 7(a) presents the step response of the DPI synaptic circuit to three V_{τ} values. Box plots present the estimated time in figure 7(b). Table 6 shows the experimental parameters, and table 7 summarizes the statistical data regarding figure 7(b).

Table 7 shows that the τ_{theo} values of 1741 ms, 1640 ms, and 1581 ms are within the 25th to 75th percentiles of the boxplots in figure 7(b). The measurements present a range of time constants resulting from errors in the estimation method and the hysteresis mechanisms.

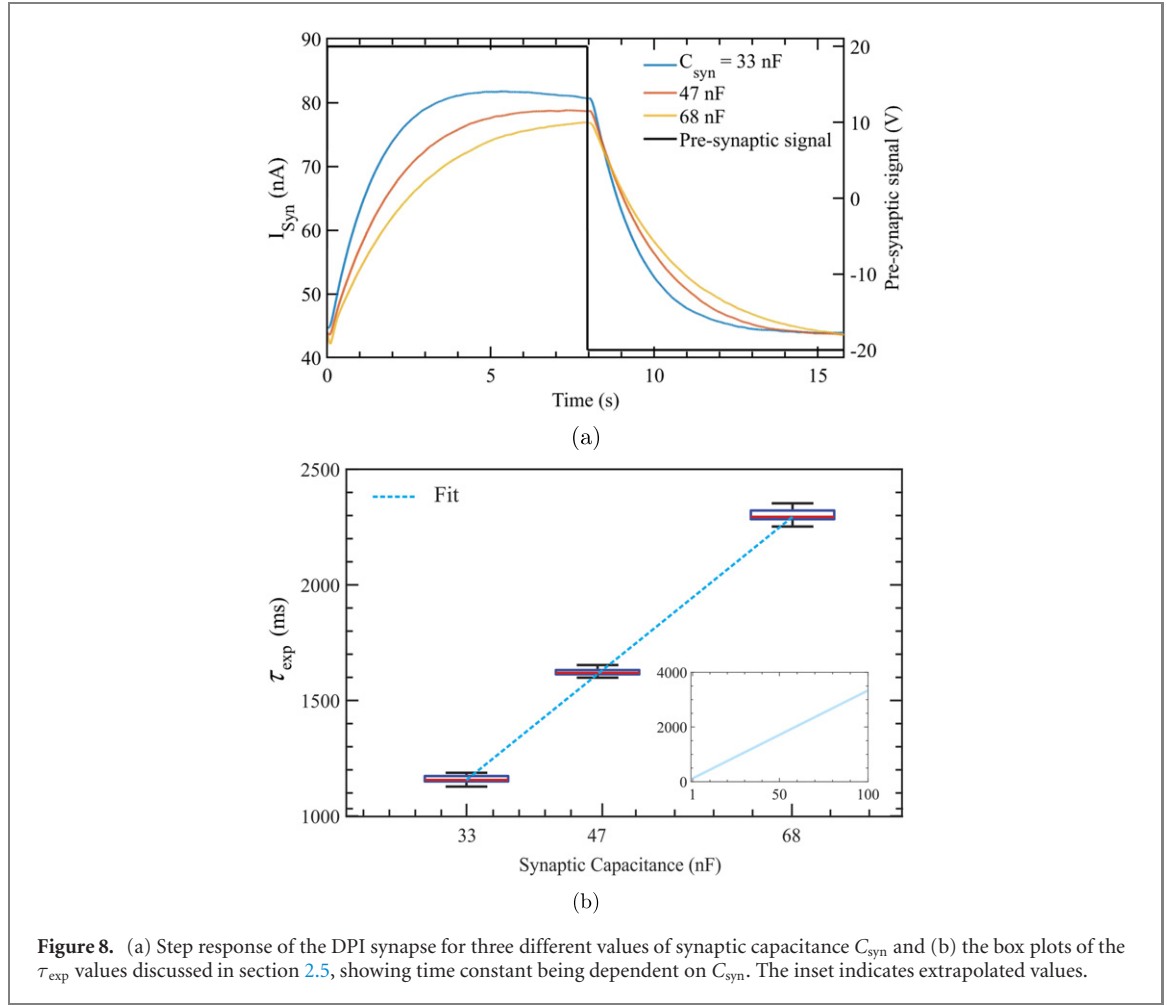


Figure 8. (a) Step response of the DPI synapse for three different values of synaptic capacitance C_{syn} and (b) the box plots of the τ_{exp} values discussed in section 2.5, showing time constant being dependent on C_{syn} . The inset indicates extrapolated values.

Table 8. Experimental parameters regarding figure 8.

C_{syn} (nF)	V_{Source} (V)	$V_{\text{DD}} - V_{\text{T}}$ (V)	$V_{\text{W}} - V_{\text{SS}}$ (V)	$V_{\text{g}} - V_{\text{SS}}$ (V)
33, 47, 68	10	9	7	30

Table 9. Statistical results regarding figure 8(b).

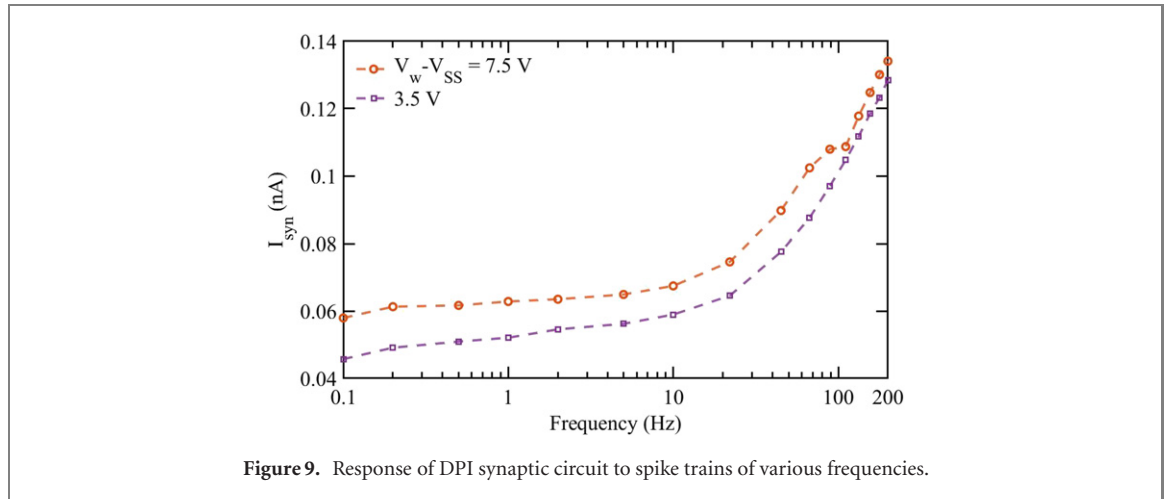
C_{syn} (nF)	Min (ms)	Max (ms)	Median (ms)	Mean (ms)	τ_{theo} (ms)
33	1128	1187	1156	1158	1152
47	1599	1653	1617	1619	1640
68	2252	2353	2298	2304	2373

The τ_{exp} values allow us to extrapolate the results and estimate the time constant for different V_{T} values. The inset of figure 7(b) demonstrates the extrapolation results according to a fitted line to the median of the time constants $\tau_{\text{exp}} = -905.5 \times (V_{\text{DD}} - V_{\text{T}}) + 9792.3$, with values as high as 4800 ms.

3.5. Synaptic capacitance

The time constant is proportional to the synaptic capacitance (C_{syn}). One of the advantages of the DPI synaptic circuit over other log-domain integrator synapses is its ability to produce a more extended response using smaller synaptic capacitors. However, in this study, a relatively large capacitor is deployed to mitigate the effect of hysteresis in the circuit and remove the parasitic capacitance caused by the test setup. Figure 8(a) shows the step response of the DPI synaptic circuit to three synaptic capacitance values, namely 33 nF, 47 nF, and 68 nF. The τ_{exp} values are displayed in figure 8 using box plots. Table 8 demonstrates the experimental parameters, and table 9 summarizes the statistical data regarding figure 8(b).

Statistical results shown in table 8 (of figure 8(b)) show that the theoretical time constants (τ_{theo}) are within the maximum and minimum τ_{exp} values. The deviation of τ_{exp} values from theory is most likely due to the



hysteresis mechanisms that trap more carrier charges due to a higher value capacitance and, consequently, affect the change in the time constant over time.

The inset of figure 8(b) shows the extrapolation of results in a range of 1 nF to 100 nF. The relationship between synaptic capacitance and the median of the τ_{exp} values is described as $\tau_{\text{exp}} = 32.48 \times (C_{\text{syn}}) + 87.48$ and indicates values as high as 3400 ms.

3.6. Frequency response

To summarize the organic DPI synapse dynamics in a single picture, the mean of the synaptic current in response to spike trains of square pulses of increasing frequency has been measured. Figure 9 demonstrates the average current-frequency (i - f) curve of the circuit in a range of 0.1 to 200 Hz that covers typical biological spiking frequencies. The results show that the mean of the synaptic current is linear and that synaptic input frequencies higher than 10 Hz can be extended beyond the plot. Also, the results show that the mean synaptic current remains almost constant for frequencies lower than 10 Hz but increases for higher frequencies. Increasing $V_w - V_{\text{SS}}$ elevates the current's levels but maintains unchanged slope.

3.7. The response to simulated biological spikes

Our previous synaptic circuit analysis used square voltage pulses to approximate presynaptic input to simplify the analysis of the synaptic output current. However, in order to elucidate synaptic response to nonideal but more realistic presynaptic input, we used a mathematically derived bio-inspired model to generate the input voltage spikes for the organic DPI synaptic circuit. We built on top of our prior work regarding the hyperbolic model of the neuronal spiking patterns [61] and applied adjustments in real time to suit the organic synapses relevant to this study.

This model is an extension of prior biological models, such as the Izhikevich model [62] and the adaptive exponential I & F model [63], with fewer parameters, less computational cost, and faster upswing, capable of generating different spiking patterns [61]. Hyperbolic functions are known for their extensive applications in solving differential equations. The model is, thus, constructed as a partial differential equation with hyperbolic functions involved, and parametrized to allow for the generation of various spiking patterns:

$$\frac{dV}{dt} = \alpha \cosh\left(\frac{V - V_{\text{rest}}}{\beta} - 1\right) - \epsilon - u + I \quad (3)$$

$$\frac{du}{dt} = a(b \times V - u). \quad (4)$$

Equation (3) indicates that the membrane potential (V) of a neuron can be modeled as a differential equation. In equations (3) and (4), u represents the membrane-recovery variable. The input current I of this model is considered the output of the synaptic circuit. Biologically, the current represents the ionic movement through cell gates (inward calcium and sodium ionic velocity). If current I is present, the membrane voltage increases and produces spiking patterns, after which it reaches a certain threshold (i.e., +30 mV) and resets to a resting value of V_{rest} . At this point, a delay is added to the membrane-recovery variable u , as denoted in equation (5):

$$\text{if } V \geq 30, \quad \text{then:} \begin{cases} V = c \\ u = u + d. \end{cases} \quad (5)$$

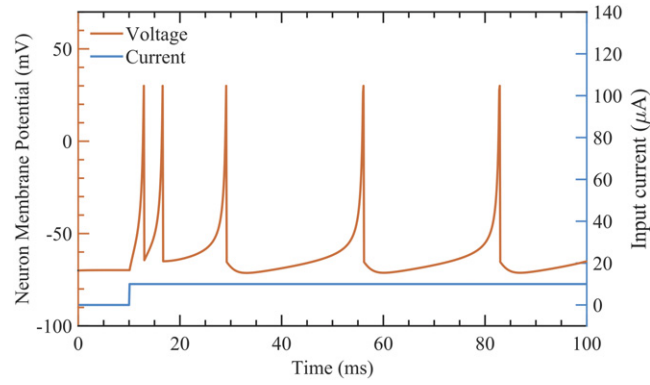


Figure 10. Tonic spike pattern generated from the hyperbolic model.

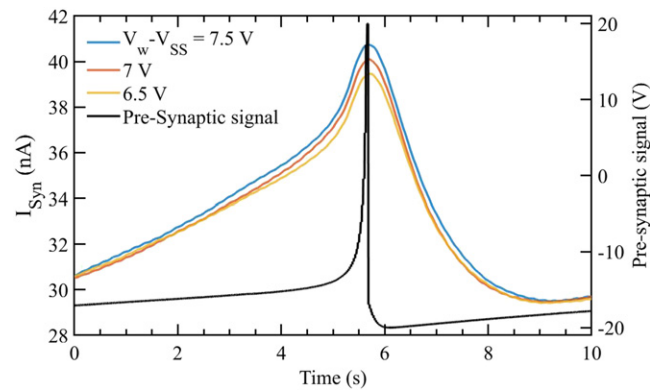


Figure 11. Response of DPI synaptic circuit to a single simulated biological spike, with three different values of V_W .

Table 10. Experimental parameters regarding figure 11.

C_{syn} (nF)	V_{Source} (V)	$V_{DD} - V_T$ (V)	$V_W - V_{SS}$ (V)	$V_g - V_{SS}$ (V)
33	10	9	6.5, 7, 7.5	30

The insulation of the cell membrane surrounding a neuron is considered a capacitor, which is defined by α in equation (3). Parameter β can determine the sharpness of the spikes, and ϵ is an empirically defined parameter related to the general gate voltage of inward calcium and sodium and outward potassium currents. The rate of the spikes, as well as their resting and peak times, can be determined by equation (4).

To observe the response of a single neuronal spiking pattern on the organic DPI synapse, the regular (tonic) spiking pattern is originally generated. For this, the following settings are used: $\alpha = 75\,000$, $\beta = 1000$, $V_{rest} = -62.5$ mV, $\epsilon = 16$, $a = 0.2$, $b = 0.02$, $c = -65$, $d = 6$, and I is a step signal \square switching from 0 to $14\,\mu\text{A}$. Initially, V is set to -70 mV. See figure 10.

The regular spiking-pattern neurons are the major type present in the cortex. If a DC-step is provided at the input current I , biologically, the neurons will produce a few (e.g., two) firing spikes with short interspikes before reaching their resting potential, after which the period of the spikes increases [62]. The hyperbolic model, in addition to allowing various spiking patterns to be generated by parameter adjustments, allows for modulating the frequency of the spikes by changing the strength of the DC current I . The frequency of the spikes is proportional to I in the model.

For real-time hardware generation of the spiking patterns, the model was emulated on a LabVIEW controlled DAQ. The dt value of the model denotes the division of time, or time steps, of the calculations (and output voltage signals) being updated. By fully eliminating the need for any vectorization or storage of array elements over time steps, and only updating V and u every dt , the computational complexity is significantly reduced and, hence, the real-time nature of the model as well. For the purpose of this real-time experiment and the stability of the computations, as well as the need to generate several seconds of data, dt has been set to 0.1 ms.

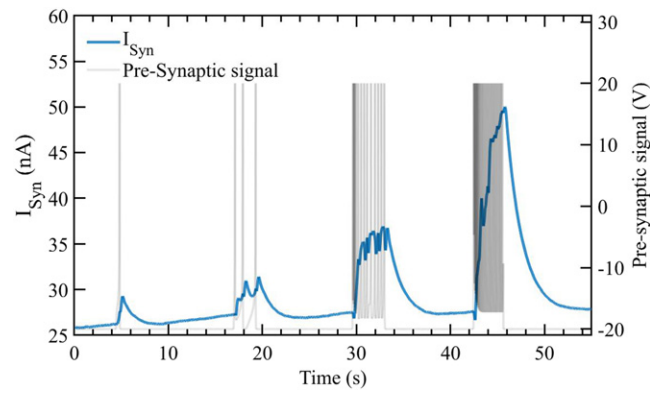


Figure 12. Response of DPI synaptic circuit to a series of simulated biological spike trains of increasing frequencies.

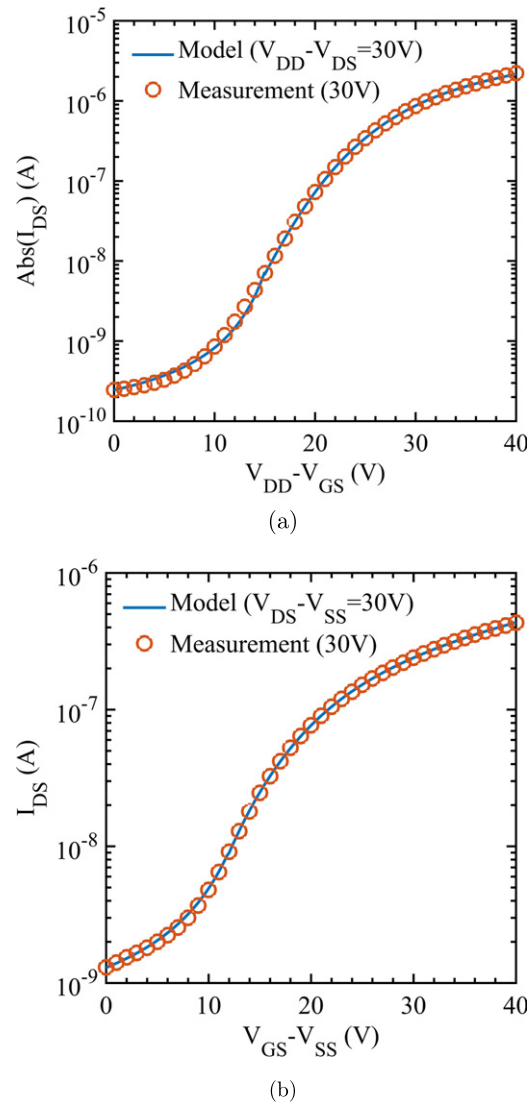


Figure 13. Comparison between the simulated and experimentally measured transconductance curves for the (a) **p-type** organic transistor and the (b) **n-type** organic transistor shown in figures 2 and 3.

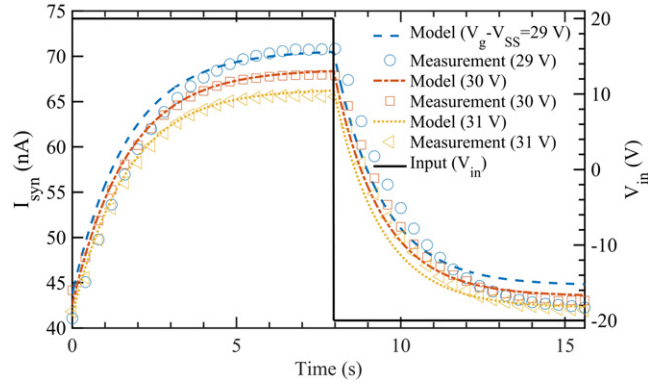


Figure 14. Comparison between the simulated and the experimentally measured step responses of the DPI synapse for three different values of V_g before the pre-synaptic input voltage.

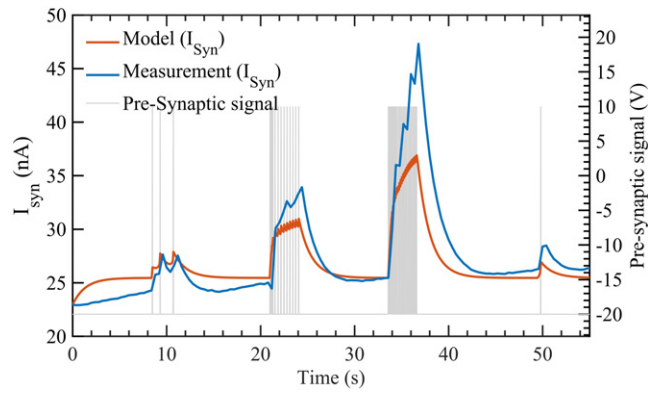


Figure 15. Comparison between the simulated and experimentally measured response of the DPI synapse to a series of simulated biological spike trains of increasing frequencies.

Voltage scaling is required for the somatic voltages of the neuronal spikes that range between approximately -70 mV and $+30$ mV (see figure 10) to be compatible with the organic synaptic circuit in the range of ± 20 V. The voltage value V generated in each time step of the model is, thus, scaled with a gain of 394.32 and an offset of 8170.347:

$$V_{\text{scaled}} = \text{gain} \times V + \text{offset}. \quad (6)$$

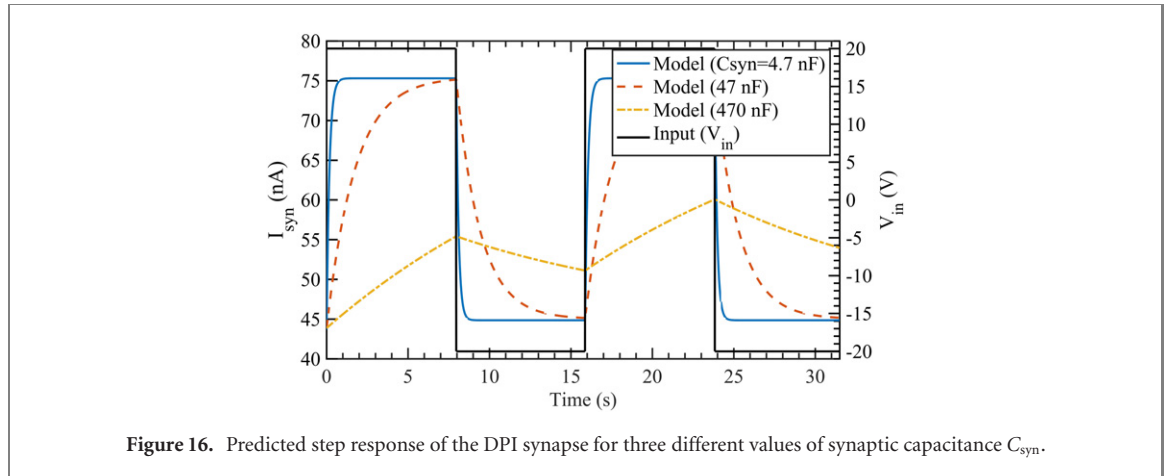
The real-time implementation of the model allows for parameter adjustment and/or frequency modulation of the neuronal spikes on the fly as the spikes (actual voltages) are being generated and delivered on the DAQ.

Figure 11 demonstrates the response of the DPI synaptic circuit to a single spike for three $V_W - V_{SS}$ values. As shown in section 3.3, V_W modulates the circuit output's amplitude. The experimental parameters are shown in table 10. Increasing the value of $V_W - V_{SS}$ leads to elevating the peak of the synaptic current.

The response of the circuit to four sets of tonic spikes with different frequencies is shown in figure 12, with experimental parameters shown in table 10 with a constant value of $V_W - V_{SS} = 7$ V. The high-frequency spikes simulate a tetanized state when a motor neuron maximally stimulates its motor unit for a given period [64]. Starting the spikes, the synaptic current reaches its peak exponentially, and a train of high-frequency spikes increases the maximum amount of current in time. As the input spikes terminate, the current returns to the leakage level in a period equal to the time constant.

3.8. Simulation versus emulation

Simulation is often used to predict the behavior of a complicated system and, so far, studies concerned with modeling neuromorphic systems have been mostly restricted to silicon-based neuronal circuits. Therefore, we developed a custom-built circuit simulation that reflects idiosyncrasies of organic transistors to deepen understanding of the organic synaptic circuit and expedite its characterization (e.g., the choice of C_{syn}) [65]. The response of an organic synaptic circuit is simulated by emulating the function of the circuit's individual organic transistors based on a compact model. From figure 13, it can be found that the simulated transconductance of both p- and n-OFETs matches well with the experimentally characterized transconductance curves,



which indicates that the transistor model in our circuit simulator can reflect the real dynamics of the built transistor blocks, not only in the above-threshold regime, but also in the subthreshold regime.

Figure 14 demonstrates a comparison between the simulated and experimentally measured step responses of the DPI synapse for three different values of V_g . As can be seen in this figure, the simulated synaptic response curves at three different V_g values are in good agreement with the experimental measurements. This observation further illustrates the effectiveness of our organic synaptic circuit simulation. In a more realistic trial, as described in section 3.7, a series of simulated biological spike trains were fed simultaneously into our circuit simulator and a real DPI synaptic circuit, and their post-synaptic outputs are presented in figure 15. It can be seen that the simulated post-synaptic current in response to irregular pre-synaptic spike patterns can exhibit similar evolving trends to those shown in the real synaptic circuit. However, the shape of the simulated and experimentally measured post-synaptic currents is not identical to the pre-synaptic spikes. This inconsistency between simulated and actual measured data in terms of post-synaptic current shape can be attributed to the hysteresis observed in fabricated organic transistors. As displayed in figures 2 and 3, there is generally a considerable discrepancy between the transconductance measured by forward and reverse sweeps. The transistor parameters in our simulation are only adjusted according to the reverse sweep, hence it can only reflect the dynamic characteristics of the transistor within certain limits. When the waveform or the input spiking patterns become irregular (e.g., from a pure square wave in figure 14 to a series of biological spike trains in figure 15), the inaccuracy of the model parameters caused by the hysteresis effect of the transistor will be accumulated or even magnified, leading to some inconsistency between simulation results and experimental observations.

While circuit simulation can only predict a limited range of synaptic circuit responses with great accuracy, we can still use simulation to analyze the impact of some parameters on the overall performance of a circuit in advance, thus improving the efficiency of electronic-design automation. For instance, the predicted step response of the DPI synapse for three different values of C_{syn} is shown in figure 16. We can see that the post-synaptic current I_{syn} rises more slowly with increasing C_{syn} , implying that a larger charging time constant is rendered for a larger synaptic capacitance selected. Furthermore, we can roughly estimate the theoretical time constants from the simulated step response, in this case $\tau_{sim} = 260, 1,650$ and $15,600$ ms, which indeed satisfies the linear relationship between τ and C_{syn} , obtained by fitting the experimental data.

4. Conclusion

Neuromorphic systems are biologically inspired hardware implementations of artificial neural networks that require two main functional blocks: artificial *somas* and artificial *synapses*. While somas integrate synaptic currents and produce a voltage spikes, the main functions of synapses include interfacing between individual neurons (somas), scaling the input signal, and converting the voltage spike into a synaptic current.

In contrast to two-terminal memristive devices used to approximate synaptic weighting, synaptic circuits offer advantages, including greater synaptic control (via individually tunable parameters, such as V_g , V_W , V_τ , and C_{syn}) and integration with circuits that implement other synaptic neuromorphic functions (e.g., short-term depression or short-term potentiation, voltage-gated channels, synaptic conductances), as well as fabrication integration with other neuromorphic blocks, such as somas.

Here, we show a type of biologically realistic spiking synaptic circuit, called a DPI synapse, which is implemented using physically flexible and biologically compatible complementary organic electronics. We demonstrate that, indeed, the organic synapse converts somatic voltage spikes into proportional output current.

We characterize the synaptic parameters, including the gain and weighting voltages V_g and V_w , the time-constant bias V_T , and synaptic capacitance C_{syn} . We also demonstrate the synaptic circuit response when stimulated with input spikes of different frequencies. Synaptic time constants comparable to the time constants of the neuron's membrane potential are critical in distinguishing different temporal input spiking patterns. We show that the time constant of our organic spiking synapses can reach in excess of two seconds. We demonstrate the synaptic response due to biologically realistic input voltage spikes of various frequencies. Finally, we via custom-build circuit simulation based on transconductances of p- and n-type organic transistors, that the fabricated synaptic circuit is in good agreement with simulation-predicted behavior. This work paves the way for future networks of fully organic neurons and their networks.

Acknowledgments

This work was partially supported by the Purdue Polytechnic's Realizing the Digital Enterprise graduate fellowship and the Office of Naval Research Young Investigator Program, Award No. N00014-21-1-2585. The authors would also like to acknowledge the help of Prof. Ramses Martinez, Prof. Walter Daniel Leon-Salas, Prof. Saeed Mohammadi, and Prof. Richard Voyles from Purdue University, as well as Mark Veith from SCS, for their help in device fabrication, data analysis, and fruitful discussions.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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