

# **Update on Ara**

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# Scaling

- #Lanes
- Data width
- Data type

fmatmul, 128x128x128

Lanes	Efficiency (GOPS/W)
2	30.09
4	34.33
8	?



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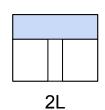
# Scaling

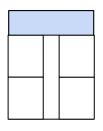
- #Lanes
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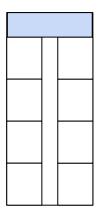
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**CVA6 Power is ~constant** 





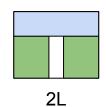


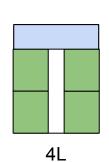
8L

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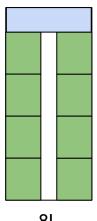
**CVA6 Power is ~constant ∑(Lane Power) ~doubles** 





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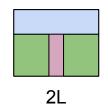


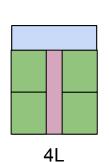
## Scaling

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CVA6 Power is ~constant

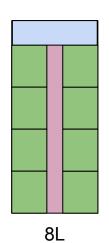
∑(Lane Power) ~doubles
Ara non-lane power?





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fmatmul, 128x128x128

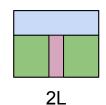
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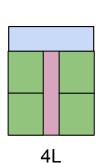
CVA6 Power is ~constant

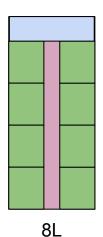
∑(Lane Power) ~doubles

Ara non-lane power?

## SLDU, MASKU, VLSU

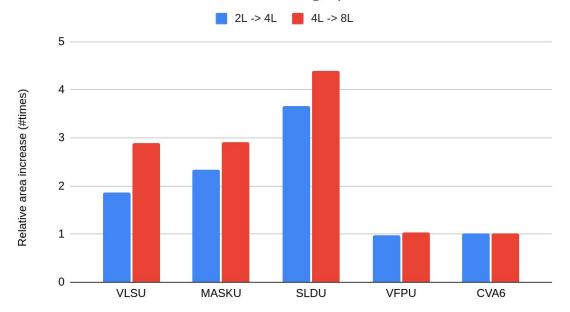








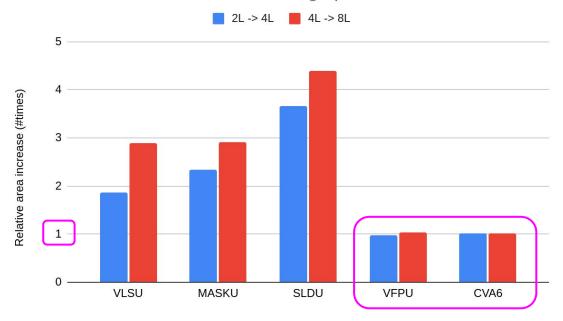
Relative area increase when scaling up



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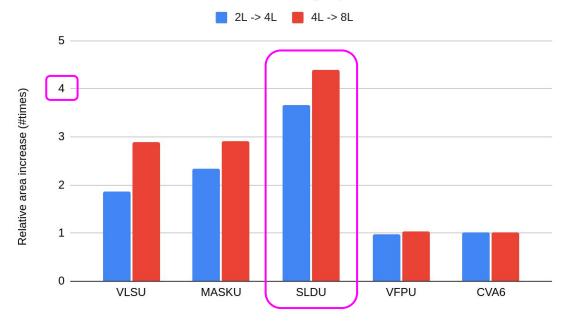


Relative area increase when scaling up



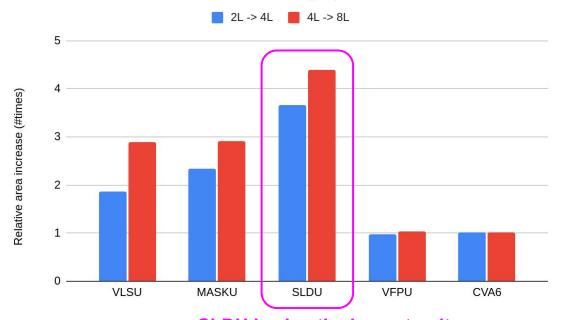


Relative area increase when scaling up

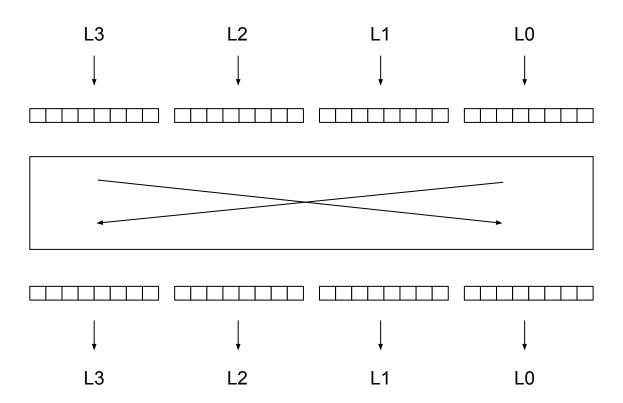


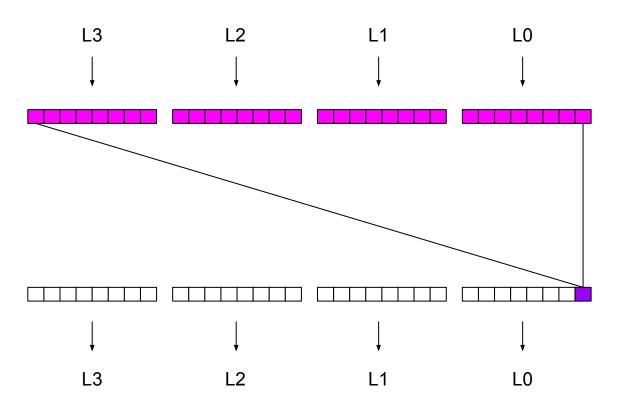


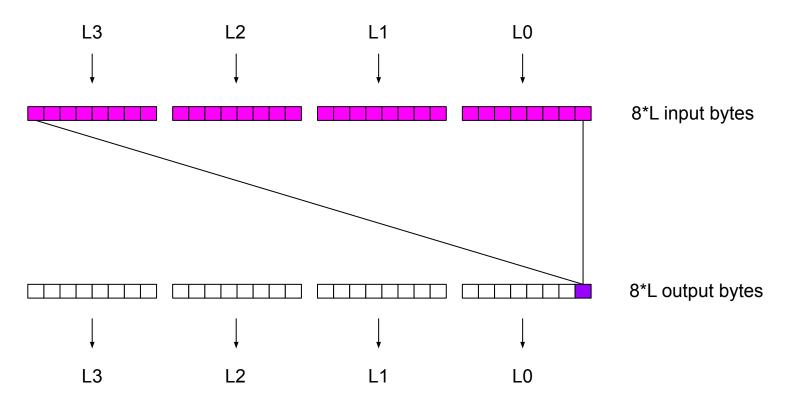
Relative area increase when scaling up

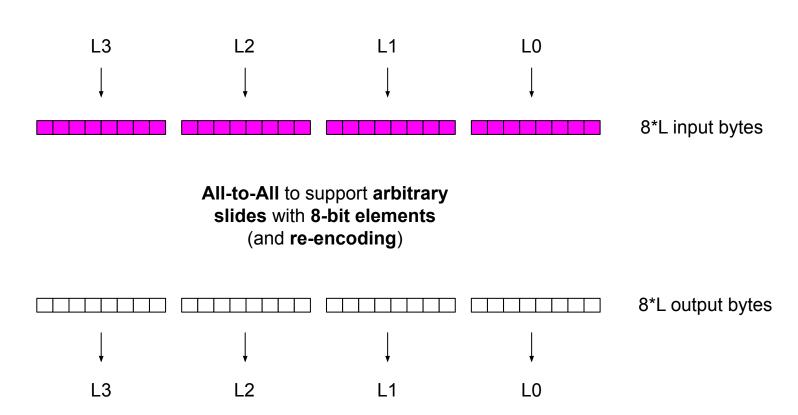


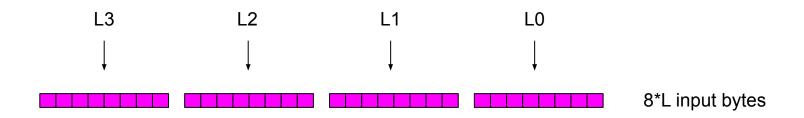
SLDU is also the largest unit 8L: SLDU area == 1.7x VLSU area



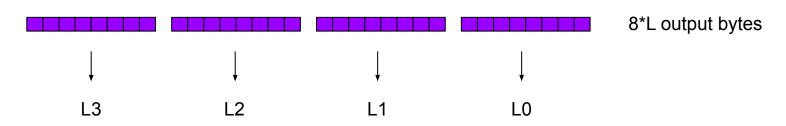






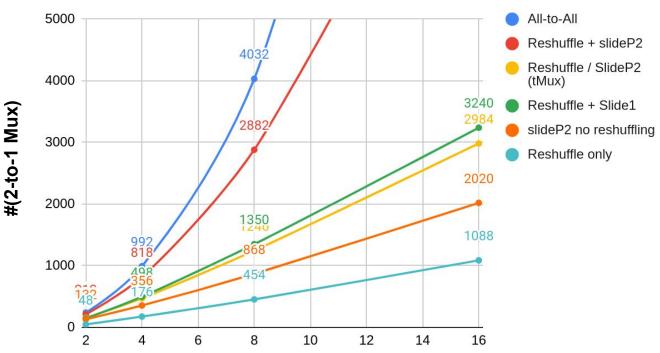


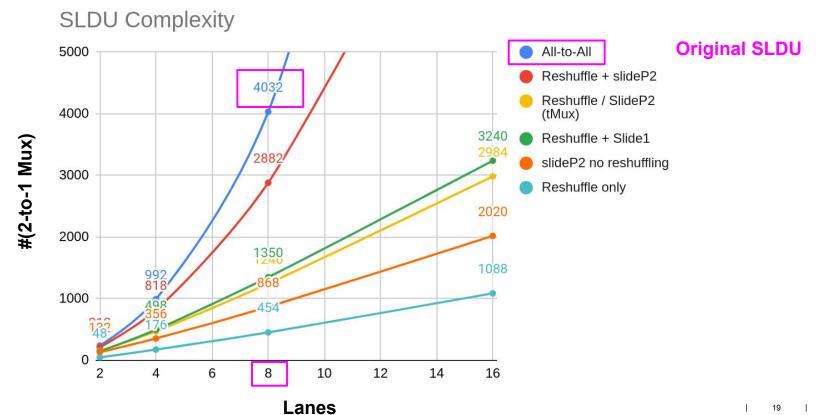
#### 64\*L<sup>2</sup> connections



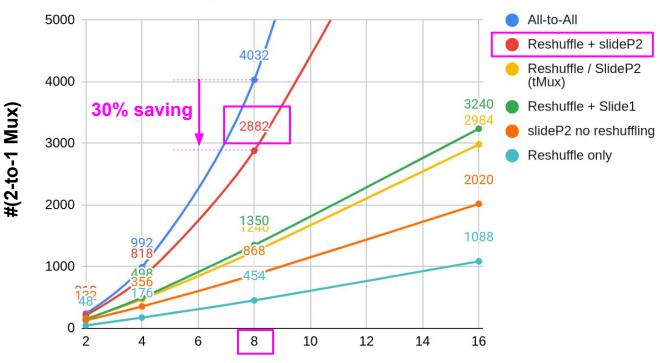
- How to simplify the SLDU?
  - Only slides by 1?
  - Only slides by powers of 2?
  - Time Multiplex slides and encoding?



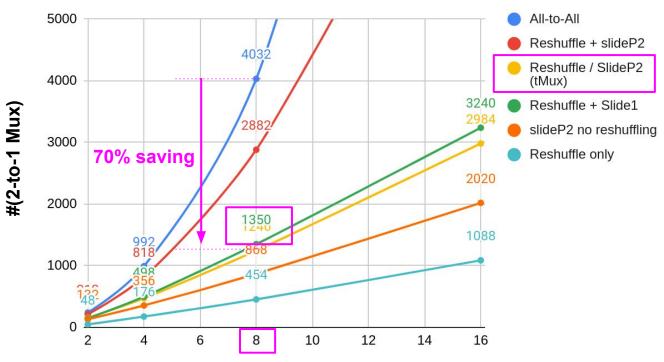












## **SLDU - A New Datapath**

- Time-multiplex p2 slides and re-encoding
- Some difficulties to support undisturbed policy
- In parallel:
  - Energy efficiency of 4L and 8L without SLDU