Update on Ara

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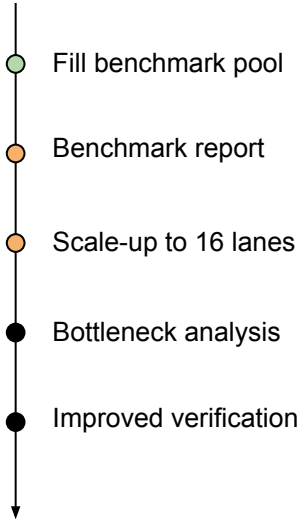
Summary

- **Software**
  - Performance summary on GitHub
  - Implement ideal dispatcher (questa)
  - Gather performance data + Report
- **Hardware (RTL + Backend)**
  - Scale to 8 lanes
  - Merge FP Reductions

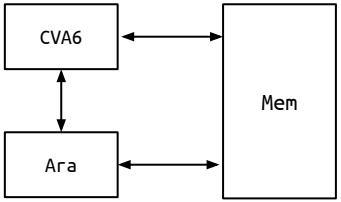


Software

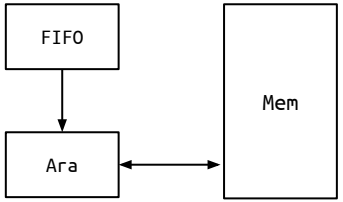
- **Software**
  - Extended “ideal dispatcher” analysis
  - Still no Verilator - Dynamic memory loading
  - Use QuestaSim offline

Software

Default System

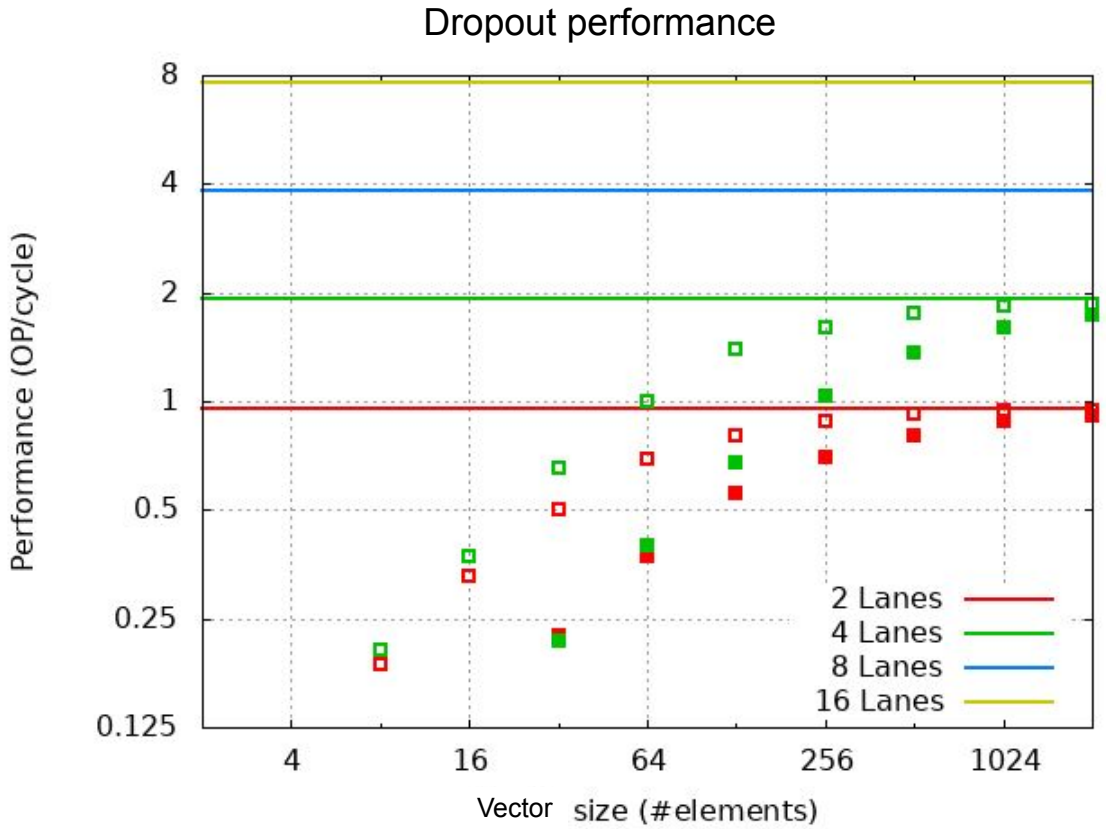


Ideal Dispatcher System



Ideal issue rate from FIFO to Ara

Software

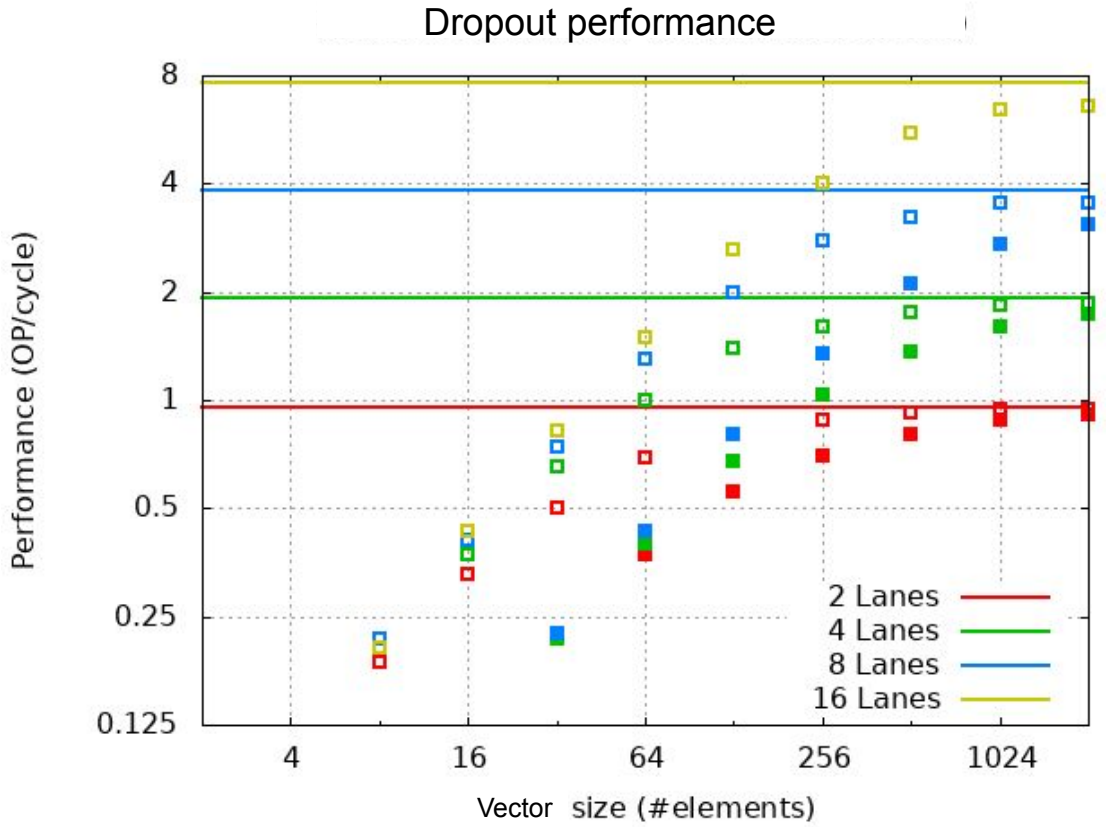


Always Memory Bound

- Ideal Dispatcher System
- Default System with CVA6

Constant arithmetic intensity!

Software



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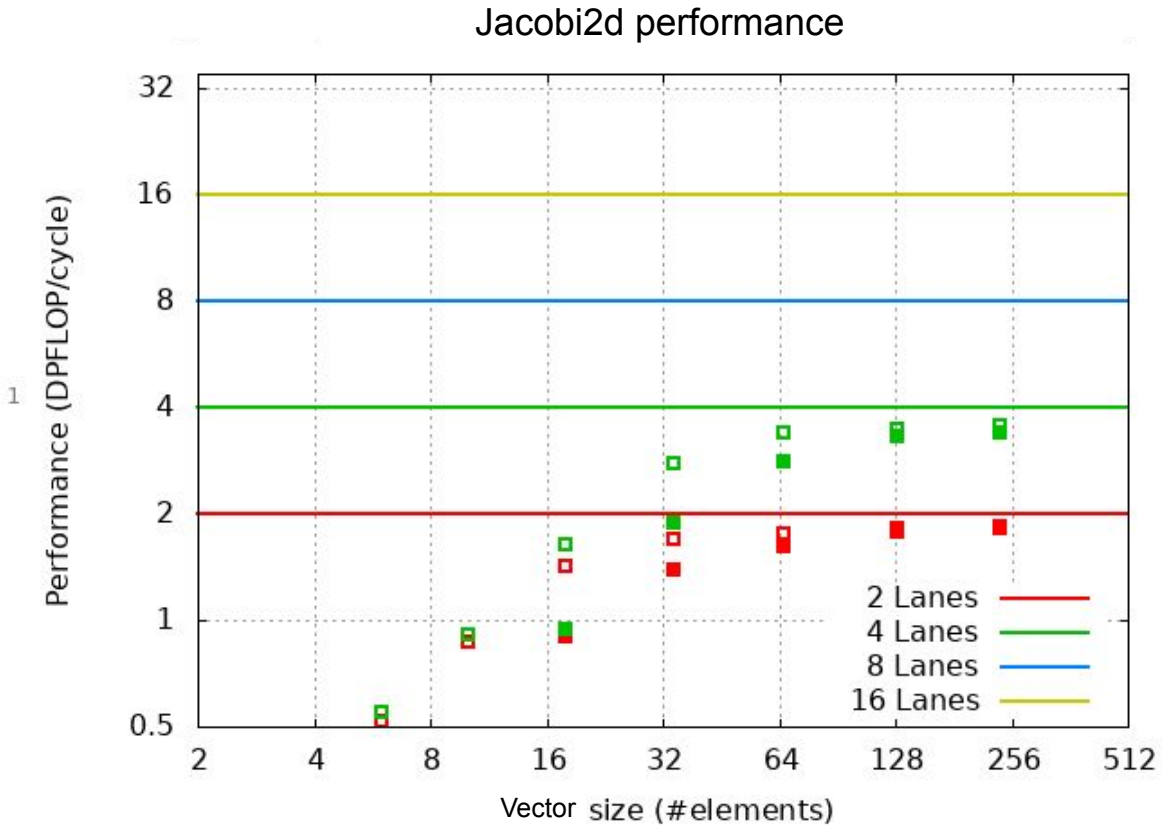
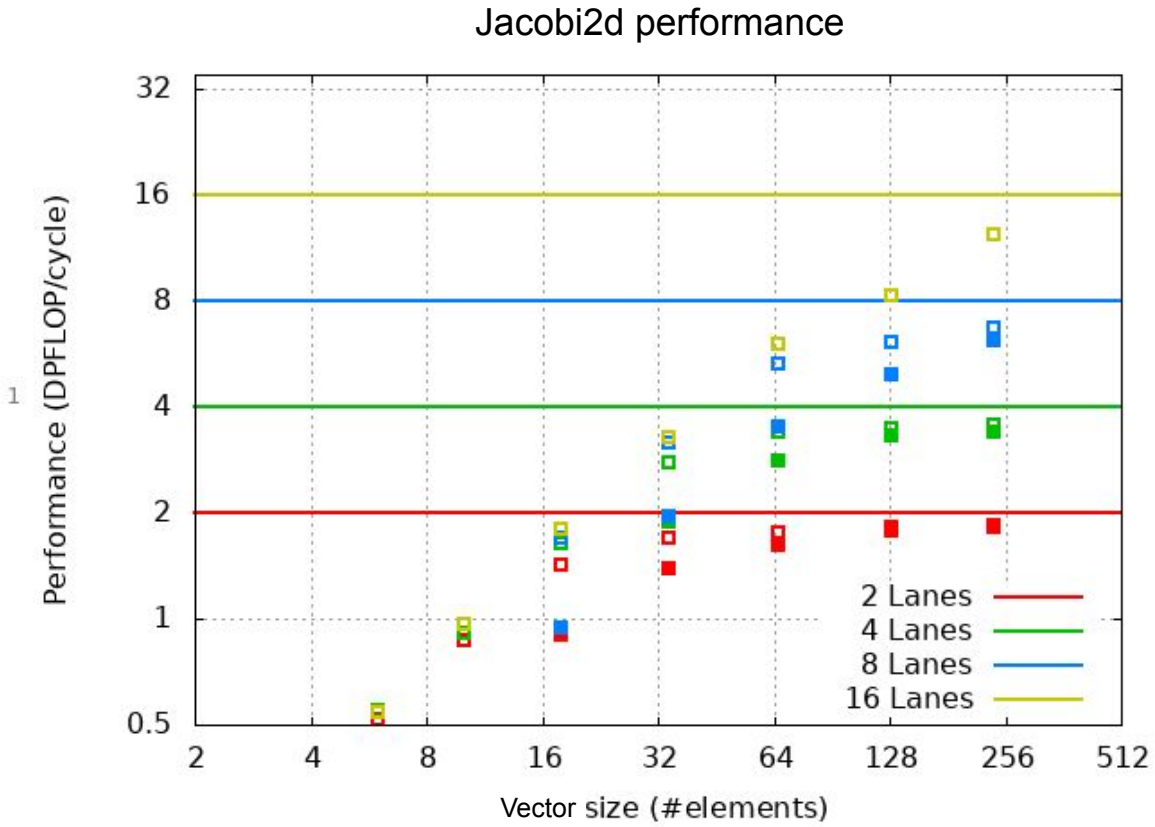


Always Computation Bound

Constant arithmetic intensity!

Software



Always Computation Bound

Ideal Dispatcher System
Default System with CVA6

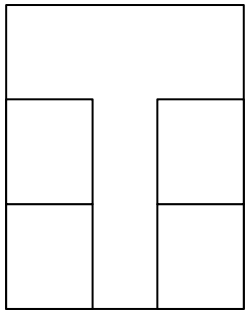
Constant arithmetic intensity!

Hardware

- **Scale up to 8 lanes**
  - Cannot close timing with hierarchical flow
  - Critical convoluted paths
    - From main sequencer to lanes
  - Different parallel trials:
    - Flat-system flow
    - Different floorplan shapes

Hardware

Hier - 4 Lanes



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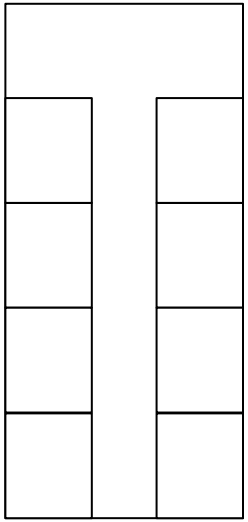
Hier - 8 Lanes



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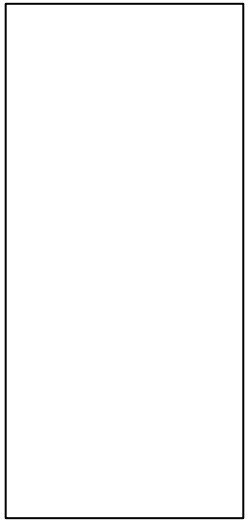
Flat - 8 Lanes



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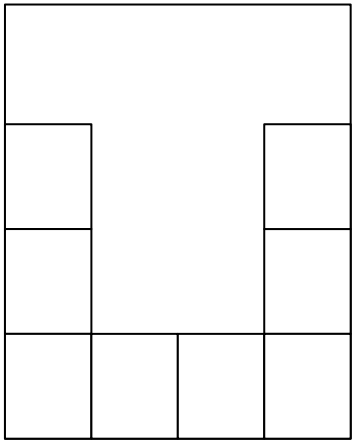
Hier - 8 Lanes



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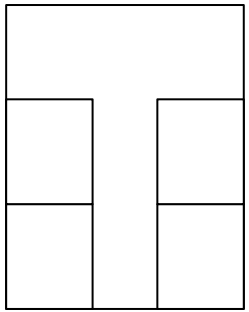
Hardware

Hier - 4 Lanes



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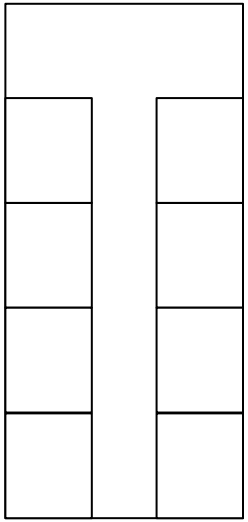
Hier - 8 Lanes



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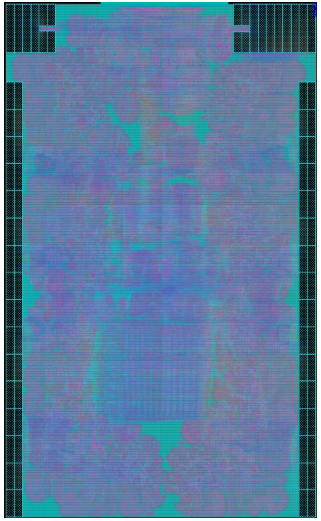
Flat - 8 Lanes



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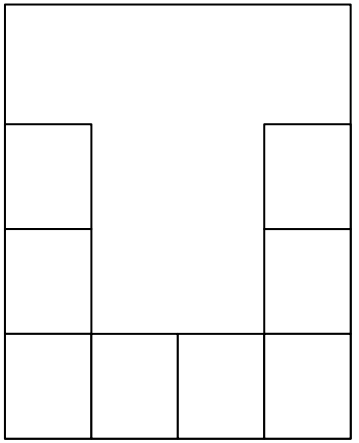
Hier - 8 Lanes



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Hardware

- **8 lanes - Flat Flow**
  - ~950 MHz in SS
  - Some spurious DRC violations
  - Add space between the caches

- Ongoing:
  - Different die shapes
  - 16 lanes - Flat Flow

Further

- **Software**
  - Merge ideal dispatcher branch
  - Gather performance data + Report
- **Hardware (RTL + Backend)**
  - Try different die shapes
  - Close timing with 16 lanes