# Update on Ara

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# Outline

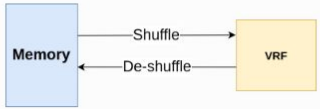
- **Documentation**

- **Hardware (RTL + Backend)**
  - Latches removal
  - Popcount Fix

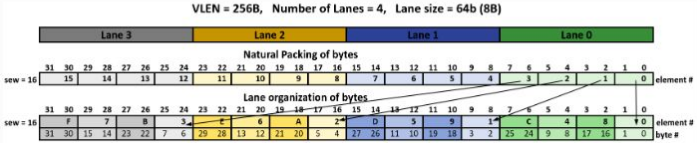
# Documentation

## Shuffle Logic

As shown in the figure below the shuffle/de-shuffle logic sits between the memory subsystem and the VRF. When data is moved from memory to the VRF (via a load instruction) it gets shuffled from the Natural Packing arrangement to the Lane Organization arrangement. Similarly When data is moved from VRF to memory (via a store instruction) it gets de-shuffled from the Lane Organization to the Natural Packing arrangement.




The mapping of bytes from Natural Packing to Lane Organization for 4 lanes and SEW of 16 is shown in the figure below. For element 0, byte indices are the same, 0 & 1, for Natural Packing and Lane Organization. Element 1 is mapped to byte index 8 in the VRF with its two bytes in indices 8 & 9 in the VRF. Shuffle logic takes the sequential bytes from memory as shown in the natural Packing row and converts it into the Lane Organization arrangement as shown in the Lane Organization row. De-shuffle logic does the opposite.




Documentation preview: https://10x-engineers.github.io/ara/lane.html

Author: Sharafat Hussain

# Fixes

- **Popcount in MASKU does not scale**
  - Congestion is high
- **Move popcount** tree **in** the **lanes**
- **Latches cleanup** to run post-layout sim

# PRs - Compliance

WIP

[HW] Add support for vector permute instructions ✓
#180 opened 2 days ago by M-ljaz-10x 3 tasks done

Merged

[HW] Add support for vfrec7 instruction ✓
#191 opened last week by Shafi10x • Changes requested 3 tasks done

Merging

[HW] Add support for vfrsqrt7 instruction ✓
#184 opened last month by Shafi10x • Changes requested 3 tasks done

Merging

Documentation of Ara ✓
#199 opened 2 weeks ago by sharafat-10xEngineers • Changes requested 3 tasks done

WIP

[HW] Shift popcount logic for vcpop.m instruction to lanes •
#198 opened 2 weeks ago by M-ljaz-10x 3 tasks done

Planned

[HW] Seg load ×
#136 opened on Aug 24 by OttG • Draft

- ➢ Vector complex shuffling
- ✓ Documentation
- ➢ Popcount fix
- ✓ vfrsqrt7
- ✓ vfrec7
- ✗ Segment memory ops

# Further

- **Software**
  - Stall analysis
  - WAW / WAR profiling
- **Hardware (RTL + Backend)**
  - Compliance + Verification
  - Scale up to 16 lanes