

Update on Ara

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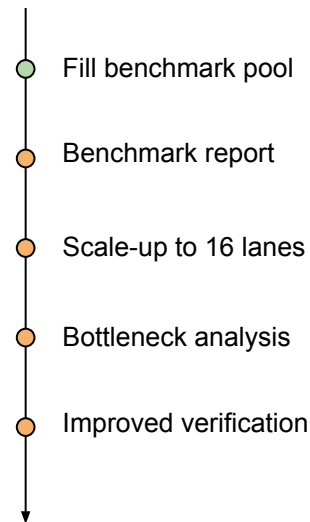
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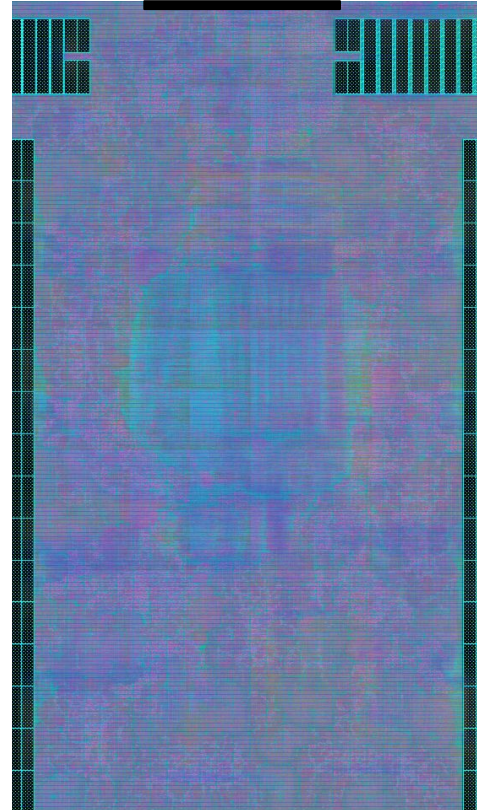
Summary

- **Software**
 - Power Analysis Env
 - SpyGlass Flow
- **Hardware (RTL + Backend)**
 - 8-lanes
 - 16-lanes pipelined SLDU
 - Barber-Pole
 - New instructions



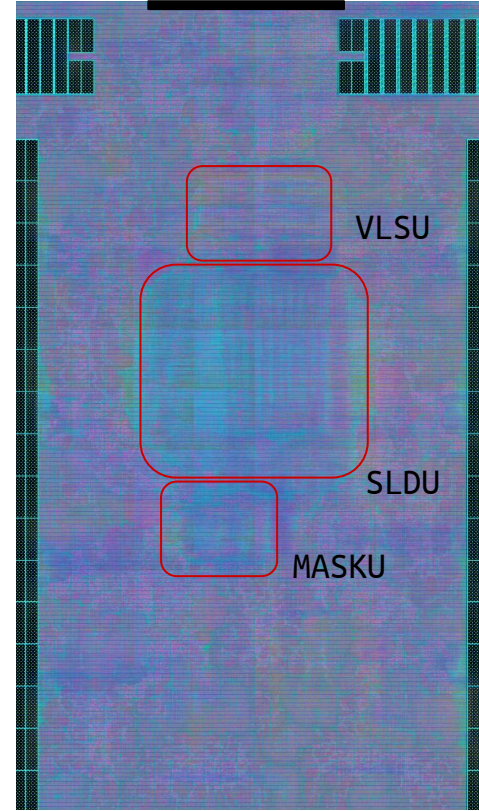
Scale-up

- 8 lanes
 - Area
 - Die Area: $\sim 1.75 \text{ mm}^2$
 - Cell Area: $\sim 1.30 \text{ mm}^2$
 - +10% cell area w.r.t. Ara V1



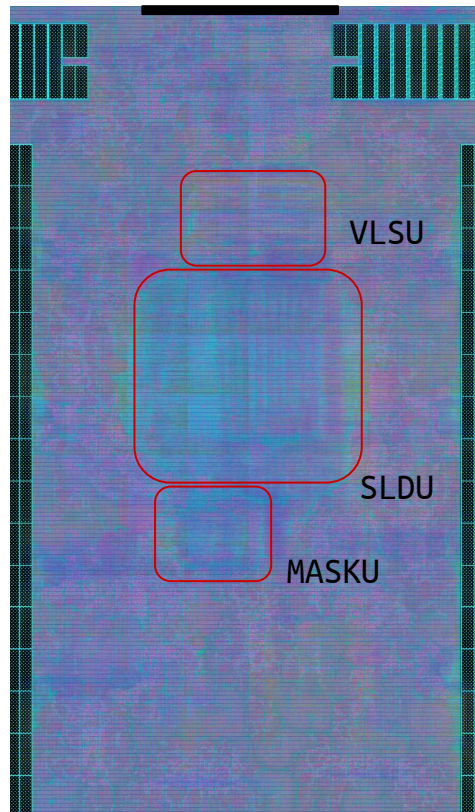
Scale-up

- 8 lanes
 - Area
 - Die Area: $\sim 1.75 \text{ mm}^2$
 - Cell Area: $\sim 1.30 \text{ mm}^2$
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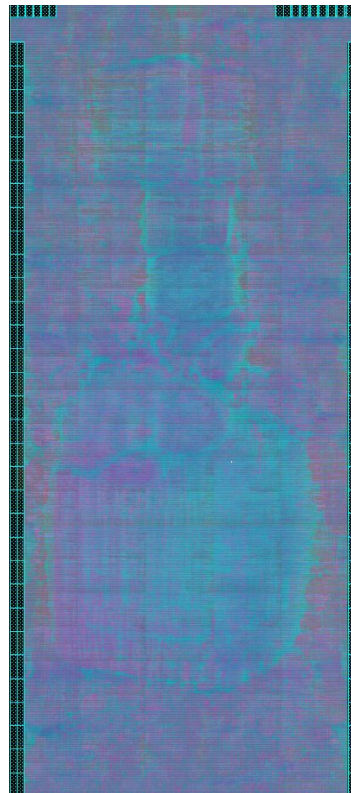
Scale-up

- 8 lanes
 - Area
 - Die Area: $\sim 1.75 \text{ mm}^2$
 - Cell Area: $\sim 1.30 \text{ mm}^2$
 - +10% cell area w.r.t. Ara V1
 - Frequency
 - SS Freq: 935 MHz
 - TT Freq: 1.3 GHz
 - +10% TT Freq w.r.t. Ara V1



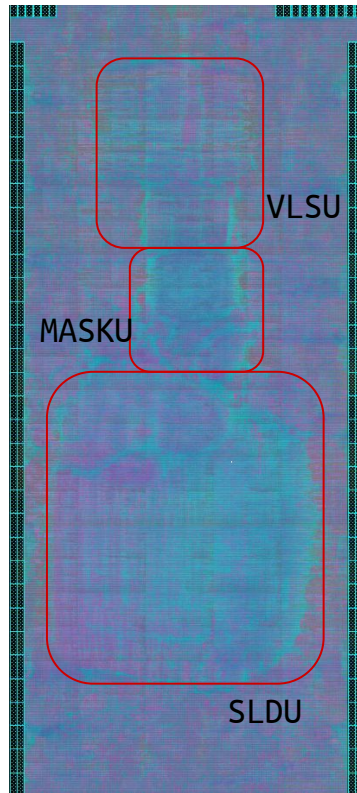
Scale-up

- 16 lanes (pipelined sldu)
 - Area
 - Die Area: $\sim 4.34 \text{ mm}^2$
 - Cell Area: $\sim 3.02 \text{ mm}^2$
 - +40% cell area w.r.t. Ara V1



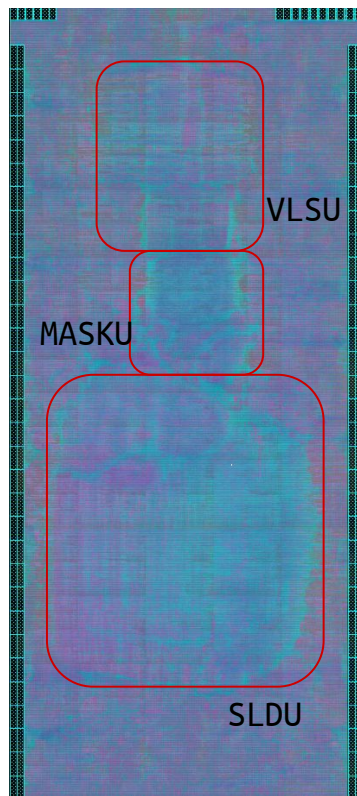
Scale-up

- 16 lanes (pipelined sldu)
 - Area
 - Die Area: $\sim 4.34 \text{ mm}^2$
 - Cell Area: $\sim 3.02 \text{ mm}^2$
 - +40% cell area w.r.t. Ara V1



Scale-up

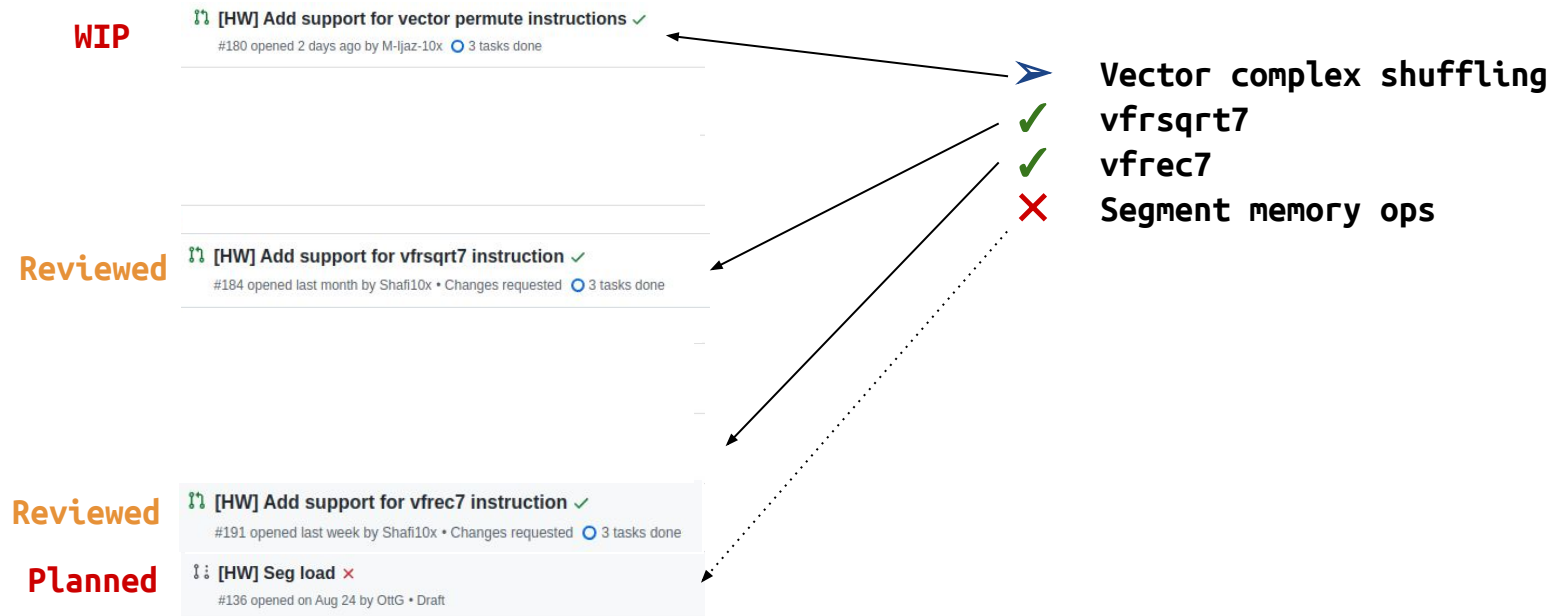
- 16 lanes (pipelined sldu)
 - Area
 - Die Area: ~4.34 mm²
 - Cell Area: ~3.02 mm²
 - +40% cell area w.r.t. Ara V1
 - Frequency (ignoring in/out paths)
 - SS Freq: 720 MHz
 - TT Freq: 1 GHz
 - -4% TT Freq w.r.t. Ara V1



PRs - Compliance

- **New instructions**
 - **Mask**
 - vcpop, vfirst, vmsbf, vmsof, vmsif, viota, vid
 - **Fixed-Point**
 - vssra, vssrl, vnclip, vnclipu, vsmul, vaadd, vaaddu, vsadd, vsaddu, vssub, vssubu, vasub, vasubu

PRs - Compliance



Further

- **Software**
 - Stall analysis
 - WAW / WAR profiling
- **Hardware (RTL + Backend)**
 - Compliance + Verification
 - Scale up to 16 lanes

