

# QUANTUM Series

Semester - 3 & 4 ME/CE/AG/EE/CSE & Allied Branches

## Electronics Engineering



- Topic-wise coverage of entire syllabus in Question-Answer form.
- Short Questions (2 Marks)

Session  
**2019-20**  
Odd & Even  
Semester

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# **QUANTUM SERIES**

*For.*

B.Tech Students of Second Year  
of All Engineering Colleges Affiliated to  
**Dr. A.P.J. Abdul Kalam Technical University,**  
**Uttar Pradesh, Lucknow**

(Formerly Uttar Pradesh Technical University)

**Electronics Engineering**

**By**

**Ankit Tyagi**

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## KOE 038 / KOE 048 : Electronics Engineering

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### **UNIT-2 : DIODE APPLICATION**

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### **UNIT-3 : BJT AND FET**

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UNIT

# 1

UNIT

## Semiconductor Diode

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**PART- 1**

*PN Junction Diode : Introduction of Semiconductor Materials.*

**CONCEPT OUTLINE**

**Semiconductors :** The elements whose conductivity lies between metal and insulator. Most frequently used semiconductors in construction of electronic devices are Ge, Si, and GaAs.

- It is of two types :
  - i. **Intrinsic** : Pure form of semiconductor
  - ii. **Extrinsic** : The electrical conductivity of intrinsic semiconductor can be increased by adding some impurity in the process of crystallization. This process is called doping and the semiconductor is called extrinsic.
- Extrinsic semiconductor is of two types :
  - i. *p*-type
  - ii. *n*-type

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 1.1.** Explain *n*-type and *p*-type semiconductors.

**Answer****i. *n*-type Semiconductor :**

1. When a small amount of pentavalent impurity is added to pure semiconductor crystal during the crystal growth, the resulting crystal is called as *n*-type extrinsic semiconductor.
2. The Fig. 1.1.1 shows the arsenic (As) atom is added in germanium (Ge) crystal in such a way that its four valence electrons form covalent bond with four germanium atom.
3. The fifth electron of arsenic is not bonded and acts as free electron.
4. This electron is available as a carrier of current. This free electron acts as donor whenever required with any other semiconductor.
5. The electrons are the majority carriers while holes are the minority carriers in such cases.

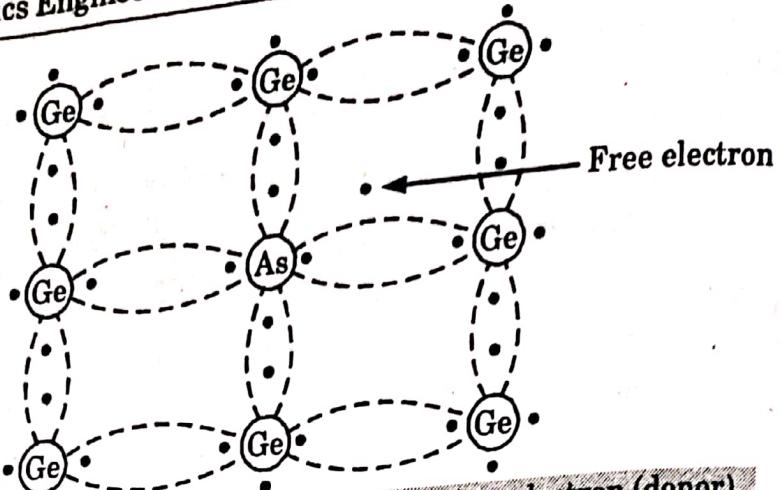


Fig. 1.1.1. Arsenic electron as free electron (donor).

## ii. *p*-type Semiconductor :

- When a small amount of trivalent impurity is added to pure crystal during the crystal growth, the resulting crystal is called *p*-type extrinsic semiconductor.
- Fig. 1.1.2 shows each atom of boron *i.e.*, trivalent impurity is added to pure germanium crystal.

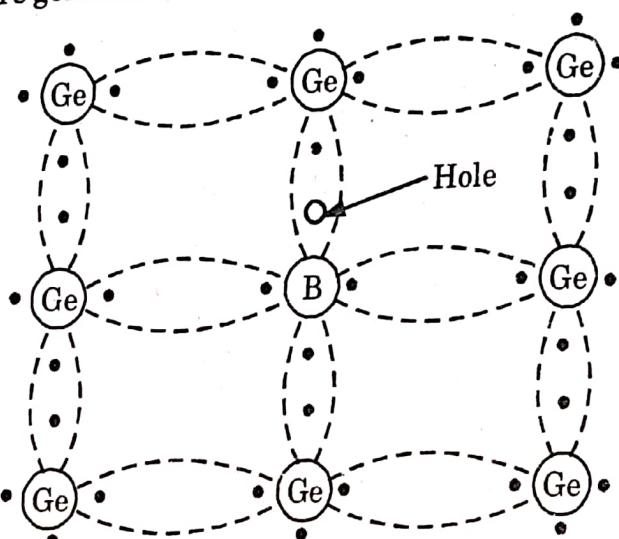


Fig. 1.1.2. Boron hole (acceptor).

- The three valence electrons form covalent bond while the fourth covalent bond is formed due to germanium atom contribution and deficiency of one electron is left in form of hole.
- The remaining fourth electron also tries to form a bond and treated as acceptor.
- In *p*-type semiconductor, the majority carriers are holes while minority carriers are the electrons.

## PART - 2

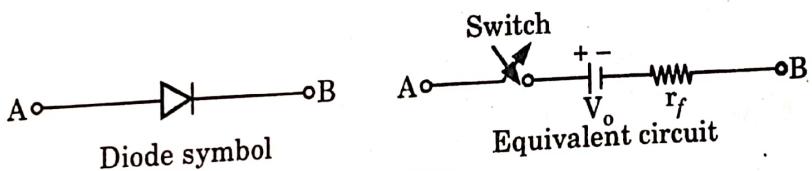
*Semiconductor Diode : Depletion Layer, V-I Characteristics, Ideal and Practical, Diode Equivalent Circuits.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 1.2.** Explain semiconductor diode and also draw its equivalent circuit.

**Answer****Semiconductor diode :**

1. A diode is an electrical device allowing current to flow only in one direction (forward bias) with far greater ease than in the other direction (reverse bias).
2. The most common type of diode in modern circuit design is the semiconductor diode ( $p-n$  junction).
3. A diode is a two-layer semiconductor consisting of  $p$ -type semiconductor material and  $n$ -type semiconductor material the equivalent circuit of diode is shown in Fig. 1.2.1.

**Fig. 1.2.1.**

4. In an equilibrium,  $p-n$  junction, the free electrons from the  $n$ -type region will diffuse across the junction to the  $p$ -type side where they will recombine with some of the holes in the  $p$ -type material. Similarly, holes will diffuse across the junction in the opposite direction and recombine.
5. The recombination of free electrons and holes in the vicinity of the junction leaves a narrow region on either side of the junction that contains no mobile charge. This narrow region which has been depleted of mobile charge is called the depletion layer.
6. Diffusion of electrons into the  $p$ -region will leave positively charged ions (donors) in the  $n$ -region.
7. Similarly, diffusion of holes near the  $p-n$  interface in the  $n$ -type region leaves fixed ions (acceptors) with negative charge.
8. The regions nearby the  $p-n$  interfaces lose their neutrality and become charged, forming the space charge region or depletion layer.

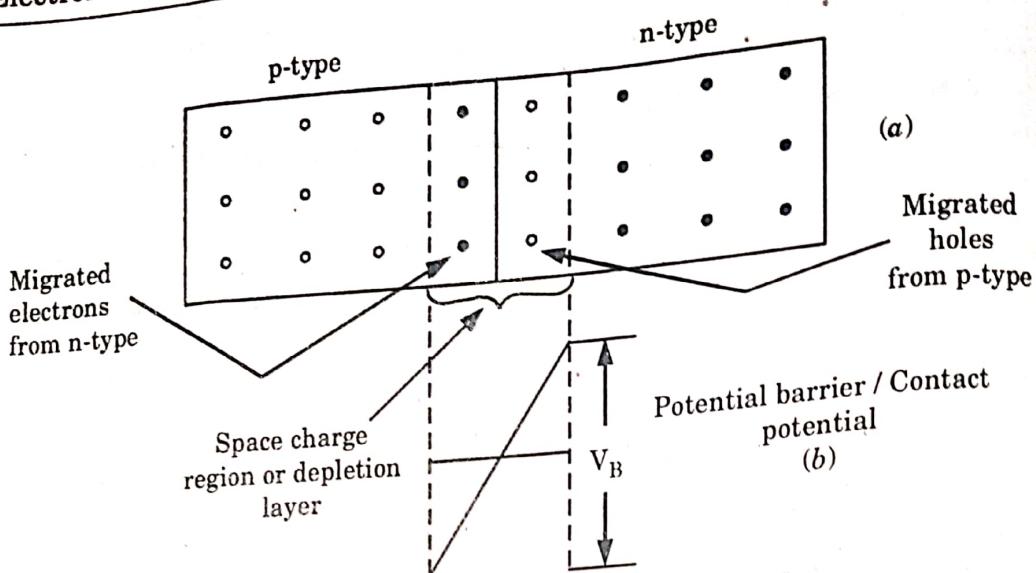


Fig. 1.2.2. p-n junction semiconductor.

9. This separation of charges causes an electric field to extend across the depletion layer. A potential difference must therefore exist across the depletion layer.

**Que 1.3.** Explain the V-I characteristics of p-n junction diode.

AKTU 2014-15, (Sem-I) Marks 05

OR

Compare the V-I characteristics of silicon and germanium diode.

OR

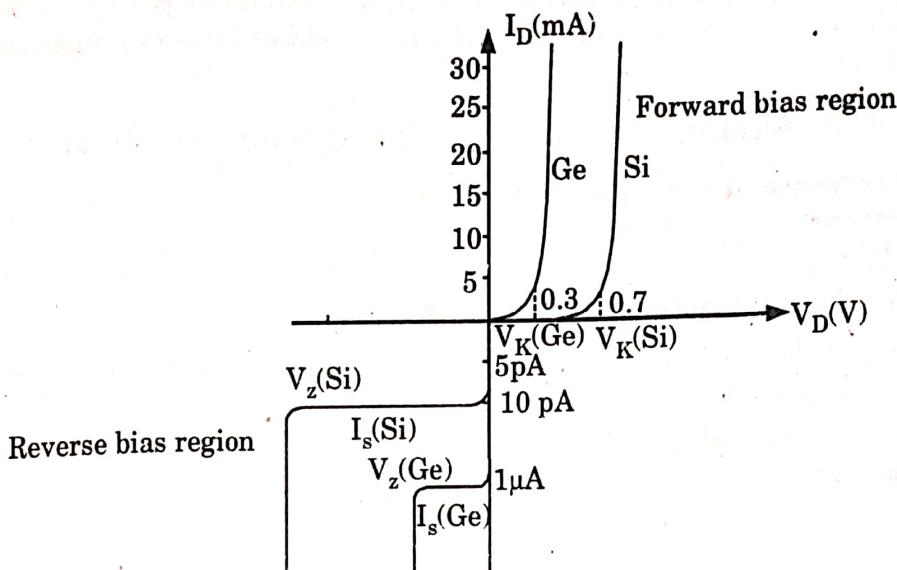
Explain the V-I characteristic of p-n junction diode. Draw well labelled characteristic.

AKTU 2016-17, (Sem-I) Marks 05

**Answer**

i. Forward bias :

- For the forward bias of a p-n junction, p-type is connected to the positive terminal while the n-type to negative terminal of battery.
- The potential can be varied with potential divider. At some forward voltage (0.3 V for Ge and 0.7 V for Si) the potential barrier is eliminated and current starts flowing. This voltage is known as threshold or knee voltage ( $V_K$ ).
- As the forward voltage applied increases beyond threshold voltage, the forward current rises exponentially as shown in Fig. 1.3.1.
- Beyond a certain safe value, it produces an extremely large current which may destroy the junction due to overheating.

Fig. 1.3.1. Volt-ampere characteristics of  $p-n$  junction.

**ii. Reverse bias :**

1. The  $p$ -type is connected to the negative terminal while  $n$ -type is connected to the positive terminal of a battery.
2. In this case, the junction resistance becomes very high and practically no current flows through the circuit.
3. In practical, a small current of the order of  $\mu A$  flows in the circuit due to minority carriers. This is known as reverse current. The reverse current is shown in Fig. 1.3.1.
4. As the reverse bias is increased from zero, the reverse current quickly rises to its maximum or saturation value. The slight increase is due to impurities on the surface, which behaves as a resistor and hence obeys ohm's law. This gives rise to a current called surface leakage current.
5. If the reverse voltage is further increased, the kinetic energy of electrons becomes so high that they knock out from the semiconductor atoms. At this stage, breakdown of junction occurs and there is a sudden rise of reverse current. Now the junction is destroyed completely.
6. Thus,  $p-n$  junction diode is one-way device which offers a low resistance when forward biased and behaves like an insulator when reverse biased. Thus, it can be used as a rectifier *i.e.*, for converting alternating current into direct current.

**Comparison of V-I characteristics of silicon and germanium diode :**

1. The knee voltage for silicon diode is 0.7 V and for germanium diode is 0.3 V.
2. The breakdown voltage for silicon diode is greater than germanium diode.

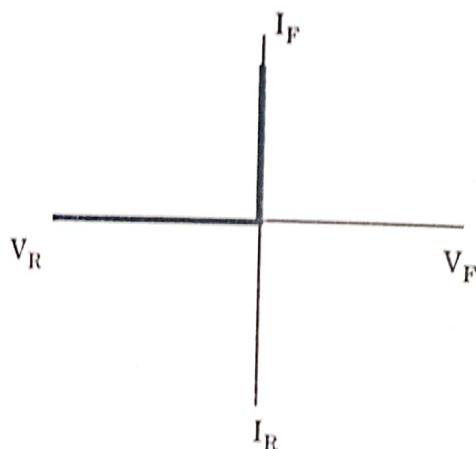
3. The reverse saturation current in a germanium diode is 1,000 times greater than the reverse saturation current in silicon diode of comparable ratings.

**Que 1.4.** Sketch and explain ideal and practical V-I characteristics of a *p-n* junction diode.

**Answer**

**Ideal V-I characteristic :**

1. An ideal diode is perfect conductor in forward bias and a perfect resistor in reverse bias.
2. The current-voltage characteristic of the ideal diode is shown in Fig. 1.4.1.



**Fig. 1.4.1.** V-I characteristics of an ideal diode.

3. A diode acts as a short circuit when it is forward biased. When it is reverse biased, it acts as an open circuit.
4. Therefore, an ideal diode acts as unilateral switch. No power is dissipated in an ideal diode biased in either direction. Since in forward direction, the voltage across the diode is zero and in the reverse direction, the current through the diode is zero as shown in Fig. 1.4.1.

**Practical :**

1. In practical, the battery introduced a small offset voltage ( $V_o$ ) in forward biased. The value of the offset voltage is determined by the type of semiconductor used in a *p-n* junction but cannot be measured directly.
2. The resistor approximates the semiconductor resistance when diode is ON / OFF or forward bias / reverse bias.
3. A reverse biased diode conducts a very small amount of current called leakage current.
4. The ability of diode to withstand reverse-bias voltage is limited. If the applied reverse-bias voltage becomes too large diode will experience a heavy conduction known as breakdown, which is usually destructive.

5. The current versus voltage curve for a real diode looks like as shown in Fig. 1.4.2.

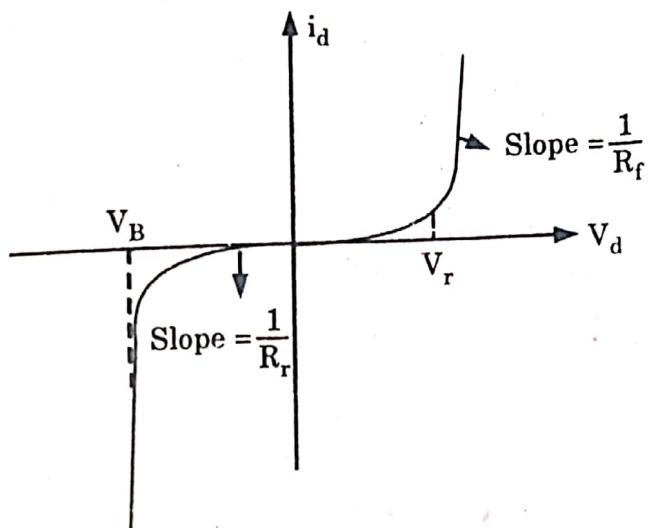


Fig. 1.4.2.

**PART-3***Diode Resistance.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 1.5.** Explain the resistance of a semiconductor diode and derive the expression for diode resistance.

**Answer**

Resistance of diode is,

**i. DC or static resistance ( $R_D$ ) :**

1. DC resistance is defined as the ratio of the voltage to the current in the forward bias characteristics of the  $p-n$  junction diode.
2. In general, higher the current through a diode, the lower is the DC resistance level.

$$R_D = \frac{V}{I}$$

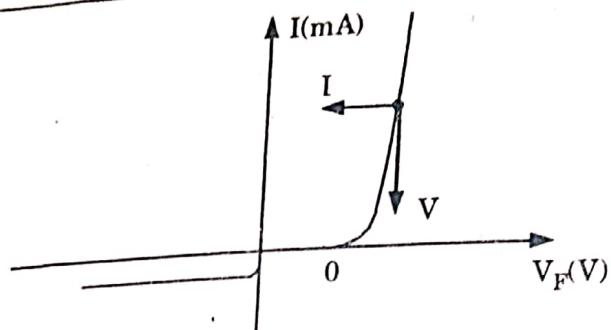


Fig. 1.5.1. Forward bias characteristics of a diode.

3. The DC resistance at the operating point is determined by using corresponding levels of voltage  $V$  and current  $I$ .
4. The DC resistance is independent of the shape of the characteristics in the region surrounding the point of interest.
- ii. **AC or dynamic resistance ( $r_d$ ) :**

  1. AC resistance is defined as the reciprocal of the slope of the V-I characteristics of a diode.
  2. It is determined as

$$r_d = \frac{\text{change in voltage}}{\text{resulting change in current}} = \frac{\Delta V}{\Delta I}$$

3. AC resistance is determined by a straight line drawn tangent to the curve through the Q-point in the forward characteristics of the diode.

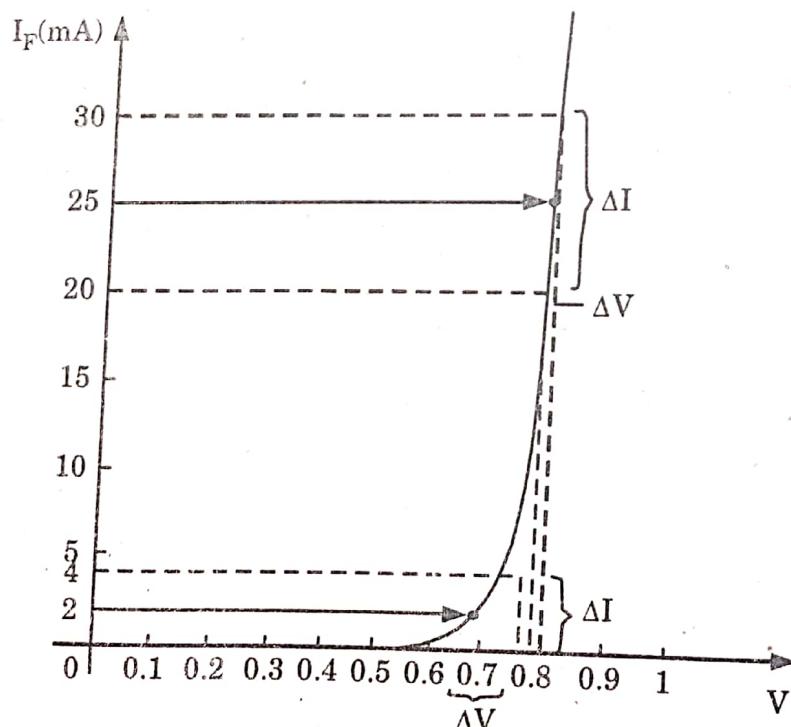


Fig. 1.5.2.

4. Lower the  $Q$ -point of operation (smaller current or lower voltage), higher is the AC resistance.

5. The Shockley's equation for the forward and reverse bias is given by

$$I = I_o (e^{V/\eta V_T} - 1) \quad \dots(1.5.1)$$

6. We know, the derivative of a function at a point is equal to slope of the tangent line drawn at that point.

7. Taking derivative of eq. (1.5.1) with respect to applied voltage  $V$ , we get

$$\frac{dI}{dV} = I_o \frac{d}{dV} (e^{V/\eta V_T} - 1) = I_o \left( \frac{e^{V/\eta V_T}}{\eta V_T} \right) = \frac{I + I_o}{\eta V_T}$$

Generally,

$$I \gg I_o$$

$$\therefore \frac{dI}{dV} \approx \frac{I}{\eta V_T}$$

$$\text{But } r_d = \frac{dV}{dI}$$

$$\therefore r_d = \frac{\eta V_T}{I}$$

where  $V_T = 26 \text{ mV}$  at room temperature.

$$\text{For Ge diodes, } r_d = \frac{0.026}{I_o} \Omega$$

8. AC resistance is the sum of ohmic resistance of the  $p$  and  $n$  type semiconductor and junction resistance,  $r_j$ .

$$\therefore r_d = R_p + R_n + r_j$$

- iii. Average AC resistance ( $r_{av}$ ): It is the resistance associated with the device for the region, if the input signal is sufficiently large to produce a wide range of characteristics.

$$r_{av} = \left. \frac{\Delta V}{\Delta I} \right|_{\text{point to point.}}$$

**Que 1.6.** Sketch output voltage ( $V_O$ ) for the network of Fig. 1.6.1 for the input given. Assume diodes are ideal.

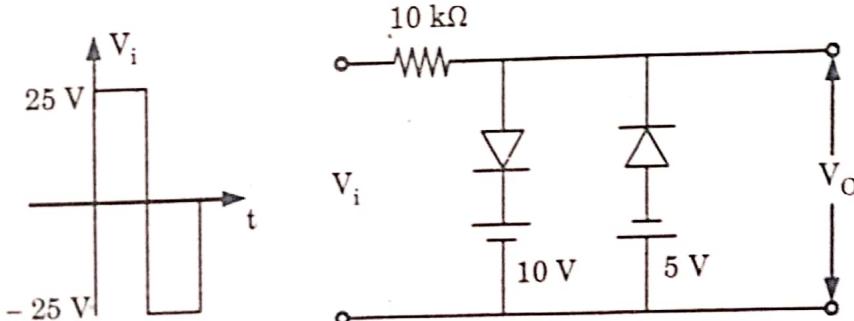


Fig. 1.6.1.

AKTU 2013-14, (Sem-II) Marks 10

**Answer**

1. When  $V_i > 10$  V, diode  $D_1$  conducts and  $D_2$  remains OFF.

$$\text{Thus } V_O = 10 \text{ V}$$

2. When  $V_i < -5$  V, diode  $D_2$  conducts and  $D_1$  remains OFF.

$$\text{Thus } V_O = -5 \text{ V}$$

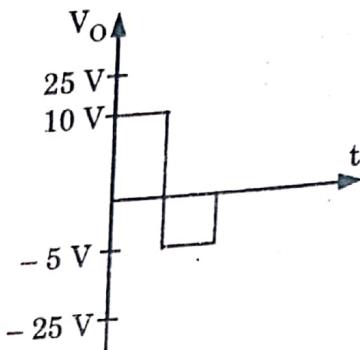


Fig. 1.6.2.

**PART-4**

*Capacitance : Transition and Diffusion Capacitance.*

**Questions-Answers**

**Long Answer Type and Medium Answer Type**

**Que 1.7.** Explain the transition and diffusion capacitance.

**AKTU 2017-18, (Sem-I) Marks 3.5**

**Answer**

i. **Space charge or transition capacitance ( $C_T$ ) :**

1. When a  $p-n$  junction is reversed biased, the depletion region acts like an insulator, while  $p$  and  $n$ -type region on either side have low resistance and acts as the plate.
2. In this way  $p-n$  junction may be regarded as parallel plate capacitor.
3. The junction capacitance is called space charge capacitance or transition capacitance and is denoted by  $C_T$ .

$$C_T = \frac{K}{(V_K + V_R)^n}$$

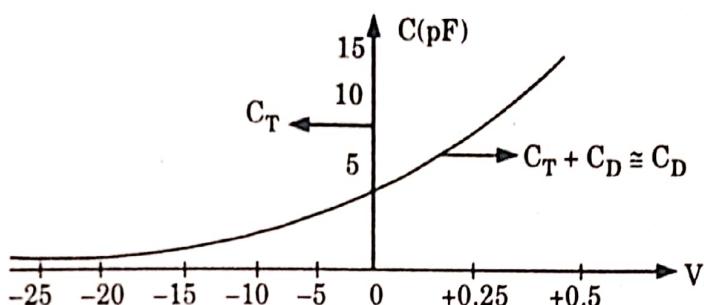
where  $V_k$  = Knee voltage

$V_R$  = Applied reverse voltage

**K = Constant depending on semiconductor material**

$n = (1/2)$  for alloy and  $(1/3)$  for diffusion junction.

4. Fig. 1.7.1 shows the variation of transition capacitance with applied reverse voltage.



**Fig. 1.7.1.** Transition and diffusion capacitance versus applied bias for a silicon diode.

5. The transition capacitance ( $C_T$ ) are,

  - With no applied voltage :  $C_T = 20 \text{ pF}$
  - With forward bias :  $C_T = 25 \text{ pF}$
  - With reverse bias :  $C_T = 8 \text{ pF}$

ii. **Diffusion or storage capacitance ( $C_D$ ):**

  - When  $p-n$  junction is forward biased the potential barrier is reduced. Now, the holes from  $p$ -side enter into  $n$ -side and similarly electrons from  $n$ -side enter the  $p$ -side.
  - These carriers diffuse away from the junction and progressively recombine. Thus a charge is stored on both sides of the junction when a forward bias voltage is applied.
  - The amount of stored charge varies with the applied potential as for a true capacitor.
  - The diffusion capacitance expressed by the equation  $C_D = dQ/dV$ , where  $dQ$  represents the change in minority carriers stored outside the depletion region when a change in voltage across diode,  $dV$ , is applied.
  - The diffusion capacitance can be expressed as :

$$C_v = \frac{\tau I}{\eta V_r}$$

where,  $\tau$  = Mean life time of carrier

*I* = Forward current

$\eta = \text{Constant}$

$V_T$  = Equivalent voltage at absolute temperature

6. The value of  $C_D$  is large for forward current and small for reverse current. Large value of  $C_D$  delays both the switch-ON and switch-OFF.

**PART-5***Zener Diodes Breakdown Mechanism (Zener and Avalanche).***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 1.8.** What is zener diode ?

OR

Explain the V-I characteristic of *p-n* junction diode. How it is differ from Zener diode ?

AKTU 2016-17, (Sem-II) Marks 07

OR

Explain input and output characteristics of zener diode.

AKTU 2015-16, (Sem-II) Marks 05

**Answer**

V-I characteristic of *p-n* junction diode : Refer Q. 1.3, Page 1-5D, Unit-1.

**Zener diode :**

1. Zener diode is a reverse-biased heavily doped *p-n*-junction diode which is operated in the breakdown region. Fig. 1.8.1 shows the symbol of zener diode.



Fig. 1.8.1. Zener diode.

2. When a zener diode is forward biased, its characteristics are just same as the ordinary diode and it is shown in Fig. 1.8.2.

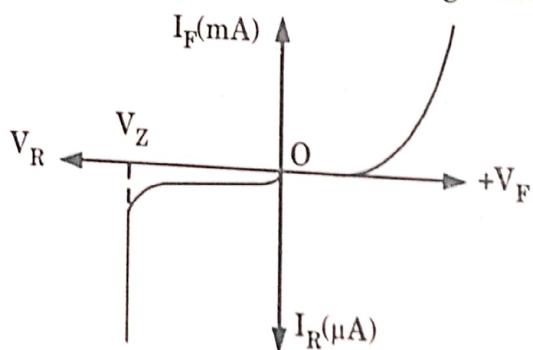


Fig. 1.8.2. V-I characteristic of zener diode.

3. When zener diode is reverse biased then it gives constant current upto a certain voltage. When the reverse bias voltage is increased beyond that voltage, the current increased rapidly as shown in Fig. 1.8.2.
4. The cut-off value of voltage beyond which zener diode reverse current increases rapidly is called zener voltage  $V_z$  or breakdown voltage.
5. The breakdown or zener voltage depends upon the amount of doping.
6. A zener diode can be used as a voltage regulator to provide a constant voltage to a load.

**Que 1.9.** Explain reverse breakdown of a diode.

**Answer**

Reverse breakdown can occur by two mechanisms that are zener breakdown and avalanche breakdown.

**Zener breakdown :**

1. It takes place in very thin junction (*i.e.*, depletion layer is narrow due to heavily doped junctions on both sides).
2. When a small reverse bias voltage is applied, a very strong electric field (approximately  $10^7 \text{ V/m}$ ) is set up across the thin depletion layer.
3. This field is enough to break the covalent bonds. This breaking of covalent bonds produces large number of electrons and holes which constitute the reverse saturation current (*i.e.*, zener current).
4. Zener current is independent of the applied voltage. It depends only on the external resistance.
5. This breakdown is called as zener breakdown as shown in Fig. 1.9.1. This breakdown occurs at low voltage.

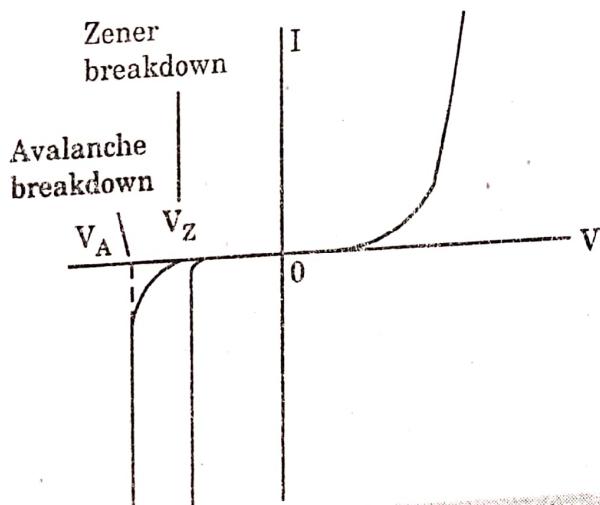


Fig. 1.9.1. The I-V characteristics comparison between Zener and avalanche breakdown

**Avalanche breakdown :**

1. Avalanche breakdown takes place in slightly thick junction than the zener breakdown case. It means both sides of junction are lightly doped.
2. In this case, the electric field across the depletion region (layer) is not so strong to produce zener breakdown for the same applied voltage of zener breakdown case.
3. Here, the minority carriers accelerated by the field collide with the semiconductor atoms in the depletion region.
4. During collision the kinetic energy of electrons is transferred to other covalent bonds, thus the energy transferred to covalent bonds increases the band energy, hence covalent bonds are broken and electron-hole pairs are generated.
5. The newly generated carriers transfer their energy to other covalent bonds and break more bonds and thus extremely large numbers of carriers are generated due to cumulative process of avalanche multiplication.
6. This breakdown is called avalanche breakdown as shown in Fig. 1.9.1. This breakdown occurs at higher voltages.

**Que 1.10.** What is the difference between Zener and Avalanche breakdown ? For the given Zener diode network shown in Fig. 1.10.1, determine  $V_L$ ,  $V_R$ ,  $I_Z$  and  $I_R$ .

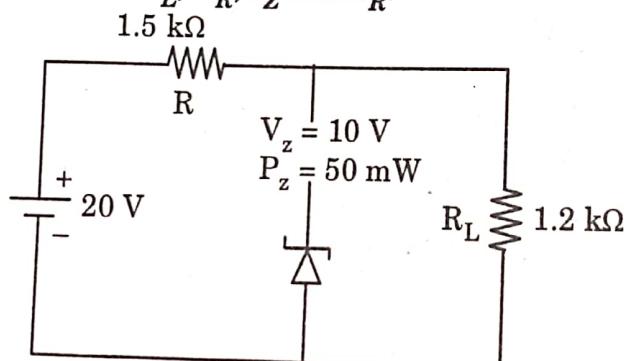


Fig. 1.10.1.

AKTU 2013-14, (Sem-I) Marks 10

**Answer****Difference :**

S.No.	Zener Breakdown	Avalanche Breakdown
1.	The process in which the electrons move across the barrier from the valence band of <i>p</i> -type material to the conduction band of <i>n</i> -type material is known as zener breakdown.	The process of applying high voltage and increasing the free electrons or electric current in semiconductors and insulating materials is called an avalanche breakdown.

2.	Zener breakdown voltage $V_z$ of 5 to 8 volts.	Avalanche breakdown voltage $V_A$ greater than 8 volts.
3.	The valence electrons are pulled into conduction due to the high electric field in the narrow depletion region.	The valence electrons are pushed to conduction due to the energy imparted by accelerated electrons, which gains its velocity due to its collision with other atoms.
4.	The increase in temperature decreases the breakdown voltage.	The increase in temperature increases the breakdown voltage.
5.	It occurs in diodes that are highly doped.	It occurs in diodes that are lightly doped.

**Numerical :**

1. Voltage across zener diode,

$$V_o = V_L = \frac{R_L \cdot V_i}{R + R_L} = \frac{1.2 \times 20}{1.5 + 1.2} = 8.88 \text{ V}$$

2. Given,  $V_z = 10 \text{ V}$

3. Here,  $V_o < V_z$ .

So, the zener diode is OFF and no current will flow through it.

$$I_z = 0$$

4. Voltage across  $R$ ,

$$V_R = V_i - V_L = 20 - 8.88 = 11.11 \text{ V}$$

5.  $I_R = I_z + I_L = 0 + \frac{8.88}{1.2 \times 10^{-3}} = 7.4 \text{ mA}$

**VERY IMPORTANT QUESTIONS**

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

- Q. 1. Explain  $n$ -type and  $p$ -type semiconductors.**

**Ans.** Refer Q. 1.1.

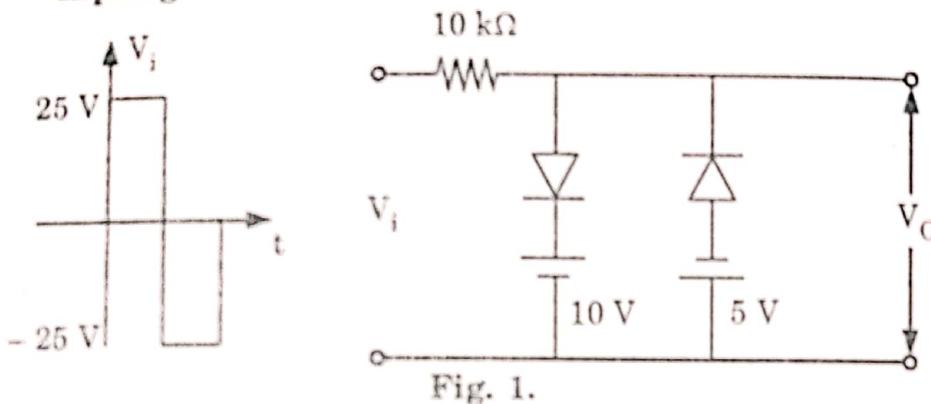
- Q. 2. Explain the V-I characteristics of  $p-n$  junction diode. the active mode.**

**Ans.** Refer Q. 1.3.

**Q. 3.** Explain the resistance of a semiconductor diode and derive the expression for diode resistance.

**Ans.** Refer Q. 1.5.

**Q. 4.** Sketch output voltage ( $V_O$ ) for the network of Fig. 1 for the input given. Assume diodes are ideal.



**Ans.** Refer Q. 1.6.

**Q. 5.** Explain the transition and diffusion capacitance.

**Ans.** Refer Q. 1.7.

**Q. 6.** Explain reverse breakdown of a diode.

**Ans.** Refer Q. 1.9.

**Q. 7.** What is the difference between Zener and Avalanche breakdown? For the given Zener diode network shown in Fig. 2, determine  $V_L$ ,  $V_R$ ,  $I_Z$  and  $I_R$ .

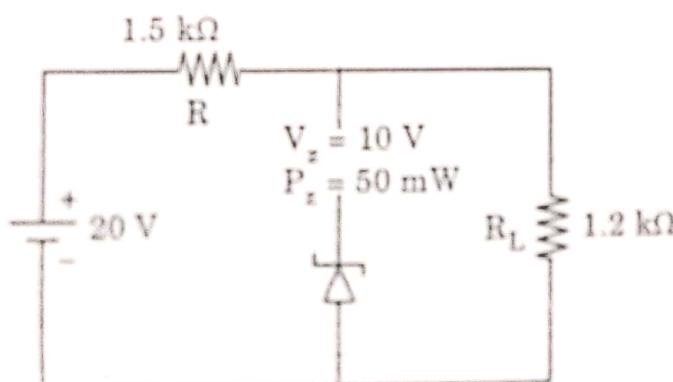


Fig. 2.

**Ans.** Refer Q. 1.10.





## Semiconductor Diode (2 Marks Questions)

- 1.1. Why Si is preferred over Ge for manufacturing of electronics devices ?

**AKTU 2015-16(Sem-I), Marks 02**

**Ans.** Si is preferred over Ge for manufacturing of electronic devices due to following reasons :

- Silicon is available in plenty amount on the surface of earth. This is the main reason why silicon is very much used by semiconductor device manufacturers.
- Cheaper.
- Smaller leakage current.
- Suitable for low power and high power applications.

- 1.2. Explain the effect of temperature on conductivity of a semiconductor.

**AKTU 2015-16(Sem-I), Marks 02**

**Ans.** In intrinsic semiconductor, as temperature increases the mobility of charge carrier reduces and this will reduce the conductivity by a smaller value and at the same time, a large number of covalent bond will be broken and a large number of electrons and holes are created and this will increase the conductivity by a large value.

- 1.3. Distinguish between avalanche and zener breakdown.

**AKTU 2016-17(Sem-I), Marks 02**

**AKTU 2013-14(Sem-II), Marks 02**

**Ans.**

S.No.	Zener breakdown mechanism	Avalanche breakdown mechanism
1.	This breakdown mechanism occurs in very thin junction.	This breakdown mechanism occurs in slightly thick junction.
2.	Zener current is independent of applied voltage.	Avalanche breakdown occurs at high voltages.
3.	Temperature coefficient is negative i.e., $-1.4 \text{ mV}/^\circ\text{C}$ .	Temperature coefficient is positive i.e., $2\text{mV}/^\circ\text{C}$ .

1.4. Differentiate between Transition capacitance ( $C_T$ ) and Diffusion capacitance ( $C_D$ ) of a  $p-n$  junction diode.

Ans.

S.No.	Transition capacitance ( $C_T$ )	Diffusion capacitance ( $C_D$ )
1.	This capacitance is obtained in reverse biased connection of $p-n$ junction.	This capacitance is obtained in forward biased connection of $p-n$ junction.
2.	Transition capacitance can be given as $C_T = \frac{K}{(V_R + V_K)^n}$ where, $V_K$ = knee voltage $V_R$ = applied reverse voltage $K$ = constant depending on semiconductor material $n$ = constant called the gradient coefficient.	Diffusion capacitance can be expressed as $C_D = \frac{\tau I}{\eta V_T}$ where, $\tau$ = mean life time of carrier $I$ = forward current $\eta$ = constant $V_T$ = volt equivalent of temperature

1.5. Draw the characteristics of transition and diffusion capacitance v/s applied bias voltage.

AKTU 2013-14(Sem-I), Marks 02

AKTU 2013-14(Sem-II), Marks 02

Ans.

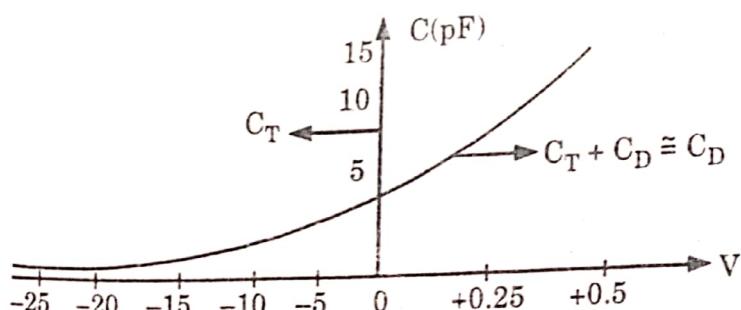


Fig. 1.5.1. Transition and diffusion capacitance versus applied bias for a silicon diode.

1.6. Calculate the dynamic forward and reverse resistance of a  $p-n$  junction diode when the applied voltage is 0.25 V at

$T = 300\text{ K}$  given  $I_0 = 2\text{ }\mu\text{A}$ . [AKTU 2013-14(Sem-II), Marks 02]

**Ans:**

Given :  $V = 0.25$  V,  $T = 300$  K,  $I_O = 2 \mu\text{A}$  at  $T = 300$  K  
 To Find : Dynamic forward and reverse resistance.

...(1.6.1)

We know,  $I = I_O (e^{V/\eta V_T} - 1)$

$$\text{where, } V_T = \frac{T}{11600} = \frac{300}{11600} = 26 \text{ mV}$$

Assuming diode is a germanium diode, therefore  $\eta = 1$

Putting all given values in eq. (1.6.1),

$$I = 2 \times 10^{-6} \left( e^{\frac{0.25}{1 \times 26 \times 10^{-3}}} - 1 \right) = 0.0299 \text{ A} \approx 0.03 \text{ A}$$

Now dynamic forward resistance,  $r_f = \frac{\eta V_T}{I}$

$$r_f = \frac{1 \times 26 \times 10^{-3}}{0.03} = 0.867 \Omega$$

Dynamic reverse resistance,  $r_r = \frac{V}{I_o} = \frac{0.25}{2 \times 10^{-6}} = 125 \text{ k}\Omega$

**1.7. Draw the V-I characteristic of a zener diode regulates the voltages.**

**Ans:**

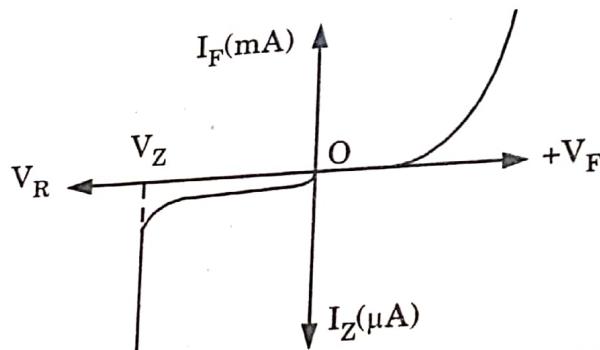


Fig. 1.7.1. V-I characteristic of zener diode.

**1.8. Compare the properties of Si and Ge Semiconductors.**

AKTU 2015-16(Sem-II), Marks 02

**Ans:**

S. No.	Properties	Si	Ge
1.	Conductivity.	Comparatively low.	Conductivity is comparatively higher.
2.	Atomic radius.	Has a smaller atomic radius than germanium.	Has comparatively a larger atomic radius.

**1.9. Define depletion layer in a diode.**

**AKTU 2015-16(Sem-II), Marks 02**

**OR**

**Define depletion layer of PN junction diode.**

**AKTU 2015-16(Sem-I), Marks 02**

**Ans.** The region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.

**1.10. Define bulk resistance of the diode.**

**AKTU 2015-16(Sem-II), Marks 02**

**Ans.** Bulk resistance of diode depends on how it is biased. It is the approximate resistance of diode when it is forward biased.

**1.11. Calculate the dynamic forward resistance of p-n junction diode when applied voltage is 0.80 V at temperature of 43 degree celsius and reverse saturation current is 8 microampere ?**

**AKTU 2016-17(Sem-I), Marks 02**

**Ans.** The procedure is same as Q. 1.6, Page SQ-2D, Unit-1, 2 Marks Questions.

$$\text{Ans. } r_f = 6 \times 10^{-10} \Omega.$$

**1.12. Classify the materials with help of energy band.**

**AKTU 2016-17(Sem-II), Marks 02**

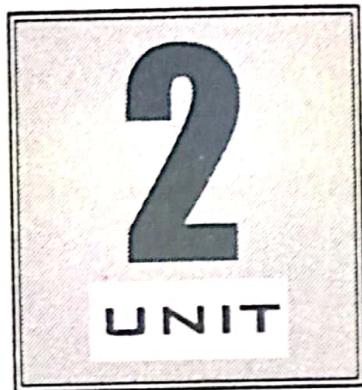
**Ans.** On the basis of energy band diagram, materials are classified into three types :

1. **Insulators** : In insulators, valence band is full and conduction band is empty. The energy gap between valence and conduction band is very large.
2. **Conductors** : In case of conductors, the valence and conduction bands overlap each other.
3. **Semiconductors** : In case of semiconductors, the valence band is almost full and conduction band is almost empty, also the energy gap between valence and conduction band is very small.



2

UNIT



## Diode Applications

### CONTENTS

- Part-1 :** Diode Application : Series, ..... 2-2D to 2-6D  
Parallel and Series, Parallel  
Diode Configuration
- Part-2 :** Half and Full Wave Rectifier ..... 2-6D to 2-17D
- Part-3 :** Clippers, Clampers ..... 2-17D to 2-29D
- Part-4 :** Zener Diode as Shunt Regulator ..... 2-29D to 2-34D
- Part-5 :** Voltage Multiplier Circuits ..... 2-34D to 2-37D
- Part-6 :** Special Purpose two ..... 2-38D to 2-46D  
Terminals Devices : Light  
Emitting Diodes, Varactor  
(Varicap) Diodes, Tunnel Diodes,  
Liquid Crystal Displays

## PART- 1

*Diode Application : Series, Parallel and Series, Parallel Diode Configuration.*

## Questions-Answers

## Long Answer Type and Medium Answer Type Questions

**Que 2.1.** Explain the series diode configuration.

**Answer**

1. The series circuit of diode is shown in Fig. 2.1.1.
2. The state of the diode is first determined by replacing the diode with a resistive element as shown in Fig. 2.1.2(a). The resulting direction of  $I$  is a match with the arrow in the diode symbol and since  $E > V_K$ , the diode is in the "ON" state.
3. The network is then redrawn as shown in Fig. 2.1.2(b) with the appropriate equivalent model for the forward biased silicon diode.

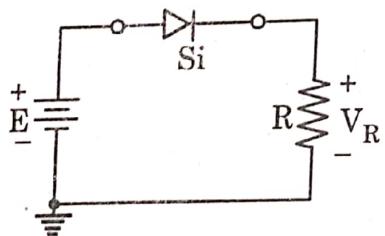


Fig. 2.1.1. Series diode configuration.

4. The resulting voltage and current level are the following :

$$V_D = V_K$$

$$V_R = E - V_K$$

$$I_D = I_R = \frac{V_R}{R}$$

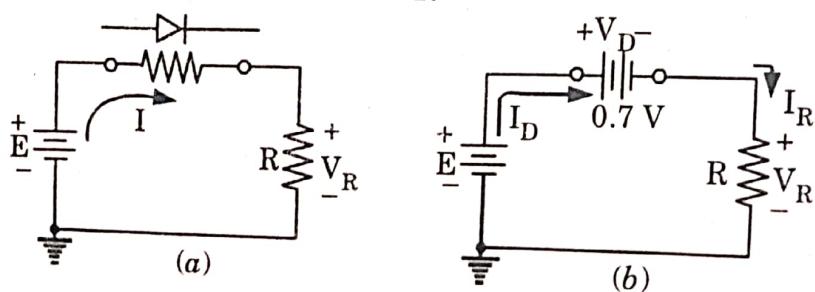


Fig. 2.1.2.

5. In Fig. 2.1.3 the diode is reversed. Replacing the diode with a resistor element as shown in Fig. 2.1.4 (a) will reveal that the resulting current direction does not match the arrow in the diode symbol.

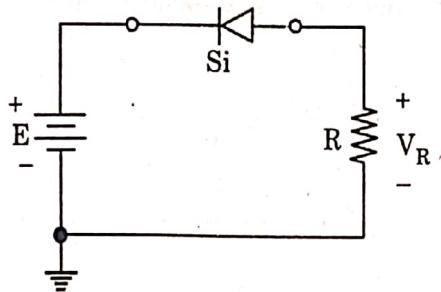


Fig. 2.1.3. Reversing the diode.

6. The diode is in the "OFF" state, resulting in the equivalent circuit of Fig. 2.1.4(b).  
 7. Due to open circuit, the diode current is 0 A and the voltage across the resistor  $R$  is the following :

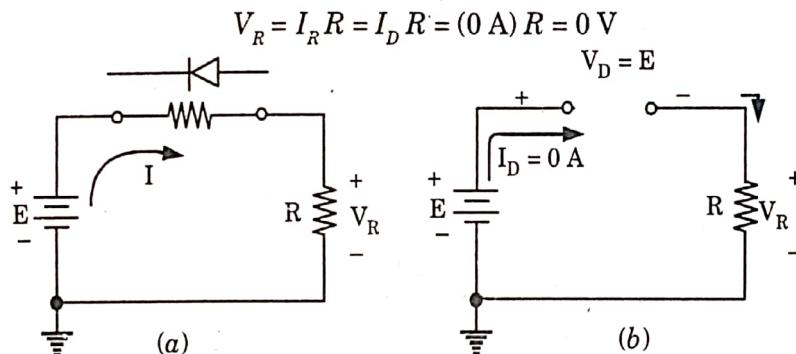


Fig. 2.1.4.

**Que 2.2.** Determine  $V_o$ , and draw the output waveform of the given network of Fig. 2.2.1.

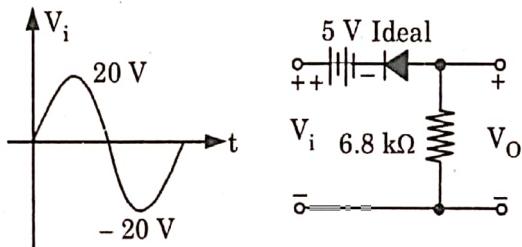


Fig. 2.2.1.

**AKTU 2015-16(Sem-I), Marks 05**

**Answer**

- For  $V_i \leq 5$  V, the 5 V battery will ensure the diode is forward-biased and  $V_o = V_i - 5$  V.
- At  $V_i = 5$  V

3. At  
 $V_O = 5 \text{ V} - 5 \text{ V} = 0 \text{ V}$   
 $V_i = -20 \text{ V}$   
 $V_O = -20 \text{ V} - 5 \text{ V} = -25 \text{ V}$
4. For  $V_i > 5 \text{ V}$ , the diode is reverse-biased and  $V_O = 0$ .

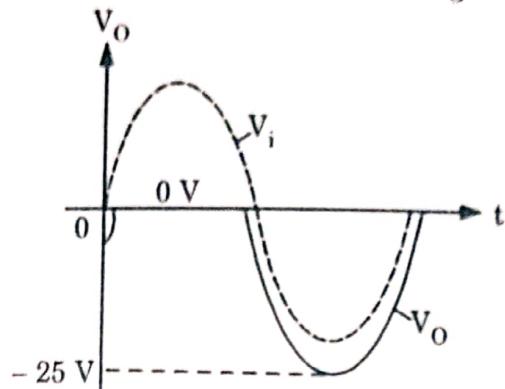


Fig. 2.2.2.

**Que 2.3.** For the circuit shown in Fig. 2.3.1, determine  $I_1, I_2, I_3, I_4, V_O$ .

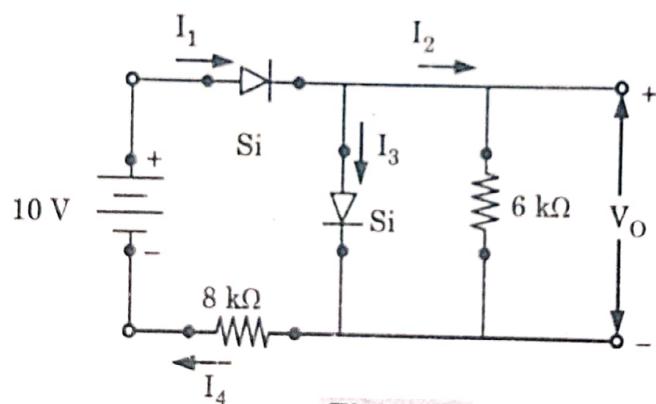


Fig. 2.3.1.

AKTU 2016-17(Sem-I), Marks 05

**Answer**

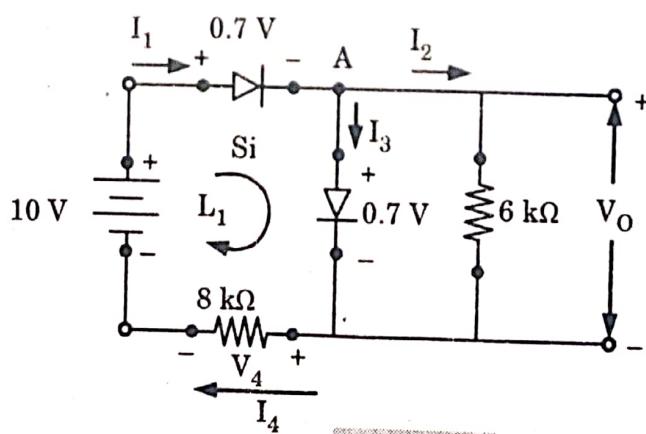


Fig. 2.3.2.

$$I_2 = \frac{0.7 \text{ V}}{6 \text{ k}\Omega} = 0.1167 \text{ mA}$$

$$V_O = 0.7 \text{ V}$$

Voltage across  $8 \text{ k}\Omega$ , applying KVL in loop  $L_1$ ,

$$-V_4 + 10 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} = 0$$

$$V_4 = 8.6 \text{ V}$$

$$\text{We have, } I_4 = \frac{V_4}{R} = \frac{8.6 \text{ V}}{8 \text{ k}\Omega} = 1.075 \text{ mA}$$

$$I_4 = I_1 = 1.075 \text{ mA}$$

Apply KCL at node A,  $I_3 = I_1 - I_2 = 1.075 \text{ mA} - 0.1167 \text{ mA}$

$$I_3 = 0.96 \text{ mA}$$

**Que 2.4.** Sketch  $V_O$  of the following network as shown in Fig. 2.4.1.

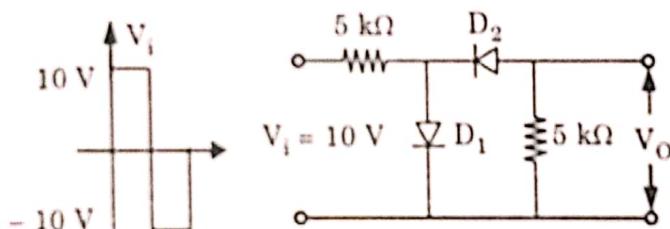


Fig. 2.4.1.

AKTU 2013-14(Semi-II), Marks 05

**Answer**

- When  $V_i = 10 \text{ V}$ ,  $D_1$  is forward biased and  $D_2$  is reverse biased and hence  $D_2$  does not conduct.
- The circuit will be as shown in Fig. 2.4.2 and output will be 0 V.

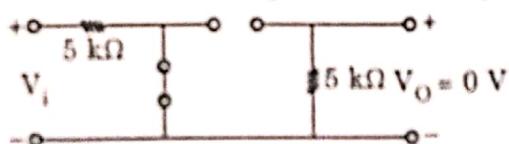


Fig. 2.4.2.

- When  $V_i = -10 \text{ V}$ , Diode  $D_1$  does not conduct and  $D_2$  conducts, and circuit will be as shown in Fig. 2.4.3.
- Using voltage-divider rule,  $V_O = \frac{5 V_i}{5 + 5} = \frac{5 \times -10}{5 + 5} = -5 \text{ V}$

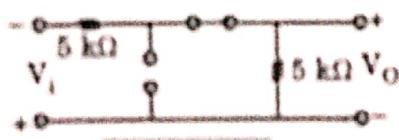
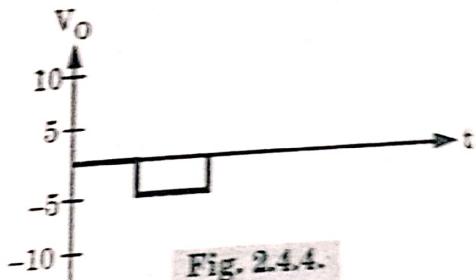


Fig. 2.4.3.

**PART-2***Half and Full Wave Rectifier.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.5.** Explain the working of half wave and full wave bridge rectifier. What are the advantages of full wave rectifier ?

OR

Explain the bridge rectifier with clear diagram.

**AKTU 2017-18 (Sem-I), Marks 3.5**

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveform.

**AKTU 2016-17 (Sem-I), Marks 05****Answer**

1. **Half wave rectifier :** It is shown in Fig. 2.5.1. As the name signifies only half portion of input is rectified (either positive half or negative half). Only single diode and a step down transformer are required for this circuit.

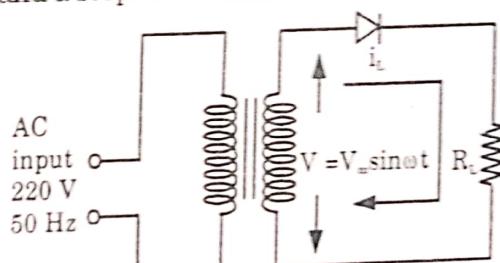


Fig. 2.5.1. Half wave rectifier circuit.

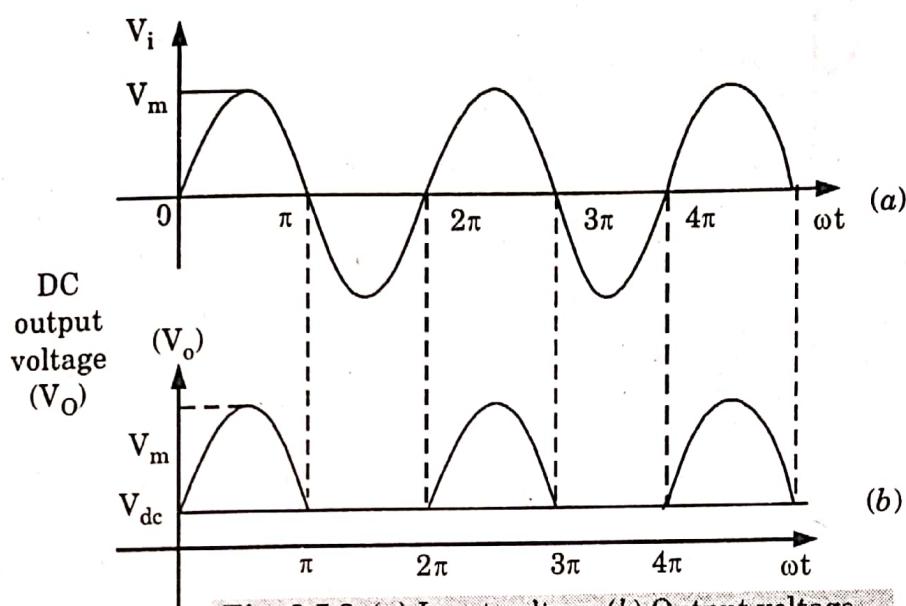


Fig. 2.5.2. (a) Input voltage (b) Output voltage.

2. **Full wave rectifier :** This circuit gives the output for full cycle (*i.e.*, for both positive and negative half cycles). There are two types of circuits used for it :
- Center tap rectifier :**

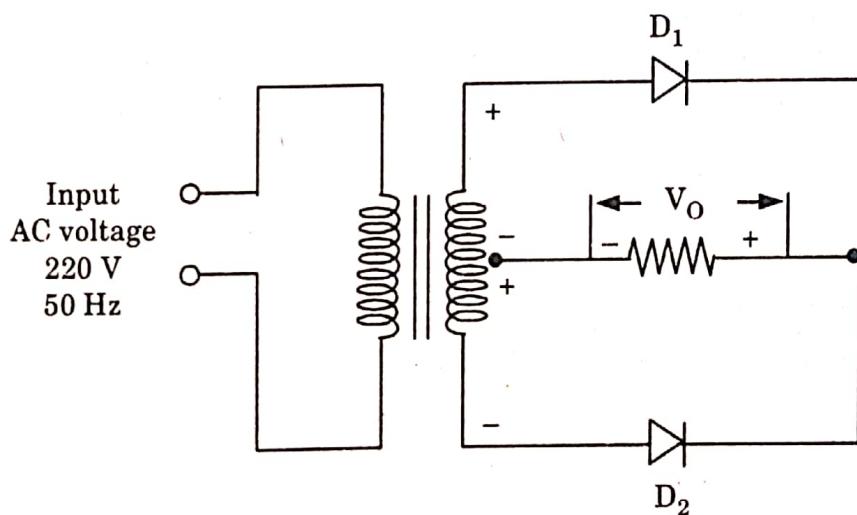


Fig. 2.5.3. Full wave rectifier.

- In center-tap full wave rectifier circuit, diode  $D_1$  will be ON for positive half cycle (*i.e.*,  $0$  to  $\pi$ ) and the diode  $D_2$  will be OFF during this cycle.
- The diode  $D_2$  will be ON for negative half cycle (*i.e.*,  $\pi$  to  $2\pi$ ) while the diode  $D_1$  will be OFF during this cycle.
- The input and output waveforms are shown in Fig. 2.5.4.

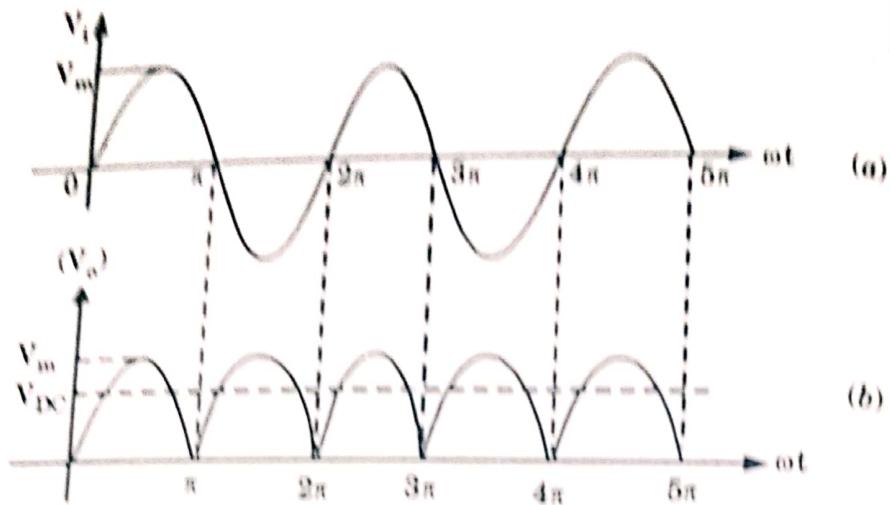
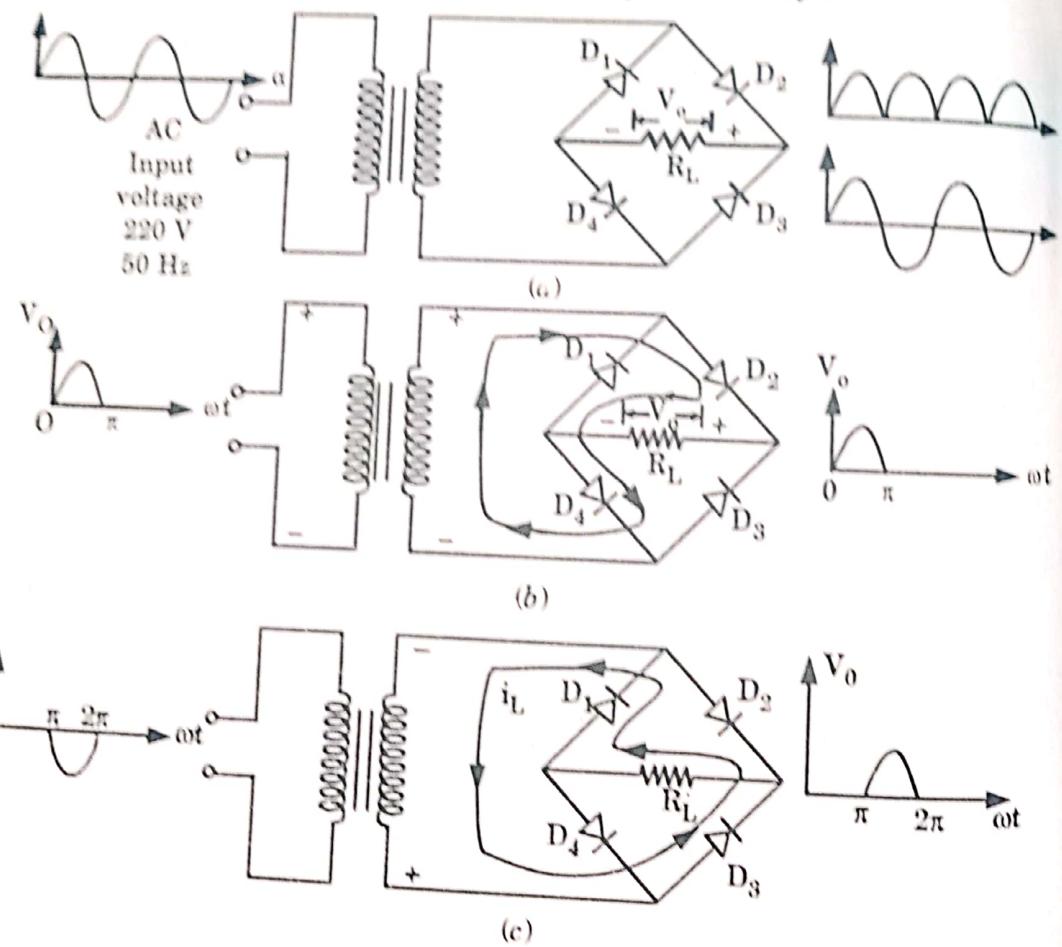
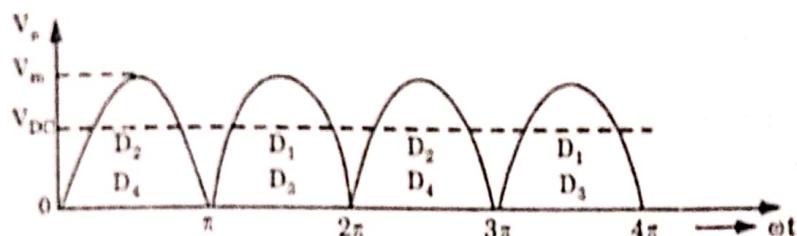


Fig. 2.5.4, (a) Input waveform (b) Output waveform.

- ii. **Bridge rectifier :** As shown in Fig. 2.5.5(b) only diodes  $D_2$  and  $D_4$  are active during positive half cycle while diodes  $D_1$  and  $D_3$  are active for negative half cycle as shown in Fig. 2.5.5(c) and Fig. 2.5.5(d) shows the total output with the active diodes for a particular cycle.





**Fig. 2.5.5.** (a) Basic bridge rectifier circuit  
 (b) Output of bridge rectifier for positive half cycle  
 (c) Output of bridge rectifier for negative half cycle.  
 (d) Output for full cycle.

#### Advantages of full wave rectifier :

1. Full wave rectifiers are more efficient than half wave rectifier. The maximum efficiency of full wave rectifier is 81.2 % while the maximum efficiency of half wave rectifier is 40.6 %.
2. The output waveform of full wave rectifier has fewer ripples.
3. Full wave rectifiers have higher transformer utilization factor (TUF) and higher output power than half wave rectifier.

**Que 2.6.** Explain the following terms in context with half wave rectifier and full wave rectifier :

- i. PIV (Peak Inverse Voltage)
- ii. DC voltage and DC current
- iii. RMS value of current
- iv. Ripple factor
- v. Rectification efficiency

OR

For a half wave rectifier, derive an expression for ripple factor.

**AKTU 2015-16(Sem-II), Marks 7.5**

OR

Elucidate the operation of half wave rectifier in detail and derive the expression for ripple factor.

**AKTU 2014-15(Sem-I), Marks 05**

OR

Explain the operation of full wave bridge rectifier with the help of a circuit diagram. Also sketch the input and output waveforms. Define its PIV. Also derive its ripple factor and rectification efficiency.

**AKTU 2017-18(Sem-II), Marks 07**

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveforms. What is PIV of bridge rectifier ?

**AKTU 2016-17(Sem-II), Marks 07**

**Answer****1. Half wave rectifier :**

**Operation :** Refer Q. 2.5, Page 2-6D, Unit-2.

**i. PIV:**

- As we know during negative half cycle, diode will be reverse biased and there will be no output voltage.
- In the negative half cycle the voltage across diode will be maximum when input reaches to its maximum value  $V_m$ . This maximum voltage during negative half cycle is called as the peak inverse voltage (PIV).
- PIV for half wave rectifier is given by

$$\text{PIV} = V_m$$

**ii. DC voltage and DC current :** Suppose current in load

$$\begin{aligned} i_L &= I_m \sin \omega t & 0 \leq \omega t \leq \pi \\ &= 0 & \pi \leq \omega t \leq 2\pi \end{aligned} \quad \dots(2.6.1)$$

Here,  $I_m$  = peak value of current  $i_L$

$$I_m = \frac{V_m}{R_L}$$

DC voltage for half wave rectifier,  $V_{DC} = I_{DC} \times R_L$

$$V_{DC} = \frac{I_m}{\pi} \times R_L$$

$$V_{DC} = \frac{V_m}{\pi} \quad \dots(2.6.2)$$

$$I_{DC} = \frac{I_m}{\pi} \quad \dots(2.6.3)$$

**iii. RMS value of current :** The rms value of the current flowing through the load is given as

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_L^2 d(\omega t)}$$

Replacing the value of  $i_L$  from eq. (2.6.1)

$$\begin{aligned} I_{rms} &= \sqrt{\frac{1}{2\pi} \left[ \int_0^\pi I_m^2 \cdot \sin^2 \omega t \cdot d(\omega t) + \int_\pi^{2\pi} 0 \cdot d(\omega t) \right]} \\ &= \sqrt{\frac{I_m^2}{2\pi} \int_0^\pi \frac{(1 - \cos 2\omega t)}{2} \cdot d(\omega t)} \\ &= \sqrt{\frac{I_m^2}{2\pi \times 2} \left| \omega t - \frac{\sin 2\omega t}{2} \right|_0^\pi} \end{aligned}$$

$$I_{rms} = \frac{I_m}{2} \quad \dots(2.6.4)$$

Eq. (2.6.4) gives total current (AC and DC)

Thus instantaneous value of AC in output is

$$\begin{aligned}
 i_{AC} &= i_L - I_{DC} \\
 (I_{AC})_{rms} &= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (i_L - I_{DC})^2 d(\omega t)} \\
 &= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (i_L^2 + I_{DC}^2 - 2i_L I_{DC}) d(\omega t)} \\
 &= \sqrt{I_{rms}^2 + I_{DC}^2 - 2I_{DC}^2} \\
 (I_{AC})_{rms} &= \sqrt{I_{rms}^2 - I_{DC}^2} \quad \dots(2.6.5)
 \end{aligned}$$

**iv. Ripple factor :** The ripple factor is given as

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

Since,  $I_{rms} = I_m/2$  and  $I_{DC} = I_m/\pi$ . So,  $r = 1.21$

**v. Rectification efficiency :** The efficiency is given as

$$\eta = \frac{\text{Output DC power}}{\text{Input AC power}} = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_L + r_d)}$$

where,  $R_L \rightarrow$  load resistance,  $r_d \rightarrow$  diode resistance

$$\begin{aligned}
 &= \frac{(I_m / \pi)^2 \cdot R_L}{(I_m / 2)^2 (r_d + R_L)} \\
 \eta &= 0.406 \quad (\because r_d \ll R_L) \\
 \eta &= 40.6 \%
 \end{aligned}$$

**2. Full wave rectifiers :**

**Operation and waveforms of full wave bridge rectifier :**

Refer Q. 2.5, Page 2-6D, Unit-2.

**i. RMS value of current :**

$$\begin{aligned}
 I_{rms} &= \sqrt{\frac{1}{\pi} \int_0^\pi I_L^2 d(\omega t)} = \sqrt{\frac{1}{\pi} \int_0^\pi I_m^2 \sin^2 \omega t d(\omega t)} \\
 &= \sqrt{\frac{I_m^2}{\pi} \int_0^\pi \frac{(1 - \cos 2\omega t)}{2} d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi} \left| \omega t - \frac{\sin 2\omega t}{2} \right|_0^\pi} \\
 I_{rms} &= \frac{I_m}{\sqrt{2}} \quad \dots(2.6.6)
 \end{aligned}$$

**ii. PIV (Peak Inverse Voltage) :** It is same as the half wave rectifier, but the value of PIV is different for center tap type full wave rectifier.

In centre tap full wave rectifiers,  $PIV = 2V_m$

In bridge type full wave rectifiers,  $PIV = V_m$

**iii. DC voltage and DC current :**

$$I_{DC} = \frac{1}{\pi} \int_0^{\pi} i_L d(\omega t) = \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t d(\omega t)$$

$$I_{DC} = \frac{2I_m}{\pi} \quad \dots(2.6.7)$$

$$V_{DC} = I_{DC} \times R_L$$

$$V_{DC} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi} \quad \dots(2.6.8)$$

**iv. Ripple factor :**

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1}$$

$$r = 0.482$$

**v. Rectification efficiency :**

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{(2I_m/\pi)^2 R_L}{(I_m/\sqrt{2})^2 (r_d + R_L)} \times 100 \% \\ = 81.2 \% \quad (\because r_d \ll R_L)$$

**Que 2.7.** Differentiate between half wave and full wave rectifiers.

**AKTU 2015-16(Sem-I), Marks 05**

**Answer**

S. No.	Full wave rectifier	Half wave rectifier
1.	Full wave rectifier is an electronic circuit which converts entire cycle of AC into Pulsating DC.	A Half-Wave rectifier is an electronic circuit which converts only one-half of the AC cycle into pulsating DC.
2.	Full-wave Rectifier, is bi-directional, it conducts for positive half as well as negative half of the cycle.	The Half-Wave Rectifier is unidirectional; it means it will allow the conduction in one direction only.
3.	Peak inverse voltage (PIV) is twice of the maximum value of supplied input.	Peak inverse voltage (PIV) is the maximum value of supplied input.
4.	Ripple factor is low.	Ripple factor is high.

**Que 2.8.** Sketch  $V_O$ ,  $V_{DC}$  for the network of Fig. 2.8.1, and determine the peak inverse voltage of each diode.

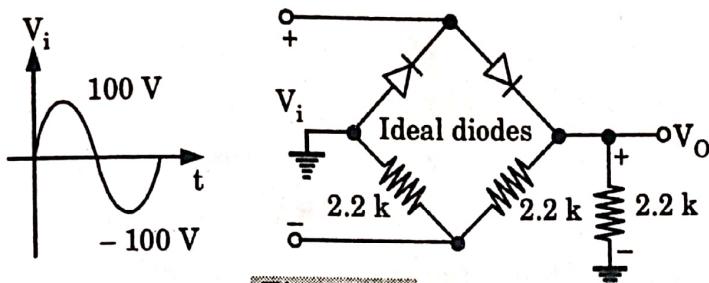


Fig. 2.8.1.

AKTU 2015-16(Sem-I), Marks 05

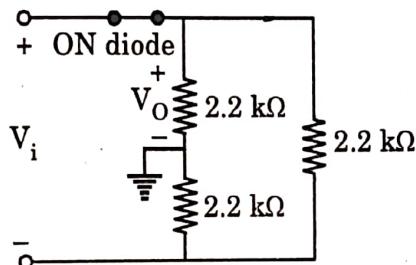
**Answer****For positive half-cycle of  $V_i$ :**

Fig. 2.8.2.

**Voltage divider rule :**

$$V_{o\max} = \frac{2.2 \text{ k}\Omega (V_{i\max})}{2.2 \text{ k}\Omega + 2.2 \text{ k}\Omega}$$

$$= \frac{1}{2} (V_{i\max}) = \frac{1}{2} (100 \text{ V}) = 50 \text{ V}$$

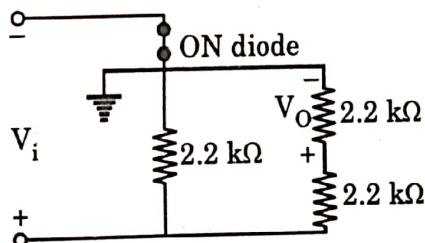
**For negative half cycle of  $V_i$ :**

Fig. 2.8.3.

Polarity of  $V_o$  across the  $2.2 \text{ k}\Omega$  resistor acting as a load is the same.  
Using voltage divider rule,

$$V_{o\max} = \frac{2.2 \text{ k}\Omega (V_{i\max})}{2.2 \text{ k}\Omega + 2.2 \text{ k}\Omega}$$

$$= \frac{1}{2} (V_{i\max}) = \frac{1}{2} (100 \text{ V}) = 50 \text{ V}$$

$$V_{DC} = 0.636 V_{o\max} = 0.636 (50 \text{ V}) = 31.8 \text{ V}$$

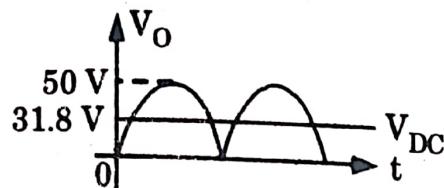


Fig. 2.8.4.

Peak inverse voltage of each diode =  $V_m = 100 \text{ V}$

**Que 2.9.** Determine the output waveform for the given network as shown in Fig. 2.9.1. Determine the output DC level and compute PIV for each diode.

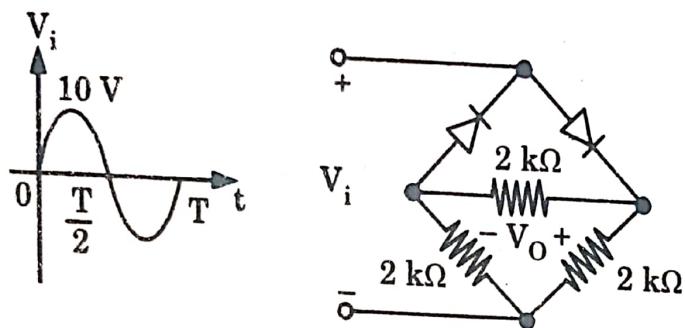


Fig. 2.9.1.

AKTU 2017-18(Sem-II), Marks 07

### Answer

For positive half-cycle of  $V_i$ :

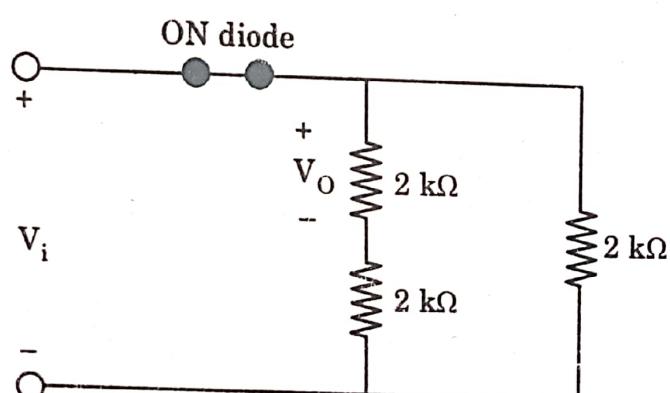


Fig. 2.9.2.

Using voltage divider rule,

$$V_{O\max} = \frac{2 \text{ k}\Omega (V_{i\max})}{2 \text{ k}\Omega + 2 \text{ k}\Omega} = \frac{1}{2} (10 \text{ V}) = 5 \text{ V}$$

**For negative half-cycle of  $V_i$ :**

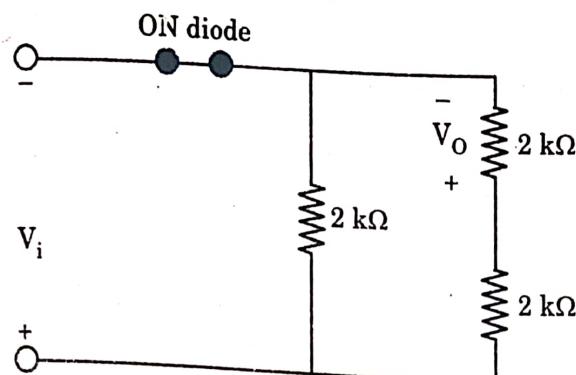


Fig. 2.9.3.

Using voltage divider rule,

$$V_{O\max} = \frac{2 \text{ k}\Omega (V_{i\max})}{2 \text{ k}\Omega + 2 \text{ k}\Omega} = \frac{1}{2} V_{i\max} = \frac{1}{2} (10) = 5 \text{ V}$$

$$V_{DC} = 0.636 V_{O\max} = 0.636 (5 \text{ V}) = 3.18 \text{ V}$$

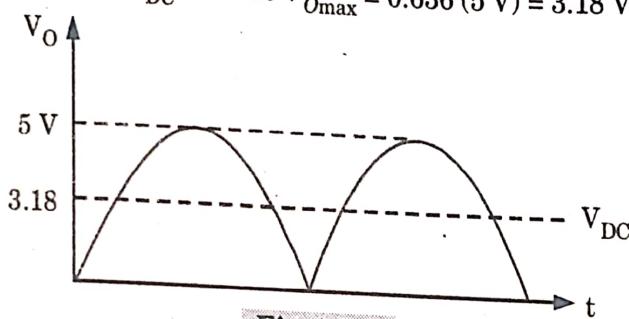


Fig. 2.9.4.

Peak inverse voltage of each diode =  $V_m = 10 \text{ V}$

**Que 2.10.** Draw a circuit diagram and explain the working of a Bridge type full wave rectifier with a forward resistance of  $20 \Omega$  each. A DC voltage across the load resistance of  $1 \text{ k}\Omega$  is  $50 \text{ V}$ . Determine the following factors :

i.  $I_{rms}$

ii. Ripple factor.

**AKTU 2013-14(Sem-I), Marks 10**

OR

Explain the operation of a bridge rectifier with the help of a circuit diagram and waveforms. Determine the DC load voltage and ripple factor.

**AKTU 2013-14(Sem-II), Marks 10**

OR

Draw and explain the working of a Bridge rectifier with input and output waveforms. Calculate efficiency and ripple factor.

**AKTU 2014-15(Sem-II), Marks 05**

**Answer**

**Bridge type full wave rectifier :** Refer Q. 2.5, Page 2-6D, Unit-2.  
**Numerical :**

**Given :**  $r_f = 20 \Omega$ ,  $R_L = 1 \text{ k}\Omega$ ,  $V_{DC} = 50 \text{ V}$

**To Find :** i.  $I_{rms}$  ii. Ripple factor.

$$\begin{aligned} \text{i. We know, } V_{DC} &= \frac{2V_m}{\pi} - I_{DC} r_f \\ I_{DC} &= \frac{2V_m}{\pi(r_f + R_L)} \\ \therefore V_{DC} &= \frac{2V_m}{\pi} \left[ 1 - \frac{r_f}{r_f + R_L} \right] \\ \frac{50\pi}{2} &= 0.98 V_m \\ V_m &= 80.1 \text{ V} \\ I_{DC} &= \frac{2 \times 80.1}{\pi(20 + 1000)} = \frac{160.2}{3204.4} \approx 50 \text{ mA} \\ I_{DC} &= \frac{2\sqrt{2} I_{rms}}{\pi} \\ I_{rms} &= 55.5 \text{ mA} \\ \text{ii. Ripple factor, } \Gamma &= \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{55.5}{50}\right)^2 - 1} = 0.482 \end{aligned}$$

**Efficiency, DC load voltage and ripple factor :** Refer Q. 2.6, Page 2-9D, Unit-2.

**Que 2.11.** Determine  $V_O$  and the required PIV rating of each diode for the configuration of Fig. 2.11.1

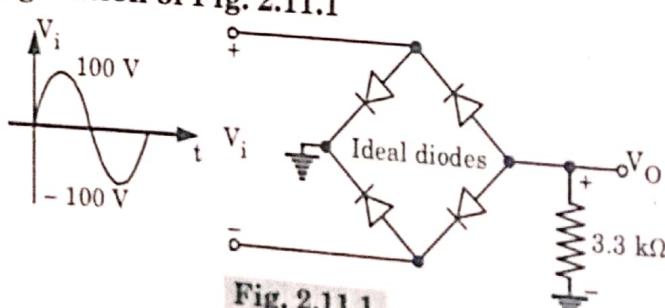


Fig. 2.11.1.

AKTU 2014-15(Sem-II), Marks 05

**Answer**

**Given :**  $V_m = 100 \text{ V}$ ,  $R_L = 3.3 \text{ k}\Omega$

**To Find :**  $V_m$ .

1. We know that peak value of load current is

$$I_m = \frac{V_m}{R_L}$$

$$I_m = \frac{100}{3.3 \times 10^3} = 30.30 \text{ mA}$$

2. Therefore,  $I_{DC} = \frac{2 I_m}{\pi}$

$$= \frac{2 \times 30.30 \times 10^{-3}}{\pi} = 19.29 \text{ mA}$$

3. The DC load voltage is

$$V_{DC} = I_{DC} \times R_L = 19.29 \text{ mA} \times 3.3 \text{ k}\Omega = 63.657 \text{ V}$$

Therefore,  $V_O = V_{DC} = 63.657 \text{ V}$

4. For the bridge rectifier, PIV for each diode is

$$\text{PIV} = V_m = 100 \text{ V}$$

**PART-3**

*Clippers, Clampers.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.12.** Draw a simple clipping circuit with suitable waveform

and explain types of clippers.

**AKTU 2014-15(Sem-I), Marks 05**

**Answer**

A wave shaping circuit which controls the shape of output waveform by removing (clipping) a portion of the applied wave is known as clipping circuit. For a clipping circuit at least one resistance and one diode is required.

**Types of clippers :** There are mainly two types of clippers i.e., positive and negative clippers. They are further divided into two categories :

## 1. Series clippers (for ideal diode) :

## a. Simple series clippers :

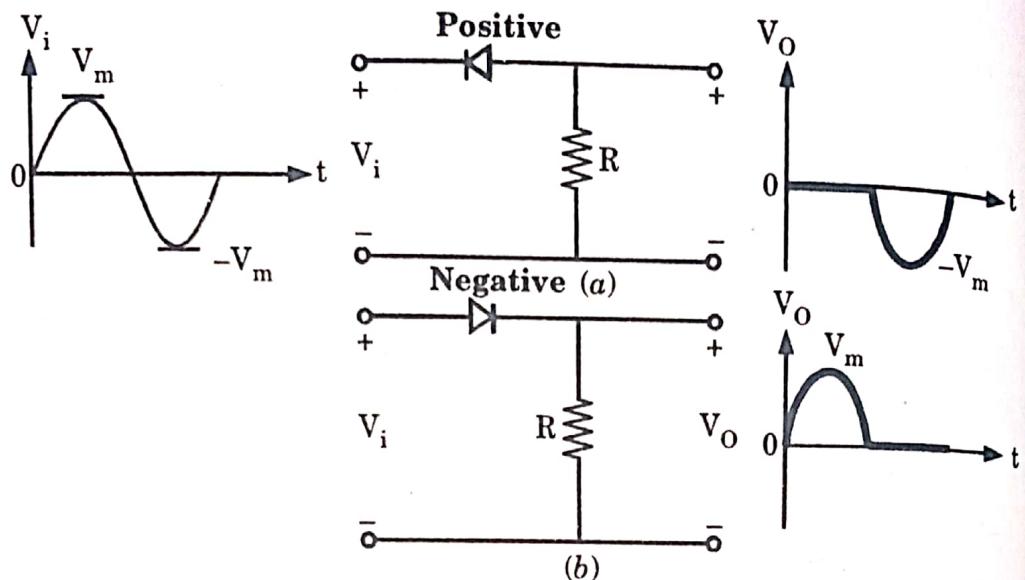


Fig. 2.12.1.

## b. Biased series clippers :

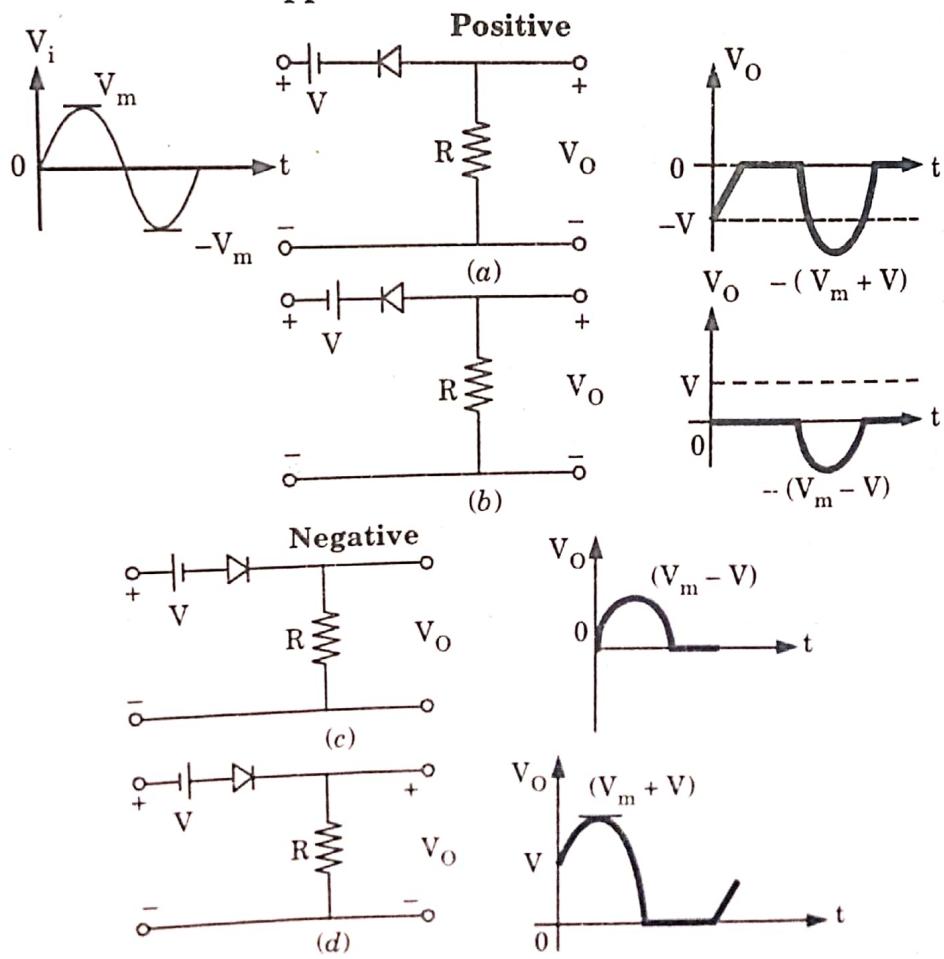


Fig. 2.12.2.

**2. Parallel clippers (for ideal diodes) :**  
**a. Simple parallel clippers :**

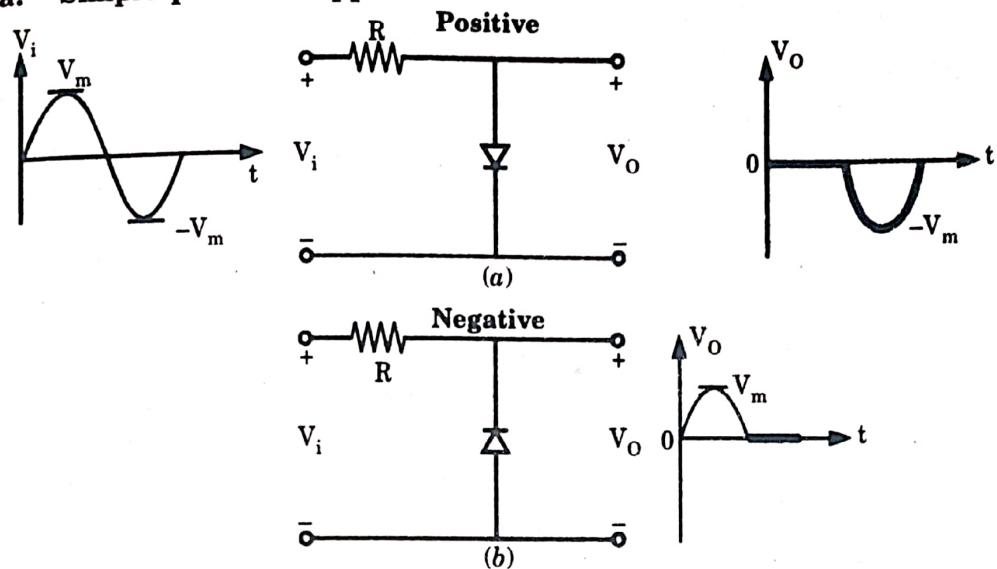


Fig. 2.12.3.

**b. Biased parallel clippers :**

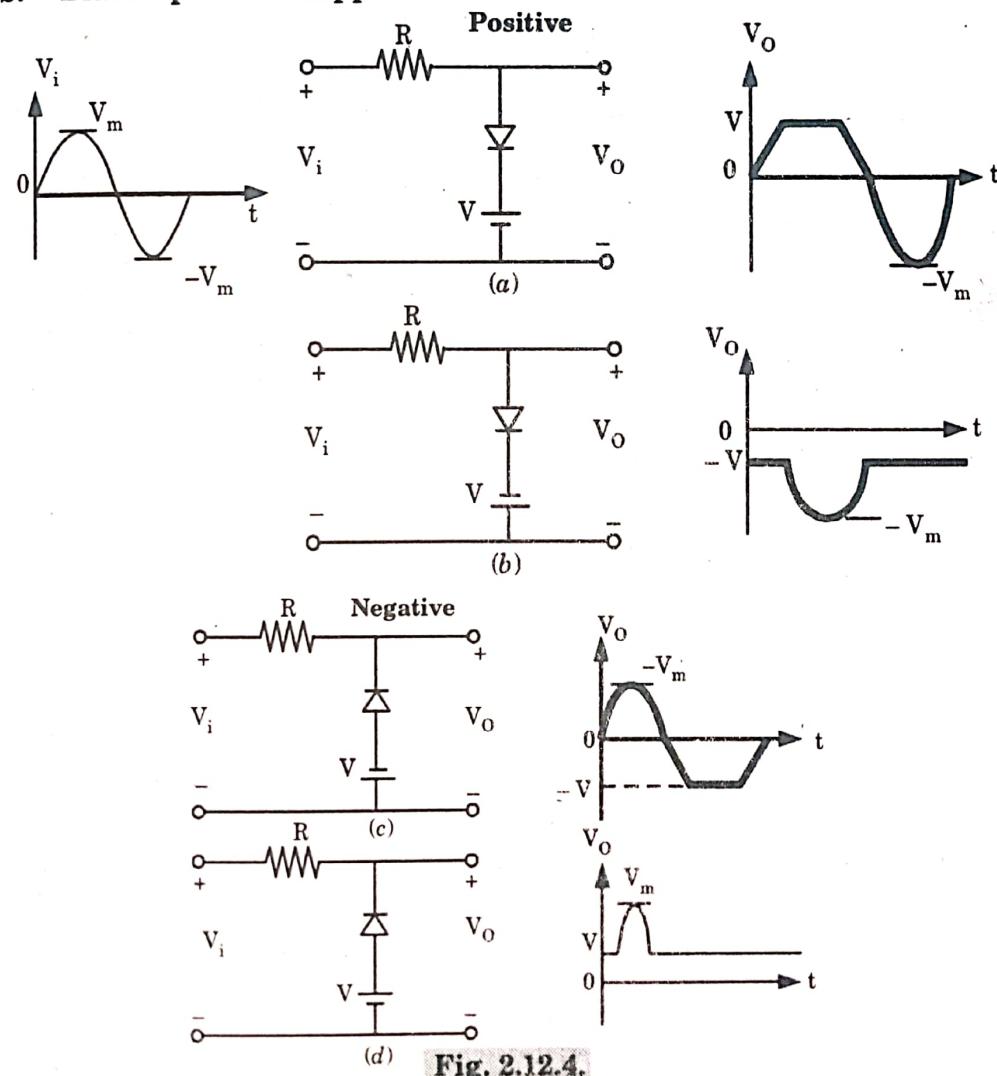
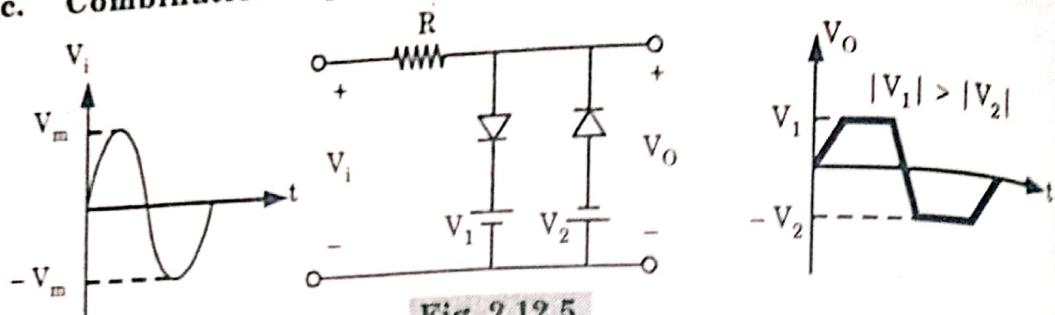


Fig. 2.12.4.

c. Combination clipper (Positive and Negative) :



**Que 2.13.** What do you mean by clamper circuit? What are the different types of clamper circuits?

**Answer**

A clamping circuit is a device that 'clamps' a signal to a different DC level. A clamping circuit must have a diode, a resistance and a capacitor, an independent DC supply is also required to introduce an additional shift.

**Types of clamper circuit:** There are two types of clamper circuits.

1. **Positive Clamper:** It shifts the original signal in vertical upward direction.

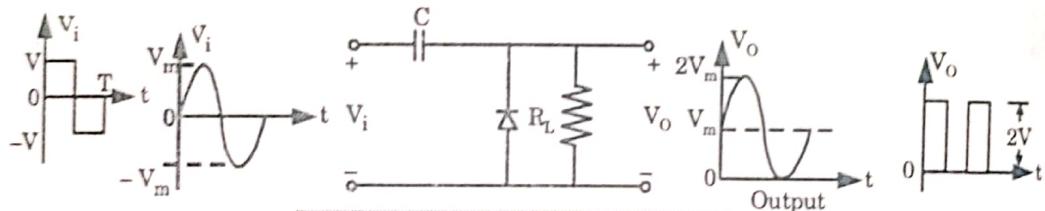


Fig. 2.13.1. Positive clamper.

$$\text{Output voltage } V_o = V_m + V_c = V_m + V_m = 2V_m$$

**Positive clamper with bias:**

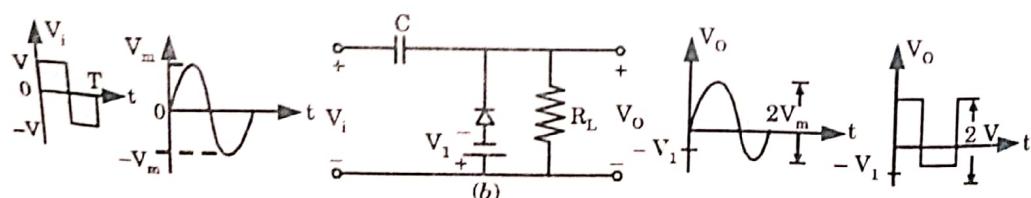
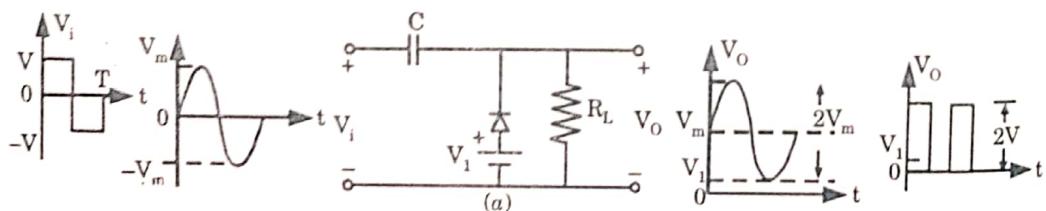


Fig. 2.13.2. (a) Positive clamper with positive biased,  
(b) Positive clamper with negative biased.

2. **Negative clamper:** It shifts the original signal in vertical downward direction.

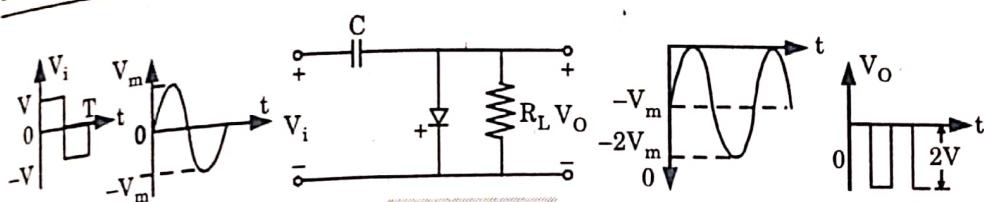


Fig. 2.13.3.

Negative clamper with bias

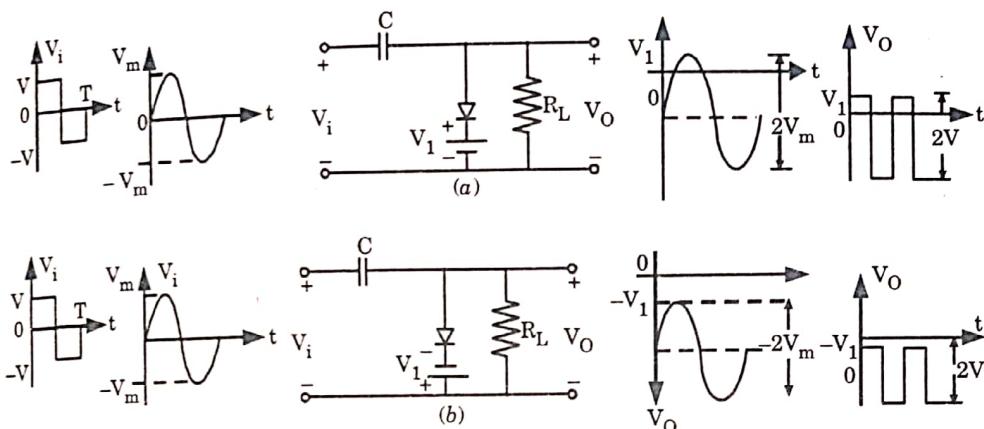


Fig. 2.13.4. (a) Negative clamper with positive bias,  
(b) Negative clamper with negative bias.

**Que 2.14.** Sketch  $V_O$  for each network of Fig. 2.14.1, for the input shown.

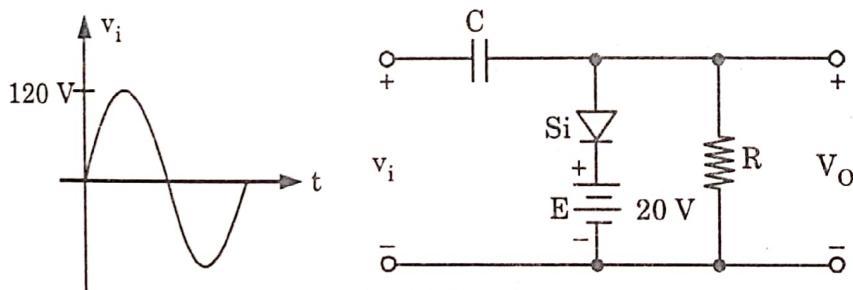


Fig. 2.14.1.

AKTU 2015-16(Sem-I), Marks 05

AKTU 2017-18(Sem-II), Marks 3.5

**Answer**

- For positive half cycle capacitor charges to peak value of  $120 \text{ V} - 20 \text{ V} - 0.7 \text{ V} = 99.3 \text{ V}$  with polarity (+ ↑ -). The output  $V_o = 20 \text{ V} + 0.7 \text{ V} = 20.7 \text{ V}$ .
- For next negative half cycle  $V_o = V_i - 99.3 \text{ V}$  with negative peak value of  $V_o = -120 \text{ V} - 99.3 \text{ V} = -219.3 \text{ V}$ .

2-22 D (ESC-Sem-3 & 4)

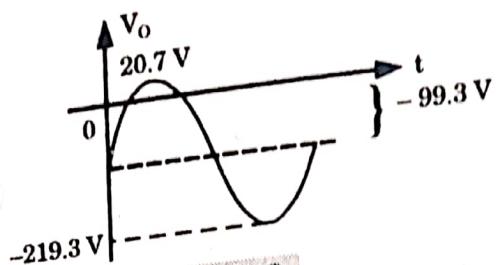


Fig. 2.14.2.

**Que 2.15.** Design a clamper to perform the function indicated in Fig. 2.15.1.

Fig. 2.15.1.

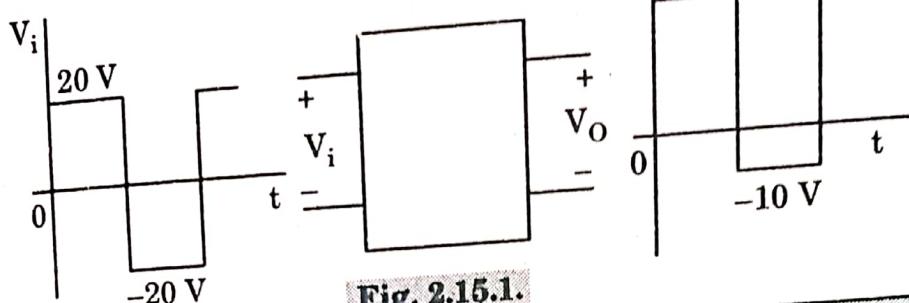


Fig. 2.15.1.

AKTU 2016-17(Sem-II), Marks 5.25

**Answer**

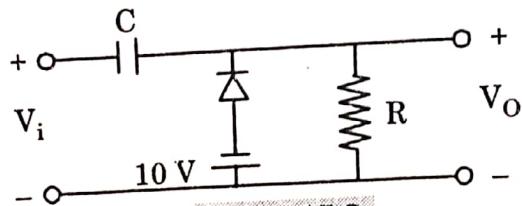


Fig. 2.15.2.

**During positive half cycle :**

$$V_o = V_i + V_c + (-10) = V_m + V_m - 10 = 20 + 20 - 10 = 30 \text{ V}$$

**During negative half cycle :**

$$V_o = -10 \text{ V}$$

**Que 2.16.** Sketch  $V_o$  for the given network shown in Fig. 2.16.1 for the input shown.

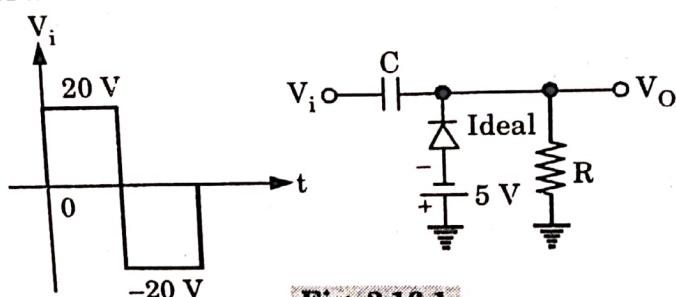


Fig. 2.16.1.

AKTU 2014-15(Sem-II), Marks 05

**Answer**

1. Fig. 2.16.1 can be modified as Fig. 2.16.2.

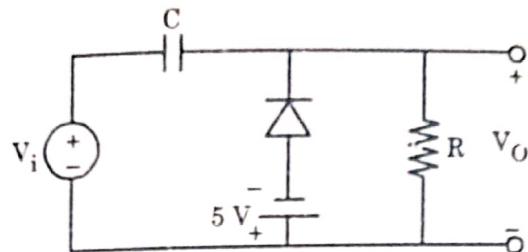


Fig. 2.16.2.

2. During positive half cycle, the diode is reverse biased and acts as an open circuit.

Applying KVL, we get

$$V_i + V_C + (-5) = V_O$$

$$V_O = 20 + 20 - 5 = 35 \text{ V}$$

3. During negative half cycle, diode is forward biased and acts as short circuit.

Applying KVL, we get

$$V_O = -5 \text{ V}$$

4. Fig. 2.16.3 shows output waveform

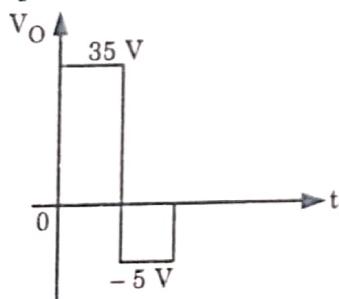


Fig. 2.16.3. Output waveform.

- Que 2.17.** Define clipper circuit. Sketch the output waveform for the circuit shown below given input.

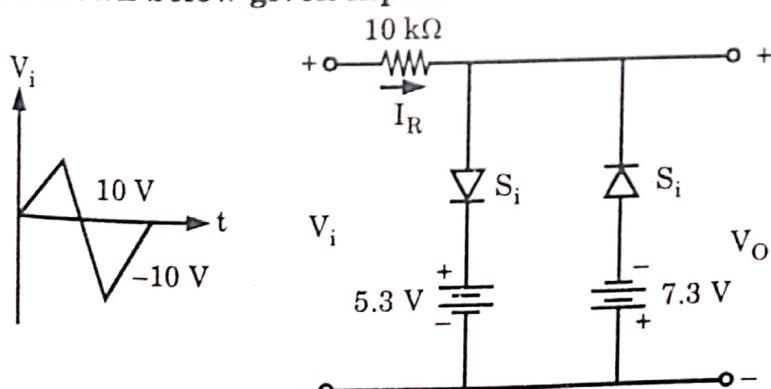


Fig. 2.17.1.

AKTU 2017-18(Sem-II), Marks 07

**Answer**

**Clipper :** Refer Q. 2.12, Page 2-17D, Unit-2.

- During positive half cycle of  $V_i$  :  
when  $0 < V_i < 6 \text{ V}$ , then both diode  $D_1$  and  $D_2$  will be reverse biased and output will follow input voltage.  
*i.e.,*  $V_o = V_i$
- When  $V_i > 6 \text{ V}$ , then  $D_1$  will be forward biased and  $D_2$  will be reverse biased.  
So,  $V_o = 0.7 + 5.3 = 6 \text{ V} (\text{constant})$
- The current  $i_R$  will flow only when either of the two diodes will be forward biased.

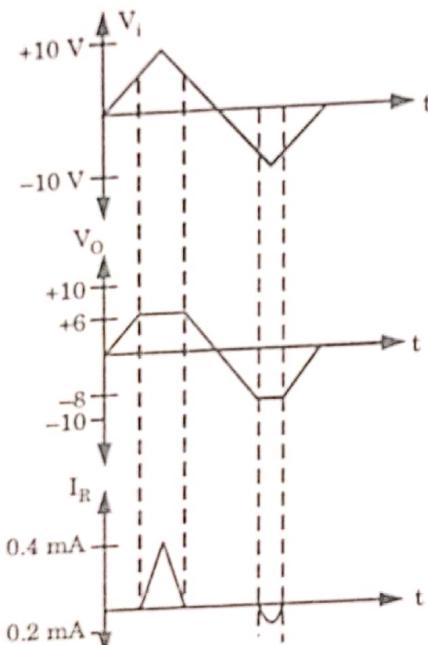


Fig. 2.17.2.

- For  $V_{in} = 10 \text{ V}$

$$I_R = \frac{V_{in} - 0.7 - 5.3}{10 \text{ k}\Omega} = \frac{10 - 6}{10 \text{ k}\Omega} = 0.4 \text{ mA (Peak).}$$

- During negative half cycle of  $V_i$  :  
when  $-7 \text{ V} < V_i < 0$ , both diodes will be reverse biased so output will follow input voltage *i.e.*,  $V_o = V_i$
  - When  $V_i < -8 \text{ V}$ , then  $D_1$  will be reverse biased and  $D_2$  will be forward biased  
*i.e.*  $V_o = -(0.7 + 6.3) = -8 \text{ V} (\text{constant})$   
So,  
For  $V_{in} = -10 \text{ V}$
- $$I_R = \frac{V_{in} + 0.7 + 7.3}{10 \text{ k}\Omega} = \frac{-10 + 8}{10 \text{ k}\Omega} = -0.2 \text{ mA.}$$

- The waveforms for  $V_o$  and  $I_R$  are shown in Fig. 2.17.2.

**Que 2.18.**

- Determine the current  $I_{D1}$  as shown in Fig. 1.18.1(a). Assume that the diodes are ideal.
- Determine the peak load and dc load voltage for the given rectifier as shown in Fig. 1.18.1(b).

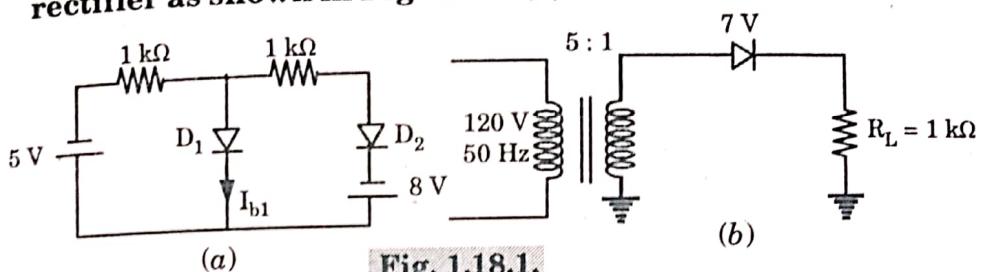


Fig. 1.18.1.

AKTU 2013-14(Sem-I), Marks 10

**Answer**

- In the given circuit, diode  $D_1$  will never be forward biased therefore it will always act as open circuit

$$\therefore I_{D1} = 0$$

- Given,  $V_{rms} = 120$ ,  $N_1 : N_2 = 5 : 1$

$$\text{Maximum primary voltage, } V_{pm} = \sqrt{2} V_{rms} = \sqrt{2} \times 120 = 169.7 \text{ V}$$

Maximum secondary voltage,

$$V_{sm} = V_{pm} \times \frac{N_2}{N_1} = 169.7 \times \frac{1}{5} = 33.94 \text{ V}$$

$$\text{DC load voltage, } V_{dc} = \frac{V_{sm}}{\pi} = \frac{33.94}{\pi} = 10.8 \text{ V}$$

$$\text{Peak load voltage, } V_{sm} = 33.94 \text{ V}$$

- Que 2.19.** Explain the function of the circuit of Fig. 2.19.1 and draw the output waveform.

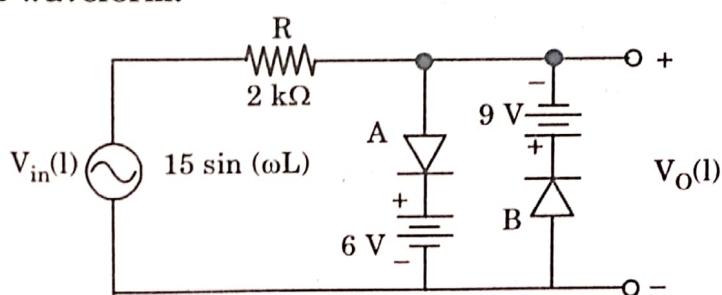


Fig. 2.19.1.

AKTU 2015-16(Sem-II), Marks 7.5

**Answer**

- During positive half cycle

## 2-26 D (ESC-Sem-3 &amp; 4)

- i. **Case-1 :** When  $V_{in} < 6 \text{ V}$   
Diode A and B, both are reverse biased  
 $V_O = V_{in}$
- ii. **Case-2 :** When  $V_{in} > 6 \text{ V}$   
Diode A is forward biased, diode B is reverse biased  
 $V_O = 6 \text{ V}$
- 2. During negative half cycle
- i. **Case-1 :** When  $V_{in} < -9 \text{ V}$   
Diode A and B, both are reverse biased  
 $V_O = V_{in}$
- ii. **Case-2 :** When  $V_{in} > -9 \text{ V}$   
Diode A is reverse biased, diode B is forward biased  
 $V_O = -9 \text{ V}$

**Que 2.20.** For the given clamper circuit shown in Fig. 2.20.1, determine the output voltage and also draw the waveform of output signal.

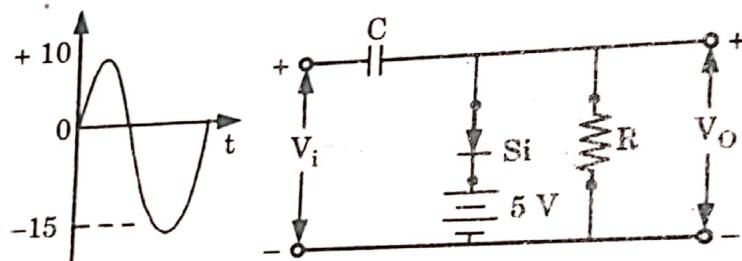


Fig. 2.20.1.

AKTU 2016-17(Sem-I), Marks 05

**Answer**

1. During positive pulse of  $V_i$ , the diode is short circuited. The voltage across  $R$  will be the same as across the battery (parallel). So,  
 $V_O = 5 \text{ V}$
2. The voltage that charge up the capacitor, applying KVL  
 $+10 \text{ V} - V_c - 5 \text{ V} = 0$ , then  $V_c = 5 \text{ V}$
3. During negative pulse of  $V_i$ , the diode is open circuited. Applying KVL,

$$V_O = -15 - 5 = -20 \text{ V}$$

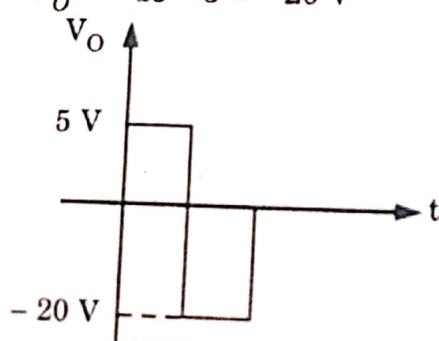


Fig. 2.20.2.

**Que 2.21.** Draw the output waveform for the following circuits for the input waveforms, given in Fig. 2.21.1(a) and (b) :

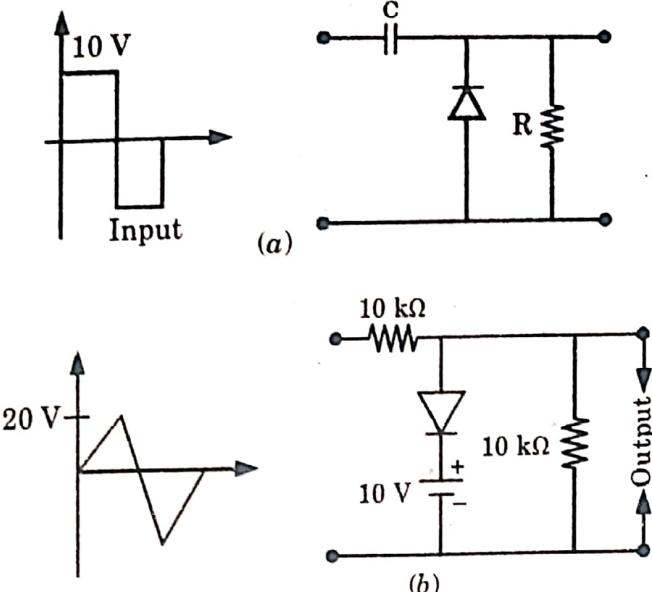


Fig. 2.21.1.

AKTU 2013-14(Sem-I), Marks 10

**Answer**

For Fig. 2.21.1 (a),

During negative cycle of input :

1. Diode will be ON, capacitor starts charging with polarity as shown in Fig. 2.21.2.

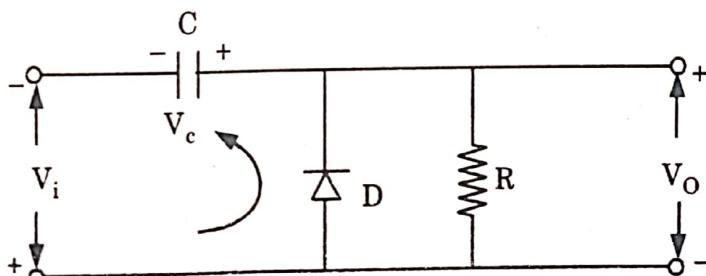


Fig. 2.21.2.

2. The diode will act as short circuit, therefore  

$$V_o = 0 \text{ and } V_c = +10 \text{ V}$$

During positive half cycle :

1. Diode D will be OFF.
2. Now, capacitor will work as battery of 10 V and discharge through 'R'.
3. Apply KVL  $V_i + V_c - V_R = 0$   

$$V_R = V_i + V_c = 10 + 10 = 20 \text{ V}$$
4. So output voltage,  $V_o = 20 \text{ V}$

5. In short,       $V_o = 20 \text{ V}$       (for positive half cycle)  
 $V_o = 0$       (for negative half cycle)

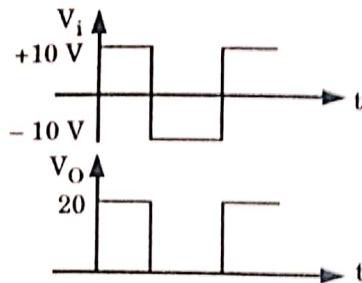


Fig. 2.21.3.

**Output waveform of Fig. 2.21.1 (b) :**

1. During positive half cycle,
- i. **Case-1 :** when  $V_i < 10 \text{ V}$   
Diode D will be reverse biased and act as open circuit  
 $V_o = V_i$
- ii. **Case-2 :** when  $V_i > 10 \text{ V}$   
Diode D will be forward biased and act as short circuit  
 $V_o = 10 \text{ (constant)}$

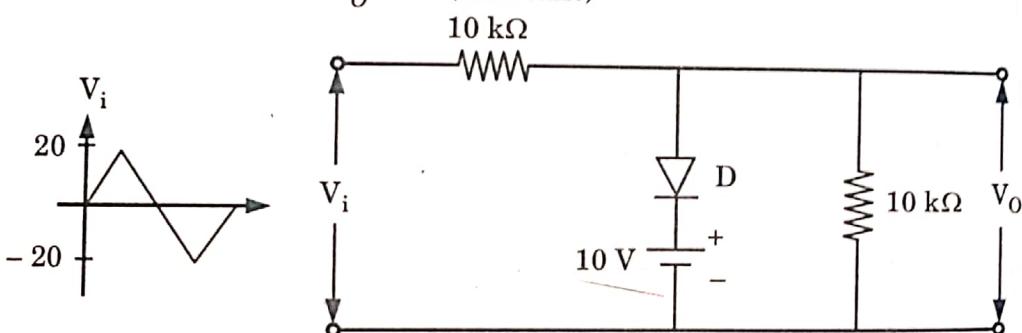


Fig. 2.21.4.

2. During entire negative half cycle, diode will be reverse biased. Therefore  
 $V_o = V_i$

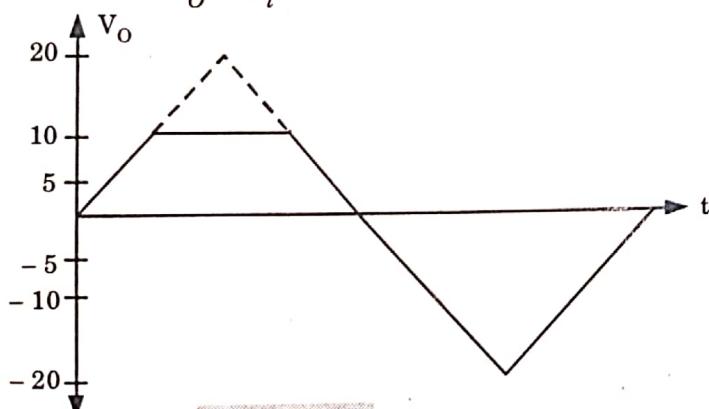


Fig. 2.21.5.

**Que 2.22.** Determine and sketch  $V_o$  for the given network shown in Fig. 2.22.1.

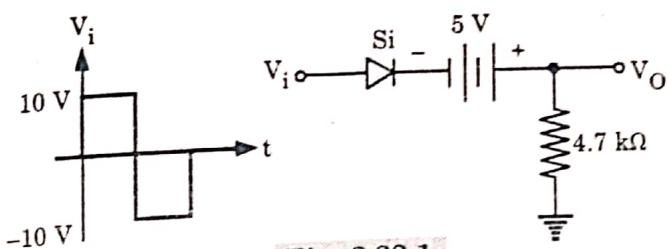


Fig. 2.22.1.

AKTU 2014-15(Sem-II), Marks 05

**Answer**

1. For  $V_i = +10\text{ V}$ , the diode is in the ON-state as shown in Fig. 2.22.2.

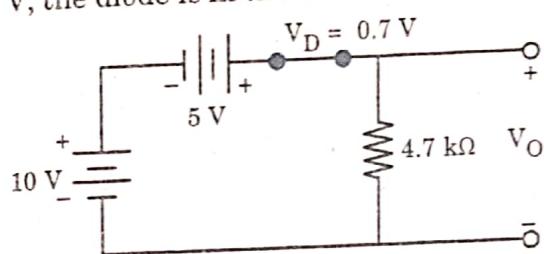


Fig. 2.22.2.

$$V_o = 10 + 5 - 0.7 = 14.3 \text{ V}$$

2. Similarly, for  $V_i = -10\text{ V}$ , the diode is in the OFF state as shown in Fig. 2.22.3.

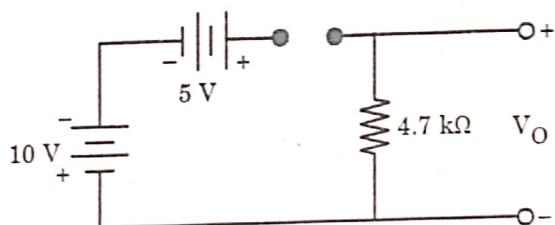


Fig. 2.22.3.

$$V_o = i_R \times 4.7 \times 10^3 = 0 \times 4.7 \times 10^3 = 0 \text{ V}$$

3. Resulting output waveform is shown in Fig. 2.22.4.

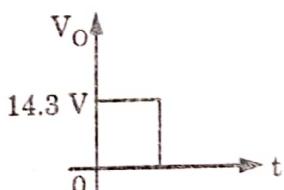


Fig. 2.22.4.

**PART-4***Zener Diode as Shunt Regulator.*

## Questions-Answers

## Long Answer Type and Medium Answer Type Questions

**Que 2.23.** How Zener diode is used as shunt regulator? Explain it

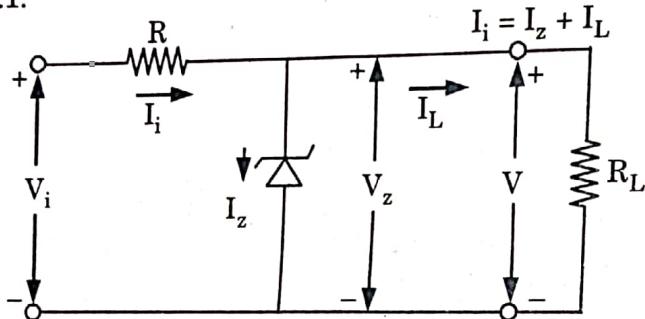
**OR**

How zener diode is used as voltage regulator? Explain with suitable circuits.

**AKTU 2014-15(Sem-I), Marks 05**

**Answer**

1. The circuit diagram for zener voltage/shunt regulator circuit is shown in Fig. 2.23.1.



**Fig. 2.23.1. Zener voltage regulator.**

2. The zener diode is selected with  $V_z$  equal to the voltage desired across the load.
  3. Under reverse biased condition, voltage across zener diode practically remains constant, even if the current through it changes by a large extent.
  4. Under normal conditions, the input current  $I_i = I_L + I_z$  flows through resistor  $R$ . The input voltage  $V_i$  can be written as
- $$V_i = I_i R + V_z = (I_L + I_z) R + V_z$$
5. When the input voltage  $V_i$  increases, as the voltage across zener diode remains constant, the drop across  $R$  will increase with a corresponding increase in  $I_L + I_z$ .
  6. As  $V$  is a constant, the voltage across the load will also remain constant and hence,  $I_L$  will be a constant.
  7. Therefore, an increase in  $I_L + I_z$  will result in an increase in  $I_z$  which will not alter the voltage across load. Thus, zener diode is used as a voltage regulator.
  8. To operate zener diode as voltage regulator, the reverse voltage applied to zener diode never exceeds PIV of the diode and at the same time, the applied input voltage must be greater than the breakdown voltage of the zener diode.

**Que 2.24.** Draw a neat diagram of zener voltage regulator circuit and determine the load resistance ( $R_L$ ) and range of series resistance ( $R$ ) value to meet the following specification : Output Voltage ( $V_{out}$ ) = 5 V, Load Current ( $I_L$ ) = 10 mA, Zener maximum wattage = 400 mW and Input Voltage ( $V_{in}$ ) =  $10 \pm 2$  V.

**Answer**

Zener voltage regulator circuit : Refer Q. 2.23, Page 2-30D, Unit-2.

Numerical :

Given :  $V_{out} = 5$  V,  $I_L = 10$  mA,  $P_{z\max} = 400$  mW,  $V_{in} = 10$  V  $\pm 2$  V

To Find : Load resistance ( $R_L$ ), Range of series resistance ( $R$ ).

1. Load resistance,  $R_L = \frac{V_{out}}{I_L} = \frac{5}{10 \times 10^{-3}} = 500 \Omega$
2. Maximum zener current,  $I_{zm} = \frac{P_{z\max}}{V_z} = \frac{400 \times 10^{-3}}{5} = 80$  mA
3. The minimum input voltage required will be when  $I_z = 0$ .  
Under this condition,  $I_{min} = I_{zmin} + I_L = 0 + 10$  mA
4. Minimum input voltage,  $V_{i(min)} = V_{out} + I_{min} R$   
 $(10 - 2) = 5 + (10 \times 10^{-3}) R$   
 $\therefore R = \frac{8 - 5}{10 \times 10^{-3}} = 300 \Omega$
5. Maximum input voltage,  $V_{i(max)} = V_{out} + I_{max} R$   
But  $I_{max} = I_{zmax} + I_L = (80 + 10)$  mA = 90 mA  
 $\therefore (10 + 2) = 5 + 90 \times 10^{-3} \times R$   
 $\frac{12 - 5}{90 \times 10^{-3}} = R$   
 $R = 77.78 \Omega$ .

So, range of  $R$  is between  $77.78 \Omega$  and  $300 \Omega$ .

**Que 2.25.** Find the range of  $I_L$  and  $R_L$  for the circuit shown in Fig. 2.25.1 if the output voltage is to be maintained constant at 10 V.

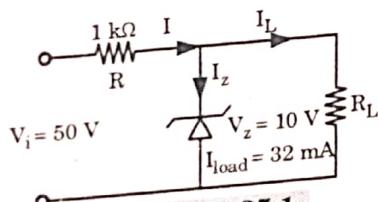


Fig. 2.25.1.

AKTU 2013-14(Sem-II), Marks 05

OR

- Find the range of  $R_L$  and  $I_L$  that will maintain a constant output of 10 V (Fig. 2.25.1).
- Also determine the maximum wattage rating of the Zener diode for given circuit.

AKTU 2017-18(Sem-II), Marks 07

**Answer**Given :  $I_{z,\max} = 32 \text{ mA}$ ,  $V_z = 10 \text{ V}$ To Find : Range of  $I_L$  and  $R_L$ , maximum wattage.

1. From the circuit,  $I = I_z + I_L$

where,  $I = \frac{V_i - V_z}{R} = \frac{50 - 10}{1 \text{ k}\Omega} = 40 \text{ mA}$

2. When  $I_L$  is minimum,  $I_z$  is maximum and vice versa.

Therefore,  $I = I_{z,\max} + I_{L,\min} = I_{z,\min} + I_{L,\max}$

$40 \times 10^{-3} = 32 \times 10^{-3} + I_{L,\min}$

$I_{L,\min} = 8 \text{ mA}$

3. Hence,  $R_{L,\max} = \frac{V_o}{I_{L,\min}} = \frac{10}{8 \times 10^{-3}} = 1.25 \text{ k}\Omega$

and  $I = I_{z,\min} + I_{L,\max}$ 

4. Let  $I_{z,\min} = 5 \text{ mA}$

Therefore,  $I_{L,\max} = 40 \text{ mA} - 5 \text{ mA} = 35 \text{ mA}$

$R_{L,\min} = \frac{V_o}{I_{L,\max}} = \frac{10}{35 \text{ mA}} = 285.72 \Omega$

5. Hence, the range of  $I_L$  is between 8 mA and 35 mA while range of  $R_L$  is between 285.72  $\Omega$  and 1.25 k $\Omega$ .

6. Maximum wattage of zener diode is,

$$P_{z\max} = I_{z\max} V_z \\ = 32 \text{ mA} \times 10 = 320 \times 10^{-3} = 0.32 \text{ W}$$

**Que 2.26.** Determine the range of  $V_i$  for the Fig. 2.26.1, that will maintain the zener diode in "ON" state.

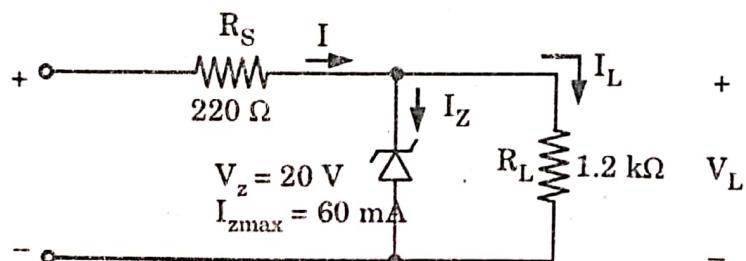


Fig. 2.26.1.

AKTU 2017-18(Sem-II), Marks 07

**Answer**

**Given :**  $R_S = 220 \Omega$ ,  $V_z = 20 \text{ V}$ ,  $I_{zmax} = 60 \text{ mA}$ ,  $R_L = 1.2 \text{ k}\Omega$ ,  $V_L = V_z = 20 \text{ V}$

**To Find :** Range of  $V_i$ .

1. We have

$$I_L = \frac{V_L}{R_L} = \frac{20}{1.2 \times 10^3} = 16.67 \text{ mA}$$

2. So,

$$V_{i\ min} = \frac{(R_S + R_L) \cdot V_z}{R_L} = \left( \frac{220 + 1200}{1200} \right) \times 20$$

$$V_{i\ min} = 23.67 \text{ V}$$

3. Now, current through  $R_S$

$$I = I_{zmax} + I_L = 60 + 16.67 = 76.67 \text{ mA}$$

4. So,

$$V_{i\ max} = I \cdot R_S + V_z = 76.67 \times 10^{-3} \times 220 + 20$$

$$V_{i\ max} = 36.87 \text{ V}$$

Hence, the range of  $V_i$  lies between 23.67 V and 36.87 V

**Que 2.27.** Design a voltage regulator that will maintain an output voltage of 20 V across a 1 kΩ load with an input that will vary between 30 V and 50 V. That is, determine the proper value of  $R_S$  and the maximum current  $I_{zmax}$ .

**AKTU 2014-15(Sem-II), Marks 05**

**Answer**

**Given :**  $V_i = 30 \text{ V}-50 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$ ,  $V_L = 20 \text{ V}$ ,

**To Find :**  $R_S$ ,  $I_{zmax}$ .

1. Consider the circuit of voltage regulator as shown in Fig. 2.27.1

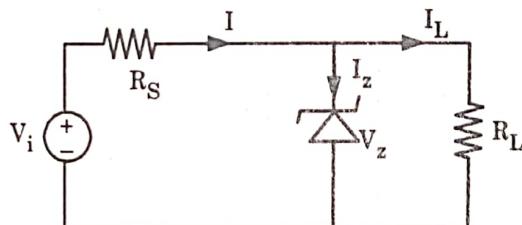


Fig. 2.27.1.

2. Minimum voltage to turn ON the zener diode,

$$V_{i\ min} = \frac{(R_L + R_S)V_z}{R_L}, \quad \left[ \therefore V_L = V_z = \frac{R_L V_i}{R_L + R_S} \right]$$

$$\Rightarrow 30 = \frac{(1 + R_S)20}{1}$$

$$\frac{30}{20} = R_S + 1 \Rightarrow R_S = 0.5 \text{ k}\Omega$$

$$I_L = \frac{V_L}{R_L} = \frac{20}{1 \times 10^3} = 20 \text{ mA}$$

3. Maximum voltage,

$$\begin{aligned} V_{i\max} &= I_{\max} R_S + V_z \\ 50 &= I_{\max} R_S + 20 \\ 50 &= I_{\max} \times 0.5 \times 10^3 + 20 \end{aligned}$$

$$\frac{30}{0.5 \times 10^3} = I_{\max} \Rightarrow I_{\max} = 60 \text{ mA}$$

Also,

$$\begin{aligned} I_{\max} &= I_{z\max} + I_L \\ 60 &= I_{z\max} + 20 \Rightarrow I_{z\max} = 40 \text{ mA} \end{aligned}$$

**Que 2.28.** For the network of Fig. 2.28.1, determine the range of  $V_i$  that will maintain  $V_L$  at 8 V and not exceed the maximum power rating of the zener diode.

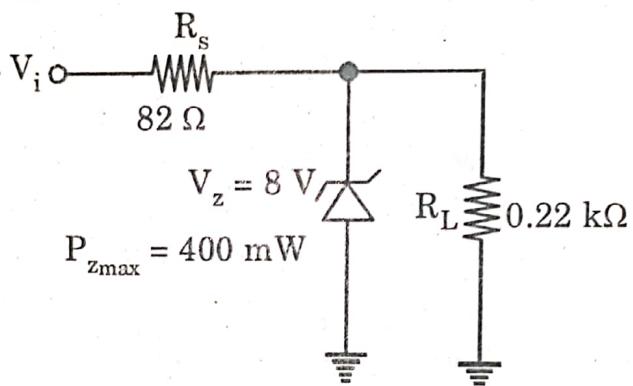


Fig. 2.28.1.

AKTU 2015-16(Sem-I), Marks 05

### Answer

The procedure is same as Q. 2.26, Page 2-32D, Unit-2.

**Ans.** Range is 10.98 V to 15.08 V.

### PART-5

#### Voltage Multiplier Circuits.

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 2.29.** Describe with the help of circuit diagram working of voltage tripler.

AKTU 2015-16(Sem-I), Marks 05

OR

Explain with suitable circuit that how diode acts as a voltage multiplier?

AKTU 2014-15(Sem-I), Marks 05

OR

Draw and discuss voltage tripler circuit.

AKTU 2016-17(Sem-I), Marks 05

**Answer**

- Fig. 2.29.1 shows a circuit of general multiplier i.e. this circuit can be used as a doubler, tripler and quadrupler.
- Circuit-1 is a Doubler ( $2V_m$ ).  
Circuit-2 is a Tripler ( $3V_m$ ).  
Circuit-3 is a Quadrupler ( $4V_m$ ).
- During positive half cycle, the diode  $D_1$  is ON and it charges capacitor  $C_1$  to  $V_m$ .
- In the first negative half cycle, the diode  $D_2$  is ON and it charges  $C_2$  to  $2V_m$  ( $V_{C2} = V_m + V_{C1} = 2V_m$ ). In this cycle the charge on capacitor  $C_1$  starts discharging.
- In the second positive half cycle the diode  $D_1$  and  $D_3$  are ON, the capacitor  $C_1$  will be charged to  $V_m$  and the capacitor  $C_3$  will be charged to

$$V_{C3} = V_i + (-V_{C1}) + V_{C2} = V_m - V_m + 2V_m \\ V_{C3} = 2V_m \text{ (Voltage across } C_3\text{)}$$

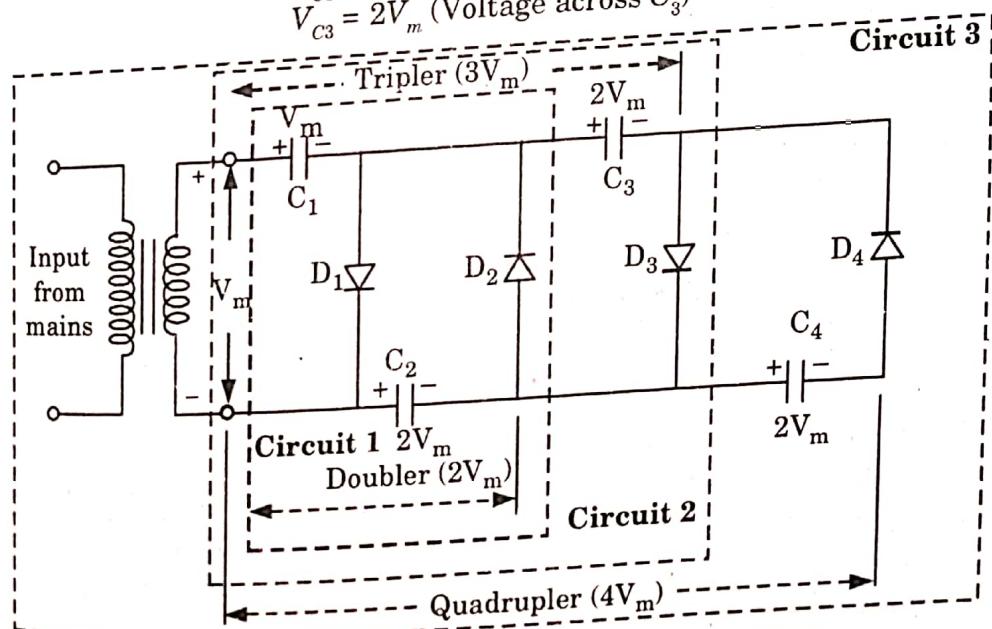


Fig. 2.29.1. General circuit diagram of multiplier.

- During second negative half-cycle, the diode  $D_2$  and diode  $D_4$  are ON. The voltage across capacitor is given as:

$$V_{C4} = V_i + (V_{C2}) + V_{C3} + V_{C1} = V_m - 2V_m + 2V_m + V_m \\ V_{C4} = 2V_m$$

## 2-36 D (ESC-Sem-3 &amp; 4)

7. Now  
 Voltage across  $C_1 \rightarrow V_{C1} = V_m$   
 Voltage across  $C_2 \rightarrow V_{C2} = 2V_m$   
 Voltage across  $C_3 \rightarrow V_{C3} = 2V_m$   
 Voltage across  $C_4 \rightarrow V_{C4} = 2V_m$
8. **Voltage doubler:** Taking output across  $C_2$ .  
 $V_o = V_{C2} = 2V_m$
9. **Voltage tripler:** Taking output across  $C_3$  and  $C_1$ .  
 $V_1 = V_{C1} + V_{C3} = V_m + 2V_m = 3V_m$
10. **Voltage quadrupler:** Taking output across  $C_2$  and  $C_4$   
 $V_o = V_{C2} + V_{C4} = 2V_m + 2V_m = 4V_m$

**Que 2.30.** What is voltage multiplier using *p-n* junction diode?

Explain the operation of voltage doublers.

OR

With the help of necessary diagram, differentiate between half wave and full wave voltage doubler. **AKTU 2014-15(Sem-II), Marks 05**

OR

Explain the full wave voltage doubler circuit using diode.

**AKTU 2013-14(Sem-II), Marks 05**

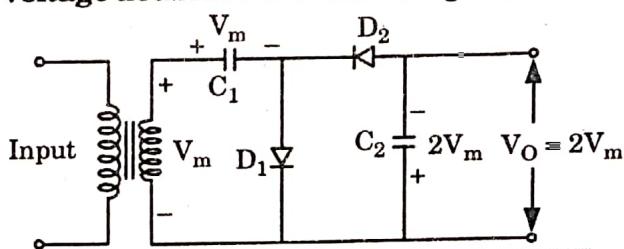
OR

Explain full wave voltage doubler with clear diagram.

**AKTU 2017-18(Sem-I), Marks 3.5**

**Answer**

- The circuit which produces a greater DC output voltage than AC input voltage using a rectifier circuit is called as voltage multiplier.
- The output of voltage doubler is twice the peak input voltage.
- There are two types of voltage doubler circuits :
  - Half wave voltage doubler:** The circuit diagram is shown in Fig. 2.30.1.



**Fig. 2.30.1.** Half wave voltage doubler.

- During positive half-cycle of the input voltage, diode  $D_1$  is forward biased (ON) and diode  $D_2$  is reverse biased (OFF). Capacitor  $C_1$  charges to the peak value of secondary voltage  $V_m$  with polarity.
- During negative half-cycle, diode  $D_2$  is ON while diode  $D_1$  is OFF. Capacitor  $C_2$  is charged upto a voltage i.e., the sum of peak-supply voltage and the voltage across  $C_1$ .
- During positive half-cycle :  $V_{C1} = V_m$

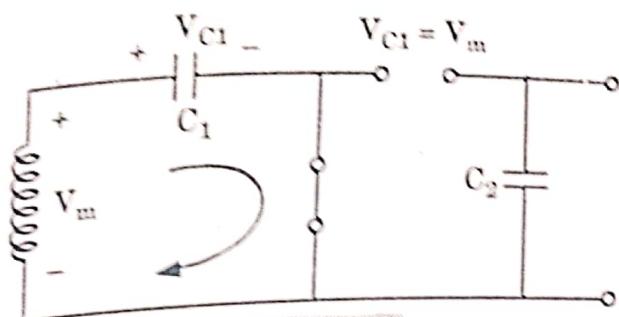


Fig. 2.30.2.

4. During negative half cycle :

$$-V_m - V_{C1} + V_{C2} = 0$$

$$-V_m - V_m + V_{C2} = 0$$

$$V_{C2} = 2V_m$$

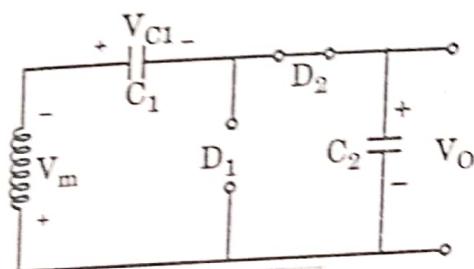


Fig. 2.30.3.

- ii. Full wave voltage doubler : The circuit diagram is shown in Fig. 2.30.4.

1. During positive half cycle,  $D_1$  is ON and  $D_2$  is OFF. Capacitor  $C_1$  will be charged to a peak value  $V_m$ .

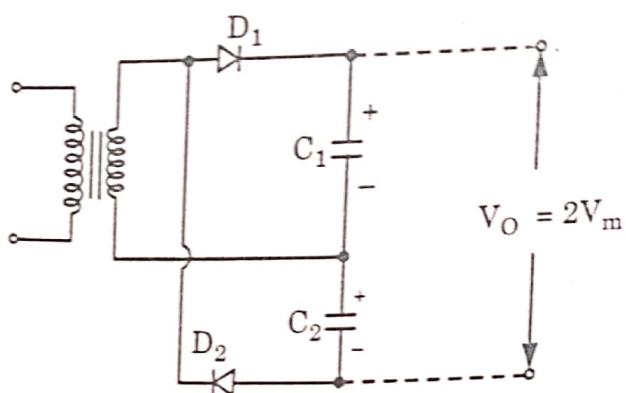


Fig. 2.30.4. Full wave voltage doubler.

2.  $V_{C1} = V_m$

- During negative half cycle,  $D_1$  is OFF and  $D_2$  is ON. Capacitor  $C_2$  is charged to peak value  $V_m$ . Thus output voltage with no load connected :

$$V_O = V_{C1} + V_{C2}$$

$$V_O = 2V_m$$

**PART-6**

*Special Purpose Two Terminals Devices : Light Emitting Diode, Varactor (Varicap) Diodes, Tunnel Diodes, Liquid Crystal Displays.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

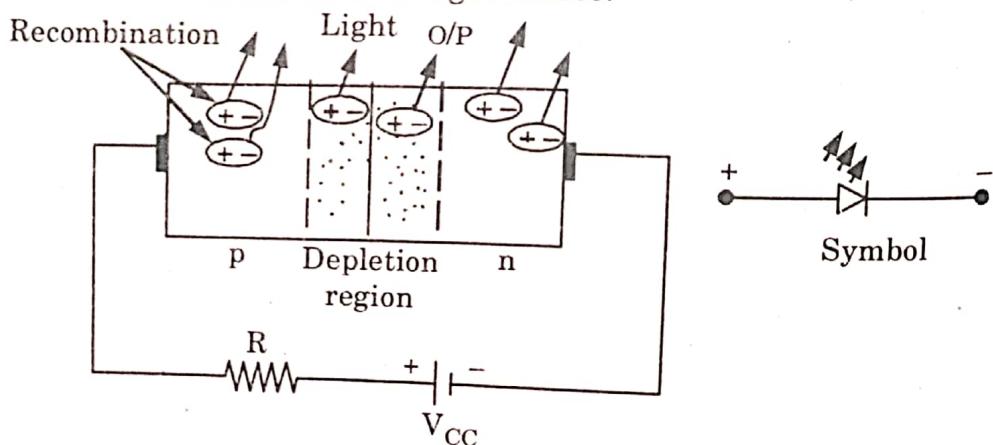
**Que 2.31.** What is LED ? Give its principle of working, construction, merits, demerits and applications.

**Answer**

**LED :** LED is a special type of semiconductor *p-n* junction that under forward bias emits external radiations in ultraviolet, visible and infrared regions of electromagnetic spectrum.

**Construction of LED :**

1. LED is just not an ordinary *p-n* junction diode where silicon is used. Here we use compound having elements like gallium, arsenic and phosphorus which are semitransparent unlike silicon which is opaque.
3. In all semiconductor *p-n* junctions, some of its energy will be given off as heat and some in the form of photons.
4. In the materials, such as gallium arsenide phosphide (GaAsP) or gallium phosphide (GaP), the number of photons of light energy emitted is sufficient to create a visible light source.

**Fig. 2.31.1****Principle of LED :**

1. The process involves :
  - i. Generation of electron-hole pair (EHP) by excitation of semiconductor.
  - ii. Recombination of EHP.
  - iii. Extraction of photons from the semiconductor.

2. The characteristic for LED is given in Fig. 2.31.2.

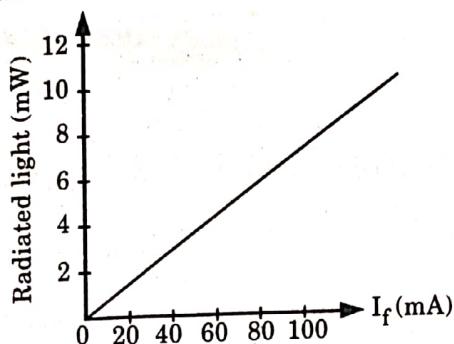


Fig. 2.31.2. Characteristics.

#### Working :

- When LED is in forward bias condition, the electrons from *n*-type material cross the *p-n* junction and recombines with holes in the *p*-type material.
- When recombination takes place, the recombining electrons release energy in the form of heat and light.
- The emission depends upon the type of material, i.e.,  
 $\text{GaAs} \rightarrow$  infrared radiation (invisible)  
 $\text{GaP} \rightarrow$  red or green light (visible)  
 $\text{GaAsP} \rightarrow$  red or yellow light (visible).

#### Applications :

- Display LEDs like calculator, digital clocks etc.
- Light source in optical fibre communication.
- Light source in a source detector package like smoke detectors, tachometers, proximity detectors etc.

#### Merits :

- Low voltage of operation.
- Long life (more than 15 years).
- Fast on-off switching.
- Cheap in cost.
- Available in wide range of colours.

#### Demerits :

- It draws considerable current requiring frequent replacement of battery in low power battery operated devices.
- Luminous efficiency of LED is low which is about 1.5 lumen/watt.
- Characteristics are affected by temperature.
- Need large power for the operation as compared to normal *p-n* junction diode.
- Sensitivity to damage by over voltage and over current.

**Que 2.32.** Write short notes on the following in terms of symbol, V-I characteristics, and diode equivalent circuit diagram : (i) Light Emitting Diode (LED), (ii) Varactor Diode.

AKTU 2013-14(Sem-I), Marks 05

OR

**Explain input and output characteristics of varactor diode.**

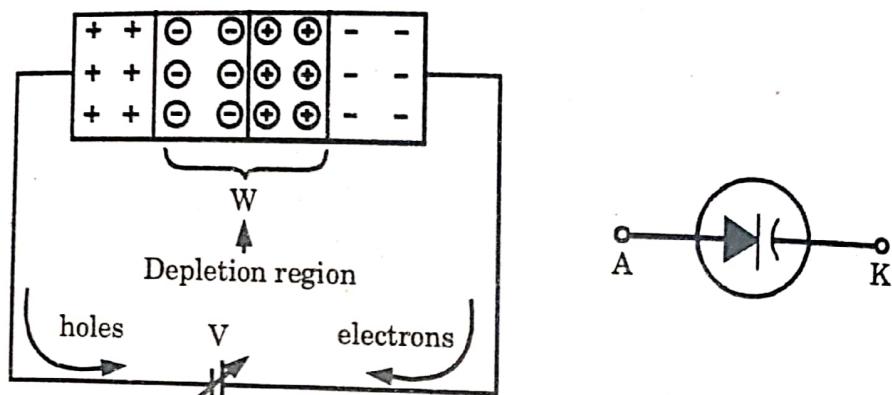
**AKTU 2015-16(Sem-II), Marks 05**

**Answer**

i. LED : Refer Q. 2.31, Page 2-38D, Unit-2.

ii. Varactor diode :

1. This is also called as varicap, VVC (voltage variable capacitance), or tuning diode.
2. This is constructed from semiconductor materials. It is simply a voltage dependent variable capacitor.



**Fig. 2.32.1.**

3. Fig. 2.32.1 shows the varactor diode in reverse-bias condition and symbol of varactor diodes.

If

$V \rightarrow$  larger, then  $W \rightarrow$  wider

$V \rightarrow$  smaller, then  $W \rightarrow$  narrower

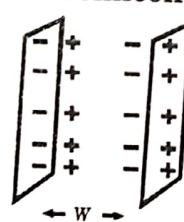
4. The depletion region  $W$  in this case acts like an insulator preventing the conduction between the  $n$  and  $p$  region of the diode, just like a dielectric which separates the two plates of a capacitor.

5. Let area of plates =  $A$

If distance between two capacitor plates =  $W$

$$\text{then capacitance, } C = \epsilon \cdot \frac{A}{W}$$

where  $\epsilon$  = Permittivity of the semiconductor materials.



**Fig. 2.32.2.**

**Varicap characteristics :**

1. Fig. 2.32.3 shows the characteristics of a typical commercially available varicap diode.
2. We see that there is the initial sharp decline in  $C_T$  with increase in reverse bias.
3. The normal range of  $V_R$  for varactor diodes is limited to about 20 V.

4. In terms of the applied reverse bias, the transition capacitance is given approximately by

$$C_T = \frac{k}{(V_T + V_R)^n}$$

where

$k$  = Constant determined by the semiconductor material and construction technique

$V_T$  = Knee potential

$V_R$  = Magnitude of the applied reverse bias potential

$n = \frac{1}{2}$  for alloy junction =  $\frac{1}{3}$  for diffused junction

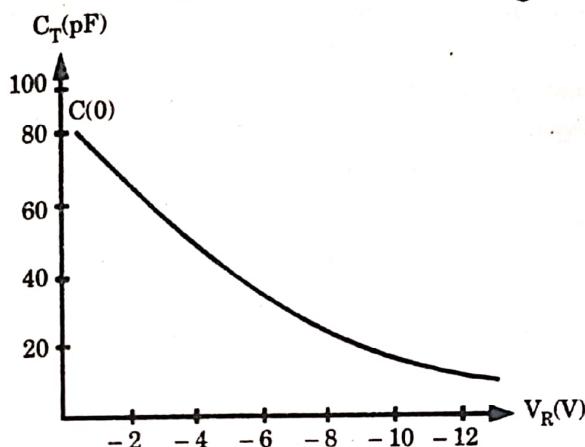


Fig. 2.32.3.

5. In terms of the capacitance at the zero-bias condition  $C(0)$ , the capacitance as a function of  $V_R$  is given by :

$$C_T(V_R) = \frac{C(0)}{(1 + |V_R/V_T|)^n}$$

**Que 2.33.** Explain working and characteristics of Tunnel diode

with the help of neat diagram. **AKTU 2015-16(Sem-I), Marks 05**

OR

Discuss the construction and working of tunnel diode. Also sketch its I-V characteristics and explain.

**AKTU 2017-18(Sem-II), Marks 07**

OR

Explain principle of operation and construction of tunnel diode.

Draw its V-I characteristic. **AKTU 2016-17(Sem-II), Marks 5.25**

OR

Explain the V-I characteristic of tunnel diode.

**AKTU 2016-17(Sem-I), Marks 05**

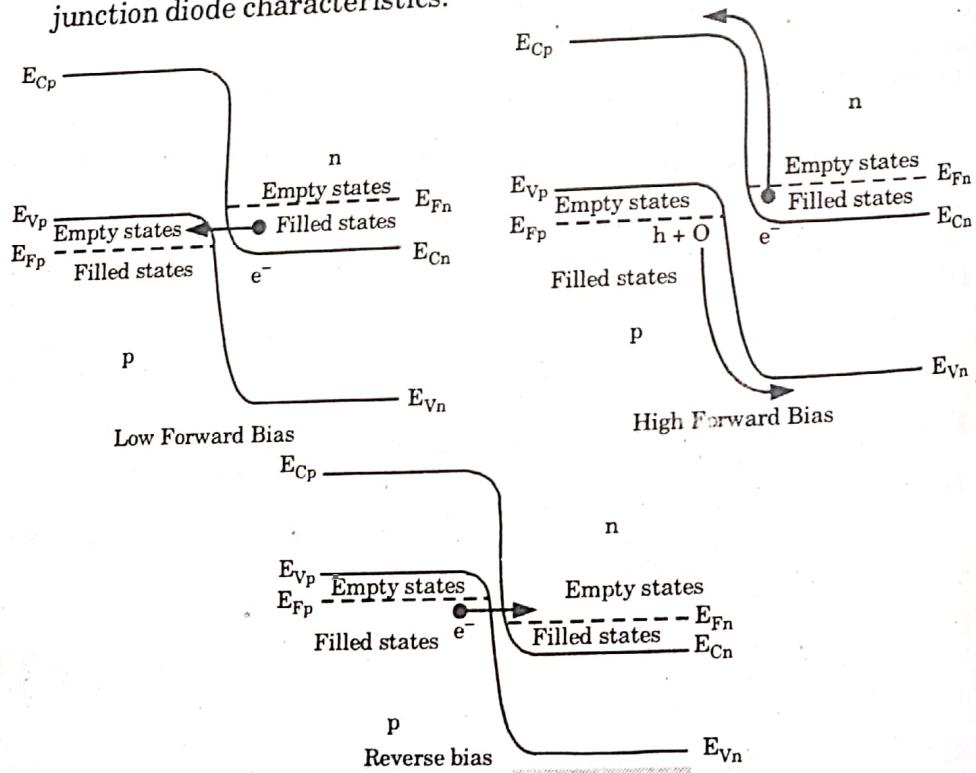
OR

Explain tunnel diode.

**AKTU 2017-18(Sem-I), Marks 3.5**

**Answer****Principle of Operation of Tunnel Diode :****In forward bias condition :**

1. A small forward bias is applied across the junction.
2. Since, the potential of the *p*-side under this condition is higher than the potential of *n*-side,  $E_{Fp}$  will move below  $E_{Fn}$ , as shown in Fig. 2.33.1 (a) and the electrons in the conduction band on the *n*-side faces empty states in the valence band on the *p*-side, at same energy level.
3. The thin barrier across the junction would permit tunneling of electrons from *n*-side to *p*-side, with the consequent current flowing from the *p*-side to *n*-side. Thus,  $I_D$  is positive for this case. As the forward bias is increased, more such filled states on the *n*-side would come opposite to the empty states.
4. With further increase in the forward bias, a specific condition would be reached when the maximum number of filled states in the conduction band on the *n*-side would face the maximum number of empty states in the valence band on the *p*-side. The tunneling current would reach a peak.
5. If the forward bias is increased further, then the conduction band of *n*-side would move away from the valence band of the *p*-side, and there would be no empty states on the *p*-side corresponding to the filled states on *n*-side.
6. Hence, tunneling current would go to zero and the normal diffusion component of current would dominate. This results in normal *p-n* junction diode characteristics.

**Fig. 2.33.1.**

**In reverse bias condition :**

1. When negative voltage is applied to the *p*-side with respect to *n*-side, this would push  $E_{Fp}$  above  $E_{Fn}$  with their separation being equal to the applied voltage.
2. The filled states of the *p*-side are directly opposite to the empty states on the *n*-side across a very narrow barrier.
3. Thus, the electrons from *p*-side would easily tunnel through this thin barrier by the process of quantum mechanical tunneling and appear on the *n*-side.
4. Since, electrons travel from *p*-side to *n*-side, the actual direction of current is from *n* to *p*-side and is negative.
5. As the amount of reverse bias is increased, more number of filled states in the valence band of the *p*-side would appear opposite to the number of empty states in the conduction band of the *n*-side and the reverse current would keep on increasing with reverse voltage.

**Characteristics :** Due to heavy doping, the current in negative resistance region is suddenly increased with a small applied voltage. Due to this reduced depletion region the sudden increase in current (at small applied voltage) is called "carrier punching through" effect.

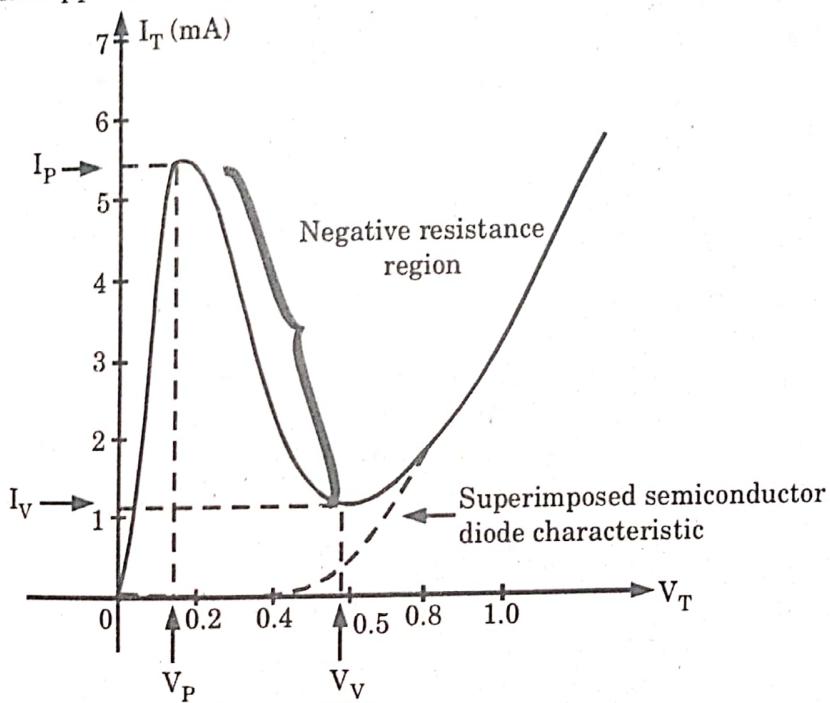


Fig. 2.33.2.

**Applications :**

- i. It is used as an ultra-high speed switch.
- ii. It is used as microwave oscillator.
- iii. In relaxation oscillator circuit.
- iv. It is used as an amplifier.

**Advantages of tunnel diode :**

- i. Low noise operation.
- ii. High speed.
- iii. Low power dissipation.

iv. Ease of operation.

**Que 2.34.** Explain Liquid Crystal Display (LCD).

OR

Explain principle of operation of LCD.

AKTU 2016-17(Sem-I), Marks 05

**Answer**

1. Liquid crystal cell displays (LCDs) are used in similar applications where LEDs are used. These applications are display of numeric and alphanumeric characters in dot matrix and segmental displays.
2. The LCDs are of two types :
  - a. **Dynamic scattering type :**

- i. The construction of a dynamic scattering liquid crystal cell is shown in Fig. 2.34.1.

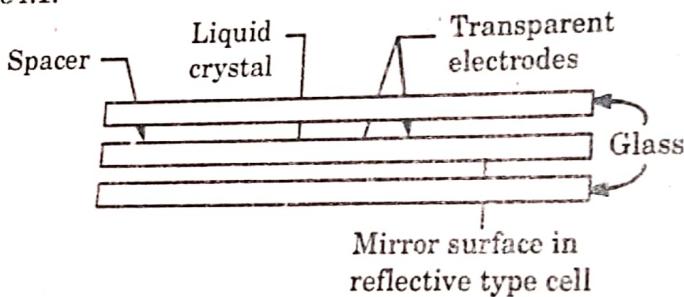


Fig. 2.34.1.

- ii. The liquid crystal material may be one of the several organic compounds which exhibit optical properties of a crystal though they remain in liquid form.
  - iii. Liquid crystal is layered between glass sheets with transparent electrodes deposited on the inside faces.
  - iv. When a potential is applied across the cell, charge carriers flowing through the liquid disrupt the molecular alignment and produce turbulence.
  - v. When the liquid is not activated, it is transparent.
  - vi. When the liquid is activated the molecular turbulence causes light to be scattered in all directions and the cell appears to be bright. The phenomenon is called dynamic scattering.
- b. **Field effect type :**
- i. The construction of a field effect liquid crystal display is similar to that of the dynamic scattering type, with the exception that two thin polarizing optical filters are placed at the inside of each glass sheet.
  - ii. The liquid crystal material in the field effect cell is also of different type from that employed in the dynamic scattering cell.
  - iii. The material used is twisted nematic type and actually twists the light passing through the cell when the latter is not energized.
  - iv. This allows the light to pass through the optical filters and the cell appears bright.

- v. When the cell is energised, no twisting of light takes place and the cell appears dull.
3. Liquid crystal cells are of two types :
- Transmittive type :**
  - i. In the transmittive type cell, both glass sheets are transparent, so that light from a rear source is scattered in the forward direction when the cell is activated.
  - Reflective type :**
  - i. The reflective type cell has a reflecting surface on one side of glass sheets.
  - ii. The incident light on the front surface of the cell is dynamically scattered by an activated cell.
  - iii. Both types of cells appear quite bright when activated even under ambient light conditions.
4. The liquid crystals are light reflectors or transmitters and therefore they consume small amounts of energy (unlike light generators).
5. Considering the case of seven segment display the current is about  $25 \mu\text{A}$  for dynamic scattering cells and  $300 \mu\text{A}$  for field effect cells.
6. Unlike LEDs which can work on DC the LCDs require AC voltage supply.
7. A typical voltage supply to dynamic scattering LCD is  $30 \text{ V}$  peak to peak with  $50 \text{ Hz}$ .

**Que 2.35. Illustrate how LCD differs from LED ?**

**AKTU 2014-15(Sem-I), Marks 05**

**Answer**

S.No.	LCD	LED
1.	It requires $10-250 \text{ mW}$ power per digit.	It requires $10-200 \text{ mW}$ power per digit.
2.	It provides off visible light when it is energised.	It requires external or internal light source.
3.	It can operate within the temperature range $-40^\circ\text{C}$ to $+85^\circ\text{C}$ .	It is limited to temperature range $-20^\circ\text{C}$ to $+60^\circ\text{C}$ .
4.	It emits red, orange, yellow and green colours.	External illumination is required.
5.	Operating voltage range is $1.6 \text{ V}$ to $5 \text{ V DC}$ .	Operating voltage range is $3 \text{ V}$ to $20 \text{ V AC}$ .

6.	Typical value of lifetime is 100000 hours.	Lifetime is limited upto 50000 hours because of its chemical degradation.
7.	The viewing angle is 100°.	The viewing angle is 150°.
8.	The response time is 50 nsec to 500 nsec.	The response time is 50 nsec to 200 nsec because of slow decay time, one can even observe the fading out of segments when switched off.

### VERY IMPORTANT QUESTIONS

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

**Q. 1.** For the circuit shown in Fig. 1, determine  $I_1$ ,  $I_2$ ,  $I_3$ ,  $I_4$ ,  $V_o$ .

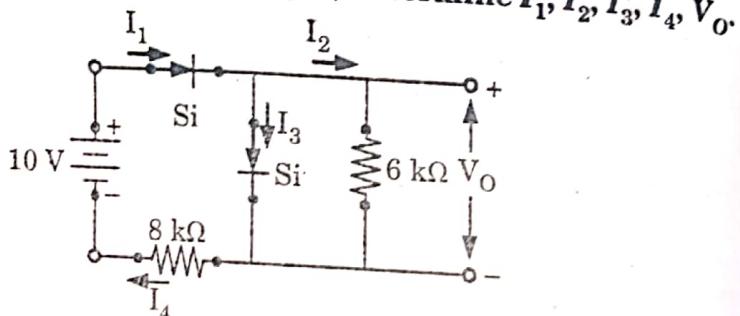


Fig. 1.

**Ans.** Refer Q. 2.3.

**Q. 2.** For a half wave rectifier, derive an expression for ripple factor.

**Ans.** Refer Q. 2.6.

**Q. 3.** Sketch  $V_o$ ,  $V_{DC}$  for the network of Fig. 2, and determine the peak inverse voltage of each diode.

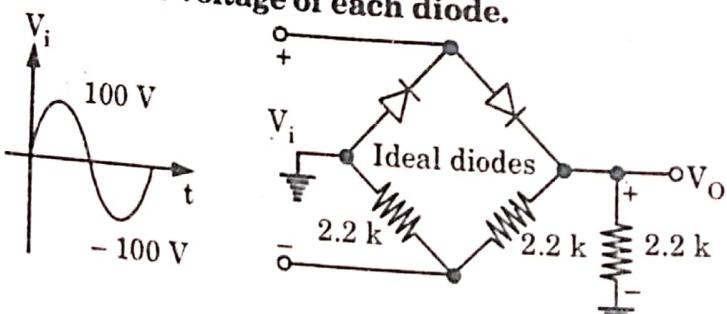


Fig. 2.

**Ans.** Refer Q. 2.8.

- Q. 4.** Explain the operation of a bridge rectifier with the help of a circuit diagram and waveforms. Determine the DC load voltage and ripple factor.

**Ans.** Refer Q. 2.10.

- Q. 5.** Explain the function of the circuit of Fig. 3 and draw the output waveform.

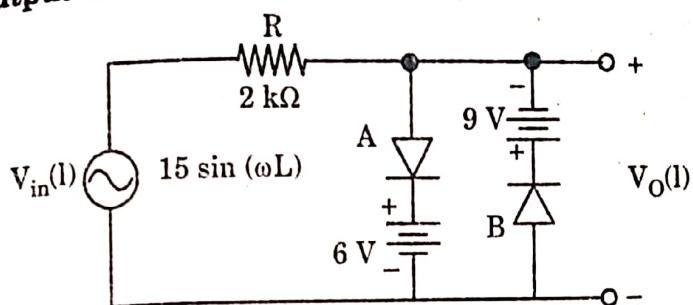


Fig. 3.

**Ans.** Refer Q. 2.19.

- Q. 6.** Draw the output waveform for the following circuits for the input waveforms, given in Fig. 4 (a) and 1 (b) :

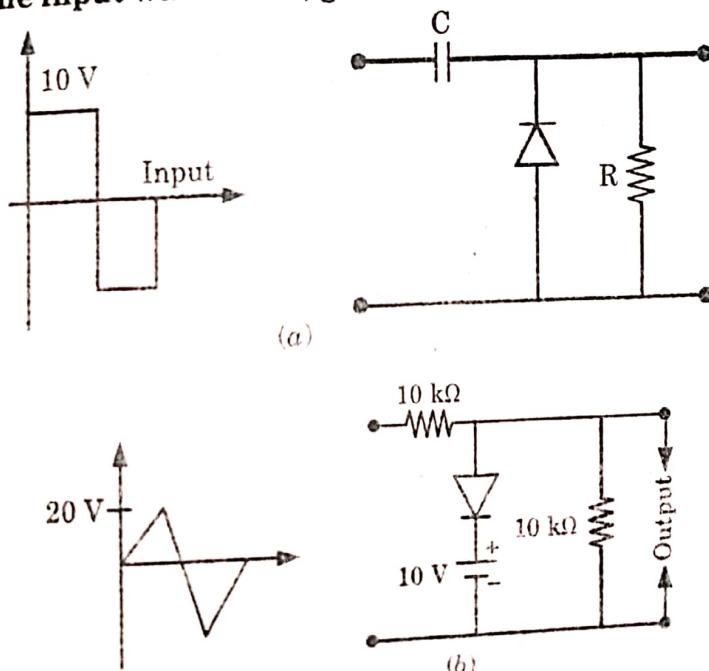


Fig. 4.

**Ans.** Refer Q. 2.21.

- Q. 7.** Find the range of  $I_L$  and  $R_L$  for the circuit shown in Fig. 5 if the output voltage is to be maintained constant at 10 V.

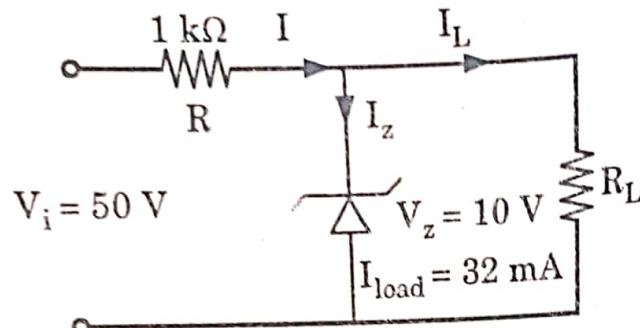


Fig. 5.

**Ans.** Refer Q. 2.25.

**Q. 8.** Describe with the help of circuit diagram working of voltage tripler.

**Ans.** Refer Q. 2.29.

**Q. 9.** What is voltage multiplier using *p-n* junction diode ? Explain the operation of voltage doublers.

**Ans.** Refer Q. 2.30.

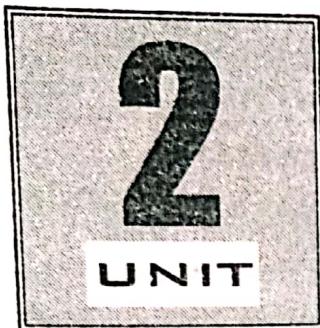
**Q. 10.** Write short notes on the following in terms of symbol, V-I characteristics, and diode equivalent circuit diagram : (i) Light Emitting Diode (LED), (ii) Varactor Diode.

**Ans.** Refer Q. 2.32.

**Q. 11.** Explain working and characteristics of Tunnel diode with the help of neat diagram.

**Ans.** Refer Q. 2.33.

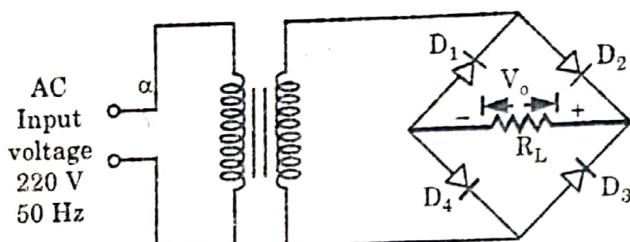




## Diode Applications (2 Marks Questions)

- 2.1.** Draw a neat diagram of a full wave rectifier bridge circuit using diode.

**Ans.**



**Fig. 2.1.1.**

- 2.2.** What are the PIV for full wave center tapped rectifier and bridge rectifier respectively?

**Ans.** In center tap full wave rectifier,  $PIV = 2 V_m$   
In bridge type full wave rectifier,  $PIV = V_m$

- 2.3.** What is the ripple factor for full wave rectifier?

**Ans.**

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_m / \sqrt{2}}{2I_m / \pi}\right)^2 - 1}$$

$$r = 0.482$$

- 2.4.** Write an expression for the ripple factor and efficiency for half wave rectifier.

**Ans.**

1. The ripple factor is given as

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

Since,  $I_{rms} = I_m / 2$  and  $I_{DC} = I_m / \pi$ . So,  $r = 1.21$

2. The efficiency is given as

$$\eta = \frac{\text{Output DC power}}{\text{Input AC power}} = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_L + r_d)}$$

where,  $R_L \rightarrow$  load resistance,  $r_d \rightarrow$  diode resistance

$$= \frac{(I_m / \pi)^2 \cdot R_L}{(I_m / 2)^2 (r_d + R_L)} = 0.406 \quad (\because r_d \ll R_L)$$

$$\eta = 40.6\%$$

**2.5. What is the voltage multiplier?**

**Ans.** Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

**2.6. Draw the circuit diagram of full wave voltage doubler using diode.**

AKTU 2013-14(Sem-I), Marks 02

**Ans.**

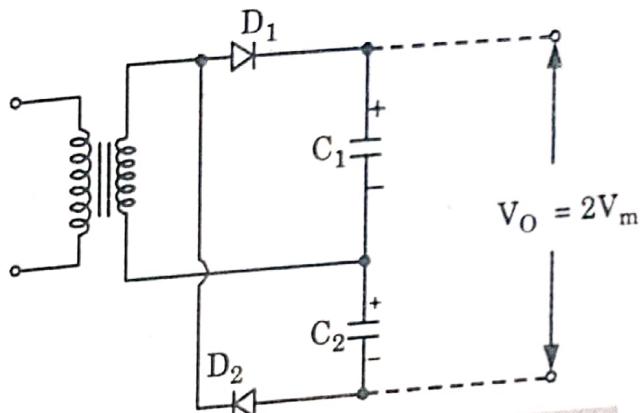


Fig. 2.6.1. Full wave voltage doubler.

**2.7. Draw the capacitance versus voltage transfer characteristics for the Varactor Diode.**

AKTU 2013-14(Sem-II), Marks 02

**Ans.**

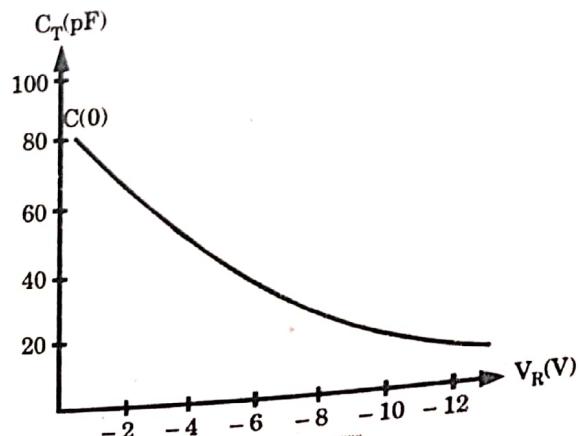


Fig. 2.7.1.

**2.8. Draw V-I characteristics of a Tunnel Diode.**

AKTU 2013-14(Sem-I), Marks 02

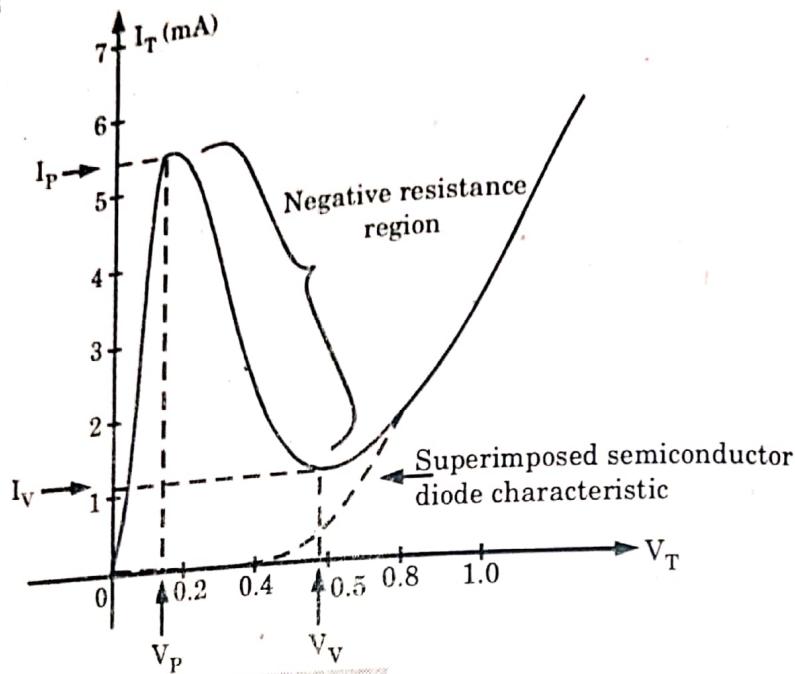
**Ans.**

Fig. 2.8.1.

- 2.9.** What will happen to the number of free electrons in a semiconductor on increasing temperature?

**Ans.** An increase in temperature in a semiconductor creates more free electrons and holes in the doped regions. Thus the number of free electrons is increased with increase in temperature.

- 2.10.** A silicon diode has a saturation current of 5 nA at 25 °C. What is the saturation current at 100 °C?

**AKTU 2013-14(Sem-II), Marks 02**

**Ans.** Given,  $I_{o1} = 5 \text{ nA}$  at  $T_1 = 25 \text{ }^{\circ}\text{C}$   
 $I_{o2} = ?$  at  $T_2 = 100 \text{ }^{\circ}\text{C}$

We know reverse saturation current doubles for every 10 °C rise in temperature.

$$I_{o2} = I_{o1} \times (2)^{\frac{T_2 - T_1}{10}}$$

$$I_{o2} = 5 \text{ nA} \times (2)^{\frac{100 - 25}{10}} = 9.05 \times 10^{-7} \text{ A} = 0.905 \mu\text{A}$$

- 2.11.** The reverse saturation current of a silicon  $p-n$  junction diode is 10  $\mu\text{A}$  at the temperature 300 K. Determine the forward bias voltage to be applied across the  $p-n$  junction to obtain a current of around 100 mA.

**AKTU 2013-14(Sem-I), Marks 02**
**AKTU 2017-18(Sem-II), Marks 02**

**Ans.** Given,

$$I_0 = 10 \mu\text{A}, \eta = 2 \text{ (for Si)}$$

$$T = 300 \text{ K}$$

$$I = 100 \text{ mA}$$

$$\text{We know, } I = I_0(e^{V/\eta V_T} - 1)$$

$$100 \times 10^{-3} = 10 \times 10^{-6} (e^{V/2 \times 0.0259} - 1)$$

$$10001 = e^{V/0.0518}$$

Taking ln both sides,

$$9.21 = \frac{V}{0.0518}$$

$$V = 0.47 \text{ V}$$

- 2.12. A 4.5 V zener is rated at 1.5 watt. What is the maximum safe current of the zener ?

**Ans.**

$$P = VI$$

$$I = \frac{P}{V} = \frac{1.5}{4.5}$$

$$= 0.33 \text{ A}$$

- 2.13. What is ripple factor ? What is the value of RF for half wave and full wave rectifier ? AKTU 2017-18(Sem-I), Marks 02

**Ans.** Ripple factor : The ripple factor is defined as ratio of rms value of the AC component in the output to the average or DC component present in the output. It is given by,

$$\text{Ripple factor} = \sqrt{\left[ \frac{I_{\text{rms}}}{I_{\text{DC}}} \right]^2 - 1}$$

Values of RF for half wave and full wave rectifier :

Refer Q. 2.3 and Q. 2.4, Page SQ-5D, Unit-2, 2 Marks Questions.

- 2.14. Explain the principle of operation of LED.

AKTU 2017-18(Sem-II), Marks 02

OR

Explain the principle of operation of LED.

AKTU 2016-17(Sem-II), Marks 02

OR

Explain the principle of operation of LED.

AKTU 2016-17(Sem-I), Marks 02

**Ans.**

- i Generation of electron-hole pair (EHP) by excitation of semiconductor.

- ii. Recombination of EHP.
- iii. Extraction of photons from the semiconductor.

2.15. Draw the double ended diode clipper circuit.

AKTU 2015-16(Sem-II), Marks 02

Ans.

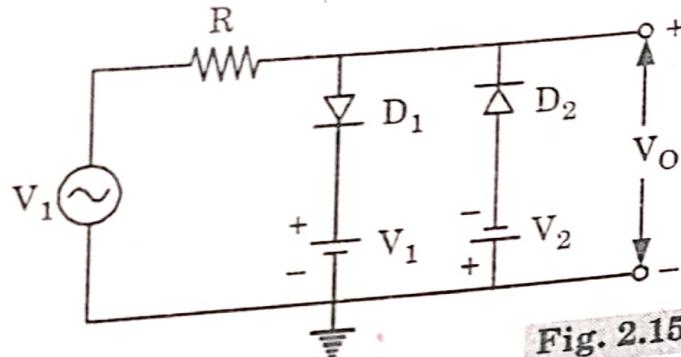
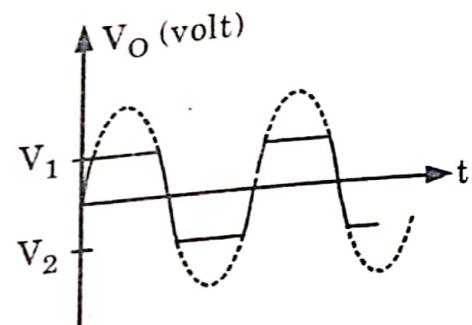


Fig. 2.15.1.



2.16. Consider a constant voltage source with 10 V and series internal resistance of 100 ohm. Calculate its equivalent to a current source.

AKTU 2015-16(Sem-II), Marks 02

Ans. Equivalent current source =  $\frac{10}{100} = 0.1 \text{ A}$



3  
3  
3

UNIT



## BJT and FET

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**PART-1**

**Bipolar Junction Transistor : Transistor Construction, Operation, Amplification Action.**

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 3.1.** Explain the basic construction and principle of operation of BJT.

**Answer**

1. A junction transistor is a three-layer semiconductor device, sandwich of one type of semiconductor material between two layers of the other type. There are two types of transistors :
  - a. *npn* transistor and
  - b. *pnp* transistor.
2. When a layer of *p*-type material is sandwiched between two layers of *n*-type material, the transistor is known as *npn*, as shown in Fig. 3.1.1(a).
3. Similarly, when a layer of *n*-type material is sandwiched between two layers of *p*-type material, the transistor is known as *pnp* transistor as shown in Fig. 3.1.1(b).
4. The transistors are made either from silicon or germanium crystal.
5. The symbols for *npn* and *pnp* transistors are also shown in Fig. 3.1.1.

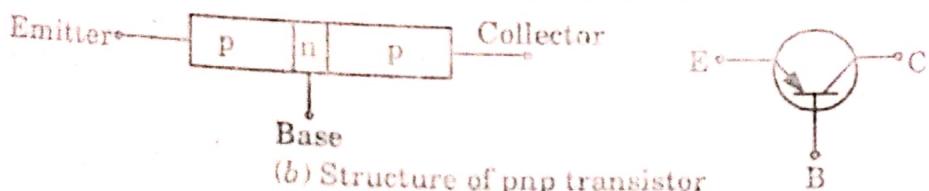
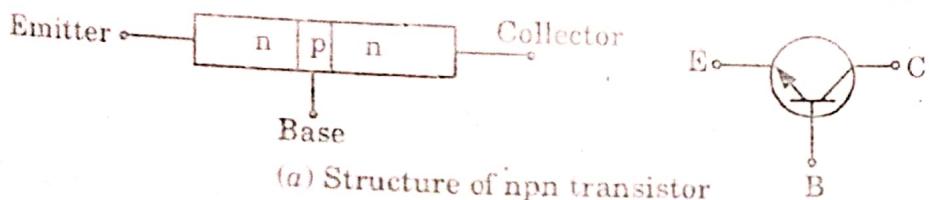


Fig. 3.1.1.

6. A transistor has three doped regions :

**a. Emitter :**

- i. This is the left hand section of the transistor.
- ii. The main function of this region is to supply majority charge carriers (either holes or electrons) to the base and hence it is more heavily doped in comparison to other regions.

**b. Base :**

- i. The middle section of the transistor is known as base.
- ii. This is very lightly doped and is very thin ( $10^{-6}$  m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

**c. Collector :**

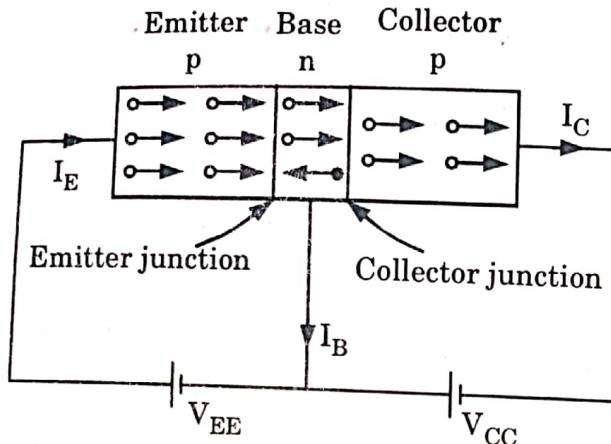
- i. The right hand section of transistor is known as collector.
- ii. The main function of the collector is to collect majority charge carriers through the base. This is moderately doped.
- 7. The arrow head direction indicates the conventional direction of current flow i.e., in case of *n-p-n* it is from base to emitter while in case of *p-n-p* it is from emitter to base.
- 8. In most of the cases the collector region is made large due to the fact that collector has to dissipate much greater power.
- 9. The junction between emitter and base may be called as emitter-base junction and junction between base and collector may be called as collector-base junction.
- 10. The emitter-base junction is always forward biased while the collector-base junction is reversed biased.
- 11. The resistance of emitter-base junction is very small as compared to collector-base junction.
- 12. So, forward bias applied to emitter-base junction is generally very small and reverse bias on collector-base junction is much higher.

**Que 3.2.** | Describe the operation of *p-n-p* transistor.

**Answer**

1. *p-n-p* transistor with emitter base junction as forward bias and collector base junction as reversed biased is shown in Fig. 3.2.1.
2. The holes of *p*-region are repelled by positive terminal of battery  $V_{EE}$  towards the base.
3. The potential barrier at emitter base junction is reduced as it is forward bias and holes cross this junction and penetrate into *n*-region, constitute the emitter current  $I_E$ .
4. The width of base is very thin and only 5 % of holes recombine with the free electrons of *n*-region which constitutes the current  $I_B$ .

5. The remaining holes are able to drift across the base and enter into the collector region.
6. They are swept up by negative collector voltage  $V_{CC}$ . This constitutes the collector current  $I_C$ .



**Fig. 3.2.1. Operation of pnp transistor.**

7. As holes reach the collector, electrons are emitted from the negative terminal of battery and neutralize these holes.
8. Now a covalent bond near the emitter electrode breaks down. The liberated electron enters the positive terminal of battery  $V_{EE}$ . This process is repeated again and again.
9. As the width of the base region is very small, the ratio of hole current to electron current is very large so the electron current may be neglected.
10. Thus only the hole current plays the important role in the operation of pnp transistor.

**Que 3.3.** Explain the operation of *npn* transistor.

OR

Explain various current components in *npn* transistor with help of suitable diagram.

**AKTU 2016-17(Sem-I), Marks 05**

**Answer**

1. The biasing of *npn* transistor is shown in Fig. 3.3.1.
2. The emitter base junction is forward biased because electrons are repelled from the negative terminal of battery  $V_{EE}$  towards the junction.
3. The collector base junction is reversed biased because electrons are flowing away from the collector junction towards the positive collector battery terminal  $V_{CC}$ .
4. The electrons in emitter region are repelled from the negative terminal of the battery towards the emitter junction.

5. Since the potential barrier at the junction is reduced due to forward bias and base region is very thin and lightly doped, electrons cross the *p*-type base region.
6. A few electrons combine with the holes in *p*-region and are lost as charge carrier.
7. Now electrons in *n*-region swept up by positive collector voltage  $V_{CC}$ . In this way electron conduction takes place, continuously so long as the two junctions are properly biased.
8. So the current conduction in *npn* transistor is carried out by the electrons.

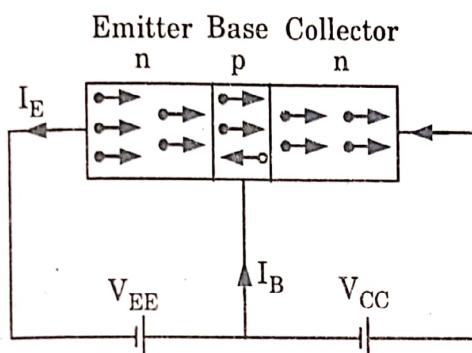


Fig. 3.3.1.

9. Applying Kirchhoff's current law,

$$I_E = I_C + I_B$$

10. The collector current has two components the majority and minority carriers. The minority current component is called leakage current ( $I_{CO}$ ).

So,  $I_C = I_{C \text{ majority}} + I_{CO \text{ minority}}$

**Que 3.4.** Describe the biasing of BJT circuit.

**Answer**

1. Biasing is necessary to establish the proper region of operation for AC amplification.
2. The emitter layer is heavily doped, base is lightly doped and collector is moderately doped.
3. This low doping level decreases the conductivity and hence increases the resistance of the material by limiting the number of "free" carriers.

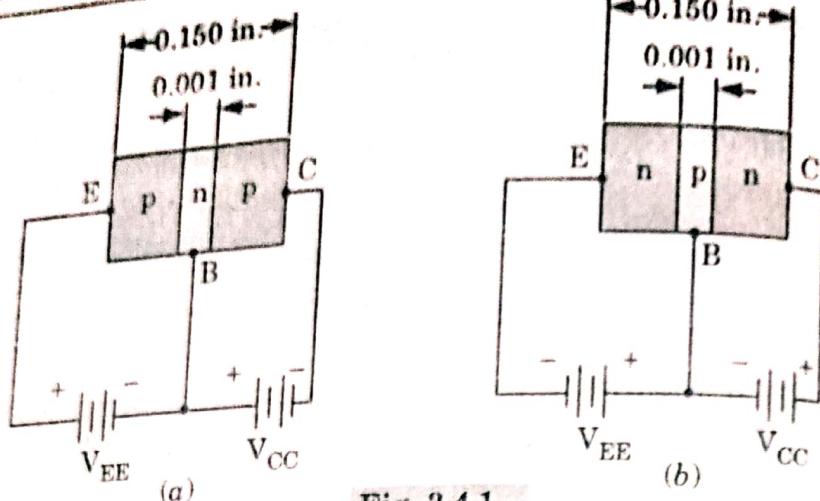


Fig. 3.4.1.

**A. For pnp transistor :**

- i. pnp transistor with emitter base junction as forward bias and collector base junction as reverse biased.
- ii. The potential barrier at emitter-base junction is reduced as it is forward biased and holes pass through this junction.
- iii. By applying a negative voltage at collector, the holes are easily drifted across the collector-base junction to constitute a current  $I_C$ .

**B. For npn transistor :**

- i. The emitter-base junction of npn is forward bias and the electron is repelled by a negative forward junction.
- ii. The collector-base function is reverse bias because electrons flow toward positive collector battery terminal  $V_{cc}$  to constitute a current  $I_C$ .

**Que 3.5.** Explain transistor as an amplifier in detail.

**Answer**

1. The transistor has two p-n junctions i.e., it is like two diodes. The junction between emitter and base may be called emitter-base diode or simply emitter diode. The junction between base and collector may be called as collector-base diode or collector diode. The basic circuit of a transistor amplifier is shown in Fig. 3.5.1.
2. The weak signal to be amplified is applied between emitter-base circuit and the output is taken across the load resistor  $R_L$  connected in the collector-base circuit.
3. Let us assume for instant  $V_{ee}$  is disconnected.
4. Now for negative peak of signal, the emitter base junction will be reversed bias, which is not desirable, because to achieve amplification, the input circuit should remain forward bias.

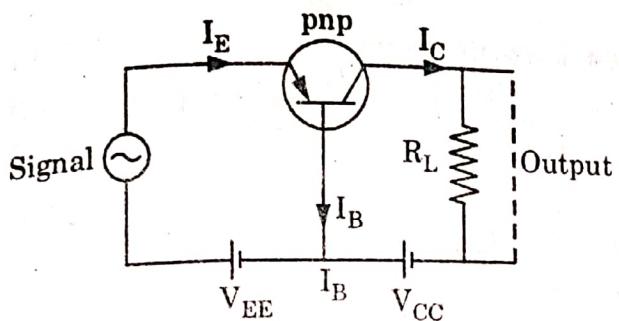


Fig. 3.5.1. Transistor as an amplifier.

5. A small change in signal voltage produces an appreciable change in emitter current because the input circuit has low resistance.
6. Due to transistor action, the change in emitter current causes almost the same change in collector current.
7. When the collector current flows through the load resistance  $R_L$ , a large voltage is developed across it.
8. In this way, a weak signal applied in the input circuit appears in the amplified form across the output circuit.
9. Let, small voltage change  $\Delta V_i$  causes large emitter current change  $\Delta I_E$ . We define it by the symbol  $\alpha$  that fraction of this current change is collected and pass through  $R_L$ .

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ i.e., } \Delta I_C = \alpha \Delta I_E$$

10. The change in output voltage across load resistor

$$\begin{aligned}\Delta V_O &= R_L \times \Delta I_C \\ &= R_L \times \alpha \times \Delta I_E\end{aligned}$$

11. The voltage amplification

$$A = \frac{\Delta V_O}{\Delta V_i}$$

will be greater than unity and transistor acts as an amplifier.

## PART-2

*Common Base, Common Emitter, Common Collector Configuration.*

### Questions-Answers

### Long Answer Type and Medium Answer Type Questions

- Que 3.6. Draw the basic structure of CB BJT and explain its principle of operation with in neat diagram along with its input and output characteristics. AKTU 2017-18(Sem-II), Marks 07

OR

**Explain the working of a common base circuit with its circuit diagram.**

AKTU 2015-16(Sem-II), Marks 06

**Answer**

**Common-base (CB) configuration :**

1. In this configuration, the input signal is applied between emitter and base. The output is collected from collector and base as shown in Fig. 3.6.1.

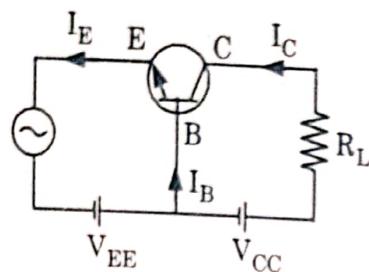


Fig. 3.6.1. Common-base *n*p*n* transistor amplifier.

**Current amplification factor ( $\alpha$ ) :**

1. It is defined as the ratio of the collector current to the emitter current of a transistor when no signal is applied and is called DC alpha ( $\alpha_{DC}$ ).

$$\alpha_{DC} = \frac{I_C}{I_E}$$

2. Simply  $\alpha_{DC}$  is  $\alpha$

Then 
$$\alpha = \frac{I_C}{I_E}$$

3. Higher the value of  $\alpha$  better is the transistor in the sense that collector current approaches the emitter current.

$$I_C = \alpha I_E \text{ and } I_B = I_E - I_C$$

$$I_B = I_E - \alpha I_E = I_E (1 - \alpha)$$

4. Now, when signal is applied, the ratio of change in collector to emitter current at constant collector base voltage is defined as current amplification factor.

$$\alpha_{AC} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB} = \text{constant}}$$

Practically  $\alpha_{DC} = \alpha_{AC} = \alpha = 0.9$  to 0.99

5. Total collector current  $I_C = \underbrace{\alpha I_E}_{\text{Majority}} + \underbrace{I_{CBO}}_{\text{Minority}}$

6. The collector current can also be expressed as

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left( \frac{\alpha}{1 - \alpha} \right) I_B + \left( \frac{1}{1 - \alpha} \right) I_{CBO}$$

7. The relation between  $\alpha$  and  $\beta$  is given by

$$\alpha = \frac{\beta}{1 + \beta} \text{ or } 1 - \alpha = \frac{1}{1 + \beta}$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

Characteristics of CB circuit :

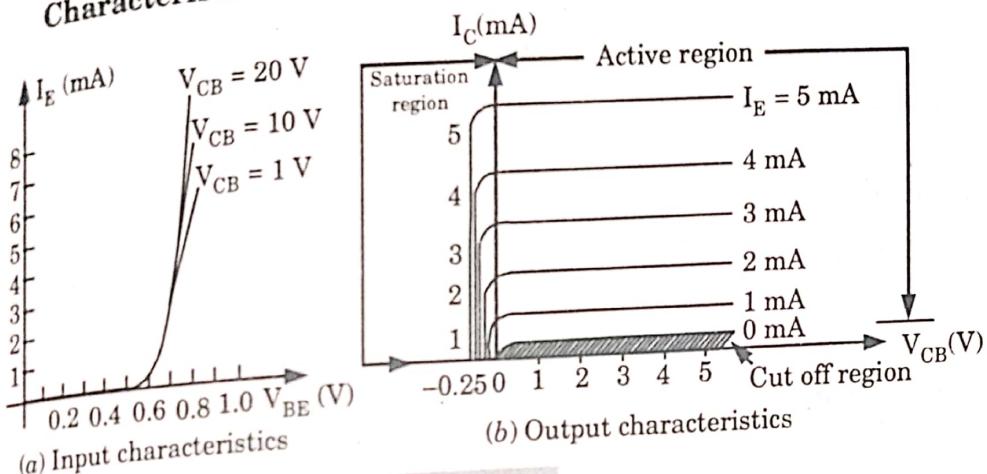


Fig. 3.6.2.

#### Input characteristics :

- i. There exists a cut in, offset or threshold voltage  $V_{BE}$  below which the current is very small.
- ii.  $I_E$  increases rapidly with small increase in  $V_{BE}$  i.e., input resistance is very small.

#### Output characteristics :

- i. In active region, the collector current is independent of collector voltage and depends upon emitter current but if  $V_{CB}$  increases beyond a certain value,  $I_C$  increases rapidly due to avalanche breakdown.  
In this region, the base-emitter function is forward biased whereas collector-base function is reversed biased.
- ii. In cut off region, a small amount of collector current flows even when  $I_E = 0$ . i.e., leakage current  $I_{CBO}$ .  
Here emitter-base and collector-base junctions both are reversed biased.
- iii. In saturation region, current  $I_C$  flows even if  $V_{CB} \geq 0$ .  
Here collector and emitter junctions both are forward biased.

**Que 3.7.** Draw and explain the input and output characteristics of common emitter configuration.

AKTU 2015-16(Sem-I), Marks 05

OR

Draw the basic structure of a CE BJT and explain its principle of operation with neat diagrams along with its input output characteristics.

AKTU 2013-14(Sem-II), Marks 05

OR

Draw the common emitter circuit and sketch the input and output characteristics. Also explain active region, cut-off region and saturation region by indicating them on the characteristics curve.

AKTU 2017-18(Sem-I), Marks 07

OR

Draw the CE configuration circuit of BJT and explain its input and output characteristics.

AKTU 2015-16(Sem-II), Marks 7.5

OR

Draw the circuit diagram of BJT in CE configuration. Draw output characteristic curves and indicate the different regions of operation.

AKTU 2016-17(Sem-I), Marks 05

OR

Draw input and output characteristics of CE npn transistor configuration with proper labels.

AKTU 2014-15(Sem-II), Marks 05

### Answer

1. In CE configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter.
2. As emitter is common to input and output circuits, hence the name common emitter configuration and is shown in Fig. 3.7.1.

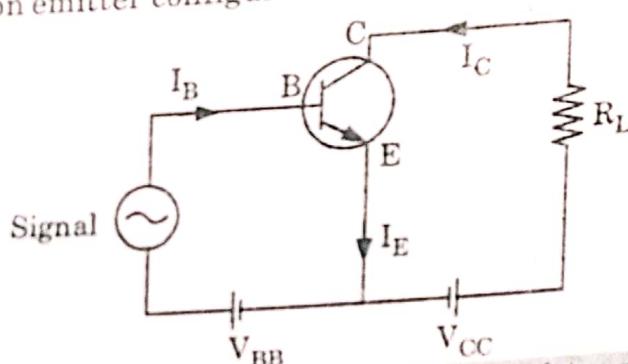


Fig. 3.7.1. Common-emitter npn transistor amplifier.

3. The base current amplification factor is the ratio of collector current to the base current and is also called DC beta ( $\beta_{DC}$ ) of a transistor, when no signal is applied.

$$\beta_{DC} = \beta = \frac{I_C}{I_B}$$

4. When signal is applied, the ratio of change in collector current to the change in base current is defined as current amplification factor.

$$\beta_{AC} = \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_C = \beta I_B$$

$\beta$  is generally greater than 20 and ranges from 20 to 500. Hence, this configuration is frequently used when current gain as well as voltage gain is required.

5. Total collector current

$$I_C = \beta I_B + I_{CEO}$$

6. We know that  $I_E = I_B + I_C$

$$I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

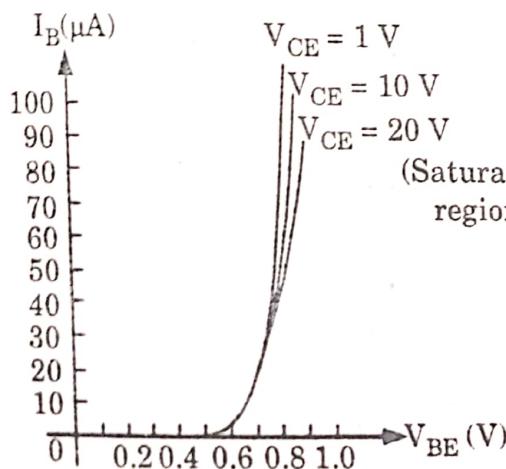
$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

7. On solving we get  $\beta = \frac{\alpha}{1 - \alpha}$  and  $I_{CEO} = \frac{1}{1 - \alpha} I_{CBO}$

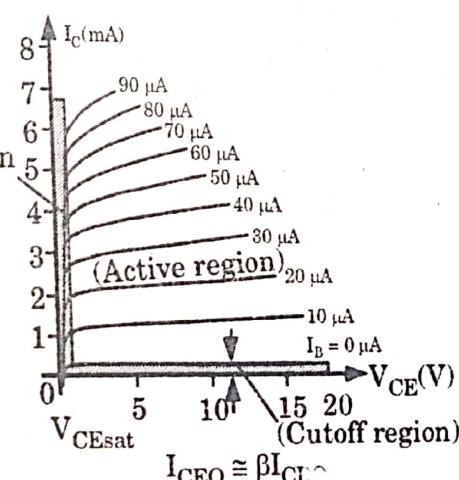
#### Characteristics of common emitter circuit :

##### Input characteristic :

- The forward biased diode curve is expected because the base emitter section of transistor is a diode and it is forward biased.
- In this case,  $I_B$  increases less rapidly with  $V_{BE}$  as compared to common base configuration i.e., input resistance of common emitter is higher than common base circuit.



(a) Input characteristics



(b) Output characteristics

Fig. 3.7.2.

##### Output characteristics :

- In active region, for small values of base current, the effect of collector voltage over collector current is small while for large base current

- values effect increases. Thus, the current gain of this configuration is greater than unity.
- When  $V_{CE}$  has very low value, the transistor is said to be saturated. The change in  $I_B$  does not produce a corresponding change in  $I_C$ .
  - In cut off region, a small amount of  $I_C$  flows even when  $I_B = 0$ , i.e.,  $I_{CBO}$  and the transistor is said to be cut-off.

**Que 3.8.** Explain the operation of common collector configuration with suitable characteristics in detail.

AKTU 2014-15(Sem-I), Marks 10

**Answer**

- The circuit diagram for determining the static characteristics of an n-p-n transistor in the common collector configuration is shown in Fig. 3.8.1.

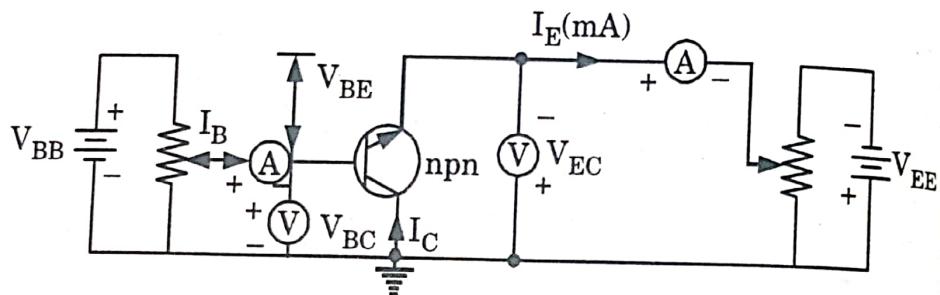


Fig. 3.8.1.

**Input characteristics :**

- To determine the input characteristics,  $V_{EC}$  is kept at a suitable fixed value.
- The base-collector voltage  $V_{BC}$  is increased in equal steps and the corresponding increase in  $I_B$  is noted.
- This is repeated for different fixed values of  $V_{EC}$ . Plot of  $V_{BC}$  versus  $I_B$  for different values of  $V_{EC}$  is shown in Fig. 3.8.2.

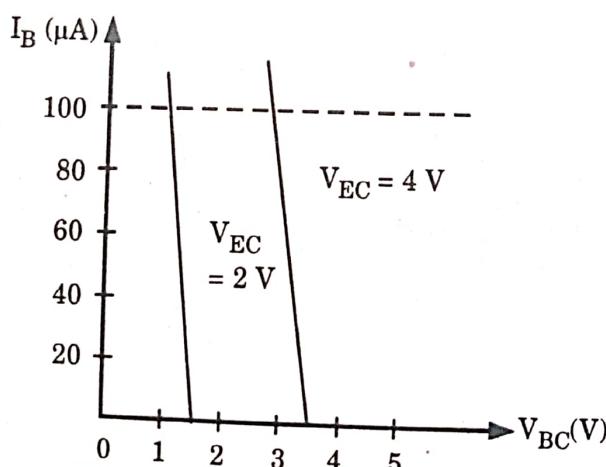


Fig. 3.8.2. Input characteristics.

1. Output characteristics :
- The output characteristics shown in Fig. 3.8.3 are the plots of  $V_{EC}$  versus  $I_C$  for different values of  $I_B$ .

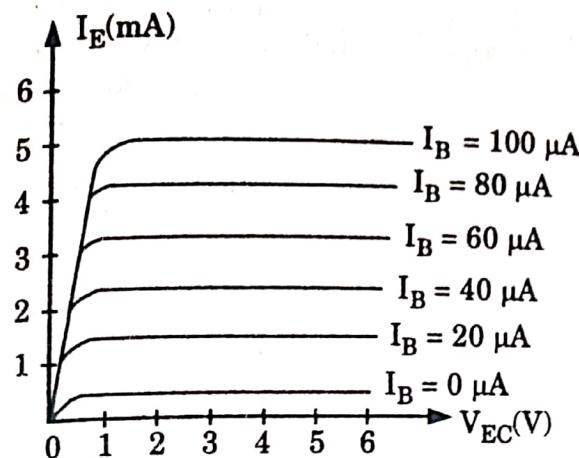


Fig. 3.8.3. Output characteristics.

Que 3.9.

Derive the relation between  $\alpha$ ,  $\beta$  and  $\gamma$ .

Answer

1.  $\alpha = \frac{I_C}{I_E}$  and  $\beta = \frac{I_C}{I_B}$

2.  $I_E = I_B + I_C$ ,  $I_B = I_E - I_C$

3. Now  $\beta = \frac{I_C}{I_E - I_C} = \frac{I_C / I_E}{1 - I_C / I_E} = \frac{\alpha}{1 - \alpha}$

$\beta(1 - \alpha) = \alpha$  or  $\beta - \beta\alpha = \alpha$

$\beta = \alpha(1 + \beta)$

$\therefore \alpha = \frac{\beta}{1 + \beta}$

or  $\frac{1}{1 - \alpha} = 1 + \beta$

4.  $\gamma = \frac{I_E}{I_B}$  and  $\alpha = \frac{I_C}{I_E}$

5. Also  $I_B = I_E - I_C$

6.  $\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - (I_C / I_E)} = \frac{1}{1 - \alpha}$  ... (3.9.1)

7. We have,  $1 - \alpha = \frac{1}{1 + \beta}$  ... (3.9.2)

8. Put values of eq. (3.9.2) in eq. (3.9.1)

$$\gamma = \frac{1}{1 - \alpha} = 1 + \beta$$

**Que 3.10.** An *n-p-n* transistor with  $\beta = 98$  is operated in the *CE* configuration, if the emitter current is 2 mA and reverse saturation current is 12  $\mu\text{A}$ . What are the base and collector current?

AKTU 2016-17(Sem-I), Marks 05

**Answer**

Given :  $\beta = 98$ ,  $I_E = 2 \text{ mA}$ ,  $I_{sat} = 12 \mu\text{A}$

To Find :  $I_B$ ,  $I_C$

$$\alpha = \frac{\beta}{1 + \beta} = \frac{98}{1 + 98} = 0.99$$

$$\therefore \alpha = \frac{I_C}{I_E}$$

$$\therefore I_C = \alpha I_E = 0.99 \times 2 = 1.98 \text{ mA}$$

$$I_B = I_E - I_C = 2 - 1.98 = 0.02 \text{ mA}$$

**Que 3.11.** For the network of Fig. 3.11.1.

- Determine  $R_B$  and  $R_E$
- Find  $V_B$ ,  $V_{CE}$ , and  $V_{BE}$

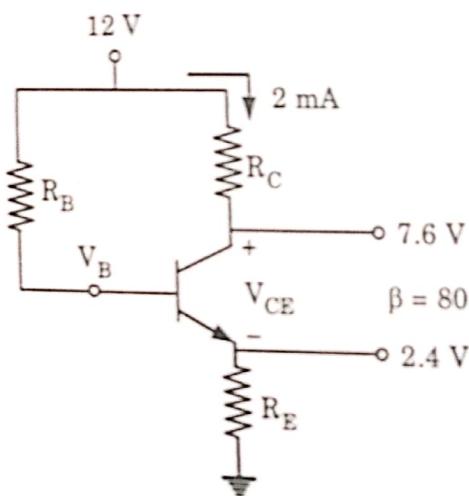


Fig. 3.11.1.

AKTU 2017-18(Sem-I), Marks 0

**Answer**

- Given,  $V_{CC} = 12 \text{ V}$ ,  $V_C = 7.6 \text{ V}$ ,  $V_E = 2.4 \text{ V}$ ,  $\beta = 80$   
then  $V_{CE} = V_C - V_E = 7.6 \text{ V} - 2.4 \text{ V} = 5.2 \text{ V}$

- Now

$$\alpha = \frac{\beta}{\beta + 1} = \frac{80}{80 + 1} = 0.98$$

So,

$$I_E = I_C/\alpha \approx 2 \text{ mA} \text{ and } I_B = I_C/80 = 0.025 \text{ mA}$$

$$R_E = \frac{V_E}{I_E} = \frac{2.4 \text{ V}}{2 \text{ mA}} = 1.2 \text{ k}\Omega$$

3. Now

$$V_{CC} = V_{CE} + I_C R_C + I_E R_E$$

$$12 = 5.2 + 2R_C + 1.2 \times 2$$

$$R_C = 2.2 \text{ k}\Omega$$

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$12 = 0.025 \text{ mA} \times R_B + 0.7 \text{ V} + 1.2 \times 2$$

$$R_B = 356 \text{ k}\Omega$$

$$V_B = V_E + V_{BE} = 2.4 + 0.7 = 3.1 \text{ V}$$

$$V_{BC} = V_B - V_C \\ = 3.1 - 7.6 = -4.5 \text{ V}$$

and

Now,

**PART-3***DC Biasing BJTs : Operating Point.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 3.12.** Give the brief explanation about the transistor circuit analysis with respect to DC load line.

**Answer**

1. Consider a common emitter *n-p-n* transistor circuit shown in Fig. 3.12.1 where no signal is applied therefore, DC conditions prevail in the circuit.

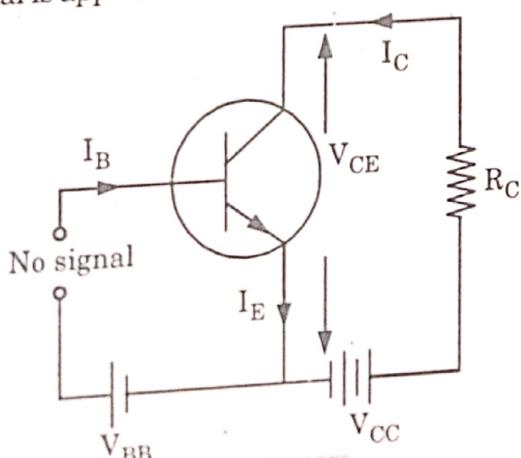


Fig. 3.12.1.

2. From Fig. 3.12.1,

$$V_{CE} = V_{CC} - I_C R_C$$

...(3.12.1)

3-16 D (ESC-Sem-3 &amp; 4)

...(3.12.2)

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \quad \dots(3.12.3)$$

$$I_C = \left( -\frac{1}{R_C} \right) V_{CE} + \frac{V_{CC}}{R_C} \quad \dots(3.12.3)$$

3. Since  $V_{CC}$  and  $R_C$  are fixed values, therefore, eq. (3.12.3) represents a straight line with slope  $-1/R_C$  the straight line represented by eq. (3.12.3) is called the DC load line. To add load line, we need two end points of the straight line. These two points can be calculated as under:
- i. When Maximum  $I_C = 0, V_{CE}$  is maximum i.e.,  $V_{CE} = V_{CC} - I_C R_C = V_{CC}$
  - ii. When Maximum  $V_{CE} = 0, I_C$  is maximum i.e.,  $V_{CE} = I_C R_C$

Thus, the DC load line AB can be drawn if the values of  $R_C$  and  $V_{CC}$  are known.

#### Operating point :

1. The zero signal values of  $I_C$  and  $V_{CE}$  are known as the operating point.
2. It is also called the quiescent point or Q-point because it is the point on  $I_C - V_{CE}$ .

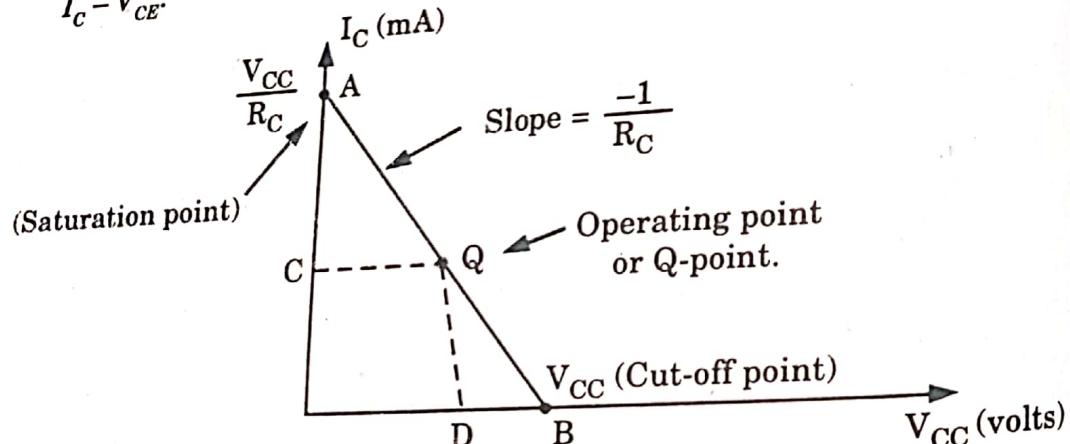


Fig. 3.12.2.

#### PART-4

*Voltage Divider Bias Configuration, Collector Feedback,  
Emitter Follower Configuration.*

#### Questions-Answers

**Long Answer Type and Medium Answer Type Questions**

**Que 3.18.** Explain the operation of voltage divider bias circuit and write down the approximate equations of  $V_B$ ,  $I_E$ ,  $I_C$  and  $V_{CE}$ .

AKTU 2014-15(Sem-I), Marks 10

OR

What is a well-designed voltage divider biasing (VDB) circuit?

AKTU 2015-16(Sem-II), Marks 05

**Answer**

**Voltage Divider Bias :**

- Fig. 3.13.1 shows the most widely used biasing circuit in this method, the base circuit contains a voltage divider ( $R_1$  and  $R_2$ ). Because of this, the circuit is called voltage divider bias (VDB).

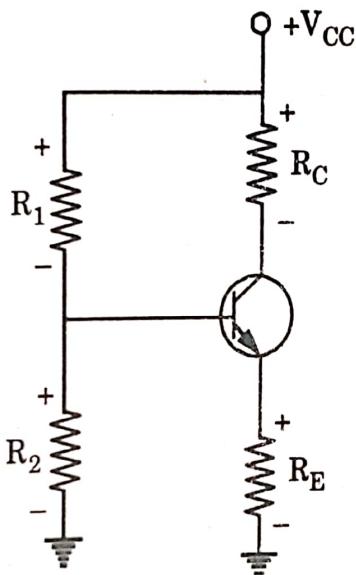


Fig. 3.13.1.

**Circuit analysis :**

- In VDB circuit, the base current is much smaller than the current through the voltage divider.
- Therefore we can open the connection between the voltage divider and the base to get the equivalent circuit of Fig. 3.13.2(a).
- In this circuit the output of the voltage divider is

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad \dots(3.13.1)$$

- Ideally, this is the base-supply voltage as shown in Fig. 3.13.2(b).

3-18 D (ESC-Sem-3 & 4)

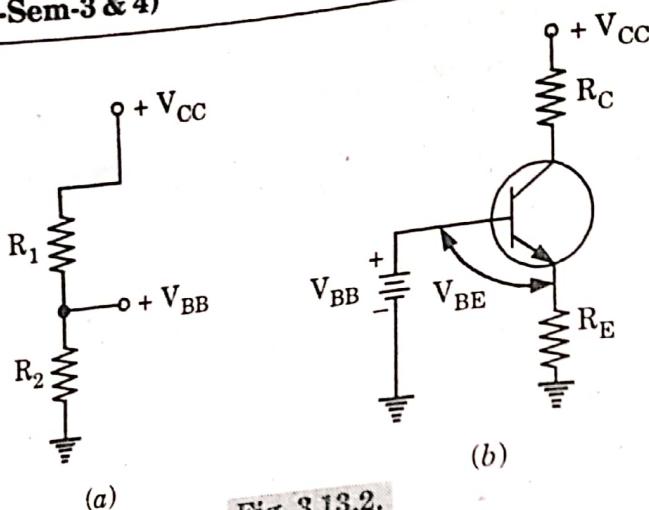


Fig. 3.13.2.

5. From Fig. 3.13.2(b)  $V_E = V_{BB} - V_{BE}$  ... (3.13.2)

$$I_E = \frac{V_E}{R_E} \quad \dots(3.13.3)$$

...(3.13.4)

$$V_C \equiv V_{CC} = I_C R_C \quad \dots(3.13.5)$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad \dots(3.13.6)$$

$$V_B = I_E R_E + 0.7$$

**Que 3.14.** Explain collector feedback configuration.

OR

Draw the CE *npn* BJT characteristics. Also explain the self bias configuration in DC bias configuration.

AKTU 2016-17(Sem-II), Marks 5.25

OR

**OR**  
Why is transistor biasing required ? Describe collector to base biasing in CE *npn* transistor circuit.

AKTU 2016-17(Sem-I), Marks 05

ANSWER

**CE npn BJT characteristics :** Refer Q. 3.7, Page 3-9D, Unit-3.

**Transistor biasing:** Refer Q. 3.4, Page 3-5D, H-unit 3.

**Transistor biasing :** Refer Q. 3.4, Pa  
**Collector feedback configuration:**

- Collector feedback configuration :**

  - Fig. 3.14.1 shows collector-feedback bias (also called self-bias).
  - Stabilizing the  $Q$  point, the basic idea is to feedback a voltage to the base in an attempt to neutralize any change in collector current.

3. For instance, suppose the collector current increases.  
 4. This decreases the collector voltage, which decreases the voltage across the base resistor.

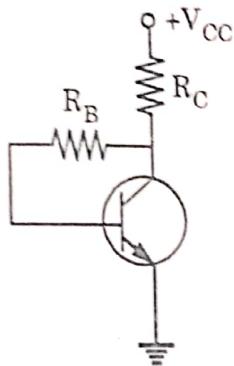


Fig. 3.14.1.

5. In turn, this decreases the base current which opposes the original increase in collector current.  
 6. The equations for analyzing collector feedback bias are :

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / (\beta_{DC} + 1)} \quad \dots(3.14.1)$$

$$V_B = 0.7 \text{ V} \quad \dots(3.14.2)$$

$$V_c = V_{CC} - I_C R_C \quad \dots(3.14.3)$$

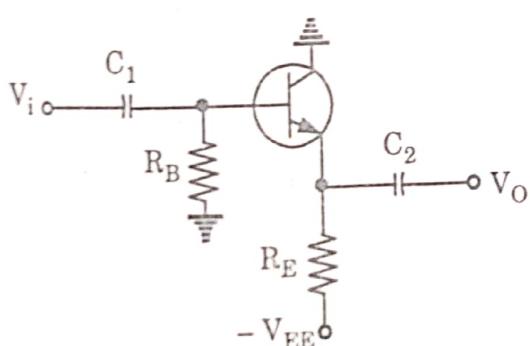
7. The *Q* point is usually set near the middle of the load line by using a base resistance of :

$$R_B = \beta_{DC} R_C \quad \dots(3.14.4)$$

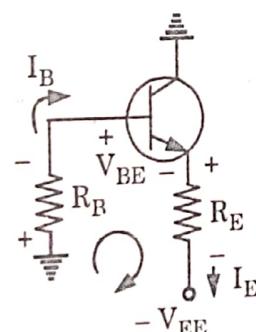
**Que 3.15.** Explain emitter follower configuration.

**Answer**

1. Here the output is taken from emitter terminal as shown in Fig. 3.15.1.



(a) Common-collector  
(emitter-follower) configuration.



(b) DC equivalent.

Fig. 3.15.1.

2. Applying Kirchhoff's voltage rule to the input circuit will result in

$$= I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\text{and using } I_E = (\beta + 1) I_B$$

$$I_B R_B + (\beta + 1) I_B R_E = V_{EE} - V_{BE}$$

$$\text{so that } I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

3. For the output an application of Kirchhoff's voltage law will result in

$$- V_{CE} - I_E R_E + V_{EE} = 0$$

$$\text{and } V_{CE} = V_{EE} - I_E R_E$$

### PART-5

*Fixed-Bias, Emitter Bias, Configuration, Bias Stabilization.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 3.16.** Explain bias stabilization.

**OR**

Derive the stability factor  $S(I_{CO})$  for the fixed bias configuration.

**AKTU 2014-15(Sem-II), Marks 05**

#### Answer

1. The stability of a system is a measure of sensitivity of a network to variation in its parameters. In any amplifier employing a transistor the collector current  $I_C$  is sensitive to each of the following parameters :
  - i.  $\beta$  increases with increase in temperature
  - ii.  $V_{BE}$  decreases about 2.5 mV per degree Celsius ( $^{\circ}\text{C}$ ) increase in temperature.
  - iii.  $I_{CO}$  (reverse saturation current) doubled in value for every  $10^{\circ}\text{C}$  increase in temperature.

#### Stability Factors :

1. A stability factor  $S$  is defined for each of the parameters affecting bias stability as follows :

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

2. Here,  $\Delta$  signifies the change in that quantity. Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

### Emitter-Bias Configuration $S(I_{CO})$ :

$$S(I_{CO}) = (\beta + 1) \frac{1 + R_B / R_E}{(\beta + 1) + R_B / R_E} \quad \dots(3.16.1)$$

1.

For  $R_B / R_E \gg (\beta + 1)$ ,

$$S(I_{CO}) = (\beta + 1) \quad \dots(3.16.2)$$

∴

3. For  $R_B / R_E \ll 1$ ,

$$S(I_{CO}) = (\beta + 1) \frac{1}{(\beta + 1)} = 1 \quad \dots(3.16.3)$$

4. For the range where  $R_B / R_E$  ranges between 1 and  $(\beta + 1)$ , the stability factor will be determined by

$$S(I_{CO}) \approx \frac{R_B}{R_E} \quad \dots(3.16.4)$$

as shown in Fig. 3.16.1.

5. The result reveals that the emitter bias configuration is quite stable when the ratio  $R_B / R_E$  is as small as possible and become stable when the same ratio approaches  $(\beta + 1)$ .

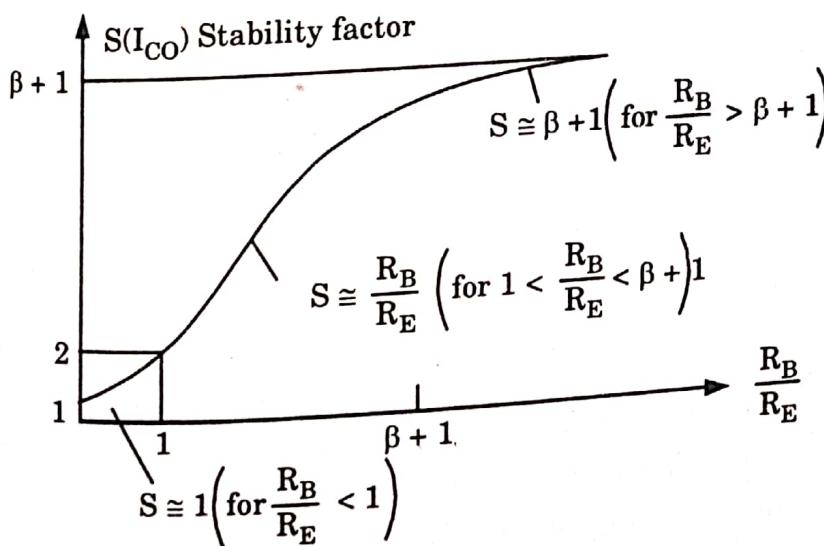


Fig. 3.16.1.

### Fixed Bias Configuration :

For the fixed-bias configuration, if we multiply the top and bottom of eq. (3.16.1) by  $R_E$  and then plug in  $R_E = 0 \Omega$ , the following equation results

## 3-22 D (ESC-Sem-3 &amp; 4)

$$S(I_{CO}) = \beta + 1$$

**Voltage-Divider Bias Configuration :**

$$S(I_{CO}) = (\beta + 1) \frac{1 + R_{th}/R_E}{(\beta + 1) + R_{th}/R_E} \quad \dots(3.16.5)$$

**Feedback-Bias Configuration :**

$$S(I_{CO}) = (\beta + 1) \frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C} \quad \dots(3.16.6)$$

**$S(V_{BE})$  :**

1. The stability factor is defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \quad \dots(3.16.7)$$

and results in the following equation for the emitter bias configuration

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E} \quad \dots(3.16.8)$$

2. If  $R_E = 0$  as it occurs for fixed-bias configuration

$$S(V_{BE}) = -\frac{\beta}{R_B} \quad \dots(3.16.9)$$

3. Eq. (3.16.8) can be written in the following form :

$$S(V_{BE}) = \frac{-\beta/R_E}{R_B/R_E + (\beta + 1)} \quad \dots(3.16.10)$$

4. If  $(\beta + 1) \gg R_B/R_E$

$$\text{then, } S(V_{BE}) \cong \frac{-\beta/R_E}{\beta + 1} \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E} \quad \dots(3.16.11)$$

which shows that larger the resistance  $R_E$ , lower is the stability factor and more stable is the system.

**$S(\beta)$  :**

1. For emitter-bias configuration,

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

where,  $I_{C_1}$  and  $\beta_1$  are used to define their values under one set of network conditions, whereas  $\beta_2$  is used to define new value of  $\beta$  established by changes in temperature

2. For fixed-bias configuration,  $S(\beta) = I_{C_1}/\beta_1$ .
3. For the collector feedback configuration with  $R_E = 0 \Omega$

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + R_C(1 + \beta_2))}$$

**PART-6**

*CE, CB, CC Amplifiers and AC Analysis of Single Stage CE Amplifier (re model).*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 3.17.** Write an expression for small signal hybrid model  $h$  parameters  $A_v, A_i, R_i, R_o$  for  $CE$  voltage divider bias amplifier circuit with emitter bypass capacitor ( $C_E$ ).

**OR**

Discuss AC equivalent model of voltage divider biased amplifier in  $CE$  configuration. AKTU 2016-17(Sem-I), Marks 7.5

**Answer**

1. Voltage divider circuit :

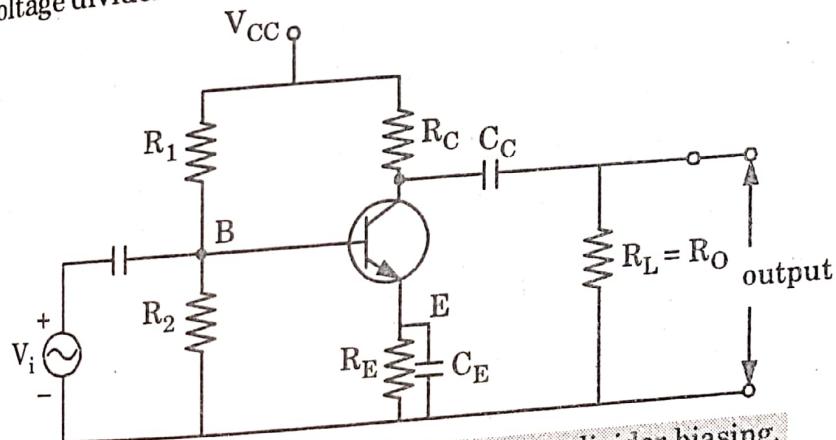


Fig. 3.17.1.  $CE$  amplifier with voltage divider biasing.

2. The equivalent  $h$ -parameter circuit for this voltage divider  $CE$  amplifier is shown in Fig. 3.17.2.

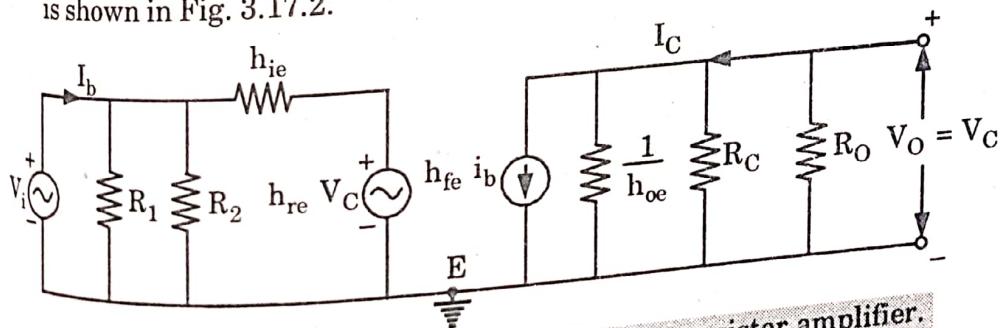


Fig. 3.17.2. AC equivalent circuit for the  $CE$  transistor amplifier.

3. On the output side, the two resistors  $R_C$  and  $R_O$  can be replaced by a single resistor

$$R_{AC} = R_C \parallel R_O = \frac{R_C R_O}{R_C + R_O}$$

4. On the input side, if the input voltage source  $V_i$  is assumed to be ideal (with zero internal resistance), the presence and absence of  $R_1$  and  $R_2$  is unimportant because the voltage across them will remain same i.e.,  $V_p$  so they can be neglected. Thus the circuit will become :

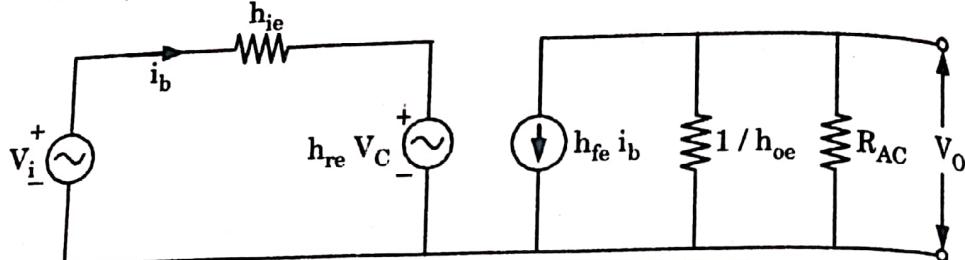


Fig. 3.17.3. AC equivalent circuit.

5. Since  $\frac{1}{h_{oe}} = 40 \text{ k}\Omega$  ( $\because h_{oe} = 25 \text{ A/V}$ )  
 $\therefore (1/h_{oe}) \parallel R_{AC} \approx R_{AC}$   
 And  $h_{re} = 1 \times 10^{-4}$

So  $h_{re} \cdot V_C$  can be neglected. Thus the equivalent circuit will be

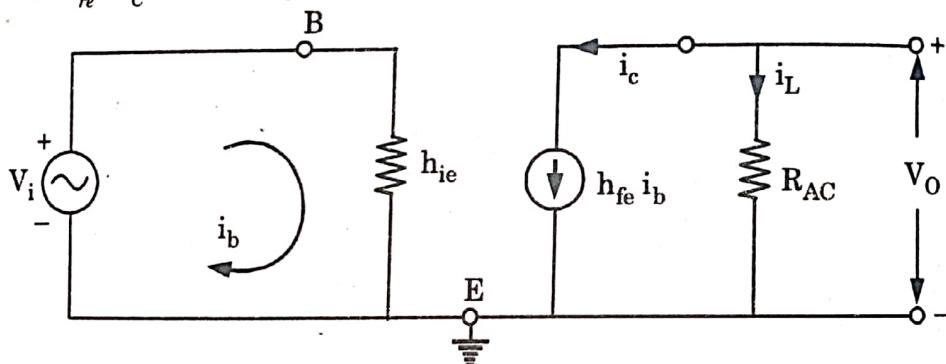


Fig. 3.17.4. AC equivalent circuit after assumption.

Current gain ( $A_i$ ) :

1. Output current,  $i_c = h_{fe} \cdot i_b$

2. Current gain,  $A_i = \frac{\text{output current}}{\text{input current}} = \frac{i_c}{i_b} = \frac{h_{fe} i_b}{i_b}$   
 $A_i = h_{fe} = \beta$

Voltage gain ( $A_v$ ) :

1. Output voltage,  $V_o = \text{output current} \times \text{output resistance}$

$$V_o = i_e \times R_{AC}$$

$$V_o = -i_c \times R_{AC}$$

$$\{\because i_e = -i_c\}$$

2. Input voltage,  $V_i = i_b \cdot h_{ie}$

3. Voltage gain,

$$A_V = \frac{\text{output voltage}}{\text{input voltage}} = \frac{V_o}{V_i} = \frac{-h_{fe} \cdot i_b \cdot R_{AC}}{i_b \cdot h_{ie}}$$

$$A_V = \frac{-h_{fe} \cdot R_{AC}}{h_{ie}}$$

$$A_V = \frac{\beta R_{AC}}{h_{ie}} \angle 180^\circ$$

or

(It means that the phase difference between input and output is  $180^\circ$ .)

Power gain ( $A_p$ ):

1. It is simply the product of current gain and voltage gain.
2. Power gain = Voltage gain  $\times$  current gain

$$A_p = A_i \cdot A_V = h_{fe} \times \frac{-h_{fe} \cdot R_{AC}}{h_{ie}} = \frac{-h_{fe}^2 \cdot R_{AC}}{h_{ie}}$$

Input impedance ( $Z_{in}$ ) or  $R_i$ :

1. Input impedance

$$Z_{in}' = \frac{\text{input voltage}}{\text{input current}} = \frac{V_i}{i_b} = \frac{i_b \cdot h_{ie}}{i_b}$$

$$Z_{in}' = h_{ie}$$

2. If biasing resistors  $R_1$  and  $R_2$  are to be considered the input impedance will be

$$Z_{in}' = R_1 \parallel R_2 \parallel h_{ie} = h_{ie}$$

(Since  $h_{ie}$  much smaller than  $R_1$  and  $R_2$ )

3. If source is not ideal and has internal resistance  $R_s$  then input impedance

$$Z_{in}' = Z_{in} + R_s$$

Output impedance ( $Z_o$ ) or  $R_o$ :

$$1. Z_o = \left. \frac{\text{output voltage}}{\text{output current}} \right|_{\text{Input } V_i=0}$$

2. If  $V_i = 0$ , the current  $i_b = 0$

$$i_c = \beta i_b = 0$$

$$\therefore Z_o = \frac{V_o}{0}$$

$$Z_o = \infty$$

3. Taking  $h_{oe}$  in account then

$$Z_o' = 1/h_{oe}$$

4. And the total impedance

$$Z_o' = Z_o \parallel R_{AC} = (1/h_{oe}) \parallel R_{AC} \quad \{ \because 1/h_{oe} \rightarrow \text{is very small} \}$$

$$Z_o = R_{AC}$$

- Que 3.18.** Derive the complete hybrid equivalent model of BJT in common emitter configuration. For the network of Fig. 3.18.1 :
- i. Determine  $I_{CQ}$  and  $V_{CEQ}$
  - ii. Find  $V_B$ ,  $V_C$ ,  $V_E$ ,  $V_{BC}$

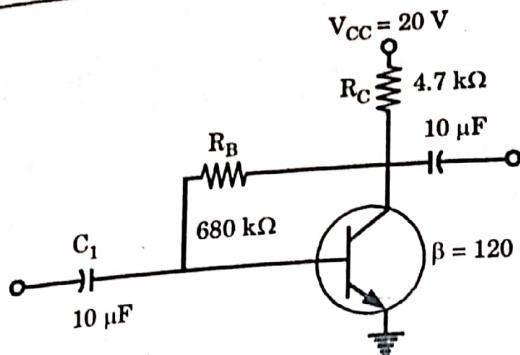


Fig. 3.18.1.

**Answer**

**Hybrid equivalent model of BJT in common emitter configuration :** Refer Q. 3.17, Page 3-23D, Unit-3.

**Numerical :**

Applying KVL

$$V_{CC} - R_C(I_C + I_B) - R_B I_B - V_{BE} = 0$$

$$20 - 4.7(\beta + 1)I_B - 680I_B - 0.7 = 0$$

$$19.3 - 4.7 \times 121I_B - 680I_B = 0$$

$$I_B = 0.0155 \text{ mA}$$

$$I_C = \beta I_B = 120 \times 0.0155 = 1.86 \text{ mA}$$

$$V_{BE} = V_B - V_E = 0.7 \text{ V}$$

$$V_{BE} = V_B - 0 = V_B$$

$$V_{BE} = V_B = 0.7 \text{ V}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 20 - 1.86 \times 10^{-3} \times 4.7 \times 10^3 = 11.258 \text{ V}$$

$$V_C = V_{CE} + V_E = 11.258 + 0 = 11.258 \text{ V}$$

$$V_{BC} = V_B - V_C = -10.558 \text{ V}$$

**Que 3.19.** Draw the hybrid equivalent circuit for common base configuration and write the expression for  $A_i$ ,  $R_i$ ,  $A_v$  and  $R_o$ .

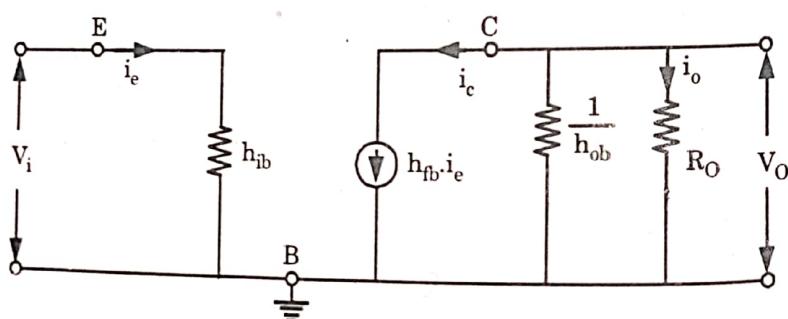
**Answer**

Fig. 3.19.1.CB amplifier equivalent circuit.

Since  $h_{\pi}$  is very small and  $1/h_{ob}$  is very large then reduced circuit will be

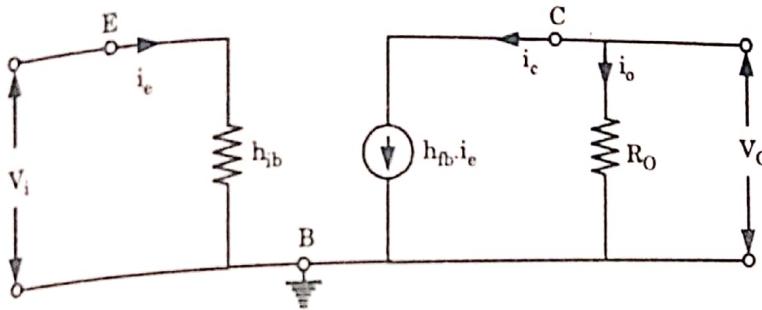


Fig. 3.19.2. Equivalent circuit for CB amplifier after assumptions.

Current gain ( $A_i$ ) :

$$A_i = \frac{i_c}{i_e} = -\frac{h_{fb} \cdot i_e}{i_e}$$

$$A_i = -h_{fb} = -\alpha$$

Voltage gain ( $A_v$ ) :

$$A_v = \frac{V_o}{V_i} = -\frac{i_o \cdot R_o}{i_e \cdot h_{ib}} = \frac{i_e h_{fb} \cdot R_o}{i_e h_{ib}}$$

$$A_v = \frac{h_{fb}}{h_{ib}} \cdot R_o$$

Input impedance ( $Z_{in}$  or  $R_i$ ) :

$$Z_{in} = \frac{\text{input voltage}}{\text{input current}} = \frac{V_i}{i_e} = \frac{i_e \cdot h_{ib}}{i_e} = h_{ib}$$

Output impedance ( $Z_o$  or  $R_o$ ) :

$$Z_o = \left. \frac{\text{output voltage}}{\text{output current}} \right|_{V_i=0} = \infty$$

**Que 3.20.** Write the expression for voltage gain, current gain, input resistance and output resistance of a common collector (CC) amplifier using  $h$ -parameters. Also write the characteristics and applications of CC amplifier.

**Answer**

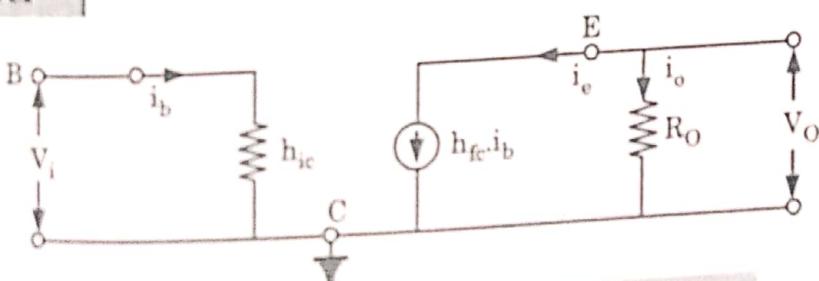


Fig. 3.20.1. Equivalent circuit for CC amplifier.

$$\begin{aligned} V_i &= i_b \cdot h_{ie} \\ i_o &= -i_e \end{aligned}$$

$$V_o = i_o R_o = -i_e R_o = -h_{fe} i_b R_o$$

**Current gain ( $A_I$ ) :**

$$A_I = \frac{\text{output current}}{\text{input current}} = \frac{h_{fe} \cdot i_b}{i_b}$$

$$A_I = h_{fe} = \gamma$$

**Voltage gain ( $A_V$ ) :**

$$A_V = \frac{V_o}{V_i} = -\frac{h_{fe} \cdot i_b \cdot R_o}{i_b \cdot h_{ic}} = -\frac{h_{fe} \cdot R_o}{h_{ic}}$$

**Input impedance ( $R_i$  or  $Z_{in}$ ) :**

$$Z_{in} = \frac{V_i}{i_b} = \frac{i_b \cdot h_{ic}}{i_b} = h_{ic}$$

with internal input resistance of source  $R_s$ .

$$Z_{in} = R_s + h_{ic}$$

**Output impedance ( $Z_o$  or  $R_o$ ) :**

$$Z_o = \frac{V_o}{i_e} = \infty$$

**Characteristics of CC amplifiers :**

- The current gain is high for low value of  $R_L$  ( $< 10 \text{ k}\Omega$ ).
- The voltage gain is less than unity.
- The input resistance is the highest of all the three configurations.
- The output resistance is the lowest of all the three configurations.

**Que 3.21.** Differentiate CB, CE and CC circuits.

**Answer**

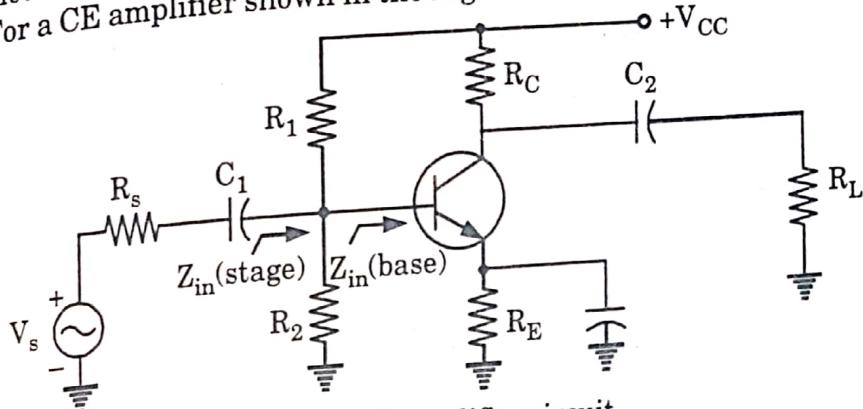
S.No.	Characteristics	CB	CE	CC
1.	Input resistance ( $R_i$ )	Very low ( $30 - 150 \Omega$ )	Low ( $1 \text{ k}\Omega$ to $2 \text{ k}\Omega$ )	High ( $20 - 500 \text{ k}\Omega$ )
2.	Output resistance ( $R_o$ )	High ( $\approx 500 \text{ k}\Omega$ )	Large (nearly equal to $50 \text{ k}\Omega$ )	Low ( $50 - 1000 \Omega$ )
3.	Current gain	$\alpha < 1$	$\beta \rightarrow \text{high}$	Higher $= (1 + \beta)$
4.	Voltage gain ( $A_V$ )	High ( $\approx 1500$ )	High ( $\approx 1500$ )	Less than 1
5.	Power gain ( $A_p$ )	High ( $\approx 7500$ )	High ( $\approx 10,000$ )	Low ( $250 - 500$ )
6.	Phase between input and output	Same ( $0^\circ$ phase difference)	Reversed ( $180^\circ$ phase shift)	same
7.	Applications	At high frequencies	At audio frequencies	Impedance matching

**Que 3.22.** Explain how the input impedance of an amplifier can load down the AC source.

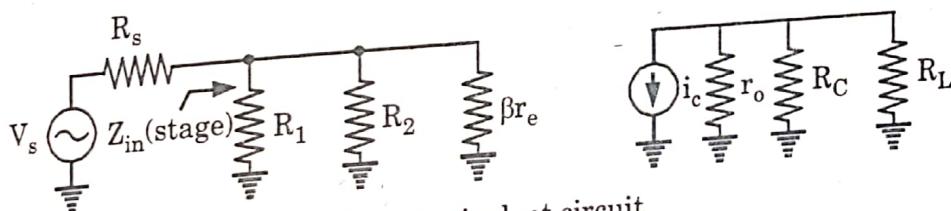
**AKTU 2015-16(Sem-II), Marks 05**

**Answer**

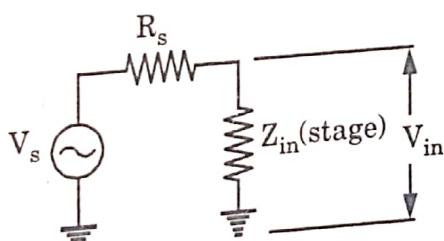
1. In practice, the voltage source has finite internal resistance. If we consider this internal resistance in the AC analysis of the amplifier we can realize that the input impedance of an amplifier can load down the AC source, that is, reduce the AC voltage appearing across the emitter diode.
2. For a CE amplifier shown in the Fig. 3.22.1.



(a) CE amplifier circuit.



(b) AC equivalent circuit.



(c) Effect of input impedance.

Fig. 3.22.1.

$$Z_{in(base)} = \beta r_e$$

$$Z_{in(stage)} = R_1 || R_2 || \beta r_e$$

and

3. The AC source has to drive the input impedance of the stage  $Z_{in(stage)}$ .
4. This input impedance includes the effects of the biasing resistors  $R_1$  and  $R_2$ , in parallel with the input impedance of the base  $Z_{in(base)}$ .

**Que 3.23.** For the voltage divider configuration of Fig. 3.23.1, determine  $r_e$ ,  $A_v$ ,  $Z_{in}$  and  $Z_o$ .

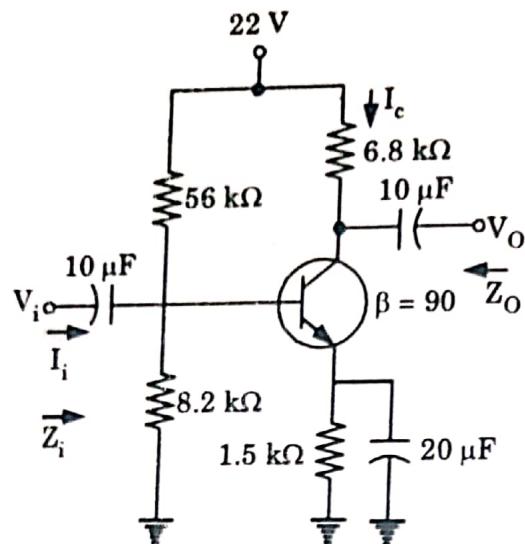


Fig. 3.23.1.

AKTU 2015-16(Sem-II), Marks 10

**Answer**

1. Using approximate approach,

$$V_B = \frac{8.2 \times 10^3 \times 22}{(56 + 8.2) \times 10^3} = 2.81 \text{ V}$$

2.

$$V_E = V_B - V_{BE} = 2.81 - 0.7 \\ = 2.11 \text{ V}$$

3.

$$I_E = \frac{V_E}{R_E} = \frac{2.11}{1.5 \times 10^3} = 1.41 \text{ mA}$$

4.

$$r_e = \frac{V_T}{I_E} = \frac{26 \times 10^{-3}}{1.41 \times 10^{-3}} = 18.44 \Omega$$

5.

$$R' = (56 \text{ k}\Omega) \parallel (8.2 \text{ k}\Omega)$$

6.

$$= \frac{56 \times 8.2 \times 10^3}{(56 + 8.2)} = 7.15 \text{ k}\Omega$$

$$Z_{in} = R' \parallel \beta r_e = (7.15 \text{ k}\Omega) \parallel (90)(18.44 \Omega) \\ = 7.15 \text{ k}\Omega \parallel 1.659 \text{ k}\Omega$$

$$= \frac{7.15 \times 1.659 \times 10^3}{(7.15 + 1.66)} = 1.35 \text{ k}\Omega$$

7.

$$A_v = -\frac{R_C}{r_e} = -\frac{6.8 \times 10^3}{18.44} = -368.76$$

8.

$$Z_O = R_C = 6.8 \text{ k}\Omega$$

**Que 3.24.** For the common emitter or fixed bias configuration in Fig. 3.24.1, determine  $r_e$ ,  $Z_i$ ,  $Z_O$ ,  $A_v$ .

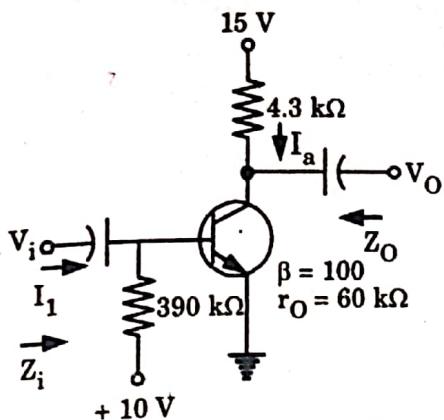


Fig. 3.24.1.

AKTU 2014-15(Sem-II), Marks 05

**Answer**

1. Given,

$$\beta = 100, r_O = 60\text{ k}\Omega$$

$$R_B = 390\text{ k}\Omega, R_C = 4.3\text{ k}\Omega$$

2. DC circuit will be as shown in Fig. 3.24.2

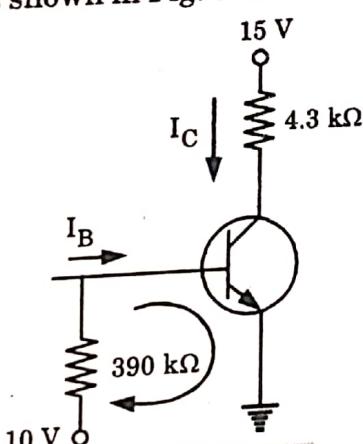


Fig. 3.24.2.

3. Applying KVL in inner loop,

$$10 - 390 \times 10^3 I_B - V_{BE} = 0$$

...(3.24.1)

4. From eq. (3.24.1),  $I_B = 0.024\text{ mA} = 24\text{ }\mu\text{A}$ 

$$I_E = (\beta + 1) I_B = 2.424\text{ mA}$$

$$r_e = \frac{V_T}{I_E} = \frac{26\text{ mV}}{2.424\text{ mA}} = 10.72\text{ }\Omega$$

$$Z_i = R_B \parallel \beta r_e = 390\text{ k}\Omega \parallel 1.072\text{ k}\Omega = 1.069\text{ k}\Omega$$

$$Z_O = r_O \parallel R_C = 60\text{ k}\Omega \parallel 4.3\text{ k}\Omega = 4.012\text{ k}\Omega$$

$$A_v = - \frac{r_O \parallel R_C}{r_e} = - \frac{4.012\text{ k}\Omega}{10.72\text{ }\Omega} = - 374.3$$

**Que 3.25.** Calculate  $I_B$ ,  $I_C$  and  $V_{CE}$  for the given network as shown in Fig. 3.25.1.

## 3-32 D (ESC-Sem-3 &amp; 4)

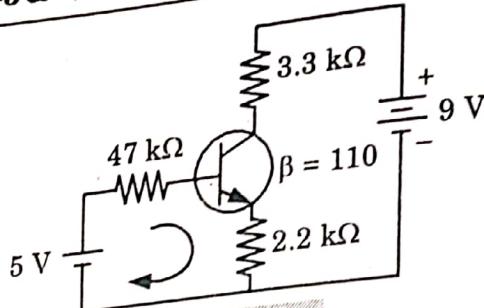


Fig. 3.25.1.

AKTU 2013-14(Sem-II), Marks 05

**Answer**

Applying KVL in input circuit,

$$5 - I_B R_B - 0.7 - I_E R_E = 0$$

$$5 - I_B \times 47 \times 10^3 - 0.7 - I_E \times 2.2 \times 10^3 = 0$$

We know,  $I_E = (\beta + 1) I_B$   
 $= (110 + 1) I_B = 111 I_B$

$$I_B = \frac{5 - 0.7}{[47 + 111 \times 2.2]} = 14.76 \mu\text{A}$$

$$I_C = 110 \times 14.76 \mu\text{A} = 1.62 \text{ mA}$$

$$I_E = I_C + I_B = 1.63 \text{ mA}$$

$$V_{CE} = 9 - (3.3 \times 1.62) - (2.2 \times 1.63) = 0.068 \text{ V}$$

**Que 3.26.** In the circuit shown in Fig. 3.26.1 if  $I_C = 2 \text{ mA}$  and  $V_{CE} = 3 \text{ V}$ , calculate  $R_1$  and  $R_C$ .

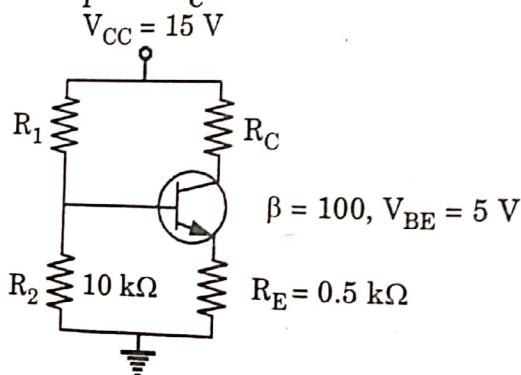


Fig. 3.26.1.

AKTU 2013-14(Sem-II), Marks 05

**Answer**

1. Given :

$$I_C = 2 \text{ mA}, V_{CE} = 3 \text{ V}, \beta = 100, V_{BE} = 5 \text{ V}$$

$$R_2 = 10 \text{ k}\Omega, R_E = 0.5 \text{ k}\Omega$$

$$R_1 \text{ or } R_C = \frac{\text{Voltage across } R_1 \text{ or } R_C}{\text{Current through } R_1 \text{ or } R_C}$$

2.

For  $R_1$ :

$$I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{100} = 0.02 \text{ mA}$$

1.

$$\text{Voltage across } R_2 \text{ or } V_{R2} = V_{BE} + V_E$$

$$= 5 + (2 \text{ mA} \times 0.5 \text{ k}\Omega) = 6 \text{ V}$$

$$3. \text{ Voltage across } R_1 = V_{CC} - V_2 = 15 - 6 = 9 \text{ V}$$

$$4. \text{ Current across } R_1 \text{ and } R_2, I_1 = \frac{V_2}{R_2} = \frac{6}{10 \text{ k}} = 0.6 \text{ mA}$$

$$5. \therefore \text{Resistance, } R_1 = \frac{\text{Voltage across } R_1}{I_1} = \frac{9 \text{ V}}{0.6 \text{ mA}} = 15 \text{ k}\Omega$$

For  $R_C$ :

$$1. \text{ Voltage across, } R_C = V_{CC} - V_{CE} - V_E$$

$$= 15 - 3 - (0.5 \times 2) = 11 \text{ V}$$

$$2. \text{ Collector resistance, } R_C = \frac{\text{Voltage across } R_C}{I_C} = \frac{11 \text{ V}}{2 \text{ mA}} = 5.5 \text{ k}\Omega$$

**Que 3.27.** Given that  $I_{CQ} = 2 \text{ mA}$  and  $V_{CEQ} = 10 \text{ V}$ , determine  $R_1$  and  $R_C$  for the network of Fig. 3.27.1.

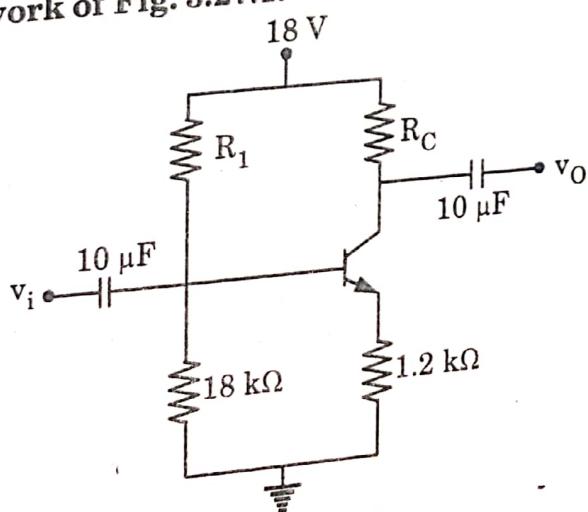


Fig. 3.27.1.

AKTU 2016-17(Sem-II), Marks 07

**Answer**

1. The procedure is same as Q. 3.26, Page 3-32D, Unit-3.

[Ans :  $R_1 = 86.5 \text{ k}\Omega$ ,  $R_C = 2.8 \text{ k}\Omega$ ]

**Que 3.28.** A BJT common emitter amplifier has a potential divider bias using  $V_{CC} = 12 \text{ V}$ ,  $R_C = 4 \text{ k}\Omega$ ,  $R_1 = 20 \text{ k}\Omega$ ,  $R_2 = 5 \text{ k}\Omega$ ,  $V_{BE} = 0.6 \text{ V}$  and  $\beta = 100$ . Determine the operating point.

AKTU 2013-14 (Sem-I), Marks 05

**Answer**

1. Given,

$$V_{CC} = 12 \text{ V}, R_C = 4 \text{ k}\Omega, V_{BE} = 0.6 \text{ V}$$

$$R_1 = 20 \text{ k}\Omega, R_2 = 5 \text{ k}\Omega$$

$$\beta = 100, R_E = 1 \text{ k}\Omega \text{ (Assume).}$$

2. Thevenin's voltage,

$$V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 12}{20 + 5} = 2.4 \text{ V}$$

3. Thevenin's resistance,  $R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{20 \times 5}{20 + 5} = 4 \text{ k}\Omega$

4. Thevenin's equivalent circuit of self bias circuit is shown in Fig. 3.28.1

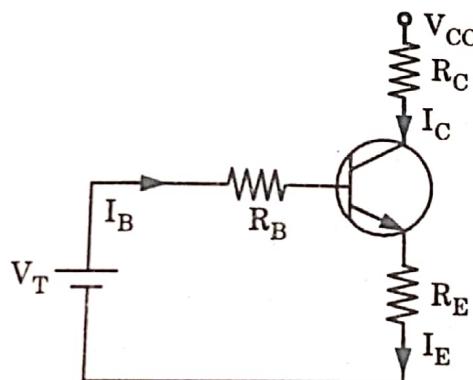


Fig. 3.28.1.

5. Applying loop equation in base circuit,

$$V_T - V_{BE} = I_B R_B + (I_B + I_C) R_E$$

$$2.4 - 0.6 = \frac{I_c}{100} \times 4 \times 10^3 + I_c \left( \frac{1}{100} + 1 \right) \times 1 \times 10^3$$

$$1.8 = 40 I_c + \frac{101}{100} \times 10^3 \times I_c$$

$$1.8 = 1050 I_c$$

$$I_c = 1.71 \text{ mA}$$

6. Since  $I_B$  is very small,  $I_C \approx I_E \approx 1.71 \text{ mA}$ .

7. Applying KVL at output,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \\ = 12 - 1.71 \times 10^{-3} (4 + 1) \times 10^3 = 3.45 \text{ V}$$

**Que 3.29.** Draw a BJT fixed bias circuit as collector bias circuit with  $V_{CC} = 9$  V,  $R_C = 500 \Omega$ ,  $V_{BE} = 0.7$  V and  $\beta = 116$ . Determine the value resistance  $R_B$  in collector fixed circuit.

**AKTU 2013-14(Sem-I), Marks 05**

**Answer**

1. Given,

$$V_{CC} = 9 \text{ V}, R_C = 500 \Omega, V_{BE} = 0.7 \text{ V}$$

$$\beta = 116, V_{CE} = 5 \text{ V}$$

2. Applying KVL at input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\frac{V_{CC} - V_{BE}}{I_B} = R_B$$

$$\frac{9 - 0.7}{I_C / \beta} = R_B$$

$$R_B = \frac{116 \times 8.3}{I_C} = \frac{962.8}{I_C} \quad \dots(3.29.1)$$

3. Applying KVL at output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\frac{9 - 5}{500} = I_C$$

$$I_C = 8 \text{ mA}$$

4. Substitute value of  $I_C$  in eq. (3.29.1), we get

$$R_B = \frac{962.8}{8 \times 10^{-3}} = 120.3 \text{ k}\Omega$$

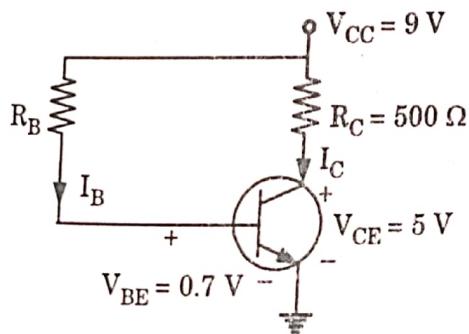


Fig. 3.29.1.

**Que 3.30.** For the circuit shown in Fig. 3.30.1, determine  $V_B$ ,  $I_C$ ,  $V_C$ . Given that  $\beta = 80$ ,  $V_{BE} = 0.7$  V.

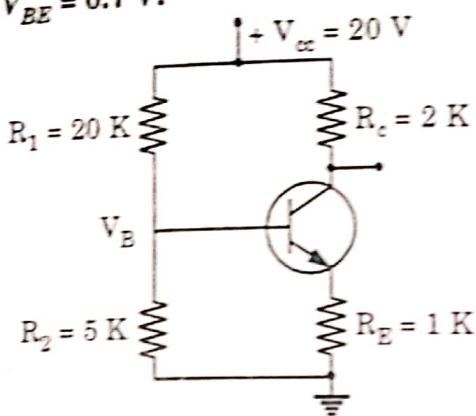


Fig. 3.30.1.

AKTU 2016-17(Sem-I), Marks 7.5

**Answer**

$$R_{th} = R_1 \parallel R_2 = \frac{20 \times 5}{20 + 5} = 4 \text{ K}$$

$$V_{th} = V_B = \frac{20 \times 5}{20 + 5} = 4 \text{ V}$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1 + \beta)R_E} = \frac{4 - 0.7}{4 + 81} = 0.0388 \text{ mA.}$$

$$I_c = \beta I_B = 80 \times 0.0388 = 3.11 \text{ mA}$$

$$V_c = V_{cc} - I_c R_c = 20 - (3.11 \times 2) = 13.8 \text{ V}$$

**PART-7**

*Field Effect Transistor : Construction and Characteristics of JFETs.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 3.31.** Describe the V-I characteristic of JFET with different operating regions in detail.

AKTU 2014-15(Sem-I), Marks 10

OR

Draw the structure of JFET and explain its principle of operation with neat diagram along with its transfer and V-I characteristics. Define pinch-off voltage and mark it on the characteristic.

**AKTU 2013-14(Sem-II), Marks 05**

OR

Explain the transconductance curve of a JFET.

**AKTU 2015-16(Sem-II), Marks 05**

OR

Draw the circuit and explain the drain characteristic for N-channel JFET.

**AKTU 2016-17(Sem-I), Marks 05**

OR

Draw and explain the n-channel JFET and draw its transfer characteristics.

**AKTU 2016-17(Sem-II), Marks 5.25**

OR

Explain the formation of depletion region in JFET.

**AKTU 2016-17(Sem-I), Marks 7.5**

OR

Explain the construction and working of N-channel JFET. Draw the drain characteristics and transfer curve.

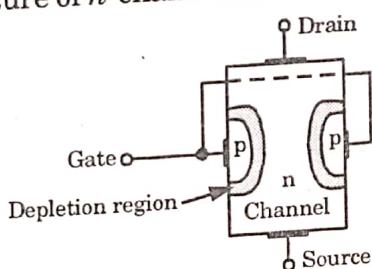
**AKTU 2017-18(Sem-I), Marks 3.5**

### Answer

JFET (Junction Field Effect Transistor) :

Basic construction :

1. The structure of n-channel field effect transistor is shown in Fig. 3.31.1.



**Fig. 3.31.1. Junction field-effect transistor (JFET).**

2. For the fabrication of n-channel JFET, a narrow bar of n-type semiconductor material is taken. Now on opposite sides of its middle part, two heavily doped p-type regions are formed by diffusion as shown in Fig. 3.31.1.
3. The junctions form two p-n diodes or gates.
4. The area between the gates is called a channel.

5. Actually the two *p*-regions are internally connected and a single lead is taken out, which is called as gate junction.
6. Ohmic contacts are made at the two ends of *n*-type semiconductor bar.
7. One lead is called as source terminal *S* and the other as drain terminal *D*.
8. When a potential difference is established between source and drain, a current flows from one end to the other end in *n*-type material which forms a sort of channel. This current consists of majority carriers which in this case are electrons.

**Operation of *n*-channel FET :**

1. The operation of *n*-channel FET can be understood with the help of Fig. 3.31.2.
2. First suppose that the gate has been reversed biased by gate battery  $V_{GG}$  and drain battery is not connected. So that space charge region or depletion region on either side of a reverse biased *p-n* junction are formed.
3. Further consider effect of drain battery  $V_{DD}$  while  $V_{GG}$  is removed.
4. The voltage  $V_{DD}$  is dropped across the *n*-channel resistance (say  $R_{DS}$ ) giving rise to a drain current.

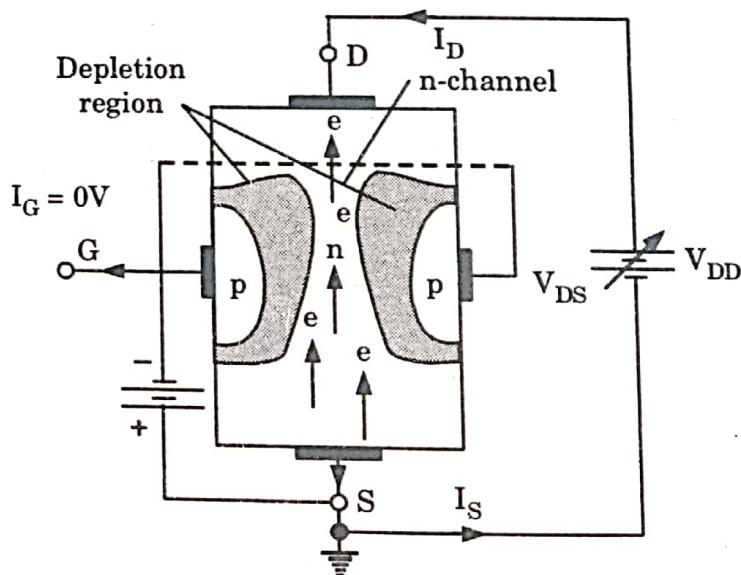


Fig. 3.31.2. Operation of FET.

5. Consider two points *A* and *B* in *n*-channel as shown in Fig. 3.31.3.
6. Let  $V_A$  and  $V_B$  be potential drop at these points. Certainly  $V_A > V_B$ , so due to progressive voltage drop, the reverse biasing effect is stronger near drain.

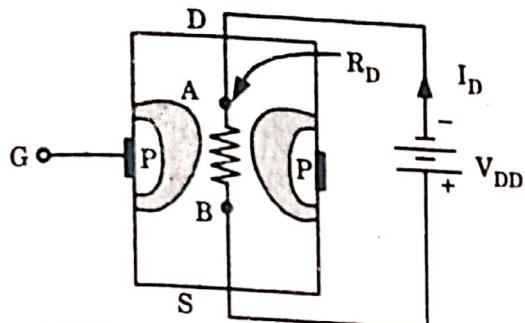
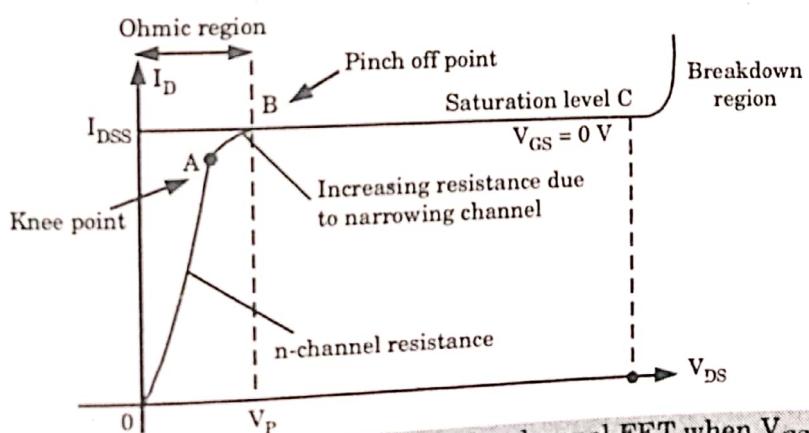


Fig. 3.31.3. Voltage drop across channel.

7. This explains why the depletion regions extend farther into the channel at point A than at point B.
8. This gate bias increases the depletion regions and thereby decreases the cross-section of  $n$ -channel due to which  $I_D$  decreases. Since negative gate voltage controls the drain current, FET is called a voltage controlled device.

#### Static Characteristics of FET (V-I) :

1. Static means  $I_D$  versus  $V_{DS}$  for different values of  $V_{GS}$ .
2. Let us consider the characteristics for  $V_{GS} = 0$ , the curve is shown in Fig. 3.31.4.
3. When  $V_{DS} = 0$ , there is no attracting potential at the drain and hence drain current  $I_D = 0$ , although the channel between the gates is fully open as  $V_{GS} = 0$ .
4. As  $V_{DS}$  is increased, the electrons flow from source to drain through channel between depletion layers and the drain current  $I_D$  increases linearly upto a point A (knee point).

Fig. 3.31.4. Drain characteristics of  $n$ -channel FET when  $V_{GS} = 0$ .

5. With the increase of  $I_D$ , the ohmic resistance drop in the material of semiconductor bar. So as the voltage  $V_{DS}$  is progressively increased, the drain current  $I_D$  from point A, increases at reverse square law rate upto point B which is called pinch-off point. The corresponding voltage is called pinch-off voltage and is denoted by  $V_P$ .

6. As  $V_{DS}$  is further increased, the channel resistance also increases in such a way, that  $I_D$  remains constant upto point C. The region BC is known as saturation region or amplifier region.

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

where  $I_{DSS}$  = drain current when gate is shorted to source.

$V_{GS}$  = voltage between gate and source.

7. With continued increase of  $V_{DS}$  corresponding to point C (called avalanche breakdown voltage  $V_A$ ), eventually breakdown across the gate junction takes place and current  $I_D$  shoots to a high value.

#### Transfer characteristics :

1. The transfer characteristics is a plot of drain current  $I_D$ , versus voltage between gate and source  $V_{GS}$  for a constant value of voltage between drain and source  $V_{DS}$ . This is shown in Fig. 3.31.5.
2. When  $V_{GS} = 0$ ,  $I_D = I_{DSS}$
3. When  $I_D = 0$ ,  $V_{GS} = V_P$
4. The transfer characteristic follows the equation

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS}(\text{off})} \right)^2$$

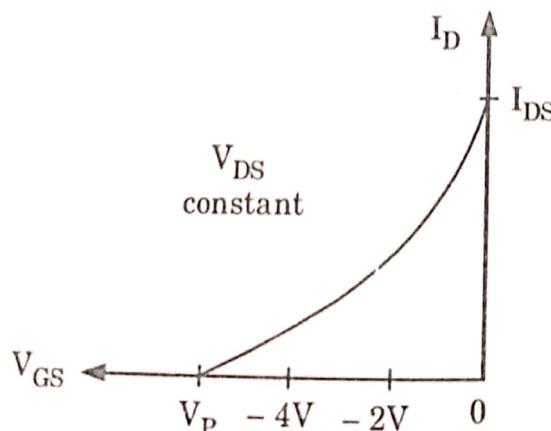


Fig. 3.31.5. Transfer characteristics.

#### Working of p-channel JFET :

1. The p-channel JFET is constructed in exactly same manner as the n-channel device but with a reversal of the p-and n-type material as shown in Fig. 3.31.6.

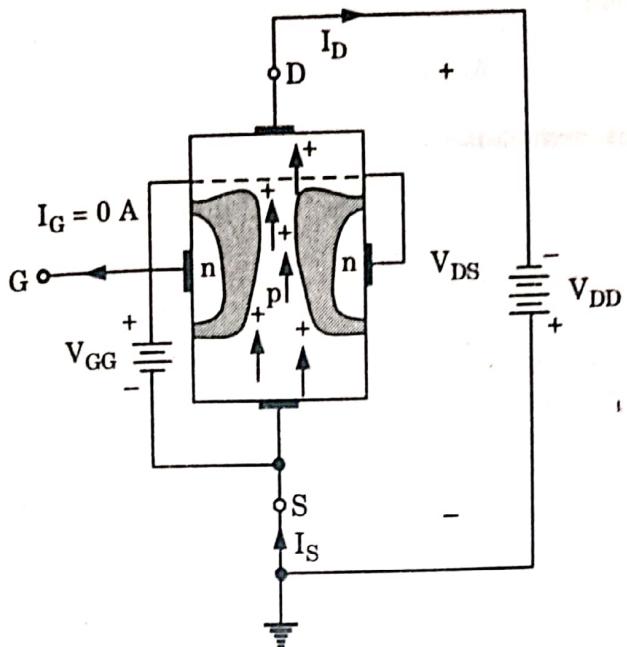


Fig. 3.31.6. p-channel JFET.

2. The defined current directions are reversed.
3. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and negative voltages from drain to source. It means source is at higher potential than the drain.

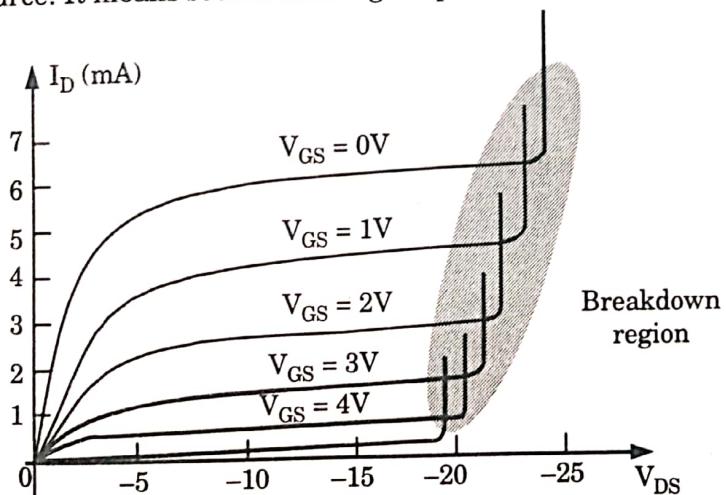


Fig. 3.31.7. p-Channel JFET characteristics  
with  $I_{DSS} = 6 \text{ mA}$  and  $V_P = +6 \text{ V}$ .

**Que 3.32.** Discuss the various FET parameters with respect to common source configuration.

**Answer**

- i. **DC drain resistance  $R_{DS}$ :** This is the static or ohmic resistance of the channel.

It is given by :

$$R_{DS} = \left[ \frac{V_{DS}}{I_D} \right]$$

ii. AC drain resistance :

$$r_d = \left[ \frac{\Delta V_{DS}}{\Delta I_D} \right] \quad V_{GS} \text{ held constant}$$

This is evaluated at  $V_{GS} = 0$  i.e., when FET is operating in the pinch off region.

iii. Transconductance : The control that the gate voltage has over drain current is measured by forward transconductance  $g_{fs}$ , and is similar to mutual conductance  $g_m$ . It is simply the slope of transfer characteristics.

$$g_{fs} = \left( \frac{\Delta I_D}{\Delta V_{GS}} \right) \quad V_{DS} \text{ held constant}$$

The unit of  $g_{fs}$  is siemens (mho).

iv. Amplification factor : The amplification factor  $\mu$  is defined as

$$\mu = \left( \frac{\Delta V_{DS}}{\Delta V_{GS}} \right) \quad I_D \text{ held constant}$$

**Que 3.33.** Explain with the help of necessary diagrams, how FET can be used as (Voltage Controlled Resistor) VVR.

**AKTU 2014-15(Sem-II), Marks 05**

**Answer**

1. In most of the linear applications, JFET is operated in constant current portion of its output characteristics i.e., in saturation region.
2. FET can also be used in the region before pinch-off where  $V_{DD}$  is small.
3. FET when used in region before pinch-off, it works as variable resistance device i.e., the channel resistance is controlled by the gate bias voltage ( $V_{GS}$ ).
4. In such applications, the FET is referred as voltage variable resistor (VVR) or voltage dependent resistor (VDR).
5. The VVR can be used to vary the voltage gain of a multistage amplifier. This action is referred as automatic gain control (AGC).
6. If the signal is low then voltage gain of the stages can be increased and when becomes high, the gain can be reduced automatically. In this way, the general level of amplification is maintained fairly constant.
7. The circuit arrangement of AGC amplifier using the FET as voltage variable resistor is shown in Fig. 3.33.1.
8. The input signal  $V_i$  is amplified by amplifier.

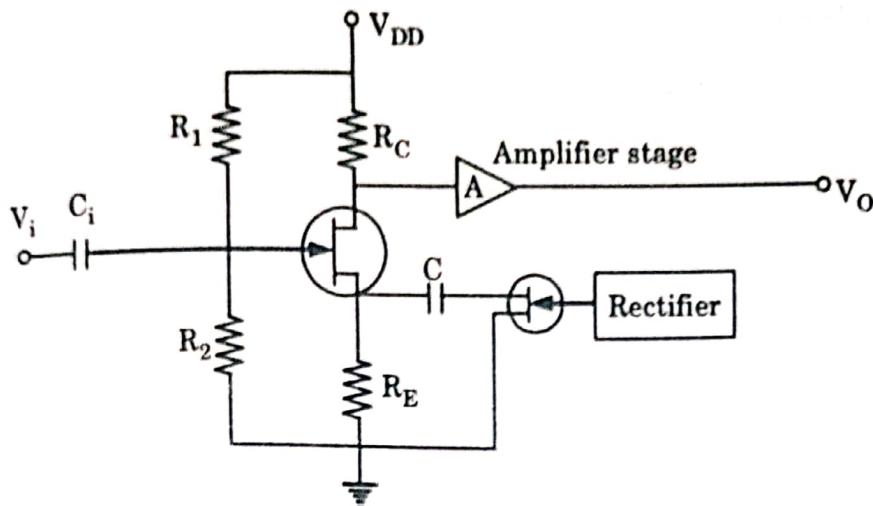


Fig. 3.33.1. FET as VVR.

9. It is then rectified and filtered to produce DC voltage proportional to output signal level. This voltage is applied to the gate of the FET so that the AC resistance between drain and source changes.
10. Capacitor 'C' isolates the transistor from FET so that the bias conditions of transistor are not affected.
11. Thus, when output increases,  $V_{GS}$  also increases and  $R_{DS}$  changes so that the gain of the transistor decreases. Thus automatically the gain is controlled.

**Que 3.34.** Show that the transconductance  $g_m$  of JFET is related to drain current  $I_{DS}$  by

$$g_m = \frac{2}{V_p} \sqrt{I_{DSS} I_{DS}}$$

**Answer**

1. As we know, the saturation drain current,  $I_{DS}$  is given by

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2 \quad \dots(3.34.1)$$

where  $V_p$  is pinch-off voltage and  $I_{DSS}$  is the value of  $I_{DS}$  when  $V_{GS} = 0$ .

2. Differentiating eq. (3.34.1) with respect to  $V_{GS}$ , we get

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2 \left( 1 - \frac{V_{GS}}{V_p} \right) \left( -\frac{1}{V_p} \right)$$

3. We know that,  $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ ,  $V_{DS}$  is constant

$$\therefore g_m = -\frac{2I_{DSS}}{V_p} \left( 1 - \frac{V_{GS}}{V_p} \right) \quad \dots(3.34.2)$$

4. From eq. (3.34.1), we have

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

5. Substituting this value in eq. (3.34.2), we get

$$g_m = \frac{-2 I_{DSS}}{V_P} \sqrt{\frac{I_{DS}}{I_{DSS}}} \\ g_m = \frac{-2}{V_P} \sqrt{\frac{(I_{DSS})^2 I_{DS}}{I_{DSS}}} = \frac{2}{|V_P|} \sqrt{I_{DSS} I_{DS}}$$

[ $\because V_P$  may be positive or negative]

**Que 3.35.** Draw and solve the self bias configuration of JFET.

OR

- Draw the schematic diagram of self-biasing JFFT amplifier.
- Explain the CMOS inverter circuit working operation.

AKTU 2015-16(Sem-II), Marks 10

### Answer

#### CMOS Inverter :

- An inverter is a logic element that "inverts" the applied signal.
- That is, if the logic level of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level 5 V, and vice versa.
- In Fig. 3.35.1, both gates are connected to the applied signal and both drain to the output  $V_O$ .
- The source of the  $p$ -channel MOSFET ( $Q_2$ ) is connected directly to the applied voltage  $V_{SS}$ , whereas the source of the  $n$ -channel MOSFET ( $Q_1$ ) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output.
- With 5 V at  $V_i$  (with respect to ground),  $V_{GS1} = V_i$ , and  $Q_1$  is ON, resulting in a relatively low resistance between drain and source as shown in Fig. 3.35.1.
- Since  $V_i$  and  $V_{SS}$  are at 5 V,  $V_{GS2} = 0$  V, which is less than the required  $V_T$  for the device, resulting in an OFF state.
- The resulting resistance level between drain and source is quite high for  $Q_2$ , as shown in Fig. 3.35.1.
- A simple application of the voltage-divider rule will reveal that  $V_O$  is very close to 0 V, or the 0-state, establishing the desired inversion process.
- For an applied voltage  $V_i$  of 0 V (0-state),  $V_{GS1} = 0$  V, and  $Q_1$  will be OFF with  $V_{SS2} = -5$  V, turning on the  $p$ -channel MOSFET.

10. The result is that  $Q_2$  will present a small resistance level,  $Q_1$  a high resistance, and  $V_O = V_{SS} = 5\text{ V}$  (the 1-state).
11. Since the drain current that flows for either case is limited by the OFF transistor to the leakage value, the power dissipated by the device in either state is very low.

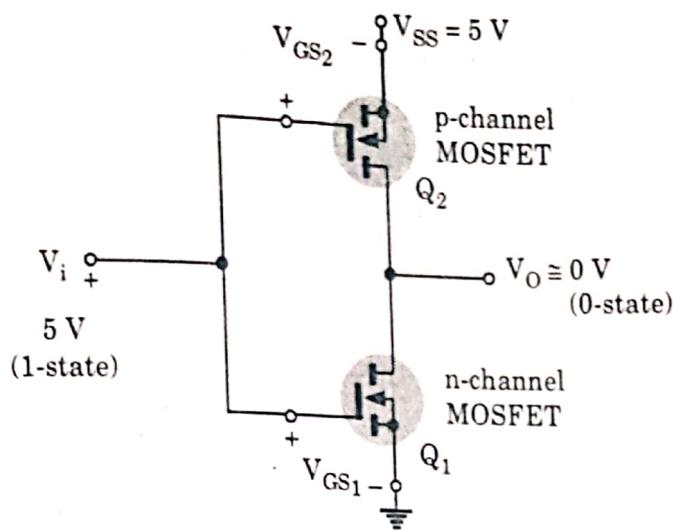


Fig. 3.35.1. CMOS inverter.

#### Self bias configuration :

1. The self bias configuration eliminates the need of two DC supplies i.e., only drain supply is used and no gate supply is connected.
2. Fig. 3.35.2 shows the arrangement, a resistor  $R_s$  is connected in the source leg of the configuration. This is known as bias resistor.
3. The DC component of drain current  $I_D$  flowing through  $R_s$  makes a voltage drop across resistor  $R_s$ .
4. The capacitor  $C_s$  bypasses the AC component of drain current.

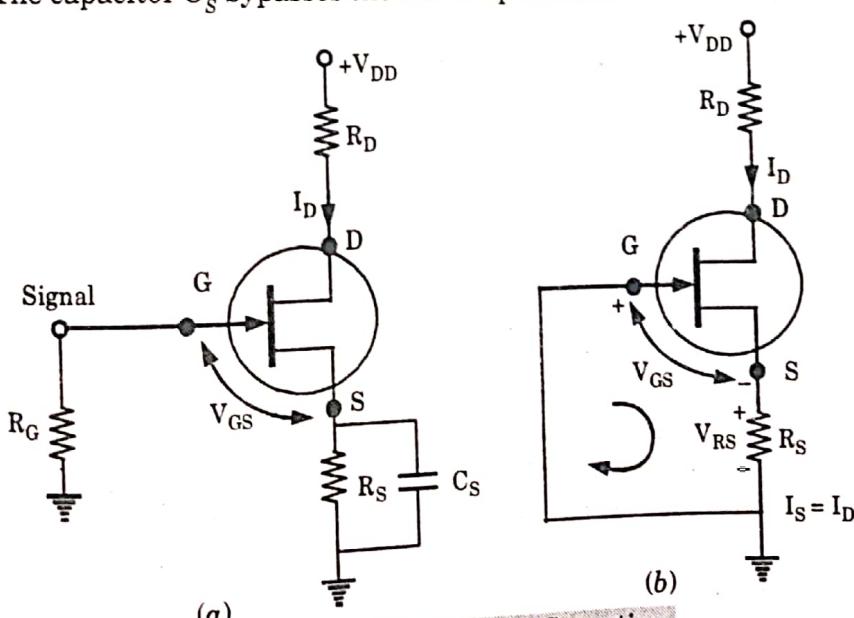


Fig. 3.35.2. Self bias configuration.

5. The addition of  $R_G$  in circuit does not upset the DC bias, but avoid the short-circuiting of the AC input voltage. Otherwise, the leakage current would build up static charge at the gate which could change the bias.
6.  $R_S$  also help to prevent any variation in FET drain current.
7. Let there be an increase in the drain current. This will increase the voltage drop across resistor  $R_S$  and this results in decrease of channel width. So, the drain current is reduced.
8. For DC analysis, the capacitors can be replaced by open circuit and the resistor  $R_G$  replaced by short-circuit equivalent. Since  $I_G = 0$  A. The equivalent circuit is shown in Fig. 3.35.2(b).
9. For the indicated loop, we have

$$\begin{aligned} -V_{GS} - V_{RS} &= 0 \\ V_{GS} &= -V_{RS} \\ V_{GS} &= -I_D R_S \end{aligned}$$

10. The gate is kept at this much negative potential with respect to ground.

but  $I_O = I_S$

and  $V_{DS} = V_{DD} - I_D (R_S + R_D)$

In addition  $V_S = I_D R_S, V_G = 0$  V

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

## PART-B

### AC Analysis of CS Amplifier.

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

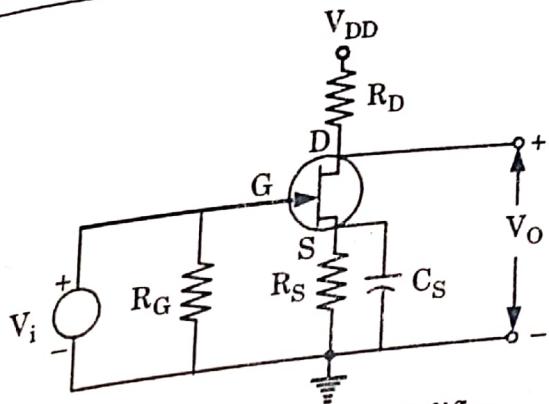
**Que 3.36.** Draw common source (CS) amplifier and find expressions for voltage gain, input impedance and output impedance.

#### Answer

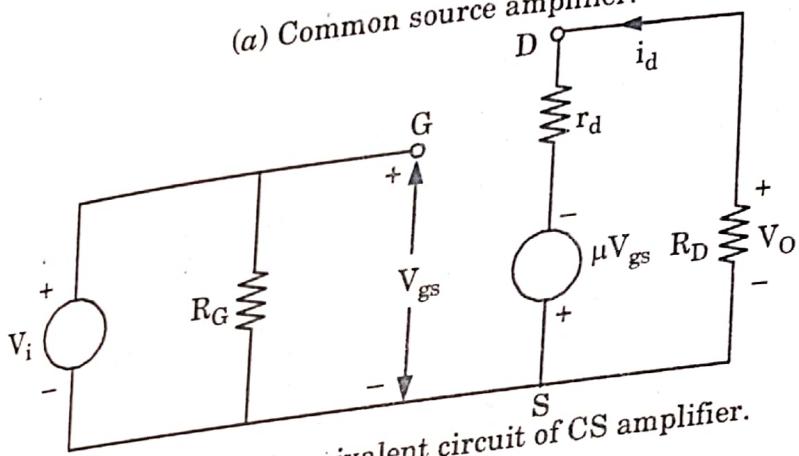
The circuit diagram for common-source amplifier is shown in Fig. 3.36.1(a) and its associated small signal equivalent circuit using the voltage-source model of FET is shown in Fig. 3.36.1(b).

#### Voltage gain $A_v$ :

1. In this amplifier,  $R_S$  is used to set the Q-point but is bypassed by  $C_S$  for mid frequency operation.



(a) Common source amplifier.



(b) Small signal equivalent circuit of CS amplifier.

Fig. 3.36.1.

2. From small signal equivalent circuit, the output voltage

$$V_O = \frac{-R_D}{R_D + r_d} (\mu V_{gs})$$

where  $V_{gs} = V_i$ , input voltage.

3. Hence, voltage gain,

$$A_V = \frac{V_O}{V_i} = \frac{-\mu R_D}{R_D + r_d}$$

Here, minus sign indicates a  $180^\circ$  phase shift between  $V_i$  and  $V_O$ .

#### Input impedance :

1. From Fig. 3.36.1(b) the input impedance is

$$Z_i = R_G$$

2. For voltage divider bias circuit of JFET,

$$R_G = R_1 \parallel R_2$$

#### Output impedance :

1. Output impedance is the impedance measured at output terminals with  $V_i = 0$ .

2. In Fig. 3.36.1(b), if  $V_i = 0$ ;  $V_{gs} = 0$ .

then

$$\mu V_{gs} = 0$$

## 3-48 D (ESC-Sem-3 &amp; 4)

3. Now, output impedance is given by

$$Z_O = r_d \parallel R_D$$

4. Normally,

$$r_d \gg R_D$$

∴

$$Z_O \approx R_D$$

**Que 3.37.** Explain the CS and CD configuration of JFET amplifiers.

**Answer**

**CS amplifier :** Refer Q. 3.36, Page 3-46D, Unit-3.

**CD Amplifier :** The circuit diagram of common drain amplifier is shown in Fig. 3.37.1(a) and its associated small signal equivalent circuit using the voltage-source model of FET is shown in Fig. 3.37.1(b).

**Voltage gain  $A_V$ :**

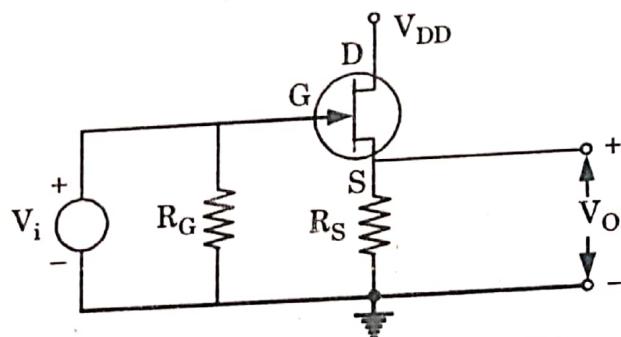
1. Since voltage  $V_{gd}$  is more easily determined than  $V_{gs}$ , the voltage source in the output circuit is expressed in terms of  $V_{gd}$  using Thevenin's theorem.
2. The output voltage

$$V_O = \frac{R_S}{R_S + \frac{r_d}{\mu + 1}} \times \frac{\mu}{\mu + 1} V_{gd} = \frac{\mu R_S V_{gd}}{(\mu + 1)R_S + r_d}$$

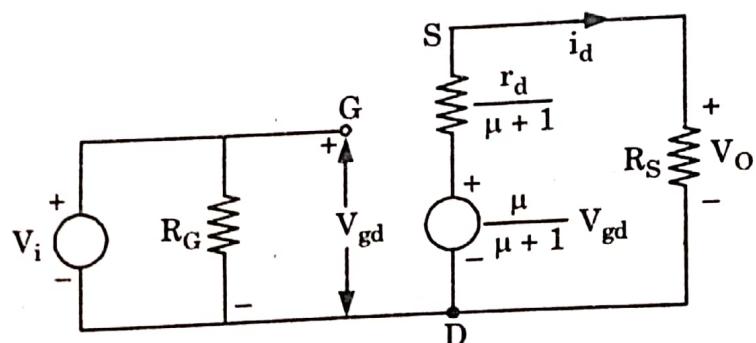
where  $V_{gd} = V_i$ , input voltage.

3. Hence voltage gain,

$$A_V = \frac{V_O}{V_i} = \frac{\mu R_S}{(\mu + 1)R_S + r_d}$$



(a) Common drain amplifier.



(b) Small signal equivalent circuit of CD amplifier.

Fig. 3.37.1.

**Input impedance  $Z_i$ :** It is clear from Fig. 3.37.1(b),  
 $Z_i = R_G$

For potential-divider bias circuit,  
 $R_G = R_1 \parallel R_2$

**Output impedance  $Z_o$ :**

- The output impedance is measured at the output terminal when  $V_i = 0$ .  
 As  $V_i = 0, V_{gd} = 0$

$$\therefore \frac{\mu}{\mu+1} V_{gd} = 0$$

- Output impedance,

$$Z_o = \frac{r_d}{\mu+1} \parallel R_s$$

When  $\mu \gg 1$        $Z_o \approx \frac{r_d}{\mu} \parallel R_s$

As  $\mu = g_m r_d$

$$\therefore Z_o \approx \frac{1}{g_m} \parallel R_s$$

### PART-9

*MOSFET (Depletion and Enhancement) Type, Transfer Characteristic.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 3.38.** Explain the construction and working of *n*-channel depletion type MOSFETs. AKTU 2014-15(Sem-II), Marks 05

OR

Draw the circuit of *n*-channel depletion type MOSFET and explain its operation. Also draw its drain and transfer characteristics. AKTU 2017-18(Sem-II), Marks 07

Describe the construction and basic connection of depletion MOSFET. AKTU 2016-17(Sem-I), Marks 05

OR

Explain construction and working of depletion MOSFET. AKTU 2017-18(Sem-I), Marks 3.5

**Answer**

- For the depletion mode, the gate is maintained at negative potential while the drain is maintained at positive potential.
- When voltage between gate and source is zero ( $V_{GS} = 0$ ), as shown in the Fig. 3.38.1., significant current flows for a given  $V_{DS}$ , like a FET.

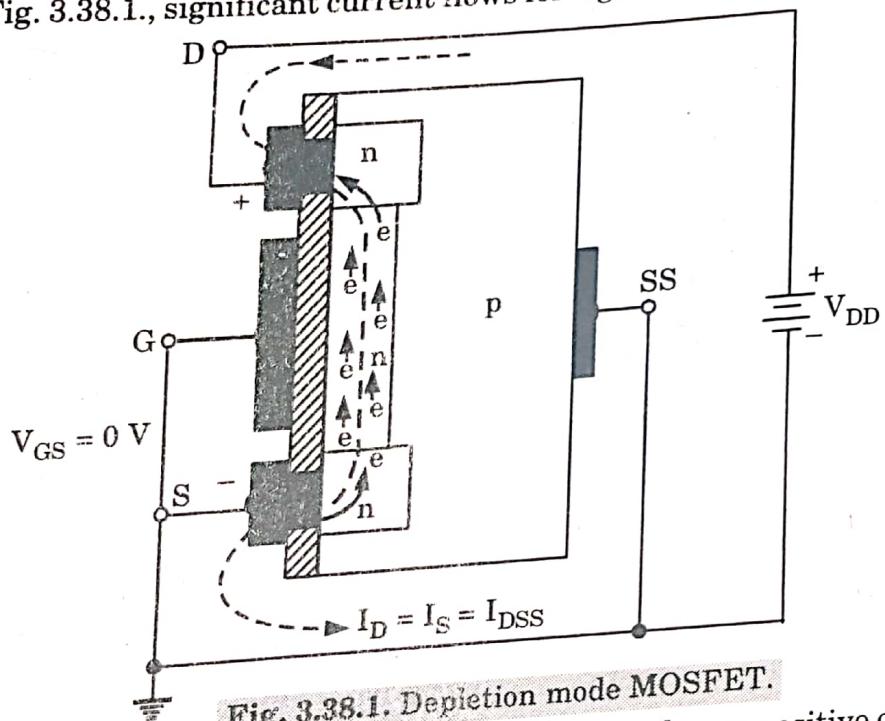


Fig. 3.38.1. Depletion mode MOSFET.

- Let negative potential is applied at the gate. In such case positive charges are induced in n-channel through  $\text{SiO}_2$  as shown in Fig. 3.38.2.

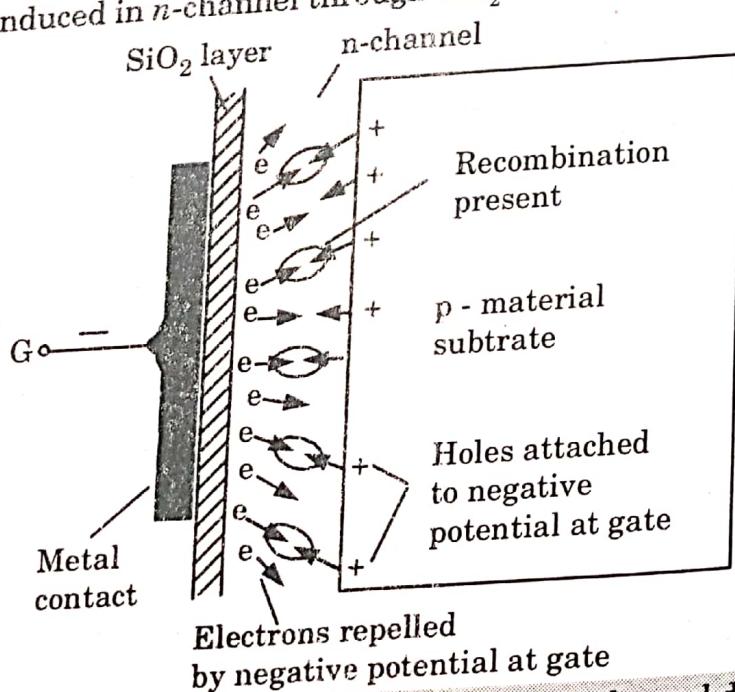
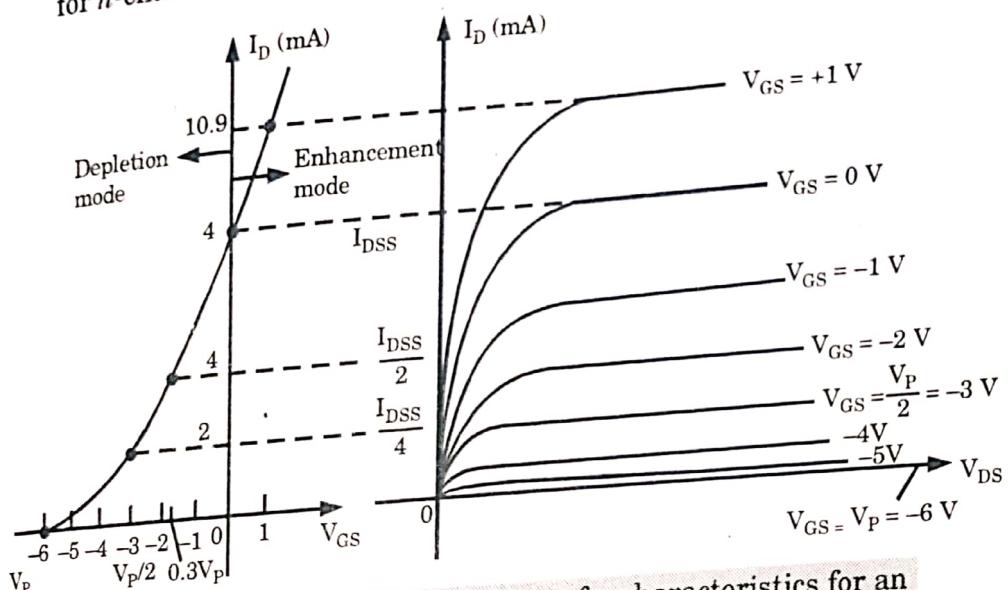


Fig. 3.38.2. Reduction in free carriers in a channel due to a negative potential at the gate terminal.

4. This mechanism depletes the channel from majority carriers i.e., electrons, and hence conductivity decreases.
5. Here it should be remembered that because of the voltage drop due to drain current  $I_D$ , the channel region near the drain end is more depleted than the region near the source.
6. Here too much negative gate voltage can pinch-off the channel. Hence a MOSFET behaves like a FET.

#### Characteristics curves of MOSFET :

1. Fig. 3.38.3 shows the drain characteristics and transfer characteristics for *n*-channel MOSFET respectively.



**Fig. 3.38.3.** Drain and transfer characteristics for an *n*-channel depletion-type MOSFET.

2. The two modes, namely depletion mode and enhancement mode correspond to negative and positive gate voltages respectively.
3. It is obvious, that for  $V_{GS} = 0$ , the drain current  $I_D$  is not zero, but it has appreciable value.
4. The gate voltage at which  $I_D$  reduces at a recommended drain voltage  $V_{DS}$  is called gate source cut-off voltage. This is denoted by  $V_{GS}$  (OFF) and corresponds to pinch-off voltage  $V_P$ .

**Que 3.39.** Draw and explain the construction and working of *p*-channel depletion type MOSFET. Also draw the characteristics of *p*-channel depletion type MOSFET.

**AKTU 2016-17(Sem-II), Marks 07**

**Answer**

1. Fig. 3.39.1 shows a *p*-channel depletion type MOSFET.

2. When zero voltage is applied to the gate, a *p*-channel or an inversion layer of holes exist under the oxide.
3. Since the *p*-channel interconnects the *p*<sup>+</sup>-type source and *p*<sup>+</sup>-type drain, a drain-to-source current flows even though the gate voltage is equal to zero.
4. The depletion states that the channel exists even at zero gate voltage.
5. If a positive gate voltage is applied between gate to source of the *p*-channel depletion type MOSFET, the device will be turned OFF.

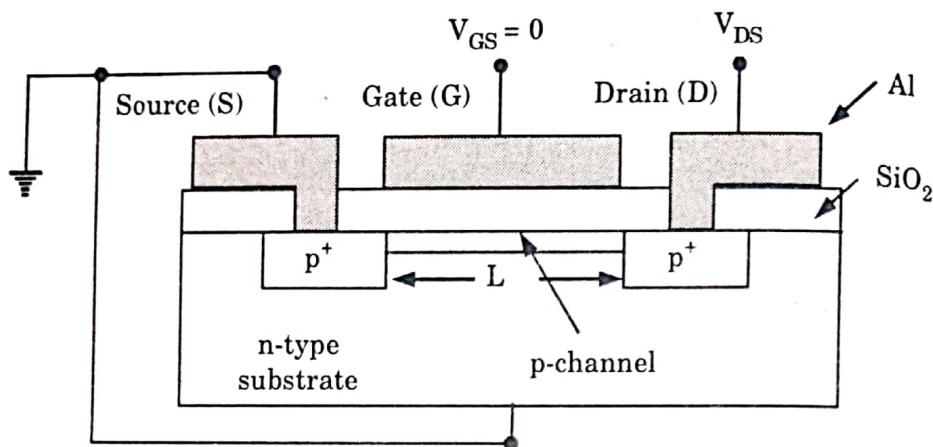


Fig. 3.39.1. Cross-section of a *p*-channel depletion type MOSFET with  $V_{GS} = 0$ .

6. A *p*-channel depletion type MOSFET with positive gate voltage is shown in Fig. 3.39.2.

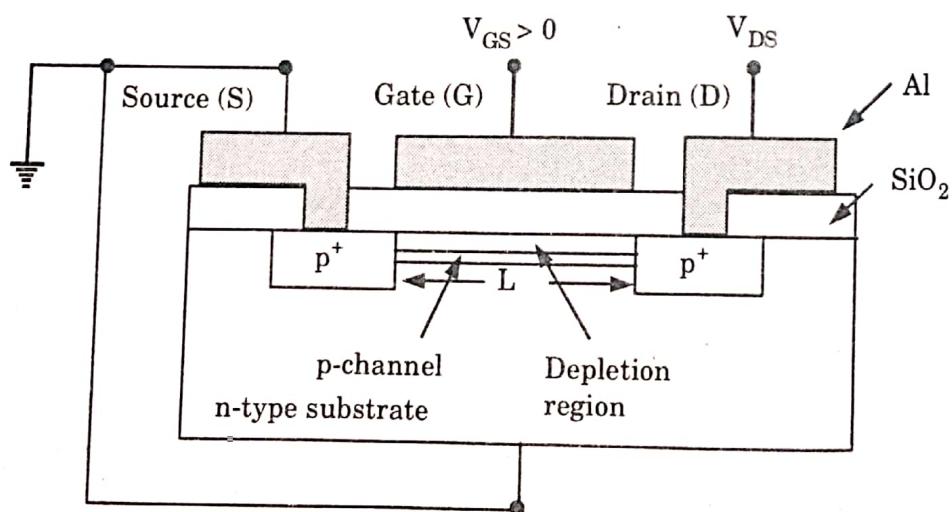


Fig. 3.39.2. Cross-section of a *p*-channel depletion type MOSFET with  $V_{GS} > 0$ .

7. Due to positive gate voltage, a space charge region is induced under the oxide. Consequently, the thickness of the *p*-channel region will be reduced.
8. Since the channel thickness is reduced, the channel conductance is also reduced and in turn drain current reduces.

9. If positive gate voltage is equal to the threshold voltage, the induced space charge region extends completely through the *p*-channel region and drain current becomes zero.
10. When a negative gate voltage is applied between gate to source, this negative gate voltage creates a hole accumulation layer as shown in Fig. 3.39.3.

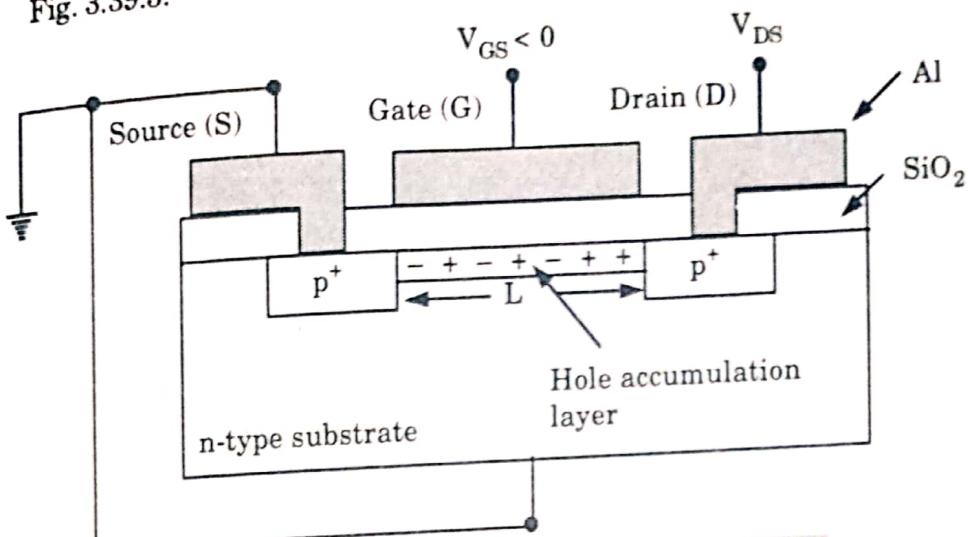


Fig. 3.39.3. Cross-section of a *p*-channel depletion MOSFET with  $V_{GS} < 0$ .

11. Due to accumulation of holes in the *p*-type channel, drain current increases.
12. The drain and transfer characteristics are shown in Fig. 3.39.4.

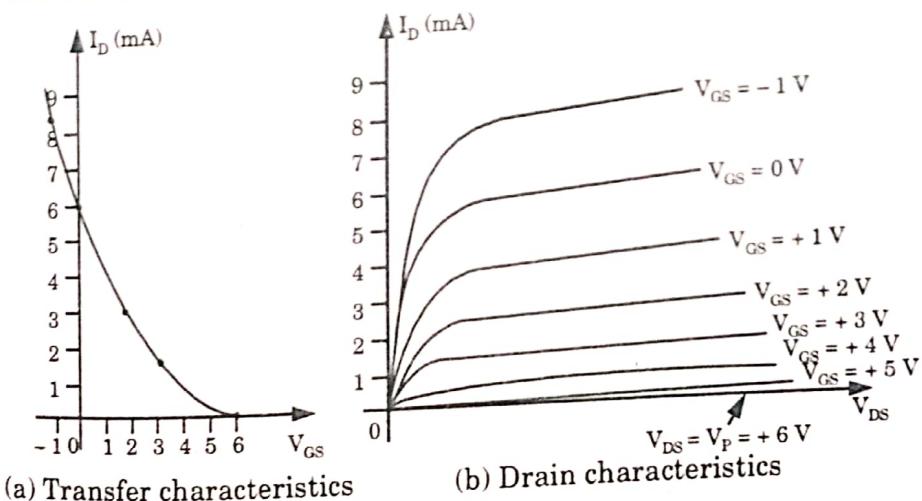


Fig. 3.39.4.

**Que 3.40.** Explain enhancement type MOSFET with diagram and draw the transfer and output characteristic.

AKTU 2013-14(Sem-I), Marks 05

**Describe the working operation of enhancement mode and depletion mode MOSFET. Also derive an expression for  $g_m$  of JFET configuration.**

**AKTU 2015-16(Sem-II), Marks 7.5**

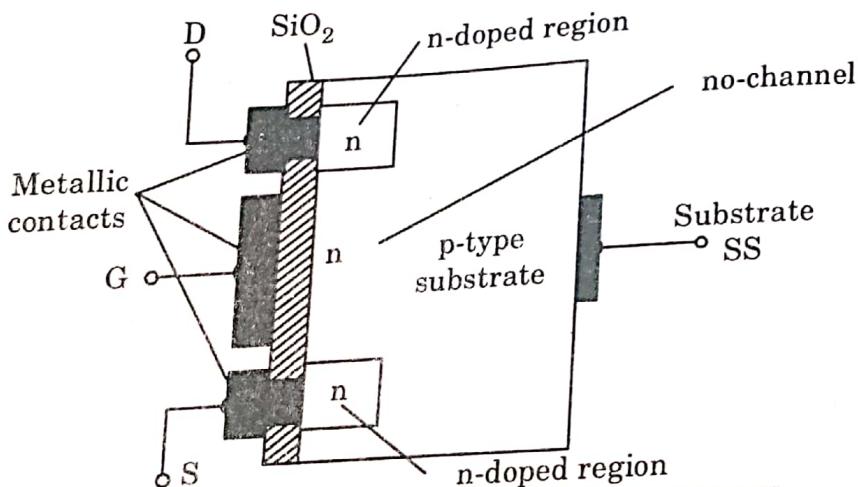
**Answer**

**Depletion mode MOSFET :** Refer Q. 3.38, Page 3-49D, Unit-3.

**Expression for  $g_m$  :** Refer Q. 3.34, Page 3-43D, Unit-3.

**Enhancement MOSFET :**

- Fig. 3.40.1 shows the cross-sectional view of *n*-channel enhancement MOSFET.
- It consists of a lightly doped *p*-type substrate into which two heavily doped *n*<sup>+</sup>-regions are diffused. This *n*<sup>+</sup>-regions act as source and drain respectively.



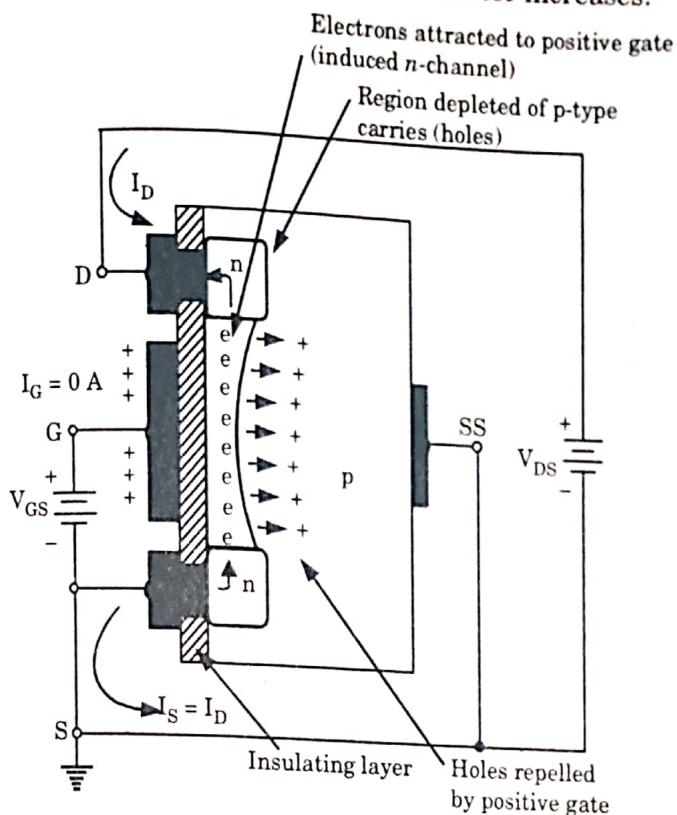
**Fig. 3.40.1. Enhancement MOSFET.**

- A thin layer of insulating  $\text{SiO}_2$  is grown over the entire surface and holes are cut into the oxide layer through which metal contacts are to be made for source and drain terminals.
- On  $\text{SiO}_2$  layer, a conducting layer of aluminium overlaid, covering entire channel length from source to drain, constitute the gate.

**Working of Enhancement MOSFET :**

- The channel, the insulating dielectric  $\text{SiO}_2$  and metal layer of gate forms a parallel plate capacitor.
- When a positive potential is applied at the gate with respect to substrate, negative charges are induced on semiconductor side.
- These negative charges, induced on *p*-type substrate consist of electrons which forms an inversion layer as shown in Fig. 3.40.2.
- The inversion layer forms an effective *n*-type channel.

5. When the positive potential at the gate is increased, the magnitude of the induced negative charges in semiconductor increases.



**Fig. 3.40.2.** Channel formation in the n-channel enhancement type MOSFET.

6. Thus, the conductivity of induced n-channel increases and results in increased drain current.
7. For a constant drain voltage, the drain current increases as the positive drain voltage increases i.e., the drain current has been enhanced by the application of positive gate voltage. Such MOSFET is termed as an enhancement MOSFET.

#### Characteristics curves of enhancement MOSFET :

1. Fig. 3.40.3 shows the static drain and transfer characteristics of n-channel enhancement MOSFET.
2. From Fig. 3.40.3, as  $V_{GS}$  is made positive, the drain current first increases slowly and then at relatively fast rate with increase of  $V_{GS}$ .
3. The threshold voltage is defined as the gate voltage at which channel is induced to produce the flow of current  $I_D$  of prescribed value and is denoted by  $V_T$ . Such type of FET is very useful in switching applications, since no gate voltage is required to hold it off.

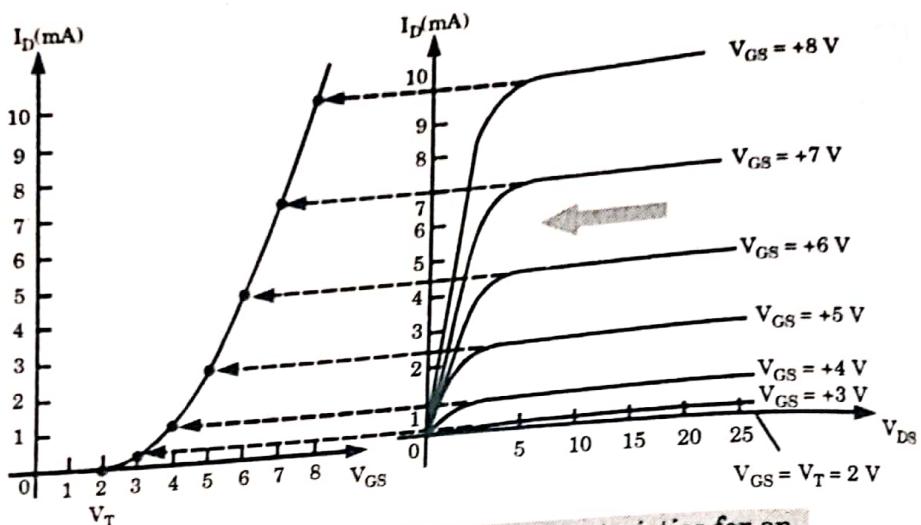


Fig. 3.40.3. Drain and transfer characteristics for an n-channel enhancement-type MOSFET.

**Que 3.41.** Explain construction, working and characteristics of p-channel enhancement MOSFET.

AKTU 2015-16(Sem-I), Marks 05

### Answer

#### Construction :

1. The construction of a p-channel enhancement type MOSFET is exactly the reverse of that n-channel enhancement type MOSFET. It is shown in Fig. 3.41.1(a).
2. There is an n-type substrate and p-doped regions under the drain and source connections.
3. The terminal remains as identified, but all the polarities and the current directions are reversed.

#### Operation :

- i. When  $|V_{SG}| < |V_{tp}|$  :  
There is no channel and transistor operates in cut-off mode i.e.,  $i_D = 0$ .
- ii. When  $|V_{DG}| > |V_{tp}|$  or  $|V_{SD}| < |V_{ov}|$  :  
The continuous channel is created and transistor operates in triode region.
- iii. When  $|V_{DG}| \leq |V_{tp}|$  or  $|V_{SD}| \geq |V_{ov}|$  :  
The channel is pinched-off and the transistor operates in saturation region.

#### Characteristics :

1. The drain characteristics will appear as shown in Fig 3.41.1(b), with increasing levels of current resulting from increasingly negative values of  $V_{GS}$ .

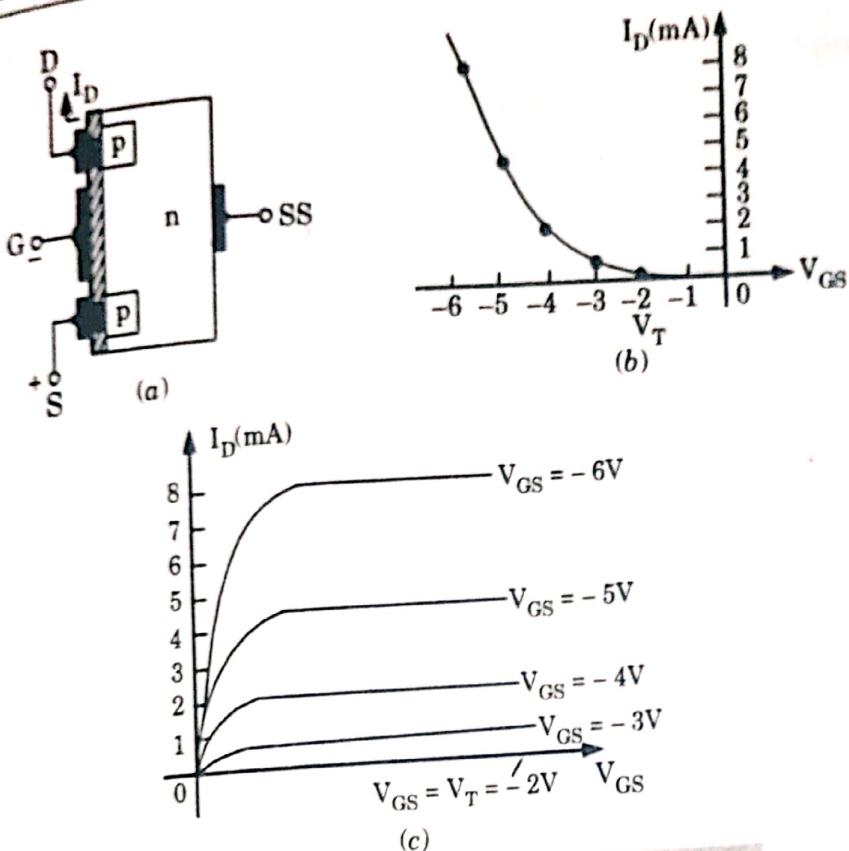


Fig. 3.41.1. p-channel enhancement-type MOSFET.

2. The transfer characteristics will be the mirror image (about the  $I_D$  axis) of the transfer curve of  $n$ -channel enhancement MOSFET.
3. The transfer curve is shown in Fig. 3.41.1(c), with  $I_D$  increasing with increasingly negative values of  $V_{GS}$  beyond  $V_T$ .

**Que 3.42.** Determine  $Z_i$ ,  $Z_o$ ,  $V_o$  for the network of Fig. 3.42.1 if

$$V_i = 20 \text{ mV.}$$

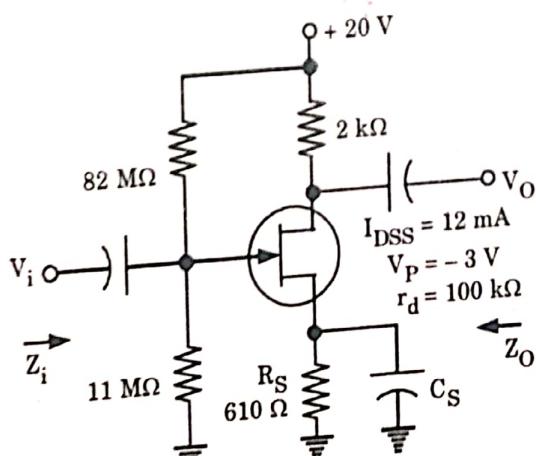


Fig. 3.42.1.

AKTU 2014-15(Sem-II), Marks 05

**Answer**

1. Converting Fig. 3.42.1 as given in Fig. 3.42.2.

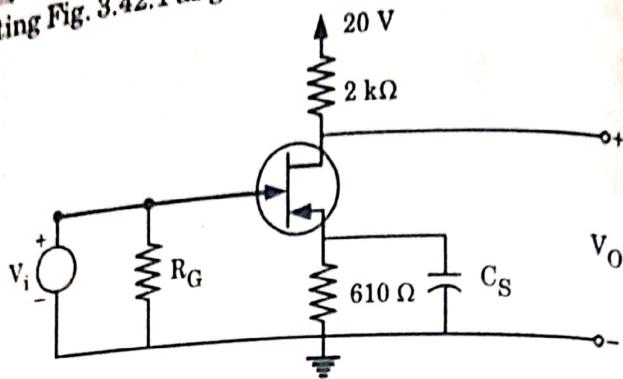


Fig. 3.42.2.

$$\text{where, } R_G = 82 \text{ M}\Omega \parallel 11 \text{ M}\Omega$$

$$2. Z_i = R_g = 82 \text{ M}\Omega \parallel 11 \text{ M}\Omega = \frac{82 \times 11 \times 10^6}{82 + 11} = 9.698 \text{ M}\Omega$$

$$3. Z_O = r_d \parallel R_D \\ = \frac{100 \times 10^3 \times 2 \times 10^3}{(100 + 2) \times 10^3} = 1.96 \text{ k}\Omega$$

$$4. V_O = -g_m V_{gs} (r_d \parallel R_D)$$

$$5. \text{ We know that } g_m = \frac{-2 I_{DSS}}{V_P} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$

$$6. \text{ For } V_{GS}, \frac{20 \times 11}{82 + 11} = I_D \times 610$$

$$I_D = 3.880 \text{ mA}$$

$$7. I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$3.88 \times 10^{-3} = 12 \times 10^{-3} \left[ 1 - \frac{V_{GS}}{-3} \right]^2$$

$$\frac{3.88 \times 10^{-3}}{12 \times 10^{-3}} = \left[ 1 + \frac{V_{GS}}{3} \right]^2$$

$$V_{GS} = -1.294$$

$$8. g_m = \frac{-2 \times 12 \times 10^{-3}}{-3} \left( 1 - \frac{(-1.294)}{(-3)} \right) = 4.55 \text{ ms}$$

$$9. V_{gs} = V_i = 20 \text{ V}$$

$$10. V_O = -4.55 \times 10^{-3} \left[ \frac{100 \times 2 \times 10^3}{100 + 2} \right] = -8.92 \text{ V}$$

**Que 3.43.** Determine  $I_D$ ,  $V_{GS}$ ,  $V_D$ ,  $V_S$  and  $V_{DS}$  for the given network as shown in Fig. 3.43.1.

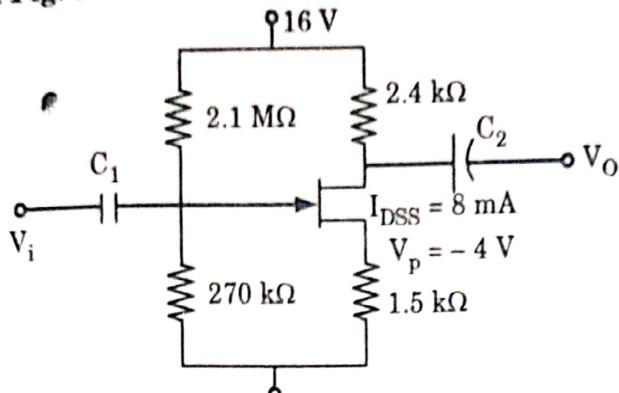


Fig. 3.43.1.

AKTU 2013-14(Sem-II), Marks 05

**Answer**

1.  $V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{270 \times 16}{2100 + 270} = 1.82 \text{ V}$

2.  $V_{GS} = V_G - I_D R_S = 1.82 - 1.5 I_D$

3. As,  $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$

4. On solving,  $I_{DQ} = 2.41 \text{ mA}$

5.  $V_{GSQ} = 1.82 - 2.41 \times 1.5 = -1.795 \text{ V}$

6.  $V_D = V_{DD} - I_D R_D = 16 - 2.41 \times 2.4 = 10.216 \text{ V}$

7.  $V_S = I_D R_S = 3.615 \text{ V}$

8.  $V_{DS} = V_D - V_S = 6.601 \text{ V}$

9.  $V_{DG} = V_D - V_G = 8.396 \text{ V}$

**Que 3.44.** For voltage divider configuration of Fig. 3.44.1 if  $V_D = 12 \text{ V}$  and  $V_{GSQ} = -2 \text{ V}$ , determine the value of resistance ( $R_S$ ).

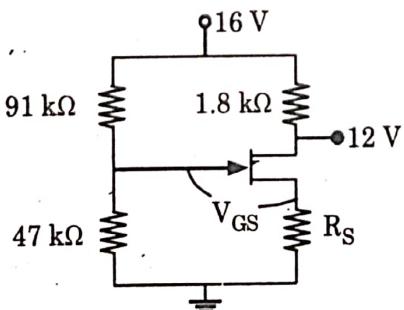


Fig. 3.44.1.

AKTU 2013-14(Sem-I), Marks 05

**Answer**

1. Given,

$$V_D = 12 \text{ V}, V_{GSQ} = -2 \text{ V},$$

$$V_{DD} = 16 \text{ V}, R_1 = 91 \text{ k}\Omega, R_2 = 47 \text{ k}\Omega$$

$$R_D = 1.8 \text{ k}\Omega.$$

2.  $V_{GG} = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{47 \times 16}{91 + 47} = 5.45 \text{ V}$

3.  $R_G = \frac{R_1 R_2}{R_1 + R_2} = \frac{91 \times 47}{91 + 47} = 31 \text{ k}\Omega.$

4. We know  $V_{GS} = V_{GG} - I_D R_S$  ... (3.44.1)  
and  $V_D = V_{DD} - I_D R_D$   
 $12 = 16 - I_D \times 1.8 \times 10^3$

$$\frac{4}{1.8 \times 10^3} = I_D$$

$$I_D = 2.2 \text{ mA.}$$

5. Substitute  $I_D$  value in eq. (3.44.1), we get.

$$-2 = 5.45 - 2.2 \times 10^{-3} R_s$$

$$-7.45 = -2.2 \times 10^{-3} R_s$$

$$R_s = 3.386 \text{ k}\Omega.$$

**Que 3.45.** Define and explain the given parameter transconductance ( $g_m$ ), drain resistance ( $r_d$ ) and amplification ( $\mu$ ) of a JFET. In JFET  $I_{DSS} = 8 \text{ mA}$ ,  $V_p = -4 \text{ V}$  biased at  $V_{GS} = -1.8 \text{ V}$ .

Determine the value  $g_m$ .**AKTU 2013-14(Sem-I), Marks 05****Answer**

**Definition of parameters :** Refer Q. 3.32, Page 3-41D, Unit-3.  
**Numerical :**

1. Given,  $I_{DSS} = 8 \text{ mA}$ 

$$V_p = -4 \text{ V}$$

$$V_{GS} = -1.8 \text{ V}$$

2. Relation between  $g_m$  and  $V_{GS}$  is given by,

$$g_m = \frac{-2 I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right) = \frac{-2 \times 8 \times 10^{-3}}{-4} \left(1 - \frac{(-1.8)}{(-4)}\right)$$

$$= 4 \times 10^{-3} \times 0.55 = 2.2 \text{ mA/V.}$$

**Que 3.46.** The *n*-channel JFET as shown in Fig. 3.46.1 has  $I_{DSS} = 1.5 \text{ mA}$ ,  $V_p = 1.5 \text{ V}$ . If the quiescent drain to ground voltage is 10 volts, find  $R_1$ .

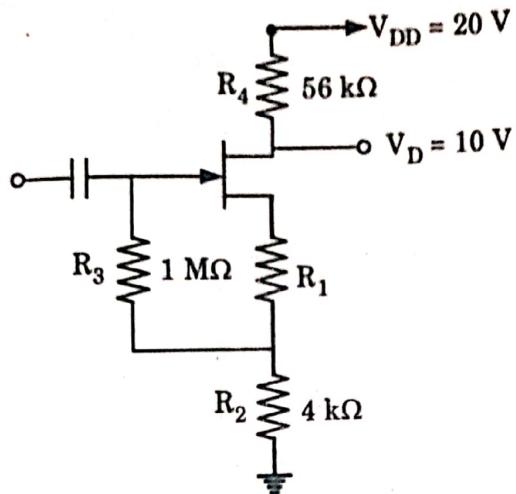


Fig. 3.46.1.

**Answer**

1. Given :

$$I_{DSS} = 1.5 \text{ mA}, V_D = 10 \text{ V}$$

$$V_p = -1.5 \text{ V}, R_1 = ?$$

$$2. I_D = \frac{V_{DD} - V_D}{R_4} = \frac{20 - 10}{56 \times 10^3} = 0.178 \text{ mA}$$

$$3. I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

$$0.178 \times 10^{-3} = 1.5 \times 10^{-3} \left( 1 - \frac{V_{GS}}{-1.5} \right)^2$$

$$0.119 = \left( 1 + \frac{V_{GS}}{1.5} \right)^2$$

$$0.344 = 1 + \frac{V_{GS}}{1.5}$$

$$V_{GS} = -0.9825 \text{ V}$$

$$4. V_{GS} = -I_O R_1$$

$$R_1 = \frac{-V_{GS}}{I_D} = \frac{0.9825}{0.178 \times 10^{-3}} = 5.519 \text{ k}\Omega$$

**Que 3.47.** Determine  $Z_i$ ,  $Z_o$  and  $A_v$  for the network of Fig. 3.47.1, if

$I_{DSS} = 12 \text{ mA}$ ,  $V_p = -6 \text{ V}$ , and  $Y_{OS} = 40 \text{ micro siemens}$ .

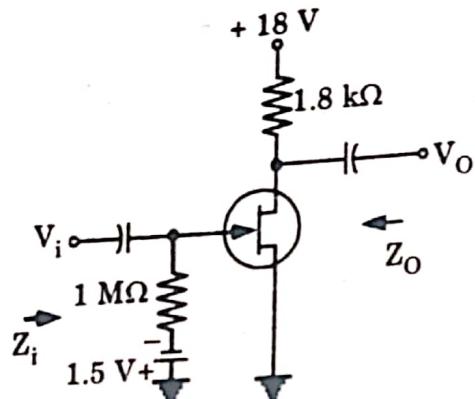


Fig. 3.47.1.

AKTU 2015-16(Sem-I), Marks 05

**Answer**

1. Given,

$$I_{DSS} = 12 \text{ mA}, V_P = -6 \text{ V} \text{ and } Y_{OS} = 40 \mu\text{S}$$

$$R_G = 1 \text{ M}\Omega, R_D = 1.8 \text{ k}\Omega$$

$$Z_i = R_G = 1 \text{ M}\Omega$$

$$Z_o = R_D \parallel r_d$$

$$r_d = \frac{1}{Y_{OS}} = \frac{1}{40 \mu\text{S}} = 25 \text{ k}\Omega$$

$$Z_o = (1.8 \text{ k}\Omega) \parallel (25 \text{ k}\Omega) = 1.68 \text{ k}\Omega$$

$$A_V = -g_{mO} (R_D \parallel r_d)$$

$$g_m = g_{mO} \left( 1 - \frac{V_{GSQ}}{V_P} \right)$$

$$g_{mO} = \frac{2 I_{DSS}}{|V_P|} = \frac{2 \times 12 \times 10^{-3}}{6} = 4 \text{ mS}$$

$$g_m = 4 \times 10^{-3} \left( 1 - \frac{(-1.5)}{(-6)} \right) = 3 \text{ mS}$$

$$A_V = -(3 \text{ mS}) (1.8 \text{ k}\Omega \parallel 25 \text{ k}\Omega)$$

$$A_V = -(3 \text{ mS}) \times (1.68 \text{ k}\Omega)$$

$$A_V = -5.04$$

**Que 3.48.** For the voltage divider network shown in Fig. 3.48.1.

Given  $I_{DSS} = 10 \text{ mA}$ ,  $V_P = -3.5 \text{ V}$ , determine  $V_G$ ,  $I_{DQ}$ ,  $V_{GSQ}$ ,  $V_D$ ,  $V_S$  and  $V_{DSQ}$ .

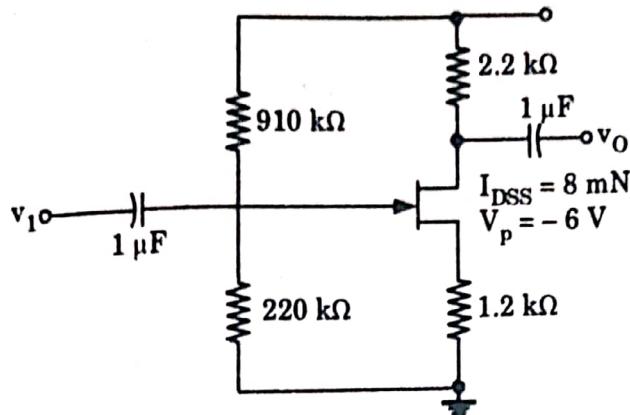


Fig. 3.48.1.

AKTU 2017-18(Sem-II), Marks 07

**Answer**

The procedure is same as Q. 3.43, Page 3-59D, Unit-3.

**Ans.**  $V_G = 3.33 \text{ V}$ ,  $V_{GS} = V_{GSQ} = -1.662 \text{ V}$ ,  $V_{DSQ} = 3.188 \text{ V}$ ,  $V_D = 8.188 \text{ V}$ ,

$V_S = 5 \text{ V}$ ,  $I_{DQ} = 4.16 \text{ mA}$

**VERY IMPORTANT QUESTIONS**

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

- Q. 1.** Draw the basic structure of CB BJT and explain its principle of operation with in neat diagram along with its input and output characteristics.

**Ans.** Refer Q. 3.6.

- Q. 2.** Draw and explain the input and output characteristics of common emitter configuration.

**Ans.** Refer Q. 3.7.

- Q. 3.** Explain the operation of common collector configuration with suitable characteristics in detail.

**Ans.** Refer Q. 3.8.

- Q. 4.** Explain the operation of voltage divider bias circuit and write down the approximate equations of  $V_B$ ,  $I_E$ ,  $I_C$  and  $V_{CE}$ .

**Ans.** Refer Q. 3.13.

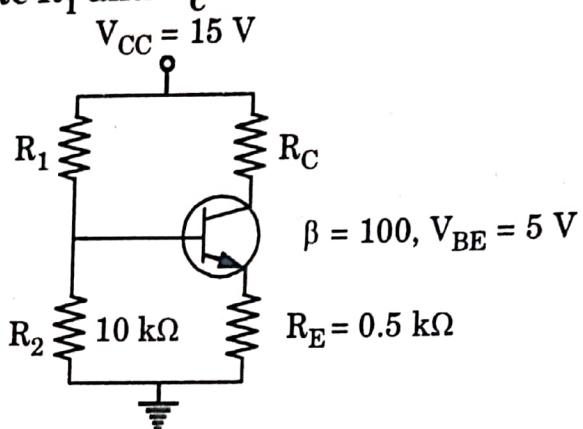
**Q. 5. Derive the stability factor  $S(I_{co})$  for the fixed bias configuration.**

**Ans.** Refer Q. 3.16.

**Q. 6. Explain how the input impedance of an amplifier can load down the AC source.**

**Ans.** Refer Q. 3.22.

**Q. 7. In the circuit shown in Fig. 1 if  $I_C = 2 \text{ mA}$  and  $V_{CE} = 3 \text{ V}$ , calculate  $R_1$  and  $R_C$ .**



**Fig. 1.**

**Ans.** Refer Q. 3.26.

**Q. 8. Explain the transconductance curve of a JFET.**

**Ans.** Refer Q. 3.31.

**Q. 9. Draw the circuit of *n*-channel depletion type MOSFET and explain its operation. Also draw its drain and transfer characteristics.**

**Ans.** Refer Q. 3.38.

**Q. 10. Explain enhancement type MOSFET with diagram and draw the transfer and output characteristic.**

**Ans.** Refer Q. 3.40.

**Q. 11. Explain construction, working and characteristics of *p*-channel enhancement MOSFET.**

**Ans.** Refer Q. 3.41.





## BJT and FET (2 Marks Questions)

**3.1. What are the various operating modes of transistor ?**

**Ans.** There are 4 different modes of transistor :

S.No.	Mode	BE	CB
1.	Active	Forward bias	Reverse bias
2.	Saturation	Forward bias	Forward bias
3.	Cut-off	Reverse bias	Reverse bias
4.	Inverse active	Reverse bias	Forward bias

**3.2. Establish the relationship between  $I_{CEO}$  and  $I_{CBO}$  of a BJT.**

**AKTU 2013-14(Sem-II), Marks 02**

**Ans.** The collector current can expressed as

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

The collector current when  $I_B = 0$ ,  $I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$

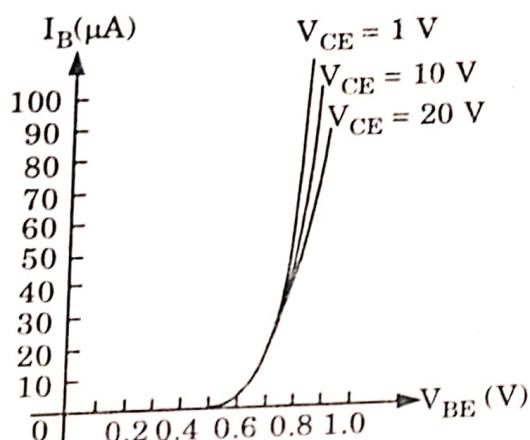
**3.3. What is major difference between a bipolar and unipolar device ?**

**Ans:**

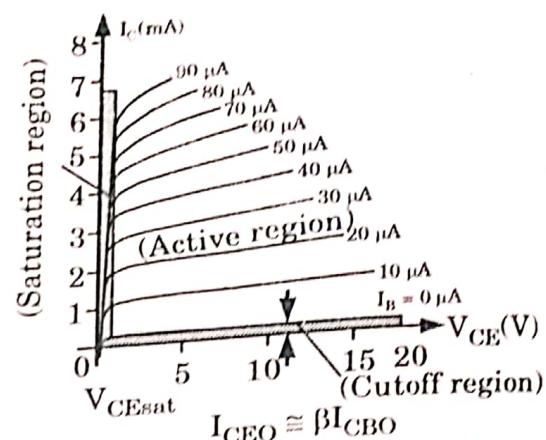
S.No.	Bipolar device	Unipolar device
1.	It has low input impedance.	It has high input resistance in order of $100 \text{ M}\Omega$ i.e., high.
2.	It is more noisy.	It is less noisy.
3.	It is more affected by radiation.	Radiation affects less.
4.	Cost is less.	Cost is high.

**3.4. Sketch the input and output characteristics (V-I) of a CE *npn* transistor configuration with proper labels.**

**Ans.**



(a) Input characteristics



(b) Output characteristics

Fig. 3.4.1.

**3.5. Enlist the difference between JFET and BJT.**

AKTU 2013-14(Sem-I), Marks 02

AKTU 2013-14(Sem-II), Marks 02

**Ans.**

S. No.	JFET	BJT
1.	Its operation depends only on majority carriers, so it is a unipolar device.	Its operation depends on both majority and minority carriers, so it is a bipolar device.
2.	It is a voltage controlled device.	It is a current controlled device.
3.	It has high input impedance.	It has low input impedance.
4.	Small in size, therefore space requirement on board is small.	Large in size, therefore space requirement on board is large.

**3.6. Draw the transfer and output characteristics of *n*-channel FET.**

AKTU 2013-14(Sem-I), Marks 02

AKTU 2013-14(Sem-II), Marks 02

**Ans.**  
A. Transfer characteristics :

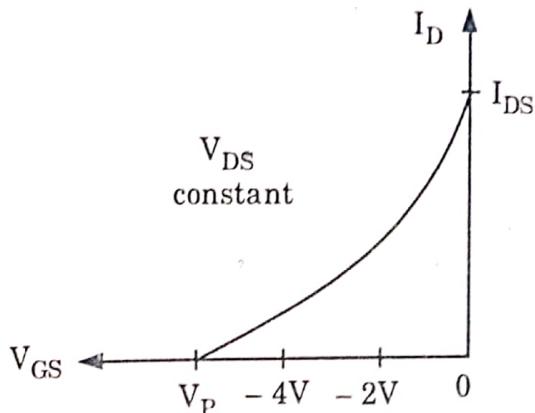
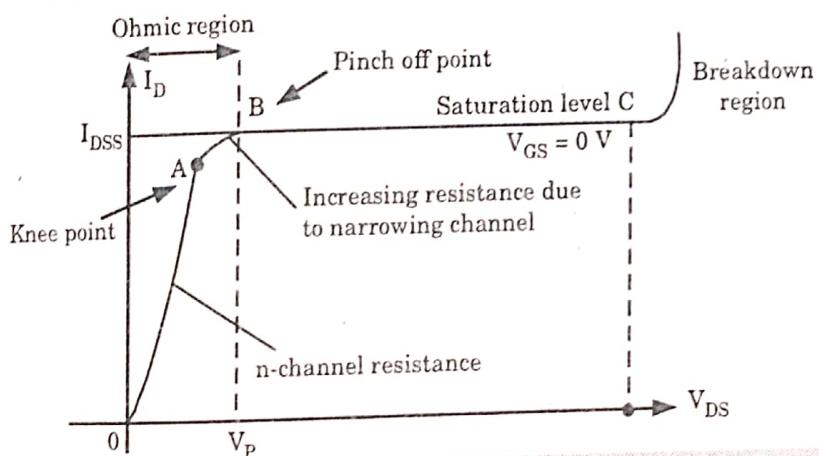


Fig. 3.6.1. Transfer characteristics.

B. Output characteristics :

Fig. 3.6.2. Drain characteristics of n-channel FET when  $V_{GS} = 0$ .

3.7. Enlist the differences between JFET and MOSFET.

AKTU 2013-14(Sem-I), Marks 02

**Ans.**

S.No.	JFET	MOSFET
1.	JFET have lower input resistance than MOSFET.	MOSFET have much higher input resistance than JFET.
2.	JFET can operate in depletion mode.	MOSFET can operate in enhancement as well as depletion mode.

3.8. Write down the constructional difference between depletion type and enhancement type MOSFET.

AKTU 2016-17(Sem-II), Marks 02

**Ans.** The main constructional difference is the absence of continuous channel between the source and drain of enhancement MOSFET but it is present in case of depletion MOSFET.

- 3.9. Mention the differences between *p*-channel and *n*-channel MOSFET.

**Ans.**

S.No.	<i>p</i> -channel MOSFET	<i>n</i> -channel MOSFET
1.	The current carriers are holes.	The current carriers are electrons.
2.	Transconductance is less in <i>p</i> -channel than <i>n</i> -channel.	Transconductance is more in <i>n</i> -channel than <i>p</i> -channel.
3.	Due to lower mobility of holes <i>p</i> -channel is not as fast as <i>n</i> -channel.	Due to higher mobility of electrons, <i>n</i> -channel MOSFET is faster.

- 3.10. Describe how FET can be used as voltage variable resistor.

AKTU 2017-18(Sem-II), Marks 02

OR

Explain FET as voltage variable resistor.

AKTU 2016-17(Sem-I), Marks 02

AKTU 2015-16(Sem-I), Marks 02

**Ans.** FET when used in the region before pinch-off, it works as variable resistance device i.e., the channel resistance is controlled by the gate bias voltage ( $V_{gs}$ ). In such applications FET is referred as voltage variable resistor (VVR).

- 3.11. The BJT circuitry has  $I_C = 10 \text{ mA}$  and  $\alpha = 0.98$ . Determine the value of  $I_E$ .

AKTU 2013-14(Sem-I), Marks 02

AKTU 2013-14(Sem-II), Marks 02

**Ans.**

Given :  $\alpha = 0.98$ ,  $I_C = 10 \text{ mA}$   
To Find :  $I_E$

We know that,

$$\alpha = I_C/I_E$$

$$\therefore I_E = \frac{10 \times 10^{-3}}{0.98} = 10.2 \text{ mA}$$

**3.12. Why BJT is called current controlled device ?**

AKTU 2017-18(Sem-I), Marks 02

**Ans.** A BJT is called current control device because the base current controls the current flow from emmitter to collector.

**3.13. Derive the relation between  $\alpha$  and  $\beta$  for BJT.**

AKTU 2017-18(Sem-II), Marks 02

AKTU 2016-17(Sem-II), Marks 02

AKTU 2016-17(Sem-I), Marks 02

**Ans.** We know that,  $I_E = I_C + I_B$  .....(3.13.1)

Dividing eq. (3.13.1) both sides by  $I_C$ , we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

But we know that  $\beta = \frac{I_C}{I_B}$  and  $\alpha = \frac{I_C}{I_E}$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} = \frac{\beta + 1}{\beta}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

**3.14. In JFET,  $I_{DSS} = 8 \text{ mA}$ ,  $V_P = -4 \text{ V}$  biased at  $V_{GS} = -1.8 \text{ V}$ . Determine the value of  $g_m$ .**

AKTU 2013-14(Sem-II), Marks 02

AKTU 2015-16(Sem-I), Marks 02

**Ans.** Given,  $I_{DSS} = 8 \text{ mA}$ ,  $V_P = -4 \text{ V}$ ,  $V_{GS} = -1.8 \text{ V}$

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{V_{GS}}{V_P} \right] = \frac{2 \times 8}{4} \left[ 1 - \frac{1.8}{4} \right] = 2.2 \text{ mS}$$

**3.15. Define Ohmic region in FET.**

AKTU 2015-16(Sem-II), Marks 02

**Ans.**

1. In the ohmic region, FET works as a linear device, i.e., a resistor. For example, voltage-variable resistor (VVR) and voltage-dependent resistor (VDR).
2. In the ohmic region, FET will work as a voltage-variable resistor by varying  $V_{GS}$ .

3.16. If  $\alpha$  of a transistor changes from 0.981 to 0.987, find the percentage change in  $\beta$ .

AKTU 2015-16(Sem-II), Marks 02

**Ans.** Here,

$$\beta_1 = \frac{\alpha_1}{1 - \alpha_1} = \frac{0.981}{1 - 0.981} = 51.632$$

$$\beta_2 = \frac{\alpha_2}{1 - \alpha_2} = \frac{0.987}{1 - 0.987} = 75.92$$

$$\% \text{ change in } \beta = \frac{\beta_2 - \beta_1}{\beta_1} = \frac{75.92 - 51.632}{51.632} = 47\%$$

3.17. The thickness of base is typically smaller than emitter and collector. Why ?

AKTU 2016-17(Sem-I), Marks 02

**Ans.** Base is very highly doped and is very thin ( $10^{-6}$  m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

3.18. Why are FET called unipolar device ?

AKTU 2016-17(Sem-II), Marks 02

**Ans.** In FET, current conduction depends only on one type of carriers (majority carriers) either electrons or holes, so it is a unipolar device.

3.19. Explain with proper reason the use of Emitter Follower.

AKTU 2015-16(Sem-I), Marks 02

**Ans.** The Emitter Follower is used as a voltage buffer for connecting a high resistance source to a low resistance load.

3.20. What is trans-conductance in FET ? What is the relationship between  $g_m$  and  $g_{mo}$  ?

AKTU 2017-18(Sem-I), Marks 02

**Ans.** The control that the gate voltage has over drain current is measured by transconductance  $g_m$ . It is simply the slope of transfer characteristics.

$$g_m = \left( \frac{\Delta I_D}{\Delta V_{GS}} \right) V_{DS} \text{ held constant}$$

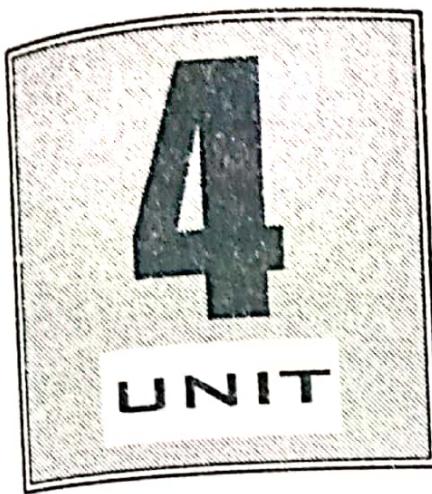
The unit of  $g_m$  is siemens (mho).

$$g_m = g_{mo} \sqrt{I_{DQ} / I_{DSS}}$$



A

UNIT



# Operational Amplifier

## CONTENTS

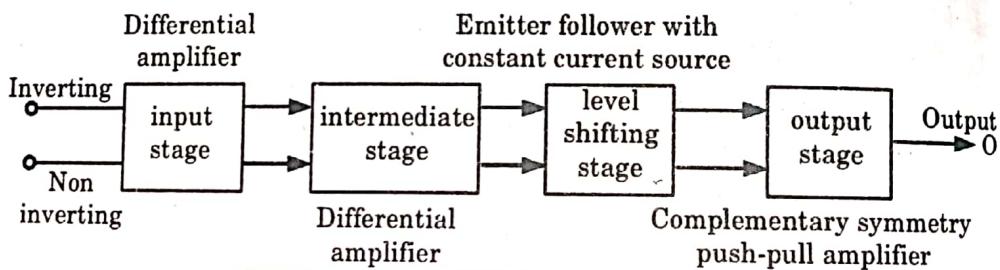
- Part-1 :** Operational Amplifier : ..... **4-2D to 4-3D**  
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of Op-amp
- Part-2 :** Ideal and Practical ..... **4-3D to 4-4D**  
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**PART - 1***Operational Amplifier : Introduction and Block Diagram of Op-amp.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 4.1.** Define op-amp with the help of block diagram. Also draw its equivalent circuit.

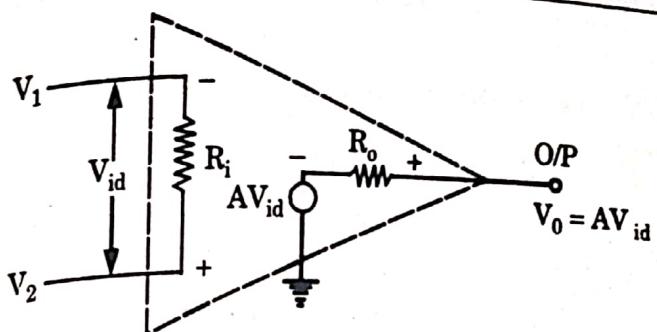
**Answer**

1. Op-amp is designed to perform various mathematical operations.
2. The Fig. 4.1.1 represents the block diagram approach of an operational amplifier.



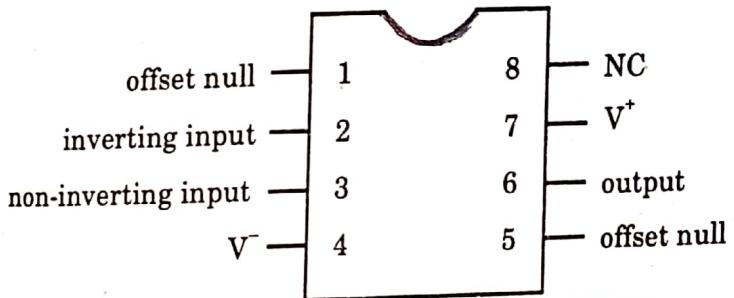
**Fig. 4.1.1. Block diagram of Op-Amp.**

3. It consists of two differential amplifiers followed by level shifter and an output stage.
4. The input stage is a dual input differential amplifier which provides most of the voltage gain to operational amplifier. It also provides high resistance to operational amplifier.
5. The intermediate stage is also dual input. This is driven by the output of first stage and is used to provide some additional gain. The DC level at the output of intermediate stage is well above the ground level.
6. The level shifter is an emitter follower using constant current source. The function of level shifter is to shift DC level at the output of intermediate stage downwards to zero volt with respect to ground.
7. The output stage is generally push-pull amplifier. Its function is to increase large output voltage swing capability and to provide low output resistance.



**Fig. 4.1.2. Equivalent circuit.**

8. Fig. 4.1.2, shows the equivalent circuit of operational amplifier.
9.  $V_{id}$  is the difference of two input voltages i.e.,  $(V_2 - V_1)$ .  $R_i$  is the input resistance.
10.  $R_o$  is the output resistance which is Thevenin's equivalent.
11. The voltage source  $AV_{id}$  is an equivalent Thevenin's voltage source.
12. The output voltage is directly proportional to the difference between the two input voltages.
13. It has open-loop voltage gain of 1,00,000, input impedance of  $2 \text{ M}\Omega$ , and output impedance of  $75 \Omega$ .
14. Fig. 4.1.3 shows popular package style and the pin diagram.



**Fig. 4.1.3. Dual in line package.**

## PART-2

### Ideal and Practical Characteristics of Op-amp.

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 4.2.** Define Op-Amp with the help of block diagram. Also describe the equivalent circuit along with its ideal and practical characteristics.

**AKTU 2014-15(Sem-II), Marks 10**

**OR**  
**Define op-amp with the help of block diagram. Also draw its equivalent circuit. List the ideal characteristics of op-amp.**

**AKTU 2017-18(Sem-II), Marks 07**

**Draw the block diagram and equivalent circuit of an Op-Amp. Explain ideal characteristics of an Op-Amp.**

**AKTU 2015-16(Sem-II), Marks 7.5**

### Answer

**Op-Amp :** Refer Q. 4.1, Page 4-2D, Unit-4.

**Characteristics of Op-Amp in ideal and practical cases :**

S.No.	Characteristic	Ideal	Practical
1.	CMRR	$\infty$	$10^6$ or 120 dB
2.	Slew rate	$\infty$	$80 \text{ V}/\mu\text{sec}$
3.	Input resistance	$\infty$	$10^6 \Omega$
4.	Output resistance	0	$100 \Omega$
5.	Voltage gain $A_V$	$\infty$	$10^6$
6.	Bandwidth	$\infty$	$10^6 \text{ Hz}$
7.	Offset voltage	0	Negligible
8.	Offset current	0	Negligible

### PART-3

#### Differential Amplifier Circuit.

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 4.3.** Draw and explain the differential amplifier circuit.

**OR**

Analyse the differential amplifier with suitable circuit in two modes of operation.

**AKTU 2014-15(Sem-I), Marks 10**

**Answer**

1. The differential amplifier circuit has two separate inputs and two separate outputs and that the emitters are connected together.
2. It also consists of two separate voltage supplies.

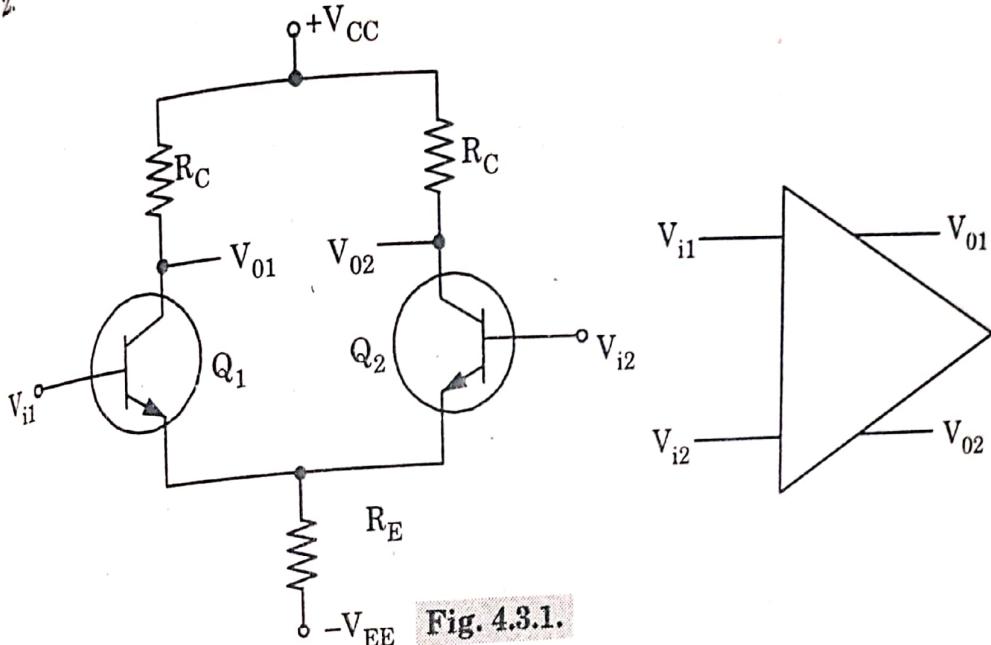


Fig. 4.3.1.

3. In differential amplifier circuit, the input signal operates both transistors in single-ended operation due to the common emitter connection, resulting in output from both collectors.
4. In double-ended operation, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.
5. In common-mode operation the common input signal results in opposite signals at each collector, these signals cancel each other so that the resulting output signal is zero.
6. The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs.
7. Let's consider DC bias operation of the differential amplifier circuit. With each base voltage at 0 V, the common emitter DC bias voltage is

$$V_E = 0 \text{ V} - V_{BE} = -0.7 \text{ V}$$

8. The emitter DC bias current is then,

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7 \text{ V}}{R_E}$$

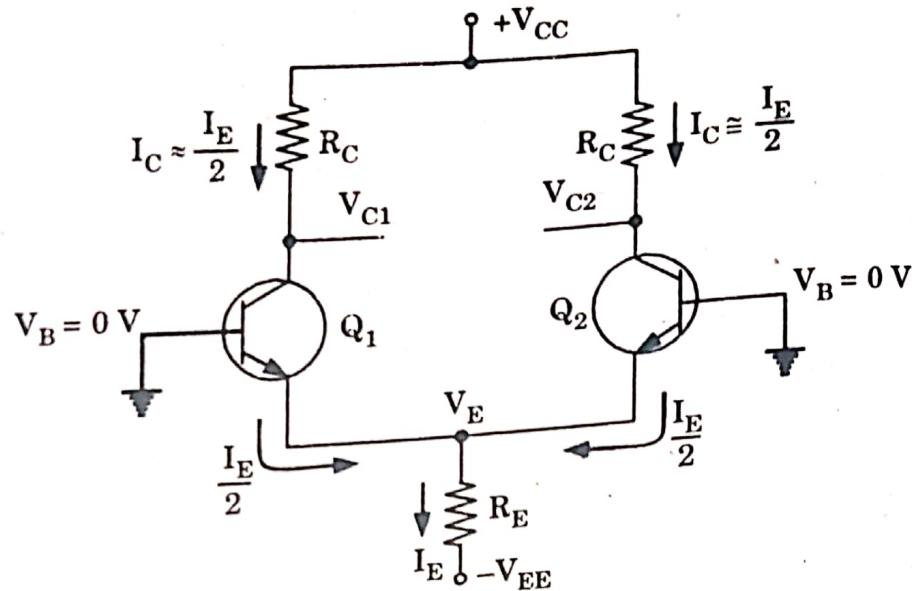


Fig. 4.3.2.

9. Assuming the transistors are well matched, we get

$$I_{C1} = I_{C2} = \frac{I_E}{2}$$

$\therefore$  Collector voltage,

$$V_{C1} = V_{C2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C$$

#### PART-4

*Practical Op-amp Circuits (Inverting Amplifier, Non-inverting Amplifier, Unity Gain Amplifier, Summing Amplifier, Integrator, Differentiator).*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 4.4.** Draw the circuit of an Op-Amp as voltage follower and find an expression for its voltage gain.

AKTU 2014-15(Sem-II), Marks 05

OR

Show that how input voltage gets reversed using operational amplifier ? And also derive the expression for voltage gain using inverting amplifier.

AKTU 2014-15(Sem-I), Marks 10

OR

Draw and derive relationship for op-amp as closed loop non-inverting amplifier circuit.

AKTU 2016-17(Sem-I), Marks 05

OR

Derive an expression for voltage gain of inverting and non-inverting ideal operational amplifier configurations.

AKTU 2017-18(Sem-I), Marks 07

**Answer****Inverting Op-Amp :**

- Fig. 4.4.1 shows the basic inverting amplifier with input resistance  $R_1$  and feedback resistance  $R_f$ .

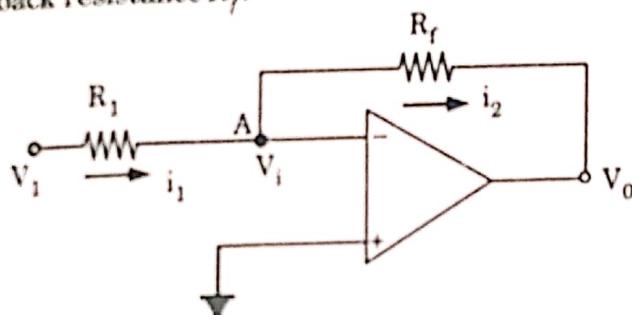


Fig. 4.4.1. Inverting amplifier.

- The current  $i_1$  flowing through  $R_1$  is given by,

$$i_1 = \frac{V_i - V_A}{R_1} = \frac{V_i}{R_1} \quad (\because V_A = 0 \text{ due to virtual ground})$$

and

$$i_2 = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$$

- At point A,

$$\frac{V_A}{R_1} = -\frac{V_o}{R_f}$$

$$A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

**Non-inverting amplifier :**

- The circuit for non-inverting amplifier is shown in Fig. 4.4.2.

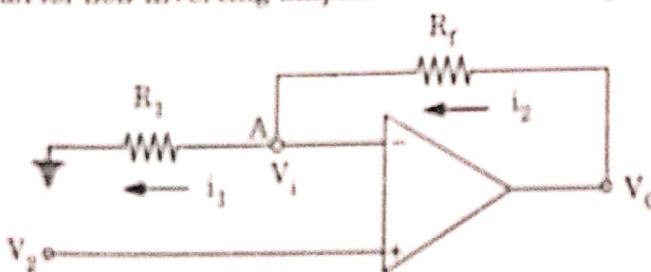


Fig. 4.4.2. Non-inverting amplifier.

- The currents  $i_1$  and  $i_2$  are given as :

**4-8 D (ESC-Sem-3 & 4)**

$$i_1 = \frac{V_2}{R_1} \text{ and } i_2 = \frac{V_0 - V_2}{R_f} \quad (\because V_i = V_2 \text{ due to virtual ground})$$

3. Applying KCL at point A,

$$(-i_1) + i_2 = 0 - \frac{V_2}{R_1} + \frac{V_0 - V_2}{R_f} = 0$$

$$\frac{V_0}{R_f} = \frac{V_2}{R_1} + \frac{V_2}{R_f} = V_2 \left( \frac{1}{R_1} + \frac{1}{R_f} \right)$$

$$\frac{V_0}{V_2} = \frac{R_1 + R_f}{R_1} = \left( 1 + \frac{R_f}{R_1} \right)$$

$$A_v = \left( 1 + \frac{R_f}{R_1} \right)$$

**Unity gain Op-Amp(Voltage Follower) :**

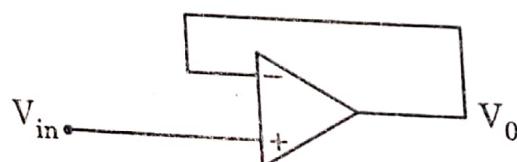
1. Fig. 4.4.3 represents unity gain Op-Amp where  $R_1 \rightarrow \infty$ .

$$A_v = 1$$

$$\frac{V_0}{V_{in}} = 1$$

$$V_0 = V_{in}$$

2. The voltage gain is unity and the output voltage follows the input voltage.



**Fig. 4.4.3.**

**Que 4.5.** Sketch a three input inverting summing circuit and derive an expression for the output voltage.

**OR**  
Explain summing amplifier using Op-amp.

**AKTU 2015-16(Sem-II), Marks 03**

**Answer**

**Adder or Summer amplifier circuit :**

1. Fig. 4.5.1 shows the three input summer circuit. This circuit provides a means of algebraically summing three input voltages, each multiplied by a constant gain factor.

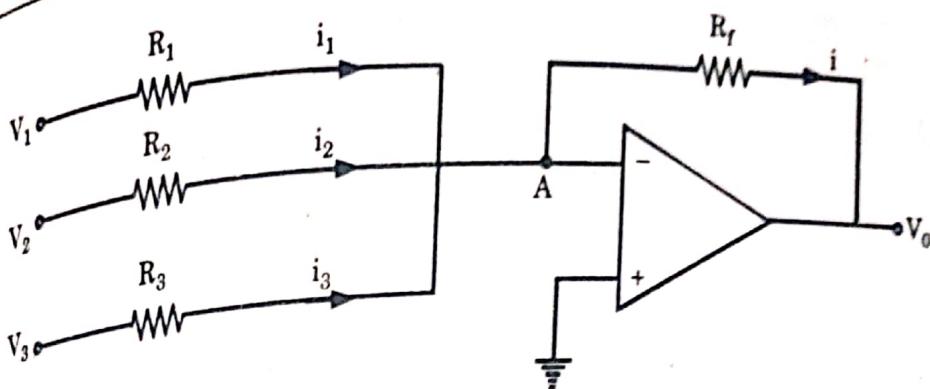


Fig. 4.5.1. Summer circuit.

2. At point A (virtual ground), the different currents are given as :  
 $i_1 = \frac{V_1}{R_1}, i_2 = \frac{V_2}{R_2}, i_3 = \frac{V_3}{R_3}$  and  $i = -\frac{V_0}{R_f}$

3. Applying KCL at point A, we get,

$$i_1 + i_2 + i_3 - i = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_0}{R_f} = 0$$

$$V_0 = - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

4. If  $R_1 = R_2 = R_3 = R$ , then

$$V_0 = - \frac{R_f}{R} [V_1 + V_2 + V_3]$$

5. Thus the output voltage is proportional to the algebraic sum of three input voltages.

Again, if  $R_f = R$ ,

$$V_0 = - [V_1 + V_2 + V_3]$$

**Que 4.6.** Calculate the output voltage for the circuit of Fig. 4.6.1

with inputs of  $V_1 = 40 \text{ mV rms}$  and  $V_2 = 20 \text{ mV rms}$ .

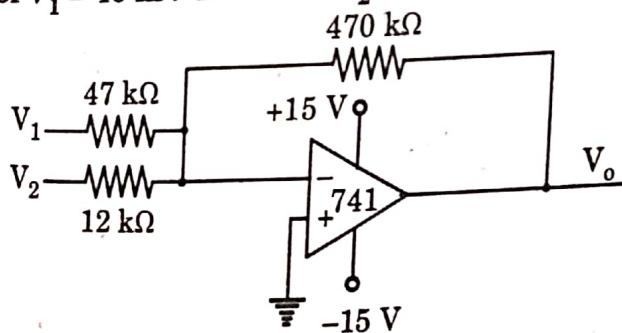


Fig. 4.6.1.

AKTU 2016-17(Sem-II), Marks 07

**Answer****Given :**

$$V_1 = 40 \text{ mV rms}, V_2 = 20 \text{ mV rms}, R_1 = 47 \text{ k}\Omega$$

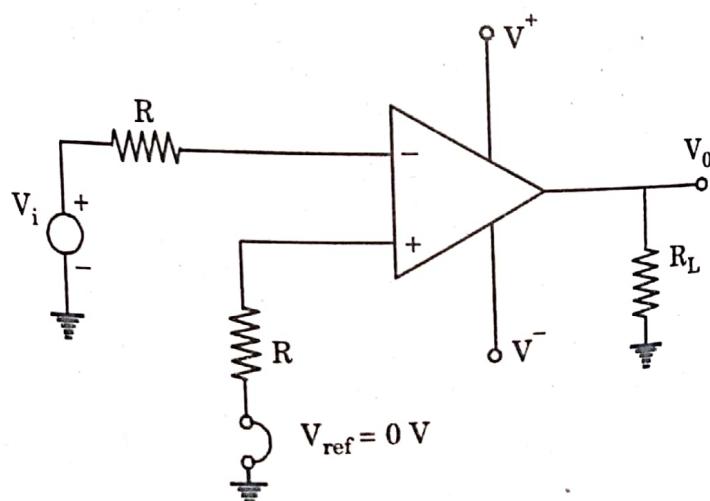
$$R_2 = 12 \text{ k}\Omega, R_f = 470 \text{ k}\Omega$$

**To find :  $V_0$** 

$$\begin{aligned} V_0 &= - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right] \\ &= - \left[ \frac{470}{47} \times 40 + \frac{470}{12} \times 20 \right] \\ &= - [400 + 783.3] = - 1183.33 \text{ mV rms} \\ &= - 1.18 \text{ V rms} \end{aligned}$$

**Que 4.7.** Explain zero crossing detector using OpAmp.**AKTU 2015-16(Sem-II), Marks 03****Answer**

The basic comparator can be used as a zero crossing detector when  $V_{ref}$  is set to zero. An inverting zero-crossing detector is shown in Fig. 4.7.1 and the output waveform for a sinusoidal input signal is shown in Fig. 4.7.2. The circuit is also called a sine-to-square wave generator.

**Fig. 4.7.1.**

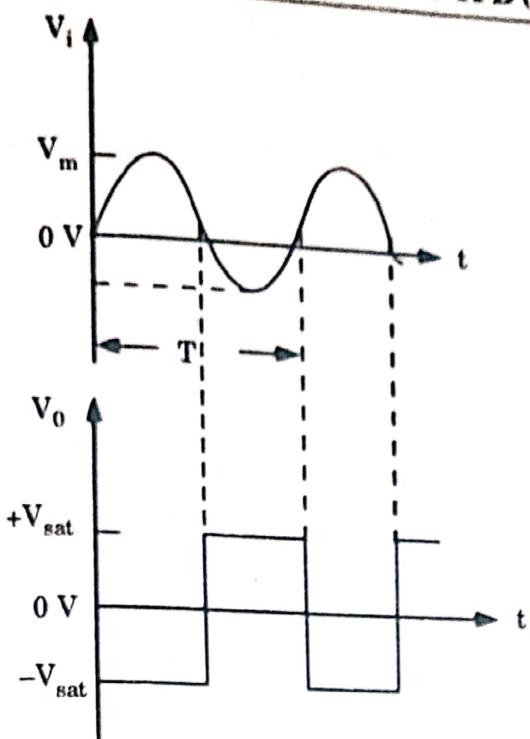


Fig. 4.7.2. Input and output waveforms.

**Que 4.8.** Explain with the help of necessary diagram :

- Inverting amplifier
- Integrator
- Differential amplifier in two modes of operation.

AKTU 2015-16(Sem-I), Marks 10

OR

Explain :

- Differentiator circuit using Op-Amp.
- Non-Inverting amplifier using Op-Amp.
- Differential amplifier using BJT with two modes of operation.

AKTU 2014-15(Sem-II), Marks 10

OR

Describe in detail account on integrator and differentiator with suitable circuit.

AKTU 2014-15(Sem-I), Marks 10

OR

Enlist the five ideal characteristics of Op-Amp. Draw an integrator circuit using Op-Amp.

AKTU 2013-14(Sem-II), Marks 05

OR

Draw and explain the circuit diagram for performing the following operation using Op-Amp (i) Integration (ii) Unit gain amplifier.

AKTU 2013-14(Sem-I), Marks 05

OR

**Explain integrator circuit using Op-amp.**

AKTU 2015-16(Sem-II), Marks 03

OR

**Explain how op-amp can be used as**

- Integrator**
- Inverting summer and**
- Voltage follower.**

AKTU 2017-18(Sem-I), Marks 07

OR

**Explain the operation of op-amp as integrator.**

AKTU 2017-18(Sem-II), Marks 3.5

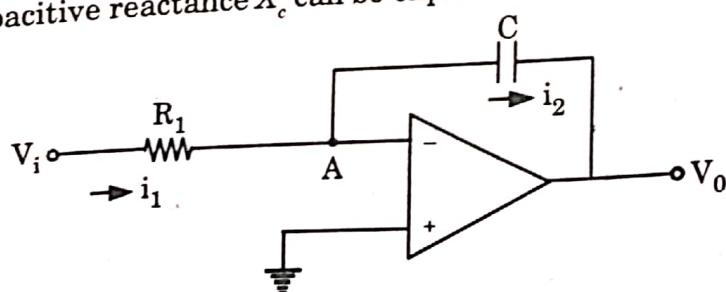
OR

**Draw the circuit diagram of an integrator using op-amp and explain its working.**

AKTU 2016-17(Sem-I), Marks 05

**Answer****Integrator :**

- The circuit of integrator is shown in Fig. 4.8.1.
- This circuit produces an output voltage which is proportional to the time integral of the input voltage. Due to this reason it is known as integrator.
- The integrator is an inverting Op-Amp in which feedback resistor  $R_f$  has been replaced by a capacitor  $C$ .
- Feedback through capacitor forces a virtual ground to exist at the inverting input terminal.
- The capacitive reactance  $X_C$  can be expressed as :

**Fig. 4.8.1.**

$$i_1 = \frac{V_1}{R_1} \text{ and } i_2 = \frac{d q_2}{dt} = C \frac{d(V_A - V_o)}{dt}$$

- At point A :  $i_1 = i_2$

$$\frac{V_1}{R_1} = -C \frac{d V_o}{dt}$$

$$d V_o = \frac{-1}{R_1 C} V_i dt$$

$$V_o(t) = - \frac{1}{R_1 C} \int V_i(t) dt$$

The above equation shows that the output is the integral of the input with an inversion and scale multiplier of  $1/R_1 C$ .

### Differentiator:

1. The function of a differentiator is to give an output voltage which is proportional to the rate of change of input voltage.
2. The circuit of a differentiator is shown in Fig. 4.8.2.
3. When we feed linearly increasing voltage to the differentiator, we get a constant DC output. So it is an inverse mathematical operation to that of an integrator.
4. At point A,  $V_1 = \frac{q}{C}$

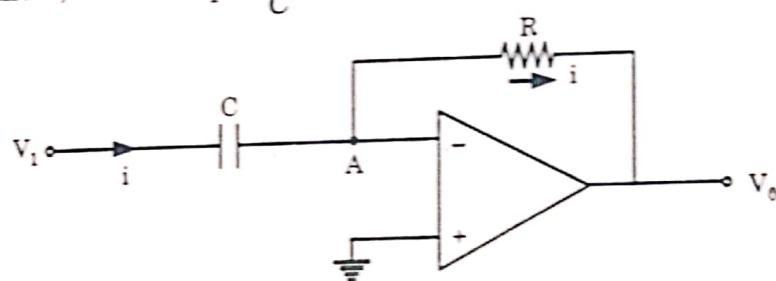


Fig. 4.8.2.

$$\frac{dV_1}{dt} = \frac{1}{C} \frac{dq}{dt} = \frac{i}{C} \quad \text{where } i = \frac{dq}{dt} \quad \dots (4.8.1)$$

$$V_o = -iR \quad \dots (4.8.2)$$

Put the value of  $i$  from eq. (4.8.1) in eq. (4.8.2)

$$V_o = -CR \frac{dV_1}{dt}$$

The above equation shows that the output voltage  $V_o$  is equal to a constant ( $-CR$ ) times the time derivative of the input voltage  $V_i$ .

**Unity gain amplifier (voltage follower) :** Refer Q. 4.4, Page 4-6D, Unit-4.

**Inverting amplifier and non-inverting amplifier :** Refer Q. 4.4, Page 4-6D, Unit-4.

**Differential amplifier :** Refer Q. 4.3, Page 4-4D, Unit-4.

**Ideal characteristics of Op-Amp :** Refer Q. 4.2, Page 4-3D, Unit-4.

**Inverting summer :** Refer Q. 4.5, Page 4-8D, Unit-4.

**Que 4.9.** Determine the output voltage for the given circuit shown in Fig. 4.9.1.

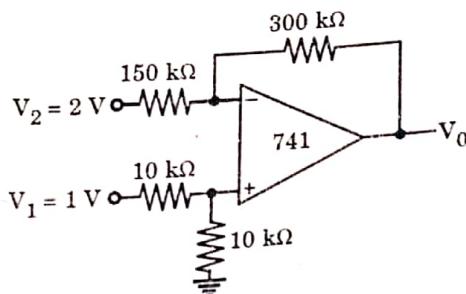


Fig. 4.9.1.

AKTU 2014-15(Sem-II), Marks 05

AKTU 2017-18(Sem-II), Marks 3.5

**Answer**

1. We can get  $V_0$  by superposition method,
2. Let  $V_1 = 1 \text{ V}$  and  $V_2$  is at ground, so output due to  $V_1$ ,  $V_{01}$ , will be due to input at non-inverting terminal,

$$\therefore V_{01} = \left(1 + \frac{300}{150}\right) \left(\frac{10}{(10+10)}\right) = \frac{1}{2} \times \frac{450}{150} = \frac{3}{2} = 1.5 \text{ V}$$

3. Let  $V_2 = 2 \text{ V}$  and  $V_1$  is at ground, so output due to  $V_2$ ,  $V_{02}$  will be due to input at inverting terminal,

$$V_{02} = -\frac{300}{150} \times 2 = -4 \text{ V}$$

4. Now total output,  $V_0 = V_{01} + V_{02}$   
 $V_0 = +1.5 - 4 = -2.5 \text{ V}$

**Que 4.10.** Determine the output voltage of an Op-Amp for input voltages of  $V_{i1} = 200 \text{ V}$  and  $V_{i2} = 140 \text{ V}$ . The amplifier has a differential gain of  $A_d = 6000$  and the value of CMRR is :

- i. 200
- ii.  $10^5$

AKTU 2015-16(Sem-I), Marks 05

**Answer**

Given :  $V_{i1} = 200 \text{ V}$ ,  $V_{i2} = 140 \text{ V}$ ,  $A_d = 6000$   
 To Find :  $V_o$ .

- For CMRR =  $200 = \frac{A_d}{A_{CM}}$   
 $V_o = A_d V_d + A_{CM} V_{CM}$

$$\begin{aligned}
 &= A_d(V_{i_1} - V_{i_2}) + \frac{A_d}{CMRR} \left( \frac{V_{i_1} + V_{i_2}}{2} \right) \\
 &= 6000(200 - 140) + \frac{6000}{200} \left( \frac{200 + 140}{2} \right) \\
 &= 365100 \text{ V} \\
 &= 36.51 \text{ kV}
 \end{aligned}$$

ii. For  $CMRR = 10^5 = \frac{A_d}{A_{CM}}$

$$\begin{aligned}
 V_o &= A_d V_d + A_{CM} V_{CM} \\
 &= 6000(200 - 140) + \frac{6000}{10^5} \left( \frac{200 + 140}{2} \right) \\
 &= 360010.2 \text{ V} \\
 &= 360 \text{ kV}
 \end{aligned}$$

**Que 4.11.** Find out the voltage  $V_2$  and  $V_3$  of the given network of Fig. 4.11.1.

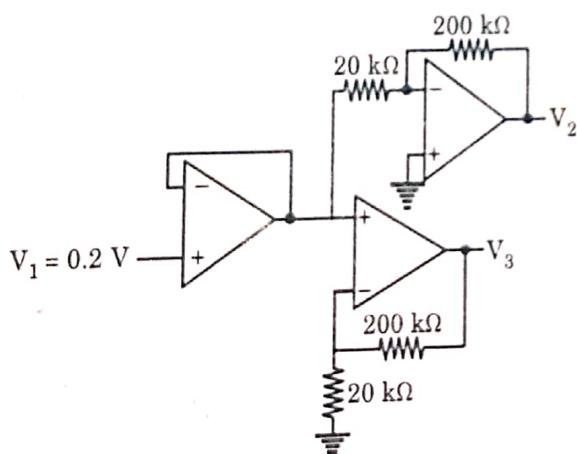


Fig. 4.11.1.

AKTU 2015-16(Sem-I), Marks 05

**Answer**

- Let  $V_A$  be the output of 1<sup>st</sup> Op-Amp.
- Thus,  $V_A = 0.2 \text{ V}$  ( $\because$  Unity gain follower)
- $V_2 = -\left(\frac{200 \text{ k}\Omega}{20 \text{ k}\Omega}\right) V_A = -10 \times 0.2 = -2 \text{ V}$
- $V_3 = \left(1 + \frac{200}{20}\right) V_A = 11 \times 0.2 = 2.2 \text{ V}$

**Que 4.12.** Determine the output voltage for the given Fig. 4.12.1.

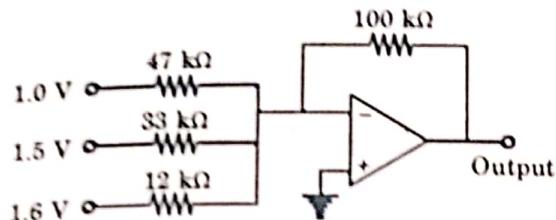


Fig. 4.12.1.

AKTU 2013-14(Sem-II), Marks 05

**Answer**

The output voltage of a summing amplifier is given by

$$\begin{aligned} V_o &= - \left[ \frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3 \right] \\ &= - \left[ \frac{100}{47} \times 1 + \frac{100}{33} \times 1.5 + \frac{100}{12} \times 1.6 \right] = -20.01 \text{ V} \end{aligned}$$

**Que 4.13.** Find the output voltage for the given Fig. 4.13.1.

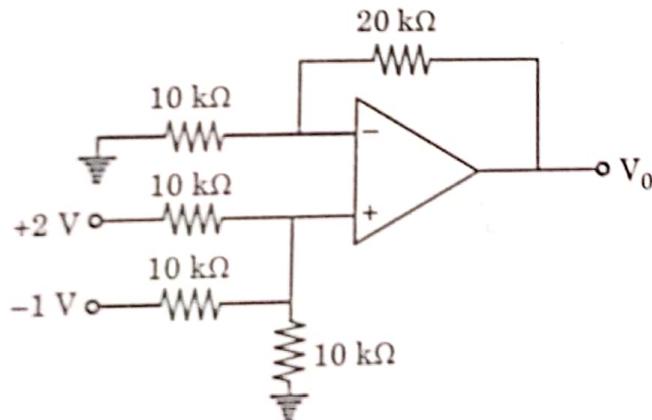


Fig. 4.13.1.

AKTU 2013-14(Sem-I), Marks 05

**Answer**

1. This circuit will be solved using superposition principle.
2. Considering only + 2 V voltage source :

$$V'_o = \left( 1 + \frac{20}{10} \right) V'_1 = (1+2) \left( \frac{5 \times 2}{10+5} \right) = 2 \text{ V}$$

3. Considering only - 1 V voltage source :

$$V''_o = \left( 1 + \frac{20}{10} \right) V''_1 = (1+2) \left( \frac{5 \times -1}{10+5} \right) = -1 \text{ V}$$

4. Total output voltage,  $V = V_0 + V_0' = 2 - 1 = 1 \text{ V}$

**Que 4.14.** Design and draw an inverting amplifier using op-amp with a gain of  $-5$  and  $R_i = 10 \text{ k}\Omega$ . **AKTU 2016-17(Sem-I), Marks 05**

**Answer**

Gain,

$$A_v = -5$$

$$R_i = 10 \text{ k}\Omega$$

$$\therefore A_v = \frac{-R_f}{R_i} = -5$$

$$\therefore R_f = 5 \times R_i = 5 \times 10 = 50 \text{ k}\Omega$$

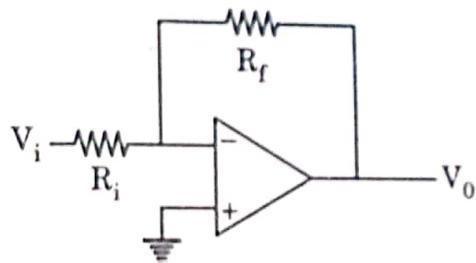


Fig. 4.14.1.

**Que 4.15.** Calculate the output voltage  $V_0$  of the circuit.

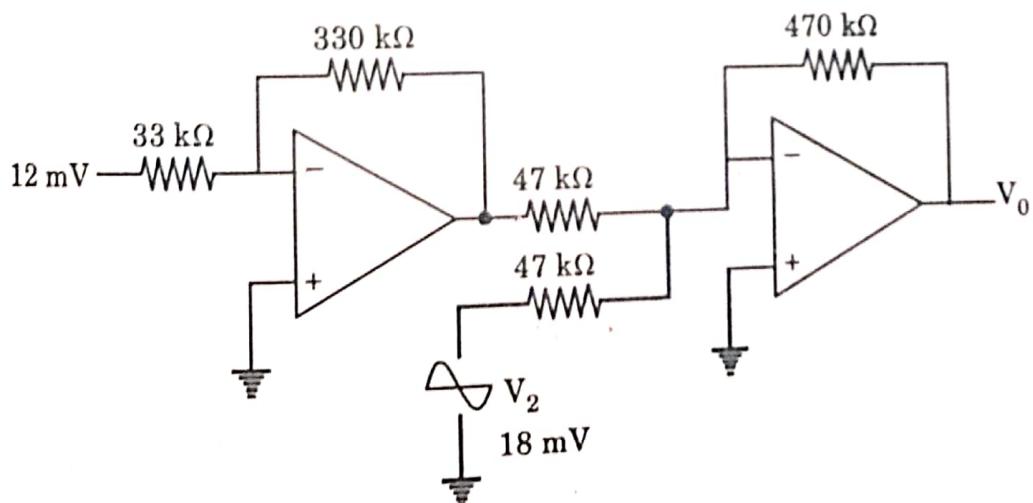


Fig. 4.15.1.

**AKTU 2017-18(Sem-I), Marks 3.5**

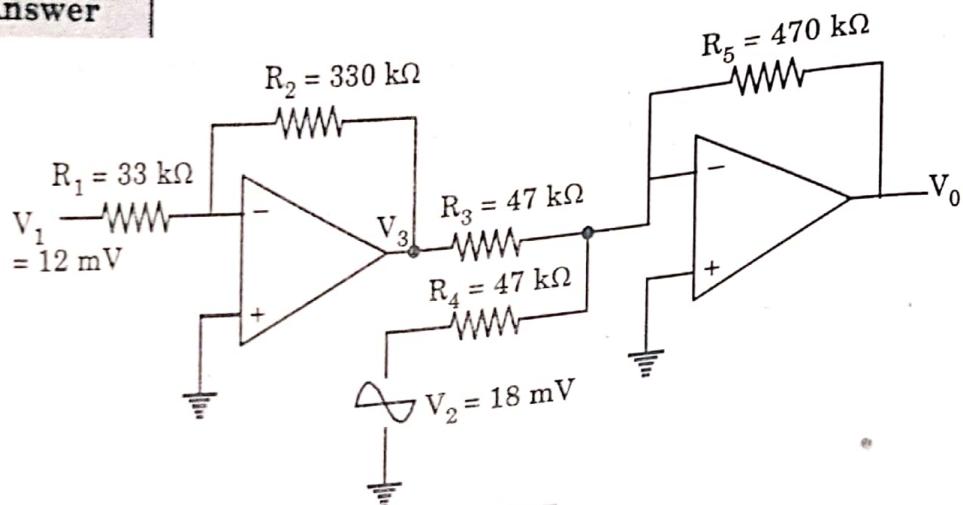
**Answer**

Fig. 4.15.2.

$$\begin{aligned}
 V_3 &= -\left(\frac{R_2}{R_1}\right)V_1 = \frac{-330}{33} \times 12 \text{ mV} = -120 \text{ mV} \\
 \text{Now } V_0 &= -\left(\frac{R_5}{R_3}V_3 + \frac{R_5}{R_4}V_2\right) \\
 &= -\left[\frac{470}{47} \times (-120) + \frac{470}{47} \times 18\right] \\
 &= -[-1200 + 180] = 1020 \text{ mV} \\
 V_0 &= 1.02 \text{ V}
 \end{aligned}$$

**PART-5**

*Op-amp Parameters : Input Offset Voltage, Output Offset Voltage, Input Biased Current, Input Offset Current, Differential and Common-mode Operation*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 4.16.** Explain the basic parameters of Op-amp.

**OR**

Explain the following characteristics of an op-amp :

- i. CMRR
- ii. Slew rate

**AKTU 2017-18(Sem-I), Marks 3.5**

**OR**  
**Draw and explain the differential amplifier. Define CMRR and slew rate in op-amp.**

**AKTU 2016-17(Cem-II), Marks 5.25**

**Answer**

**Differential amplifier :** Refer Q. 4.3, Page 4-4D, Unit-4.

1. **Input bias current :** The input bias currents  $I_{B1}$  and  $I_{B2}$  are the base bias currents of the two transistors in the input differential amplifier stage of the Op-Amp. An input bias current  $I_B$  is defined as the average of the two input bias currents  $I_{B1}$  and  $I_{B2}$  that is

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where,

$I_{B1}$  = DC bias current flowing into the inverting input

$I_{B2}$  = DC bias current flowing into the non-inverting input.

2. **Input offset current and voltage :**

- i. **Input offset current :** The input offset current,  $I_{io}$  is defined as the algebraic difference between two input bias currents  $I_{B1}$  and  $I_{B2}$

i.e.,  $I_{io} = |I_{B1} - I_{B2}|$

The value of  $I_{io}$  indicates the maximum amount by which the input bias current may differ.

- ii. **Input offset voltage :** Input offset voltage,  $V_{io}$  is the differential input voltage that exists between two input terminals of an Op-Amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero.

3. **Slew rate (SR) :** It is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro-second i.e.,

$$SR = \left. \frac{dv_o}{dt} \right|_{max} \text{ V/}\mu\text{sec}$$

Slew rate indicates how rapidly the output of Op-Amp can change in response to change in input frequency.

4. **CMRR (common-mode rejection ratio) :** It is an ability to reject the common mode noise which is present at both the inverting and non-inverting terminal.

$$CMRR = 20 \log \left| \frac{A_d}{A_{CM}} \right|$$

**Que 4.17.** For an input of  $V_i = 50 \text{ mV}$  in the circuit of Fig. 4.17.1,

determine the maximum frequency that may be used. The Op-Amp slew rate  $SR = 0.4 \text{ V/s}$ .

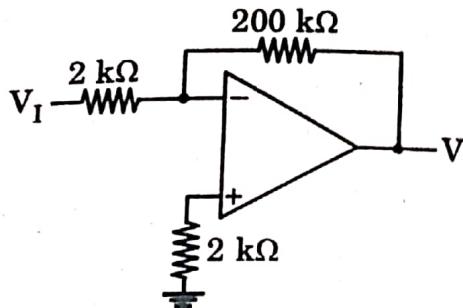


Fig. 4.17.1.

AKTU 2015-16(Sem-I), Marks 05

**Answer**

**Given :**  $R_f = 200 \text{ k}\Omega$ ,  $R_1 = 2 \text{ k}\Omega$ ,  $V_I = 50 \text{ mV}$ ,  $SR = 0.4 \text{ V/s}$

**To Find :**  $f_{max}$ .

$$1. \quad A_{CL} = \left| \frac{R_f}{R_1} \right| = \frac{200 \text{ k}\Omega}{2 \text{ k}\Omega} = 100$$

$$2. \quad \text{Output gain factor, } K = A_{CL} V_I = 100 \times 50 \times 10^{-3} = 5 \text{ V}$$

$$3. \quad \text{Maximum signal frequency} = \frac{SR}{2\pi K} = \frac{0.4}{2\pi(5)} = 0.012 \text{ Hz}$$

**VERY IMPORTANT QUESTIONS**

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

**Q. 1.** Define Op-Amp with the help of block diagram. Also describe the equivalent circuit along with its ideal and practical characteristics.

**Ans.** Refer Q. 4.2.

**Q. 2.** Draw and explain the differential amplifier circuit.

**Ans.** Refer Q. 4.3.

**Q. 3.** Draw the circuit of an Op-Amp as voltage follower and find an expression for its voltage gain.

**Ans.** Refer Q. 4.4.

**Q.4. Explain with the help of necessary diagram:**

a. Inverting amplifier

b. Integrator

c. Differential amplifier in two modes of operation.

**Ans.** Refer Q. 4.8.

**Q.5. Determine the output voltage for the given circuit shown in Fig. 1.**

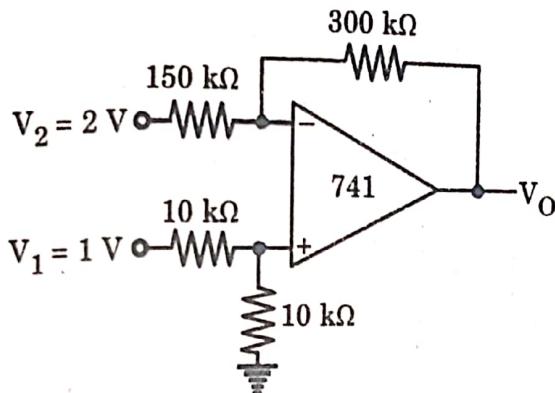


Fig. 1.

**Ans.** Refer Q. 4.9.

**Q.6. Determine the output voltage for the given Fig. 2.**

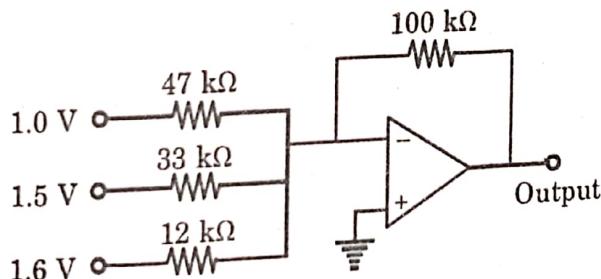


Fig. 2.

**Ans.** Refer Q. 4.12.

**Q.7. Explain the basic parameters of Op-amp.**

**Ans.** Refer Q. 4.16.





## Operational Amplifier (2 Marks Questions)

**4.1. List of ideal characteristics of op-amp.**

**AKTU 2017-18(Sem-I), Marks 02**

**OR**

**Write the characteristics of an ideal op-amp.**

**AKTU 2016-17(Sem-I), Marks 02**

**Ans:**

1. Input impedance is infinite.
2. Output impedance is zero.
3. Infinite CMRR.
4. Bandwidth is infinite.
5. Open loop gain is infinite.

**4.2. Define CMRR, slew rate of Op-Amp.**

**AKTU 2015-16(Sem-I), Marks 02**

**Ans:**

1. **CMRR :** The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio CMRR. CMRR is defined as the ratio of the differential voltage gain  $A_d$  to the common mode voltage gain  $A_{cm}$  i.e.,

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right|$$

2. **Slew rate (SR) :** It is defined as the maximum rate of change of output voltage per unit time and is expressed in volts per micro-second i.e.,

$$\text{SR} = \left| \frac{dV_o}{dt} \right|_{\max} \text{ V}/\mu\text{s}$$

Slew rate indicates how rapidly the output of Op-Amp can change its response to change in input frequency.

**4.3. What do you understand by single-ended and double-ended operations of Op-Amp ?**

**Ans.** If an input signal is applied to either input with the other input grounded, the operation is referred to as single-ended.  
If two opposite polarity input signals are applied, the operation is referred to as double ended.

#### 4.4. Define Op-Amp and draw its block diagram.

AKTU 2015-16(Sem-I), Marks 02

**Ans.** **Op-Amp :** Operational amplifier is designed to perform various mathematical operations such as addition, subtraction, integration, differentiation etc.

##### Block diagram :

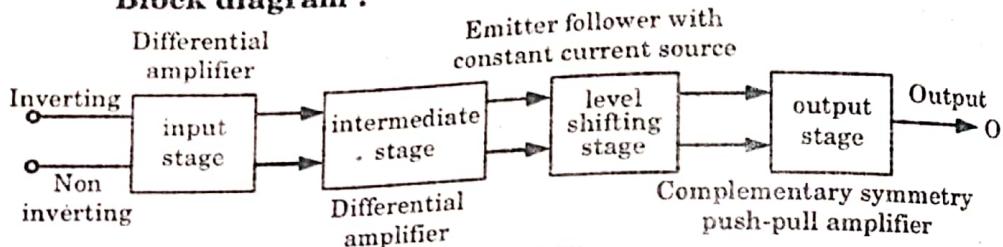


Fig. 4.4.1.

#### 4.5. Define cut off frequency and give the relation between unity gain frequency and cut off frequency.

**Ans.** Cut off frequency is defined as the frequency at which the gain drops by 3 db (or to 0.707 the DC gain,  $A_{VD}$ ) and it is denoted by  $f_c$ . Relation between unity gain frequency ( $f_1$ ) and cut off frequency ( $f_c$ ) is given by

$$f_1 = A_{VD} f_c$$

where  $A_{VD}$  = Voltage differential gain or DC gain.

#### 4.6. An operational amplifier has a differential gain of $10^3$ and a CMRR of 100, input voltages are $120 \mu V$ and $80 \mu V$ . Determine the output voltage.

AKTU 2013-14(Sem-I), Marks 02

AKTU 2017-18(Sem-I), Marks 02

**Ans.**

Given : CMRR = 100,  $A_d = 10^3$ ,  $V_1 = 120 \mu V$ ,  $V_2 = 80 \mu V$   
To Find :  $V_o$

$$\text{We know, CMRR} = \frac{A_d}{A_{cm}}$$

$$A_{cm} = \frac{10^3}{100} = 10$$

$$\begin{aligned}
 \text{Output voltage} &= A_d V_d + A_{cm} V_c \\
 &= 10^3 (V_1 - V_2) + 10 \left( \frac{V_1 + V_2}{2} \right) \\
 &= 10^3 (120 - 80) \times 10^{-6} + 10 \left( \frac{120 + 80}{2} \right) \times 10^{-6} \\
 &= 40 \times 10^{-3} + 10^{-3} = 41 \text{ mV}
 \end{aligned}$$

- 4.7. Sketch the circuit of op-amp as an integrator and differentiator.

AKTU 2017-18(Sem-II), Marks 02

OR

Derive the circuit of integrator using an ideal op-amp.

AKTU 2016-17(Sem-II), Marks 02

**Ans:** Integrator :

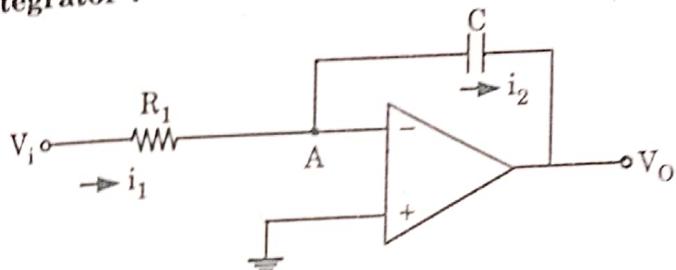


Fig. 4.7.1.

Differentiator :

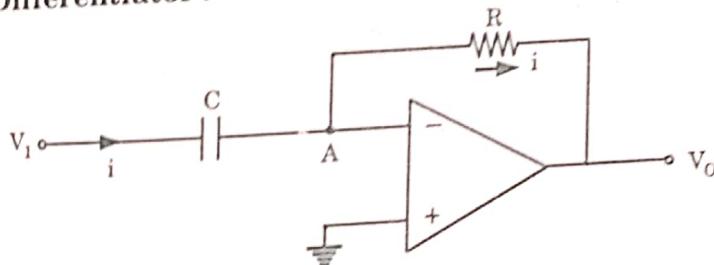


Fig. 4.7.2.

- 4.8. Determine the cut-off frequency of an Op-Amp having specified value  $B_1 = 1 \text{ MHz}$  and  $A_{VD} = 20 \text{ V/mV}$ .

**Ans:**

Given :  $f_1 = B_1 = 1 \text{ MHz}$ ,  $A_{VD} = 20 \text{ V/mV}$

Find :  $f_c$

Cut-off frequency,

$$f_c = \frac{f_1}{A_{VD}}$$

where,  $f_1$  = Unity gain frequency

$A_{VD}$  = Voltage differential gain

$$f_c = \frac{1 \times 10^6}{200 \times 10^3} = 5 \text{ Hz}$$

- 4.9. For an Op-Amp having a slew rate of  $SR = 2 \text{ V}/\mu\text{s}$ , what is the maximum closed loop voltage gain that can be used when the input varies by  $0.5 \text{ V}$  in  $10 \mu\text{s}$  ?

Ans. Closed loop gain,

$$A_{CL} = \frac{SR}{\Delta V_i / \Delta t} = \frac{2 \text{ V}/\mu\text{s}}{0.5 \text{ V}/10 \mu\text{s}}$$

$$A_{CL} = 40$$

- 4.10. How voltage follower is used for impedance matching applications ?

Ans. Voltage follower offers very high input impedance of the order of  $M\Omega$  and very low output impedance. Thus this circuit draws negligible current from the source. Thus the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

- 4.11. Draw the output waveform that will appear across  $R_L$ .

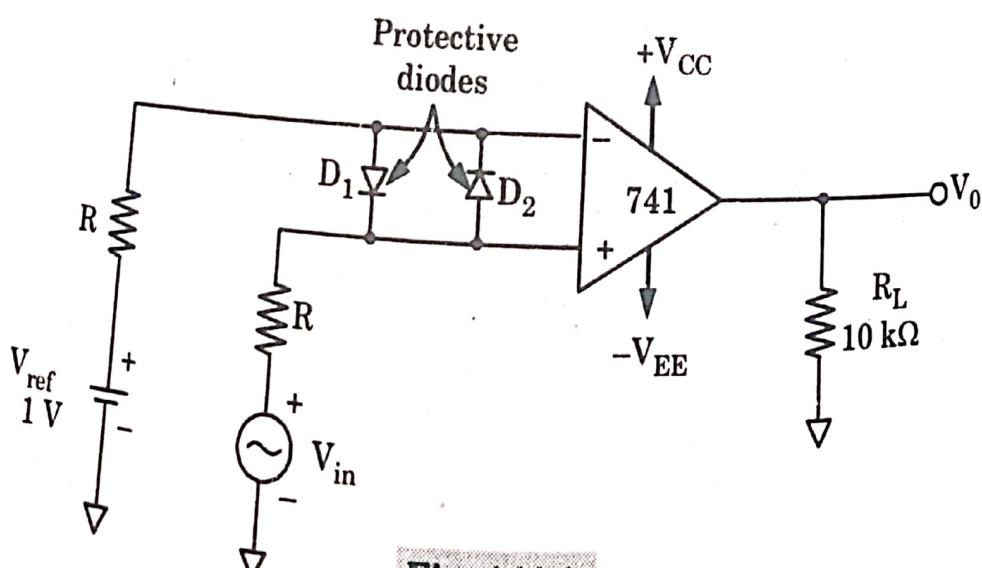


Fig. 4.11.1.

AKTU 2015-16(Sem-II), Marks 02

Ans.

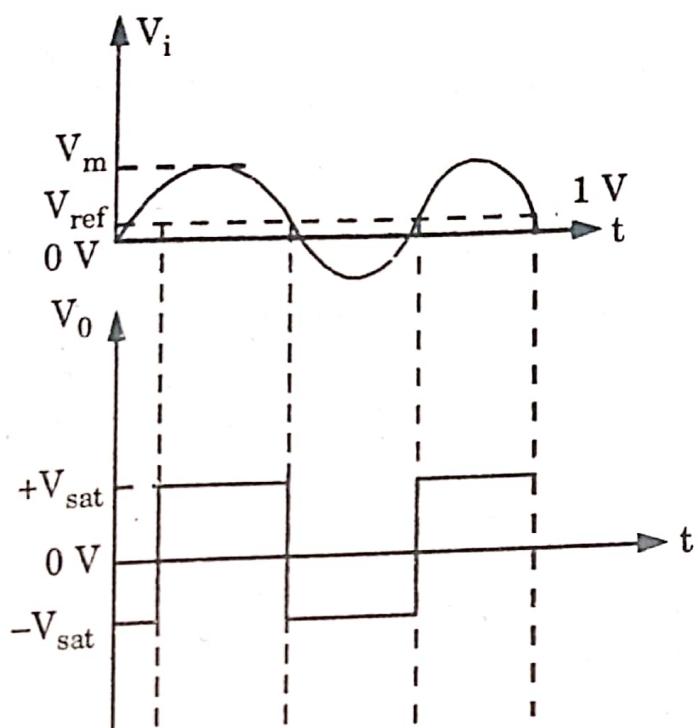


Fig. 4.11.2.

- 4.12. An operational amplifier has differential gain of  $10^2$  and CMRR of 80 dB, input voltage are 100 microampere and 60 microampere. Determine output voltage.

AKTU 2016-17(Sem-I), Marks 02

**Ans.** The procedure is same as Q. 4.6, Page SQ-17D, Unit-4, 2 Marks Questions.

**Ans.** Output voltage,  $V_o = 4 \text{ mV}$ .



50

UNIT



# Electronic Instrumentation and Measurements

## CONTENTS

- Part-1 :** Digital Voltmeter : Introduction ..... **5-2D to 5-5D**
- Part-2 :** Ramp Techniques, Digital ..... **5-5D to 5-9D**  
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Current, Phase and  
Frequency Using CRO
- Part-7 :** Introduction of Digital Storage ..... **5-19D to 5-21D**  
Oscilloscope and Comparison  
of DSO with Analog Oscilloscope

**PART- 1***Digital Voltmeter : Introduction.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 5.1.** Explain the basic principle of digital voltmeter with the help of block diagram. What are the characteristics of DVM ?

**AKTU 2014-15(Sem-II), Marks 10**

**OR**

Explain the basic principle of digital voltagemeter.

**AKTU 2013-14(Sem-II), Marks 05**

**OR**

Explain the characteristics of digital voltmeter system.

**AKTU 2015-16(Sem-II), Marks 10**

**Answer****Digital Voltmeter :**

1. Digital voltmeter (DVM) is an indicating device. The main use of DVM is to measure voltage between two points. It displays DC or AC voltage as discrete numerals.
2. It is a useful laboratory instrument for several applications. It is also a useful building block of digital instrumentation systems. The DVM is often used in data processing system.
3. An ideal voltmeter has an infinite high input resistance so that it does not draw any current from the circuit.
4. Consider a meter which has a low input resistance of  $1000\ \Omega$ . It cannot give an accurate value of the voltage across a resistance of the same magnitude because the meter shunts the resistance.
5. Therefore, it is important to measure the loading effect of a voltmeter in terms of ohms per volt.
6. The block diagram of a digital voltmeter is shown in Fig. 5.1.1. It has three stages :
  - a. Signal preparation,
  - b. Analog to digital conversion, and
  - c. Display unit.

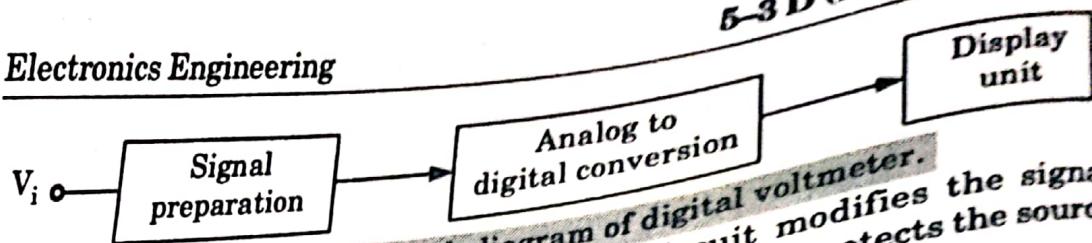


Fig. 5.1.1. Block diagram of digital voltmeter.

7. The signal preparation stage or input circuit modifies the signal amplitude according to the requirement and it also protects the source from loading.
8. Here, resistive attenuator is used to decrease the large incoming signal and amplifier is used to amplify the small incoming signal to the measurable range.
9. Digital voltmeters are essentially analog to digital converters with digital displays to indicate the measured voltage.
10. Digital voltmeter can be categorised as follows :

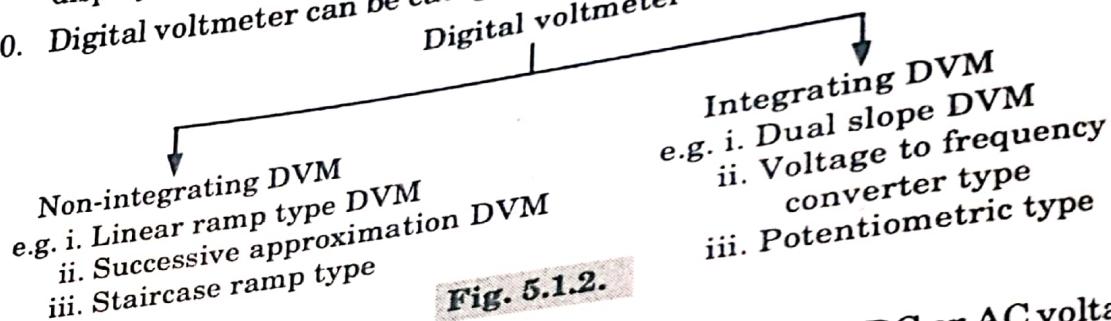


Fig. 5.1.2.

**General characteristics :**

1. The digital voltmeter (DVM) displays measurement of DC or AC voltage as discrete numerals.
2. This is advantageous in many applications because it reduces human reading and interpolation errors, increases reading speed and provides output in digital form.
3. DVM has following typical operating and performance features :
  - a. **Input range :** From  $\pm 1 \mu\text{V}$  to  $\pm 1,000.00 \text{ V}$  with automatic range selection and overload indication.
  - b. **Absolute accuracy :** As high as  $\pm 0.005\%$  of reading.
  - c. **Resolution :** 1 part in  $10^6$  ( $1 \mu\text{V}$  can be read on  $1 \text{ V}$  input range).
  - d. **Input characteristics :** Input resistance typically  $10 \text{ M}\Omega$  and input capacitance  $40 \text{ pF}$ .

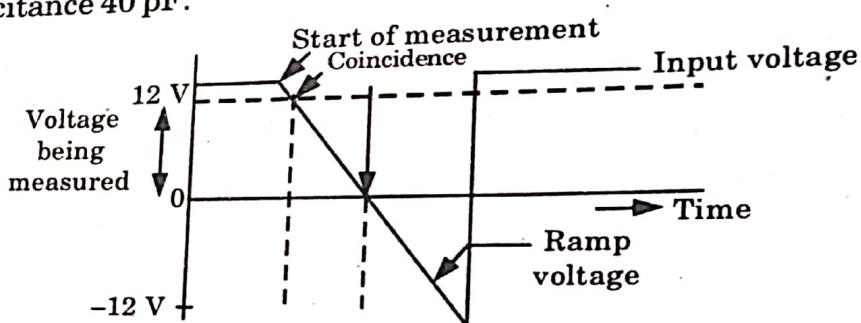


Fig. 5.1.3. Voltage to time conversion using gated clock pulses.

**Que 5.2.** Explain with the help of neat diagram, working and characteristics curve of ramp type digital voltmeter.

AKTU 2015-16(Sem-I), Marks 10

OR

Explain the functioning of a ramp type digital voltmeter.

AKTU 2014-15(Sem-I), Marks 10

OR

Using a suitable circuit diagram, explain the basic principle of a ramp type digital voltage meter.

AKTU 2013-14(Sem-I), Marks 05

OR

Draw and explain the block diagram of a ramp-type digital voltmeter (DVM).

AKTU 2017-18(Sem-I), Marks 07

OR

Draw and explain the block diagram of ramp type digital voltmeter. Also draw related voltage to time conversion waveforms.

AKTU 2016-17(Sem-II), Marks 07

### Answer

1. The operating principle of the ramp type DVM is based on the measurement of the time it takes for a linear ramp voltage to rise from 0 V to the level of the input voltage, or to decrease from input voltage level to zero.

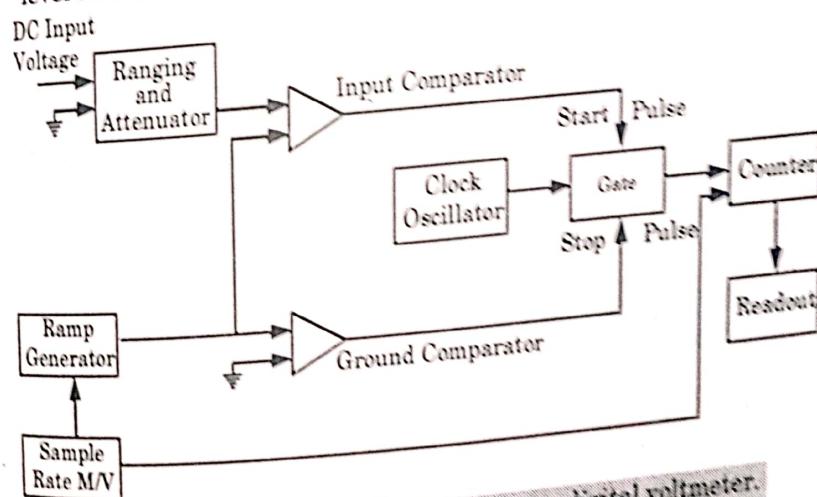
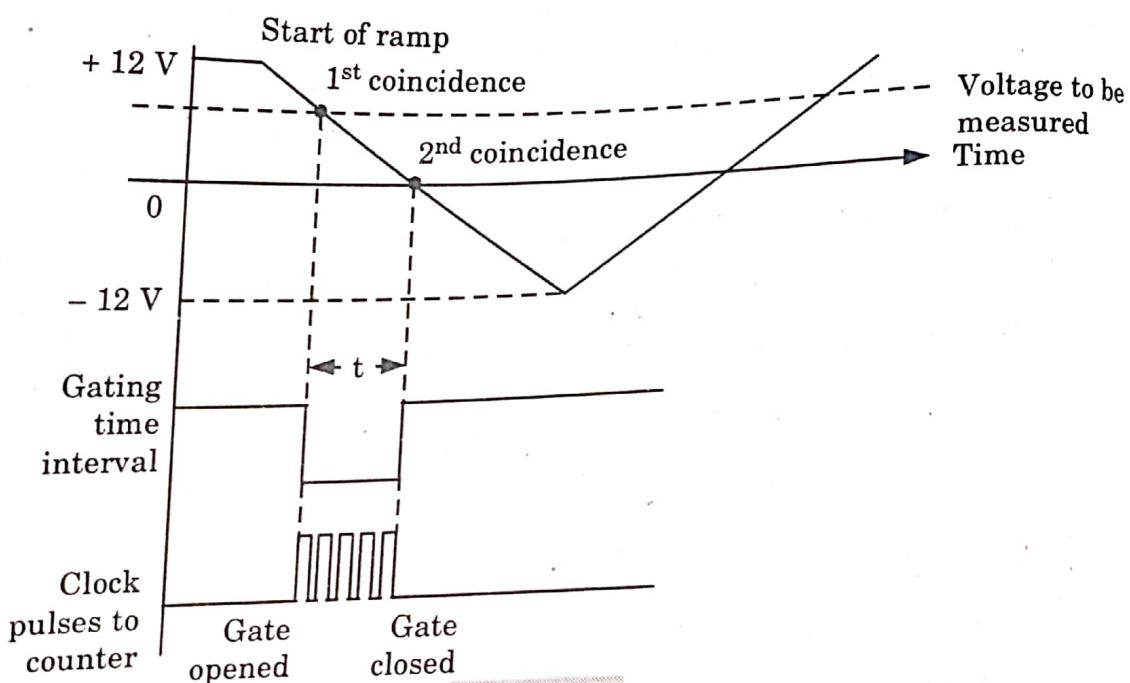


Fig. 5.2.1. Block diagram of a ramp type digital voltmeter.

2. At the start of the measurement cycle, a ramp voltage is initiated, this voltage can be positive going or negative going. The negative going ramp is compared with input voltage (unknown).

3. At the instant the ramp voltage equals the unknown voltage, comparator circuit generates a pulse which opens a gate. This gate is shown in Fig. 5.2.1.
4. The ramp voltage continues to decrease with time until it finally reaches 0 V (or ground potential) and a second comparator generates an output pulse which closes the gate.
5. An oscillator generates clock pulses which are allowed to pass through the gate to a number of decade counting units (DCUs) which totalize the number of pulses passed through the gate.
6. The decimal number, displayed by indicator tubes associated with the DCUs is a measure of the magnitude of the input voltage.

**Characteristic curve :**



**Fig. 5.2.2.**

**PART-2**

*Ramp Techniques, Digital Multimeter : Introduction.*

**Questions-Answers**

**Long Answer Type and Medium Answer Type Questions**

**Que 5.3.** Explain working principle of digital multimeter with the help of suitable block diagram.

**AKTU 2014-15(Sem-II), Marks 05**

**OR**

Enumerate with block diagram, various elements involved in digital multimeter to measure the various range of voltage and current.

**AKTU 2014-15(Sem-I), Marks 10****OR**

Using a suitable diagram, explain the basic principle of multimeter and enlist the applications of multimeter.

**AKTU 2013-14(Sem-II), Marks 05****OR**

Write the basic principle of a multimeter.

**AKTU 2013-14(Sem-I), Marks 05****OR**

Explain the basic principle of digital multimeter.

**AKTU 2016-17(Sem-I), Marks 05**

Using suitable diagram explain the basic principle of digital multimeter (DMM). Also list its applications.

**AKTU 2017-18(Sem-II); Marks 07****OR**

Explain with block diagram how DMM can measure AC and DC signals and various other electrical parameters ?

**AKTU 2017-18(Sem-I), Marks 07****Answer**

1. The digital multimeter is extensively used in laboratories and industries. The block diagram of a digital multimeter is shown in Fig. 5.3.1.
2. The instrument used to measure AC/DC voltage or AC/DC current or value of resistance is known as multimeter.
3. In a typical DMM, the input signal, the AC or DC voltage, current, resistance or any other parameter such as temperature, is converted to a DC voltage within the range of the ADC.
4. The ADC then converts the pre-scaled DC voltage into its equivalent digital number, which will be displayed on the display unit.
5. A digital control block, sometimes implemented using a microprocessor or a microcontroller, manages the flow of information within the instrument, coordinating all internal functions as well as transferring information to external devices such as printers or personal computers via industry standard interfaces.

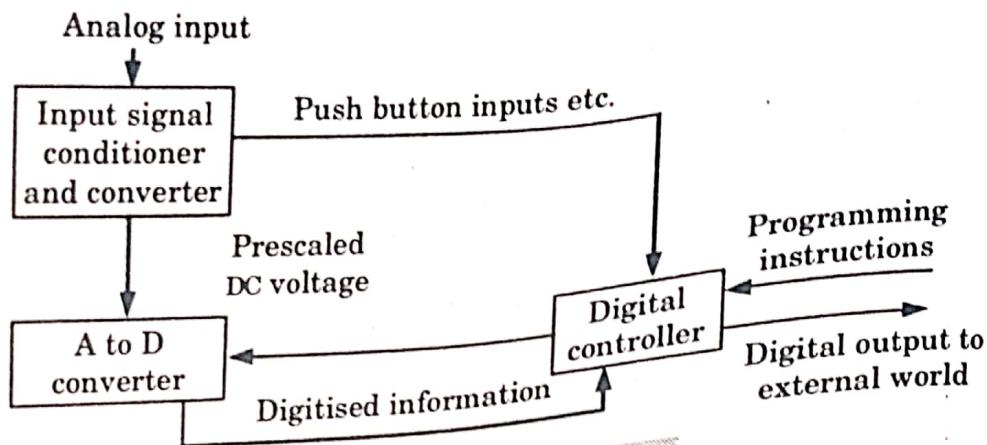


Fig. 5.3.1. Digital multimeter.

**Measurement of voltage :** The DVM for the measurement of voltage has already been discussed in previous question.

#### Measurement of current :

1. For the measurement of current either AC or DC, a series of current sensing resistors are used.
2. The current to be measured is passed through one of the sensing resistors as shown in Fig. 5.3.2.

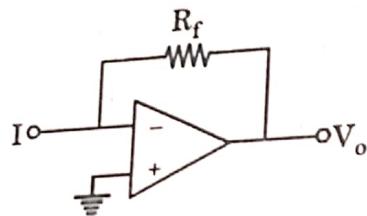


Fig. 5.3.2.

3. The output voltage is given by

$$V_o = -IR_f$$

4. The output voltage is proportional to unknown current  $I$ .

Here  $R_f$  is known resistance.

#### Measurement of resistance :

1. For the measurement of resistance with DMM, a scale changer is used. A scale changer is shown in Fig. 5.3.3.

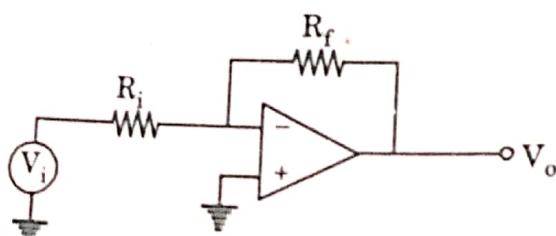


Fig. 5.3.3.

2. The output voltage of scale changer is given by

$$V_o = \frac{-R_f}{R_i} V_i$$

- where  $V_i$  and  $R_i$  are known parameters and  $R_f$  is unknown resistance.  
3. The output voltage is proportional to unknown resistance  $R_f$  is applied to the digital voltmeter section of DMM. The value of unknown resistance  $R_f$  is displayed.

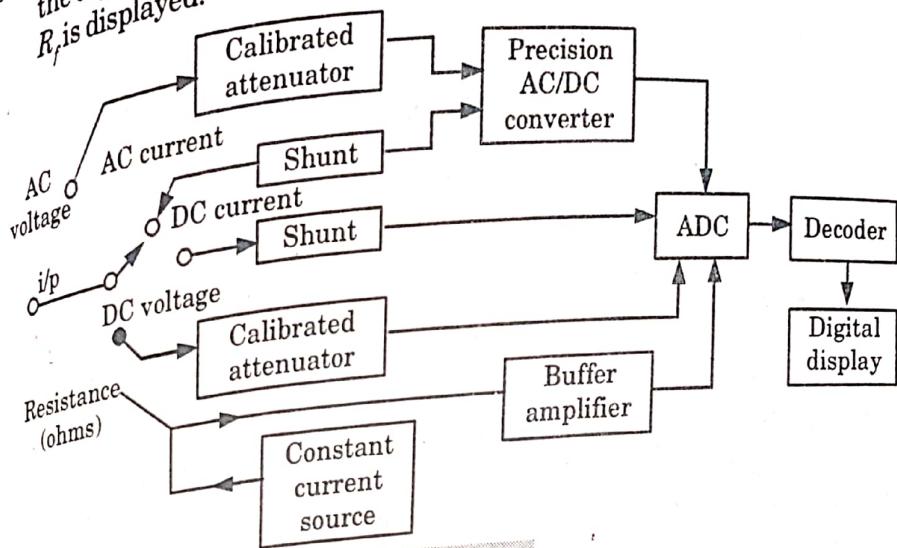


Fig. 5.3.4.

**Functions of digital multimeter :** Measurement of voltage, current and resistances.

#### i. Multimeter as voltmeter :

- In AC voltage mode, the applied AC input voltage is fed through a calibrated, compensated attenuator, here the voltage is attenuated to a suitable level which is accepted by succeeding stages.
- This attenuated voltage is converted into DC by a suitable precision AC to DC converter.
- This DC is fed to ADC and the subsequent decoder and display system which displays the output in numerical form.

#### ii. Multimeter as ammeter :

- The current is applied to the shunt and drop across an internal calibrated shunt is measured directly by ADC in the DC current mode.
- Due to the lack of precision in AC/DC conversion, the accuracy in the AC ranges is in general of the order of 0.2 to 0.5 %.

#### iii. Multimeter as an ohmmeter :

- Digital multimeter operates by measuring the voltage across the externally connected unknown resistance, resulting from a current forced through it from a calibrated internal source.
- The accuracy of resistance measurement is of the order of 0.1 to 0.5 % depending on the accuracy and stability of the internal current source.

**Applications of Digital multimeter :**

- For checking circuit continuity.
- Measurement of DC voltage across various resistor in electronic circuit.
- Measurement of AC voltage across power supply transformer.
- For ascertaining whether or not open or short circuit exists in the circuit under study.

**PART-3**

*Oscilloscope : Introduction, Basic Principle.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 5.4.** What is CRO ? Explain its basic principle.

**Answer**

- The Cathode Ray Oscilloscope (CRO) is an electronic device which gives a visual indication of a signal waveform.
- It is widely used for trouble-shooting radio and television receivers as well as for laboratory work.
- It can also be used for measuring voltage, frequency and phase shift.

**Basic principle :**

- In a CRO, the electrons are emitted from a cathode accelerated to a high velocity and brought to focus on fluorescent screen.
- The screen produces a visible spot where the electron beam strikes.
- The electron beam is deflected over the screen in response to the electrical signal, thus electrons can be made to act as an electrical pencil of light which produces a spot of light wherever it strikes.
- As electrons have negligible mass, therefore, they respond almost instantaneously when acted upon by an electrical signal and can trace almost any electrical variations no matter how rapid.
- A CRO consists of a cathode ray tube and necessary power equipment to make it operated.

**PART-4**

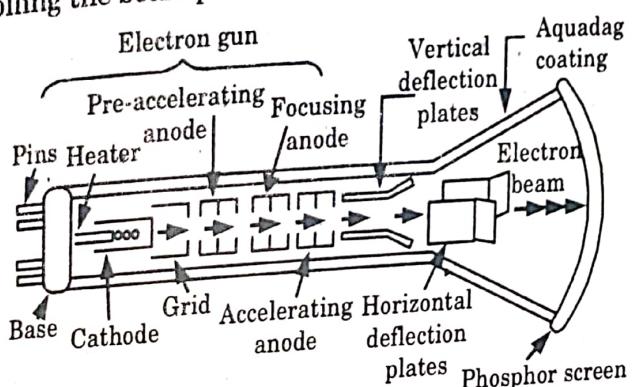
*CRT.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions****Que 5.5.****Write short note on the construction of a CRT.****OR**

**Describe the construction and working of internal structure of CRT display.**

**AKTU 2014-15(Sem-I), Marks 10****Answer**

CRT essentially consists of an electron gun for producing a stream of electrons, focusing and accelerating anodes for producing a narrow and sharply focused electron beam, horizontal and vertical deflection plates for controlling the beam path as shown in Fig. 5.5.1.

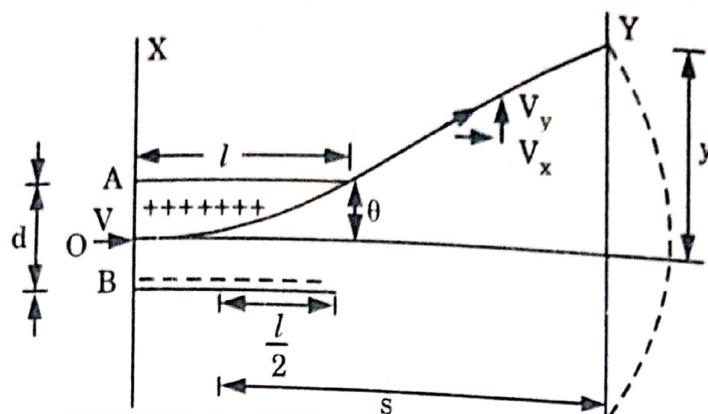
**Fig. 5.5.1. Cathode Ray Tube.****i. Electron Gun Assembly :**

1. The electron gun assembly consists of an indirectly heated cathode, a control grid surrounding the cathode, a focusing anode and an accelerating anode.
2. The sole function is to provide a focused electron beam which is accelerated towards the phosphor screen.
3. The cathode is a nickel cylinder coated with an oxide coating which emits plenty of electrons, when heated.
4. The control grid is a metal cylinder covered at one end.
5. The grid is at negative potential with respect to cathode and it has to vary electron emission and show brilliancy of spot on phosphor screen.

**ii. Deflection Plate Assembly :**

1. The electron beam, after leaving the electron gun, passes through the two pairs of deflection plates.

2. The X and Y plates deflect the electron beam in horizontal and vertical direction.
3. The amount of deflection is proportional to the voltage applied to the pair of plates as shown in Fig. 5.5.2.



**Fig. 5.5.2. Deflection of moving electrons.**

#### Deflection of moving electron in CRO tubes :

1. Let us consider an electron having initial velocity of  $u$  m/s along X-axis at point O in space between A and B, each of length  $l$  meters and separated by a distance of  $d$  meters.
2. Let potential difference across the plates is  $V$  volts.
3. The deflection  $y$  is,

$$y = \frac{e l s V_d}{md} = \frac{l s V_d}{2d V_a}$$

where  $s$  = distance along X-axis from point to screen.

4. From the above expression we can conclude that for a fixed accelerating voltage  $V_a$  and dimensions of CRT, the deflection is directly proportional to deflection voltage  $V_d$ .

#### Intensity control :

1. The knob of intensity control regulates the bias on the control grid and affects the electron beam intensity.
2. If the negative bias on the grid is increased, the intensity of electron beam is decreased, thus reducing the brightness of the spot.

### PART-5

#### Block Diagram of Oscilloscope.

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 5.6.** Describe the working of a CRO with the help of block diagram.

**OR**

With the help of neat block diagram, explain the working of a CRO.

**AKTU 2015-16(Sem-I), Marks 10**

**OR**

Draw a neat block diagram of a cathode ray oscilloscope with proper labels. Also explain its working principle.

**AKTU 2014-15(Sem-II), Marks 10**

**OR**

Draw the block diagram of a CRO and explain its working.

**AKTU 2013-14(Sem-I), Marks 05**

**OR**

Explain briefly functions of the following blocks in CRO :

- Deflection amplifier
- Cathode Ray Tube

**AKTU 2015-16(Sem-II), Marks 7.5**

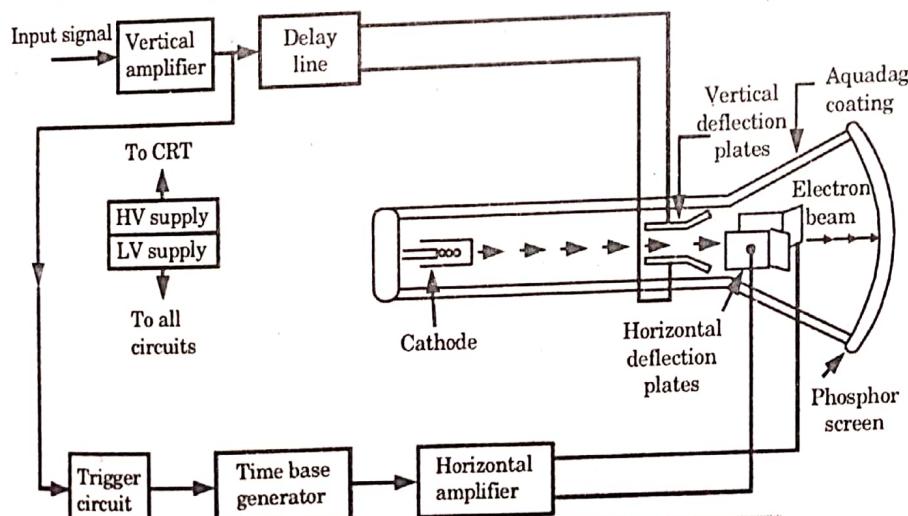
**OR**

Draw the general block diagram of CRO and explain each block.

**AKTU 2017-18(Sem-I), Marks 3.5**

### Answer

- The cathode ray oscilloscope is an extremely useful and versatile laboratory instrument used for studying wave shapes of alternating currents and voltages, for measurement of voltage, current, power and frequency.
- The block diagram of CRO is shown in Fig. 5.6.1.



**Fig. 5.6.1. Block diagram of a general purpose CRO.**

**Block Diagram :**

1. The CRO employs a cathode ray tube (CRT).
2. It generates electron beam, accelerates the beam to a high velocity, deflects the beam to create the image and contains a phosphor screen where the electron beam eventually becomes visible.
3. Low voltage supply is required for the heating of the electron gun for generation of electron beam and high voltage, of the order of few thousand volts, is required for CRT to accelerate the beam.
4. Horizontal and vertical deflection plates are fitted between electron gun and screen to deflect the beam according to input signal.
5. Electron beam strikes the screen and creates a visible spot.
6. This spot is deflected on the screen in X-axis direction with constant time dependent rate.
7. The input signal is supplied to the vertical deflection plates through the vertical amplifier, which raises the potential of the input signal to a level that will provide usable deflection of the electron beam.
8. Now electron beam deflects in 2 directions, horizontal on X-axis and vertical on Y-axis.

**Function of each block :**

1. **CRT** : This is the cathode ray tube which emits electrons that strike the phosphor screen internally to provide a visual display of signal.
2. **Vertical amplifier** : This is a wide band amplifier used to amplify signals in the vertical section.
3. **Delay line** : It is used to delay the signal for some time in the vertical sections.
4. **Time base** : It is used to generate the sawtooth voltage required to deflect the beam in the horizontal section.
5. **Horizontal amplifier** : This is used to amplify the sawtooth voltage before it is applied to horizontal deflection plates.
6. **Trigger circuit** : This is used to convert the incoming signal into trigger pulses so that the input signal and the sweep frequency can be synchronised.
7. **Power supply** :
  - a. There are two power supplies, a negative High Voltage (HV) supply and a positive Low Voltage (LV) supply.
  - b. Two voltages are generated in the CRO. The positive volt supply is from + 300 to 400 V. The negative high voltage supply is from - 1000 to - 1500 V.
  - c. This voltage is passed through a bleeder resistor at a few mA.
  - d. The intermediate voltages are obtained from the bleeder resistor for intensity, focus and positioning controls.

**PART-6**

*Measurement of Voltage, Current, Phase and Frequency Using CRO.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 5.7.** Explain how frequency and phase can be measured using CRO ?

**AKTU 2014-15(Sem-II), Marks 05**

OR

Explain how unknown signal frequency is measured using CRO ?

**AKTU 2016-17(Sem-I), Marks 05**

OR

With the help of block diagram describe the working of a CRO and explain the application and measurement of phase and frequency using CRO.

**AKTU 2013-14(Sem-II), Marks 10**

OR

Explain CRO with the help of diagram. How can we measure phase and frequency using CRO ?

**AKTU 2017-18(Sem-II), Marks 07**

OR

Describe the operation of CRT with neat block diagram. How unknown frequency is measured using CRO ?

**AKTU 2016-17(Sem-II), Marks 07**

OR

- Explain all oscilloscope controls with one example.
- How do you measure power supply performance ? Explain.

**AKTU 2015-16(Sem-II), Marks 10**

**Answer**

**CRT :** Refer Q. 5.5, Page 5-10D, Unit-5.

**Principle of CRO :** Refer Q. 5.4, Page 5-9D, Unit-5.

**Block diagram of CRO :** Refer Q. 5.6, Page 5-12D, Unit-5.

**Oscilloscope controls :**

1. The front panel and controls of a representative single-beam dual-trace analog oscilloscope are illustrated in Fig. 5.7.1.
2. The waveforms under investigation are displayed on the screen, which is protected with a calibrated flat piece of hard plastic called a graticule.
3. The graticule is used for measuring the amplitude (in vertical divisions) and the time period (in horizontal divisions) of any displayed waveform.
4. Immediately below the screen is a power POWER ON/OFF switch, an INTENSITY control to adjust the brightness of the display, a FOCUS control to focus the display to a fine line, and a pushbutton BEAM FINDER to locate a display that has been shifted off the screen.
5. To facilitate display of two waveforms, there are two separate sets of VERTICAL controls, identified as CHANNEL A and CHANNEL B:
6. The purpose of the POSITION controls is to move each waveform vertically up or down the screen to set it in the best position for viewing.

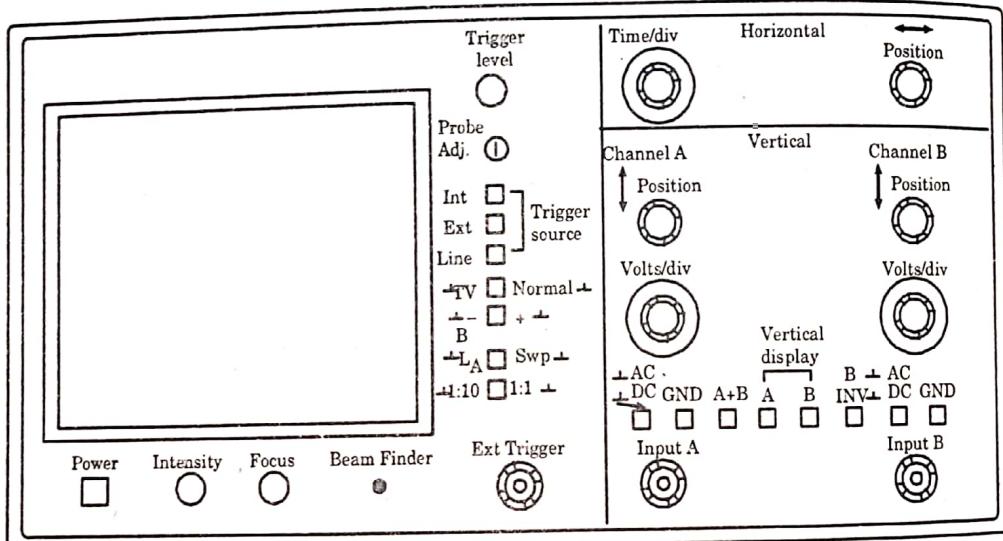


Fig. 5.7.1.

7. The VERTICAL DISPLAY A and B pushbuttons allow channel A input, channel B input, or both to be displayed on the screen.
8. The HORIZONTAL TIME/DIV selector switch determines the number of horizontal divisions occupied by each cycle of displayed waveform.
9. The TRIGGER LEVEL knob continuously adjusts the triggering point of the input wave.

**Frequency measurement :**

1. When two sinusoidal voltages are applied to the two sets of deflecting plates, a Lissajous pattern is obtained on the screen.
2. Let two voltages are  $V_x$  and  $V_y$  at X and Y plates respectively.

$$V_x = v_x \sin \omega_1 t$$

$$V_y = v_y \sin(\omega_2 t + \phi)$$

where  $\omega_1$  and  $\omega_2$  are the angular frequencies of the voltages and  $\phi$  is the phase angle.

Case 1 :  $\omega_1 = \omega_2$  and  $\phi = 0$

$$V_y = \frac{v_y}{v_x} \cdot V_x$$

i.e.,

This is an equation of straight line passing through origin and its equivalent is shown in Fig. 5.7.2.

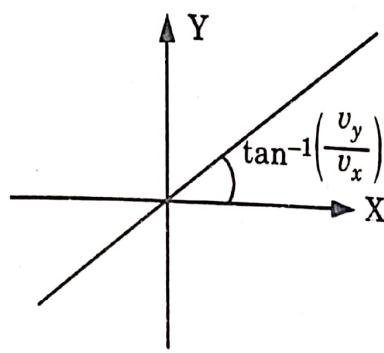


Fig. 5.7.2.

Case 2 :  $\omega_1 = \omega_2$  and  $\phi = \pi/2$

$$\frac{v_x^2}{V_x^2} + \frac{v_y^2}{V_y^2} = 1$$

This is an equation of ellipse and its equivalent pattern is shown in Fig. 5.7.3.

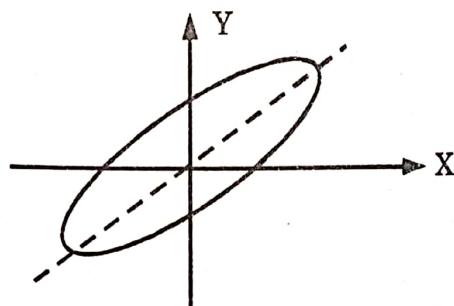


Fig. 5.7.3.

Case 3 :

$$\omega_1 = \omega_2, \phi = \pi/2 \text{ and } v_x = v_y = V.$$

$$v_x^2 + v_y^2 = 2 V^2$$

This is the equation of circle and its equivalent pattern is shown in Fig. 5.7.4.

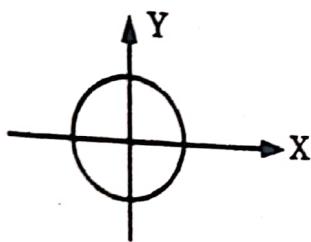


Fig. 5.7.4.

2. The unknown frequency is applied to Y plates.
3. A sinusoidal voltage is applied to X-plates.
4. The frequency of oscillator is varied until a single loop stationary pattern is obtained on the screen.

#### Phase measurement :

1. Various patterns appear on CRO screen depending upon the relative amplitude, frequencies, phases and waveforms of the ac voltages.
2. These patterns are known as Lissajous figures.
3. Let consider the case of ellipse.
4. The orientation of the ellipse with respect to coordinate axes depends upon the phase difference between two voltages.
5. The value of A and B are noted from the ellipse as shown in Fig. 5.7.5.

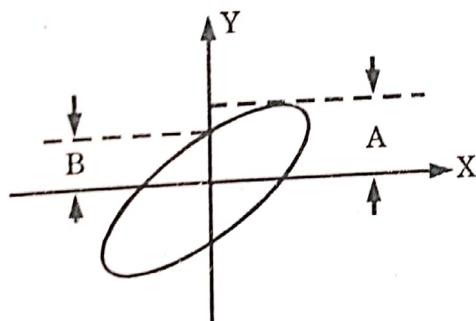


Fig. 5.7.5.

6. The phase difference  $\phi$  is calculated from the relation.

$$\sin \phi = \frac{B}{A}$$

#### Voltage Measurement (Amplitude Measurement) :

1. The oscilloscope tube face has a calibrated scale for the measurement of time and amplitude.
2. The boxes are divided into centimeters, 4 cm on each of the side of centre with each box further divided into 0.2 cm interval.
3. The vertical scale is calibrated in either volts per centimeter or millivolts per centimeter.
4. Due to such scale setting of the scope, we can measure peak-to-peak or peak voltage for an AC signal.

**Current Measurements :**

1. A CRO has very high input impedance and cannot be used for direct measurement of current.
2. The current can be measured by passing through a suitable known resistor.
3. The voltage drop across the resistor will give directly the value of current.

$$\text{i.e., } I = \frac{V \text{ (measured on CRO)}}{R}$$

The suitable arrangement is shown in Fig. 5.7.6.

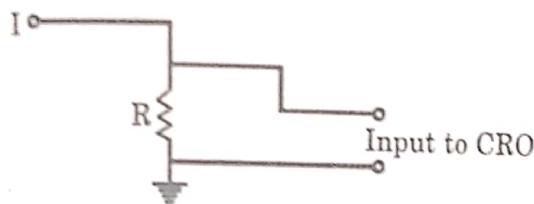


Fig. 5.7.6. Arrangement for measurement of current.

**Que 5.8.** Draw the Lissajous pattern on CRO when the ratio of the frequency of the vertical input to that of the horizontal input is 1 : 2.

AKTU 2013-14 (Sem-I), Marks 05

**Answer**

1.  $\frac{\text{Frequency of vertical input } (F_y)}{\text{Frequency of horizontal input } (F_x)} = \frac{\text{Horizontal points}}{\text{Vertical points}} = \frac{1}{2}$
2. A Lissajous pattern is a pattern which is stationary on the screen of a CRO. It means that the spot traces out the same pattern for every cycle of a voltage signal.

$$\frac{F_y}{F_x} = \frac{\text{Positive } y\text{-peaks}}{\text{Positive } x\text{-peaks}}$$

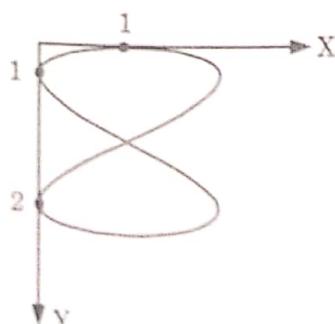


Fig. 5.8.1.

**Que 5.9.** A Lissajous pattern on an oscilloscope is stationary. It has 5 vertical tangent values and 6 horizontal tangent values. The frequency of horizontal input is 1800 Hz. Determine the frequency of vertical input.

AKTU 2017-18(Sem-I), Marks 3.5

**Answer**

Given, vertical tangent values = 5, horizontal tangent values = 6.

$$f_x = 1800 \text{ Hz.}$$

$$\text{So, } \frac{\text{Frequency of vertical input } (F_y)}{\text{Frequency of horizontal input } (F_x)} = \frac{\text{Horizontal tangent values}}{\text{Vertical tangent values}}$$

$$\frac{F_y}{1800} = \frac{6}{5}$$

$$F_y = \frac{6}{5} \times 1800$$

$$F_y = 2160 \text{ Hz}$$

**PART-7**

*Introduction of Digital Storage Oscilloscope and Comparison of DSO with Analog Oscilloscope.*

**Questions-Answers**

**Long Answer Type and Medium Answer Type Questions**

**Que 5.10.** Explain digital storage oscilloscope with block diagram.

**Answer**

1. A digital oscilloscope digitises the input signal, so that all subsequent signals are digital.
2. A conventional CRT is used, and storage occurs in electronic digital memory.
3. Fig. 5.10.1 shows a block diagram of a basic digital storage oscilloscope.
4. The input signal is digitised and stored in memory in digital form. In this state it is capable of being analysed to produce a variety of different information.

5. To view the display on the CRT the data from memory is reconstructed in analog form.

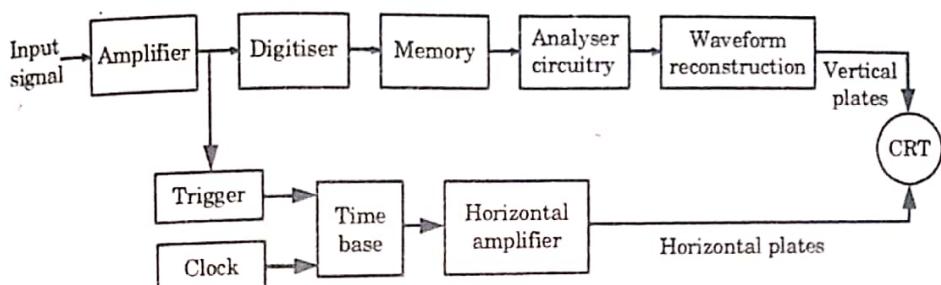


Fig. 5.10.1. Block diagram of a basic digital storage oscilloscope.

6. Digitising occurs by taking a sample of the input waveform at periodic intervals.
7. In order to ensure that no information is lost, sampling theory states that the sampling rate must be at least twice as fast as the highest frequency in the input signal. If this is not done then aliasing will result, as shown in Fig. 5.10.2.
8. This requirement for a high sampling rate means that the digitiser, which is an analog to digital converter, must have a fast conversion rate.
9. This usually requires expensive flash analog to digital converters, whose resolution decreases as the sampling rate is increased.
10. It is for this reason that the bandwidth and resolution of a digital oscilloscope is usually limited by its analog to digital converter.

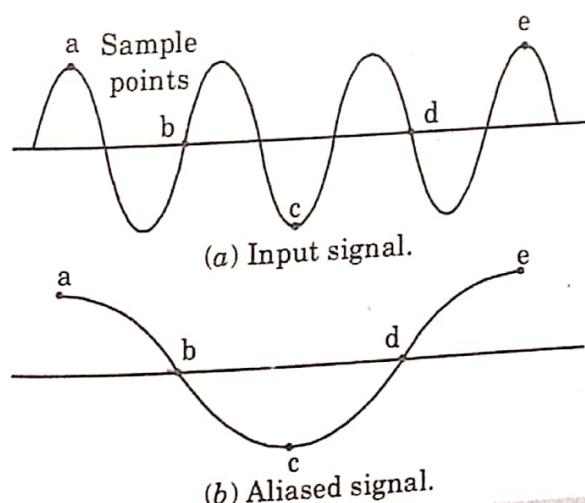


Fig. 5.10.2. Effect of a low sampling frequency.

**Que 5.11.** Give the comparison of DSO with analog oscilloscope.

**Answer**

S. No.	Analog storage oscilloscope	Digital storage oscilloscope
1.	It has higher bandwidth and writing speed.	It has lower bandwidth and writing speed.
2.	CRT used in it, is costlier.	CRT used in it, is cheaper.
3.	Capability of storage time is limited.	Capability of storage time is infinite.
4.	Time base signal in analog oscilloscope is generated by ramp circuit.	Time base signal in digital storage oscilloscope is generated by a crystal clock.
5.	It cannot work in look back mode.	It can work in look back mode.
6.	Accuracy is less.	Accuracy is high.
7.	Analog oscilloscope collects data after it is has been triggered.	DSO always collects data and trigger tells it when to stop.

**VERY IMPORTANT QUESTIONS**

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

- Q. 1.** Explain the basic principle of digital voltmeter with the help of block diagram. What are the characteristics of DVM?  
**Ans:** Refer Q. 5.1.
- Q. 2.** Explain with the help of neat diagram, working and characteristics curve of ramp type digital voltmeter.  
**Ans:** Refer Q. 5.2.
- Q. 3.** Explain working principle of digital multimeter with the help of suitable block diagram.  
**Ans:** Refer Q. 5.3.

**Q. 4. Describe the working of a CRO with the help of block diagram.**

**Ans.** Refer Q. 5.6.

**Q. 5. Explain how frequency and phase can be measured using CRO ?**

**Ans.** Refer Q. 5.7.

**Q. 6. Draw the Lissajous pattern on CRO when the ratio of the frequency of the vertical input to that of the horizontal input is 1 : 2.**

**Ans.** Refer Q. 5.8.

**Q. 7. Write short note on the construction of a CRT.**

**Ans.** Refer Q. 5.5.





## Electronics Instrumentation and Measurements (2 Marks Questions)

**5.1. Define digital voltmeter. Give its classifications.**

**Ans.** **DVM :** Digital voltmeter (DVM) is an indicating device. The main use of DVM is to measure voltage between two points. It displays DC or AC voltage as discrete numerals.

**Classification :**

- i. Non-integrating DVM
- ii. Integrating DVM

**5.2. What is multimeter and write its applications ?**

**Ans.** **Multimeter :** An electronic measuring instrument that combines several measurement functions in one unit.

**Applications :** Used to measure :

- i. AC/DC voltage
- ii. AC/DC current
- iii. resistance

**5.3. Define the horizontal and vertical sensitivity of a CRT.**

**Ans.** **Horizontal sensitivity :** The horizontal deflection ( $x$ ) produced will be proportional to the horizontal deflecting voltage,  $V_x$ , applied to  $x$ -input.

$$\begin{aligned}x &\propto V_x \\x &= K_x V_x \\K_x &= x/V_x\end{aligned}$$

where  $K_x$  expressed as cm/volt or division/volt, is called horizontal sensitivity of CRT.

**Vertical sensitivity :** The vertical deflection ( $y$ ) produced will be proportional to the vertical deflecting voltage,  $V_y$ , applied to the  $y$ -input.

$$\begin{aligned}y &\propto V_y \\y &= K_y V_y \\K_y &= y/V_y\end{aligned}$$

where  $K_y$  expressed as cm/volt or division/volt is called vertical sensitivity of CRT.

5.4. What are the functions of a delay line and trigger circuit ?  
OR

Why triggering circuit is needed in CRO ?

AKTU 2015-16(Sem-II), Marks 02

**Ans.** Delay line is used to delay the signal for some time in the vertical section while trigger circuit is used to convert the incoming signal into trigger pulses so that the input signal and the sweep frequency can be synchronized.

5.5. What is CRO ?

**Ans.** The cathode ray oscilloscope is an extremely useful and versatile laboratory instrument used for studying wave shapes of alternating currents and voltages, for measurement of voltage, current, power and frequency.

5.6. State the advantage of digital instruments over analog instruments.

AKTU 2017-18(Sem-I), Marks 02

AKTU 2016-17(Sem-I), Marks 02

AKTU 2016-17(Sem-II), Marks 02

**Ans.**

- i. Greater accuracy
- ii. Better resolution and easy readability
- iii. High input resistance.

5.7. A digital voltmeter has negligible loading effect on the circuit under test. Why ?

**Ans.** Digital voltmeter has negligible loading effect on circuit under test because digital voltmeters have very high input resistance.

5.8. A Lissajous pattern on an oscilloscope is stationary and has 4 horizontal and 3 vertical tangencies. The horizontal frequency is 50 Hz, find vertical frequency.

AKTU 2017-18(Sem-II), Marks 02

**Ans.**

$$\frac{f_y}{f_x} = \frac{\text{Number of horizontal tangencies}}{\text{Number of vertical tangencies}}$$

$$\frac{f_y}{50} = \frac{4}{3}$$
$$f_y = 66.67 \text{ Hz}$$

5.9. Draw the Lissajous pattern when the ratio of the frequency of the vertical input to that of horizontal input is 1 : 2.

**Ans.**

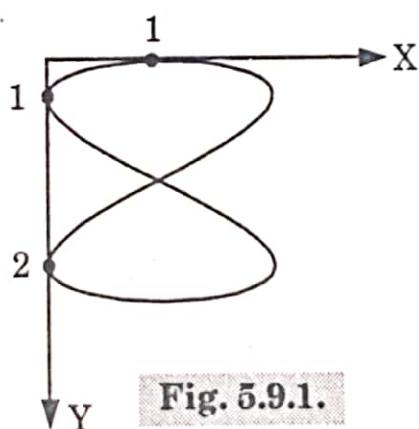


Fig. 5.9.1.

5.10. List the four specifications of unregulated power supply.

**AKTU 2015-16(Sem-II), Marks 02**

- Ans.**
- i. Current application
  - ii. Output voltage
  - iii. Output ripple
  - iv. Load regulation



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