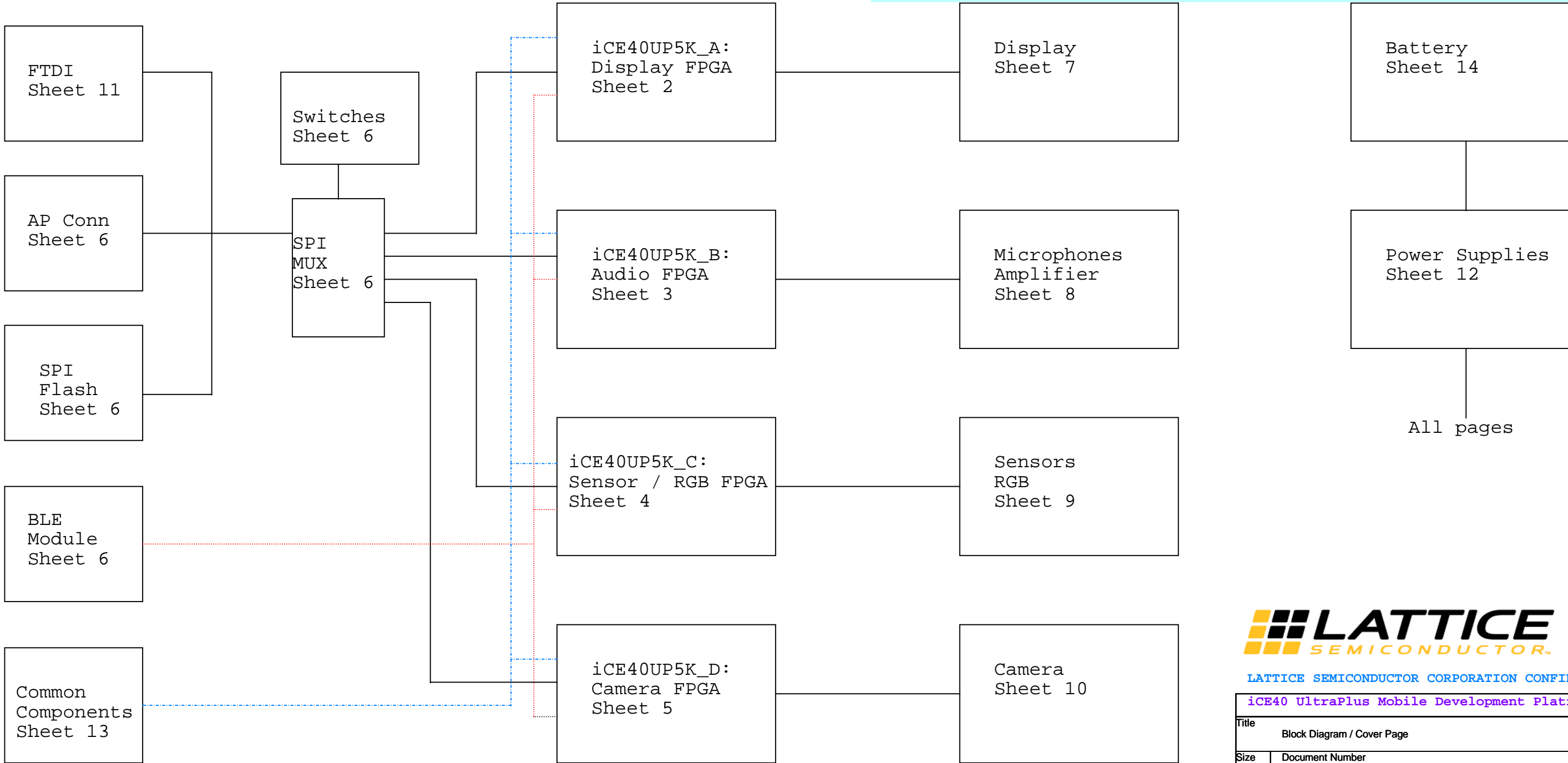


iCE40 UltraPlus Mobile Development Platform

Revision C

August 2 2016

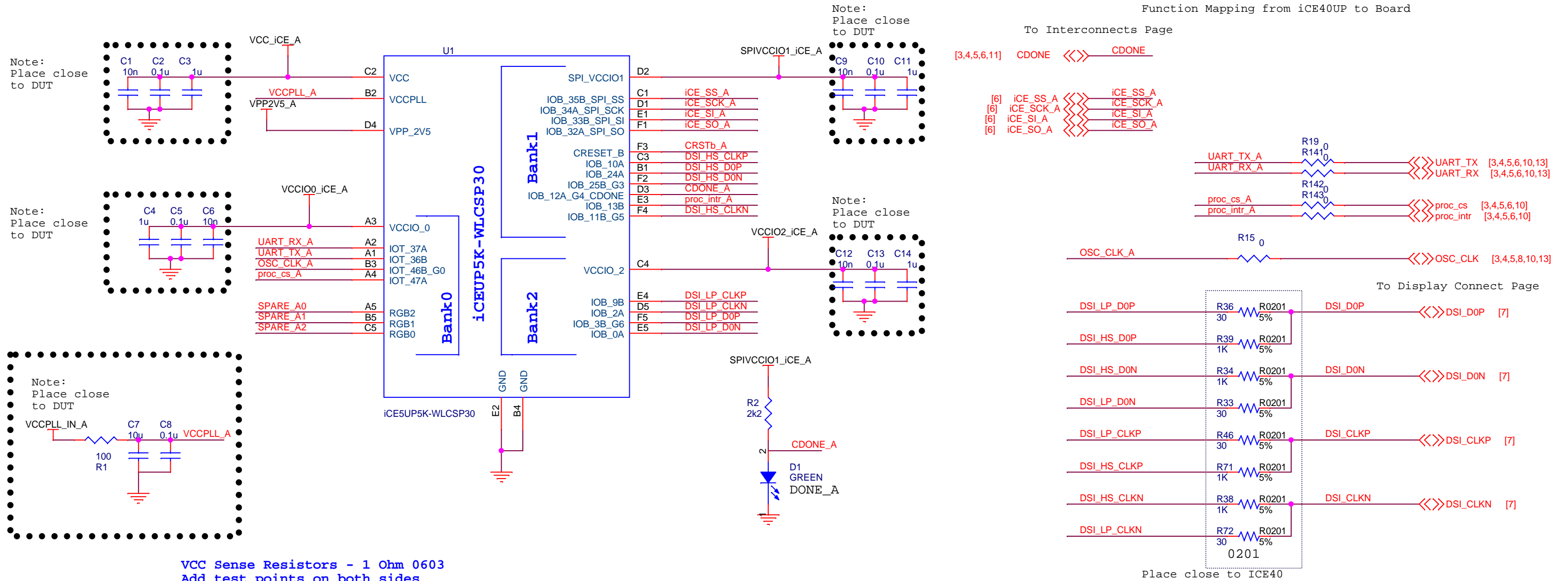
- Revision History
- Rev A - First Draft
- Rev C - Changed Gryroscope i2c address by grounding U36-27
- Inserted 2 more pins to iCEA control J25 header, pin 7 & 8
 - Added 4 resistors to allow swap of GLED & BLED on U3 device
 - Added FT_RESETh on J16.7 - AP INTERCONNECT to allow bypassing of FTDI Chip
 - Added 2 PDM Microphones
 - Added ESD protection for J5 USB
 - Changed D2 - LED2 to GREEN from RED
 - Changed R42 resistor value to 18ohm from 12ohm
 - Changed U41 and U42 to DG409LDQ-T1-E3 device
 - Changed U41 and U42 power to VSUPPLY



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Note :

- 1) Match length within pair as well as other pairs with +/- 5% tolerance
- 2) Differential impedance should be 100 Ohms and 50 Ohms as a single ended signals
- 3) All the power rails should be capable of carrying 1A current
- 4) Place MIPI TX resistor network as close to bank 1 as possible.

Trace match *HS* P & N channels as well as individual pairs.
Minimize routing and trace match *LP* signals..



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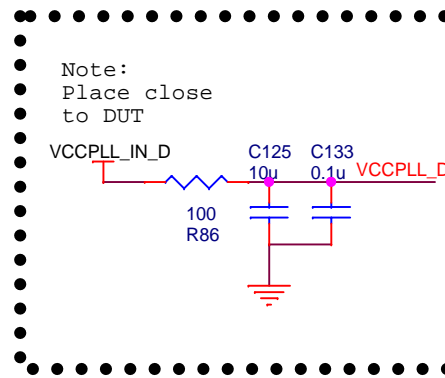
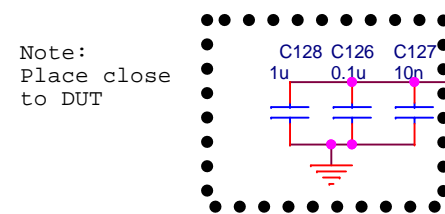
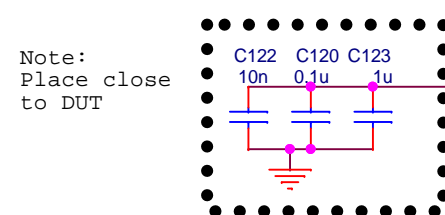
iCE40 UltraPlus Mobile Development Platform

Title
iCE40UP5K FPGA A - Display

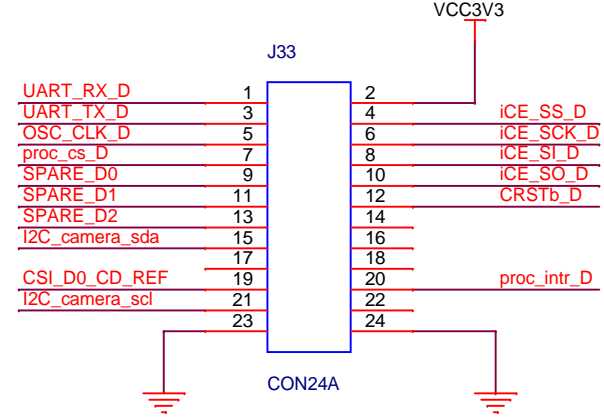
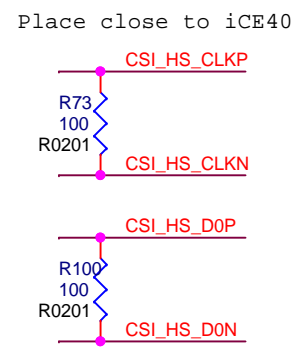
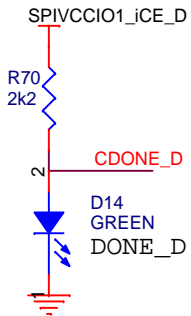
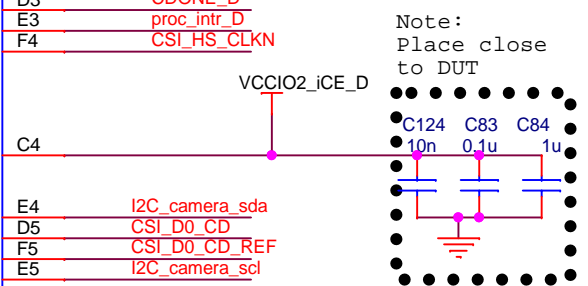
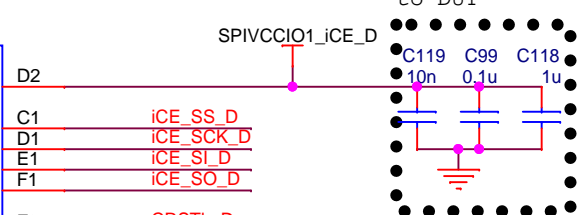
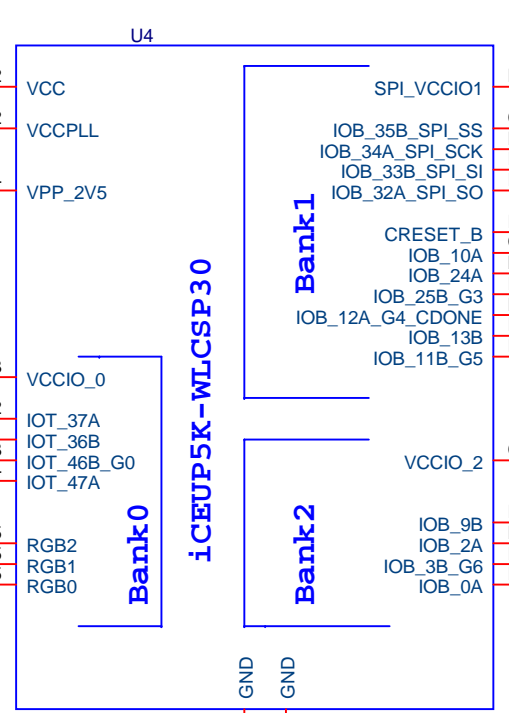
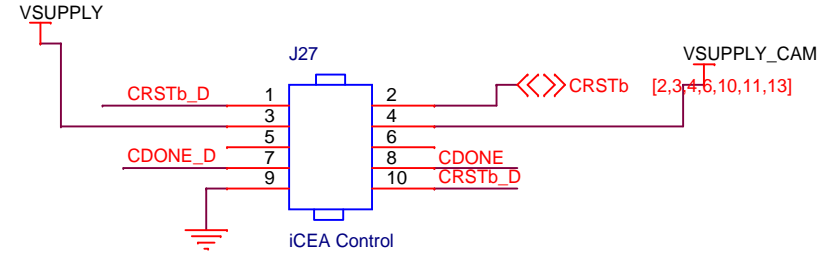
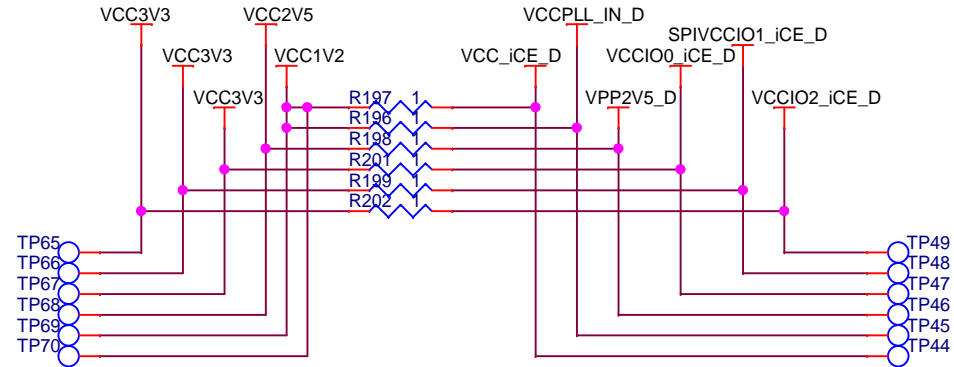
Size B Document Number

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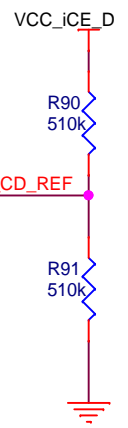
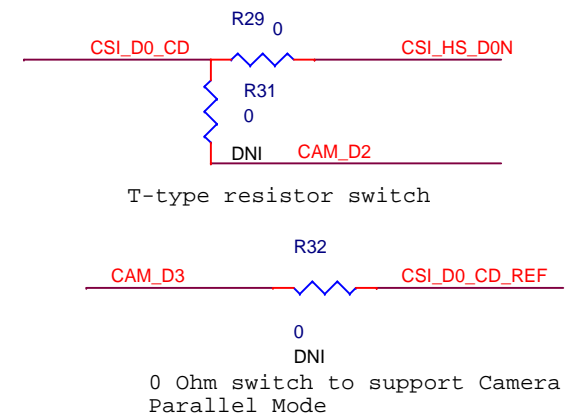
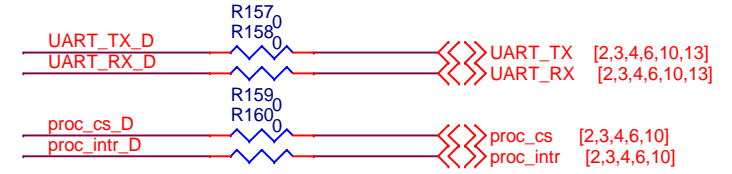
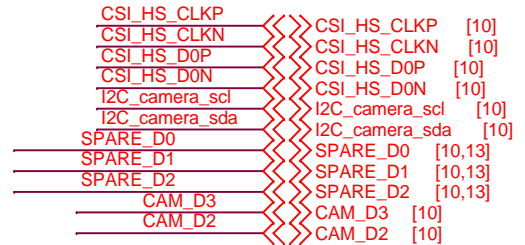
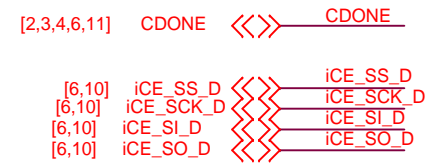


VCC Sense Resistors - 1 Ohm 0603
Add test points on both sides



Note :
1) Match length within pair as well as other pairs with +/- 5% tolerance
2) Differential impedance should be 100 Ohms and 50 Ohms as a single ended signals
3) Trace match LVDSI* pins between P and N channels as well as individual pairs.

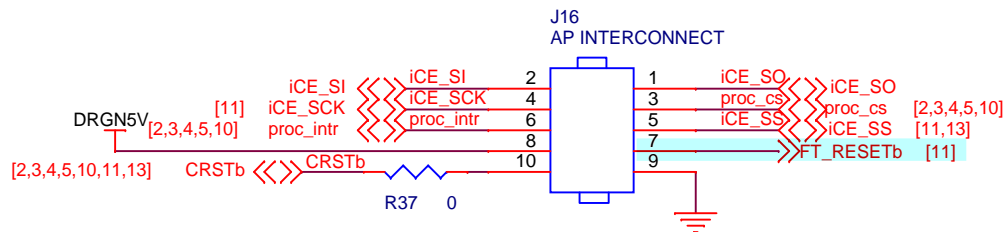
Function Mapping from iCE40UP to Board



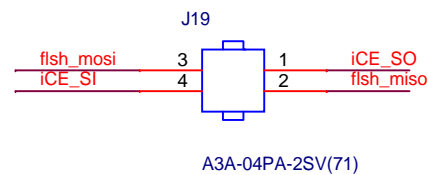
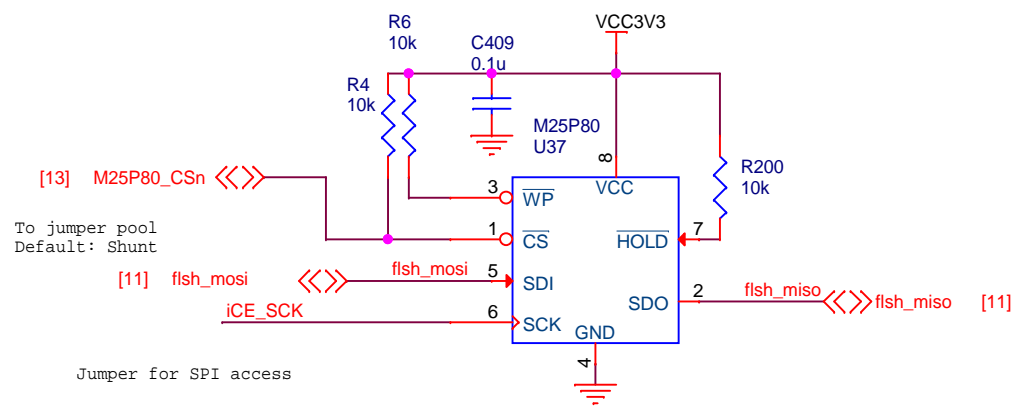
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iCE40 UltraPlus Mobile Development Platform

Title			iCE40UP5K FPGA D - Camera		
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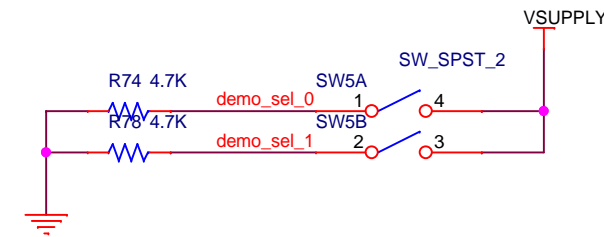
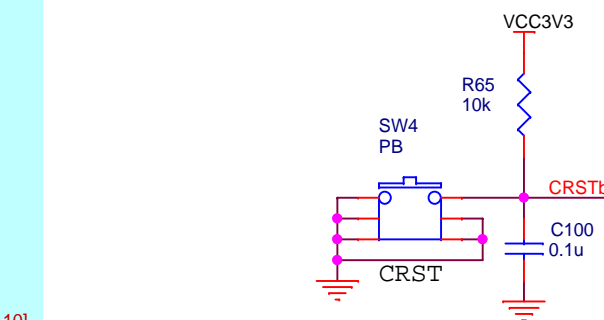
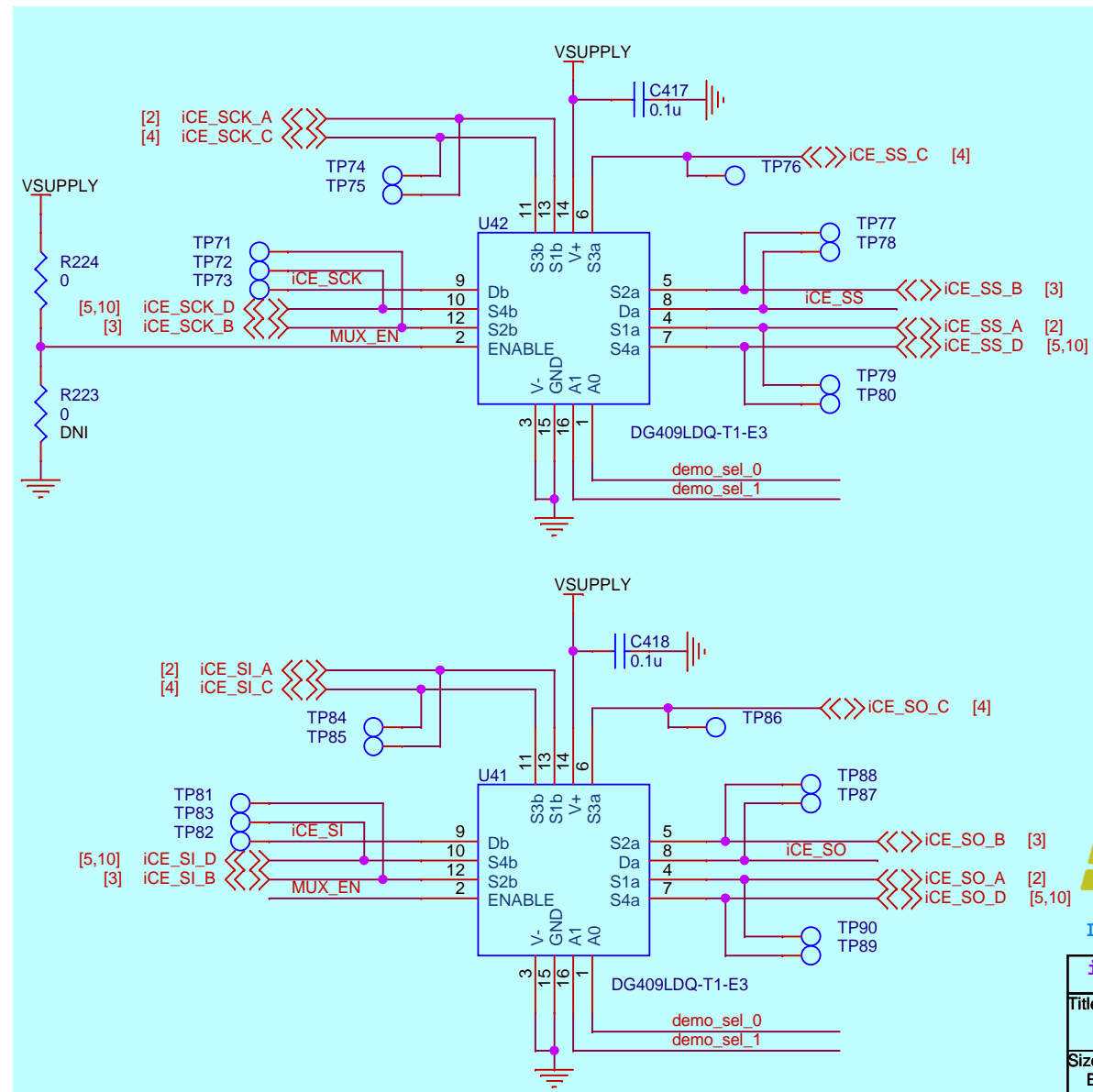
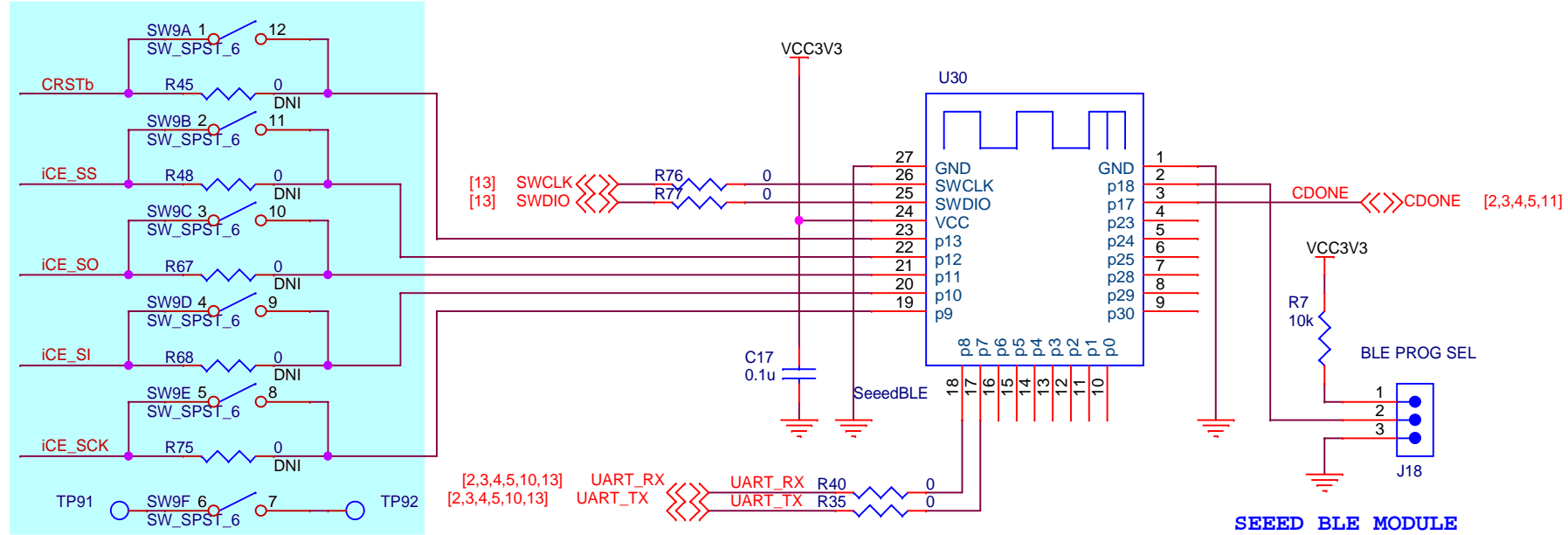
AP INTERCONNECT



For programming Flash - Shunt 1,3 and 2,4 (default)

For programming iCE - Shunt 3,4 and 1,2

SPI CONFIGURATION / FLASH



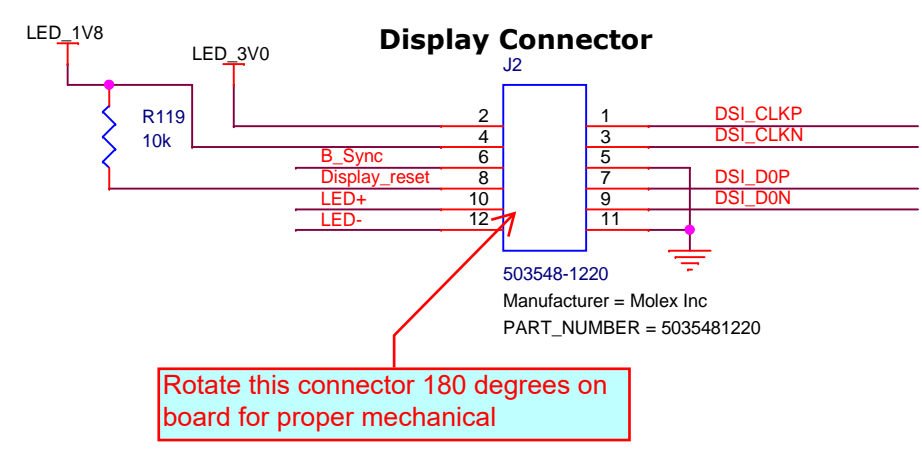
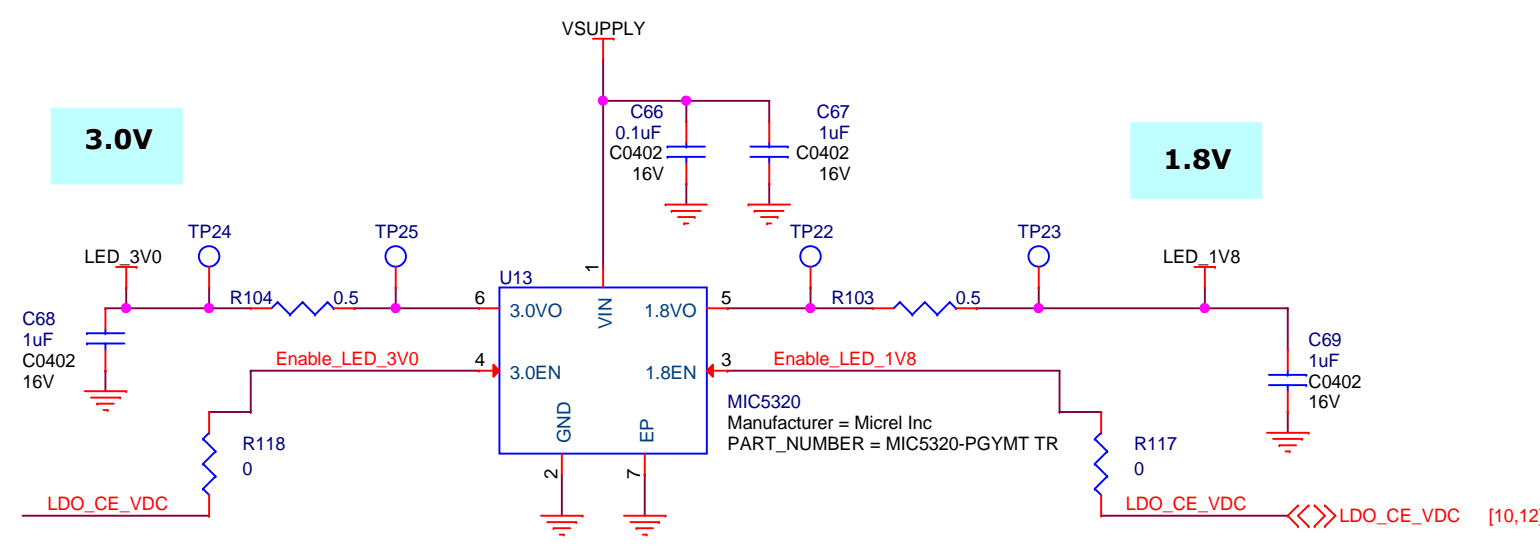
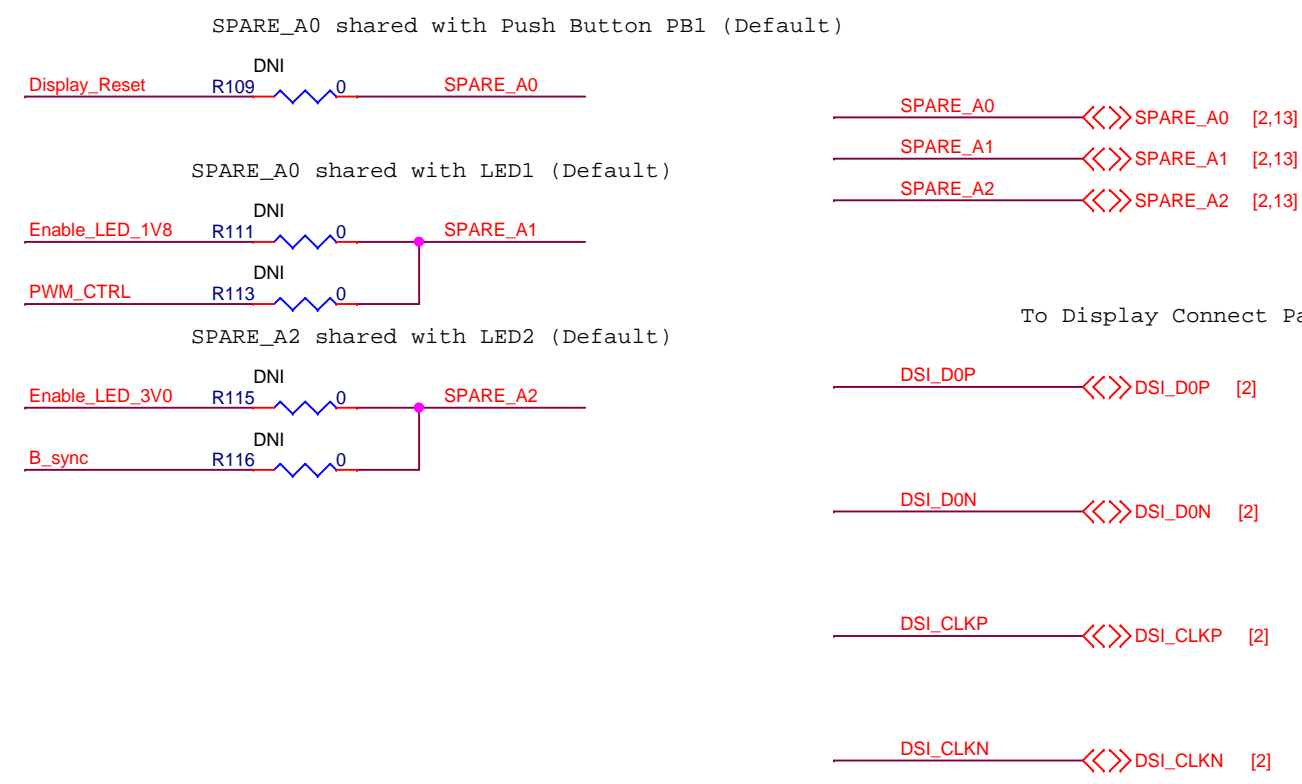
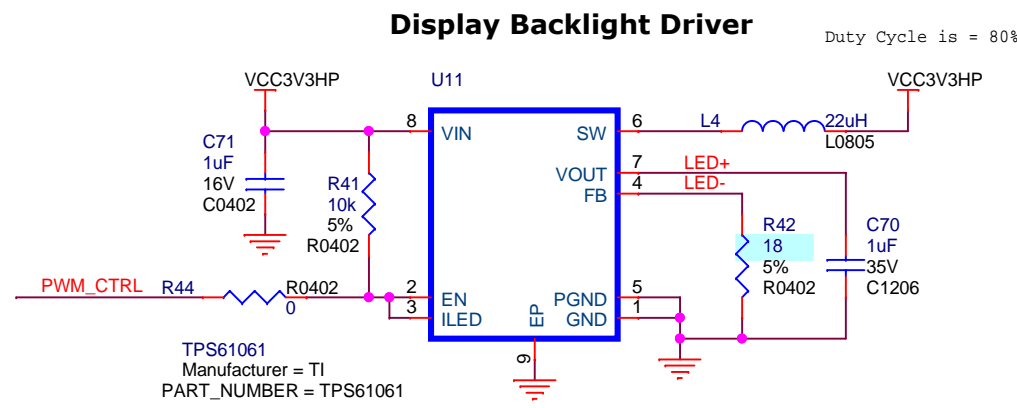
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iCE40 UltraPlus Mobile Development Platform

Title Common Components - SPI

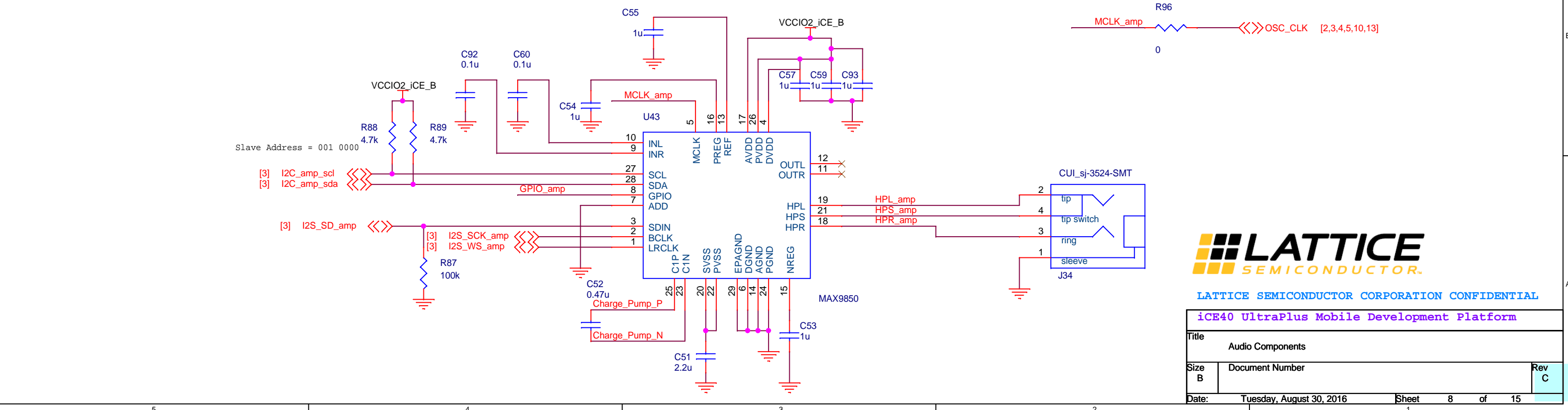
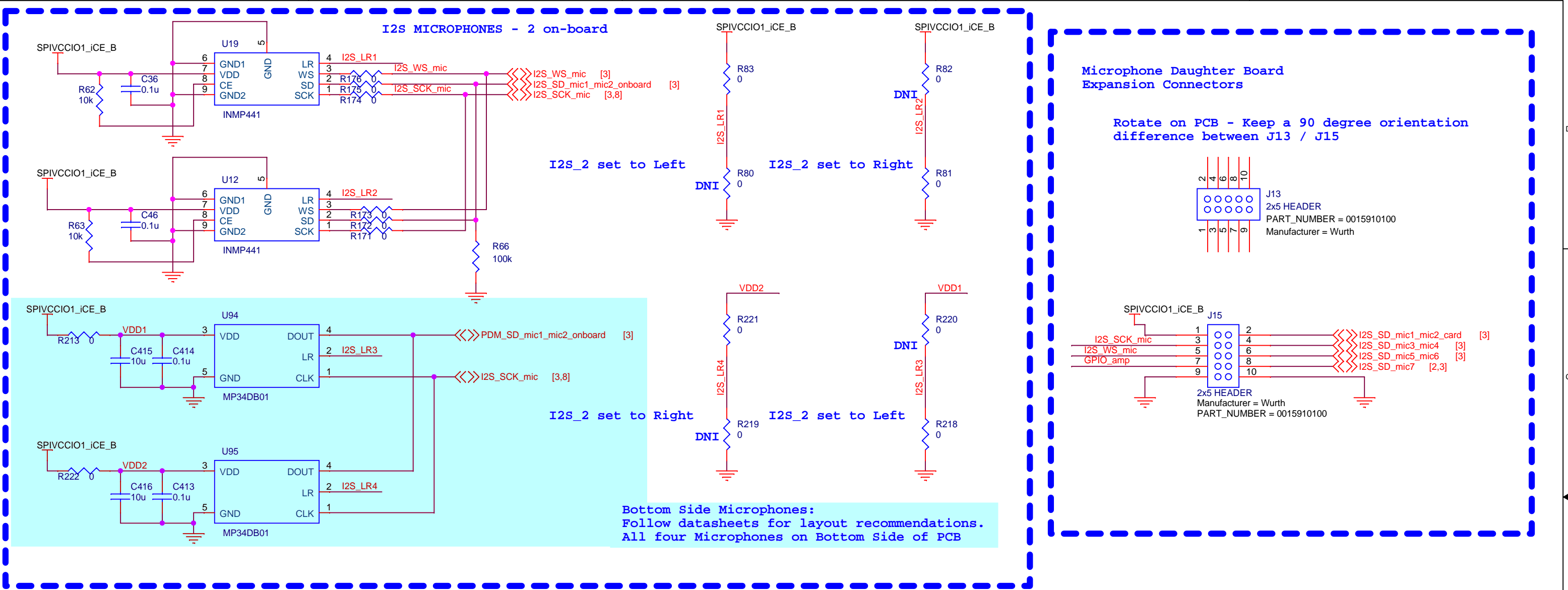
Size B Document Number Rev C

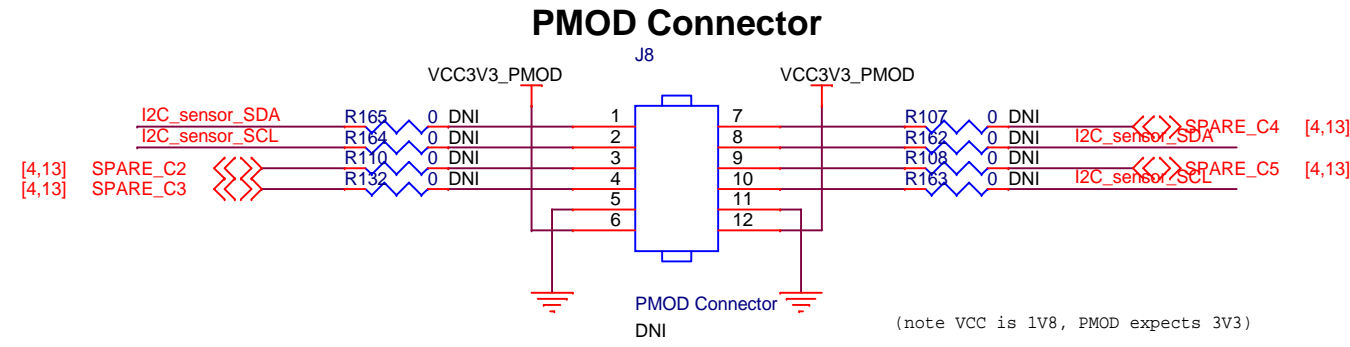
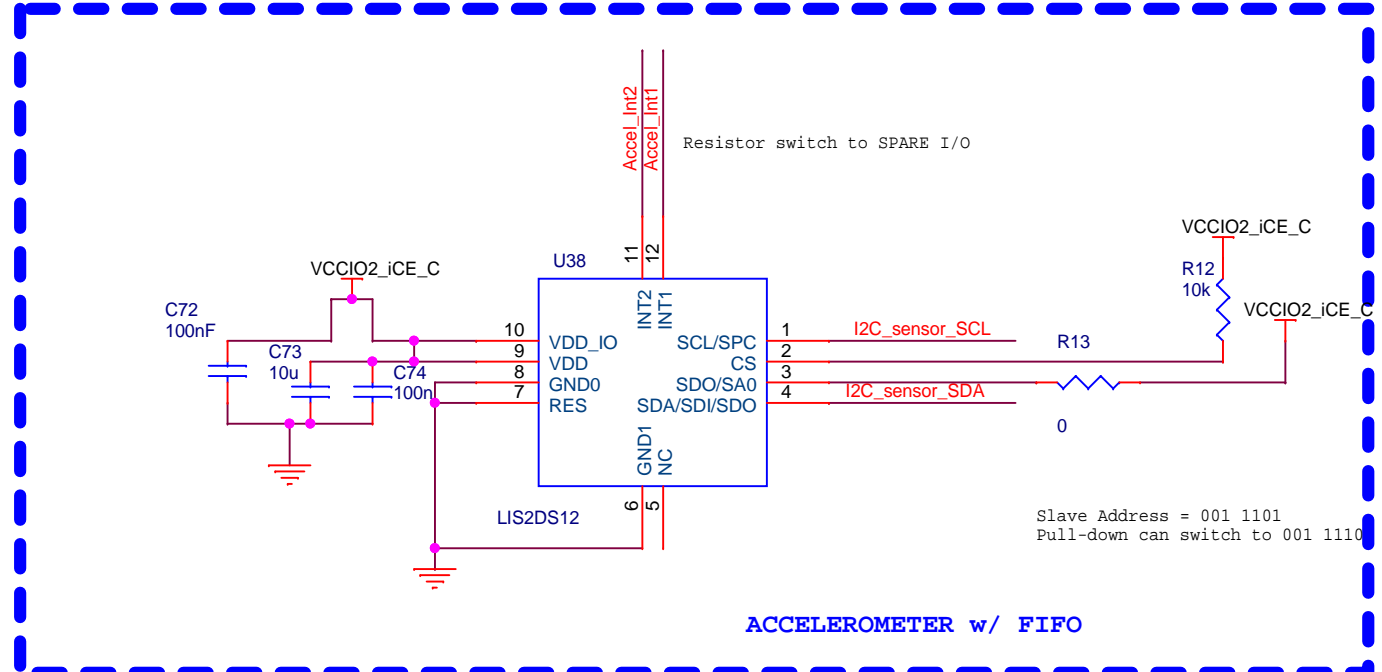
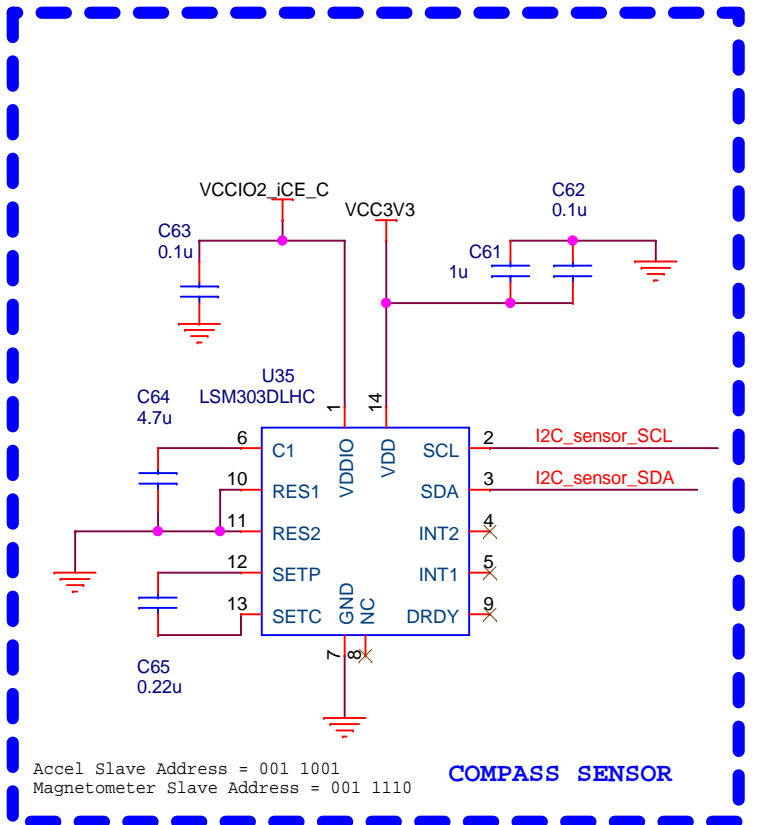
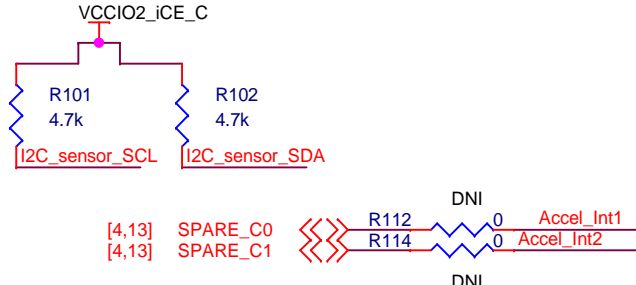
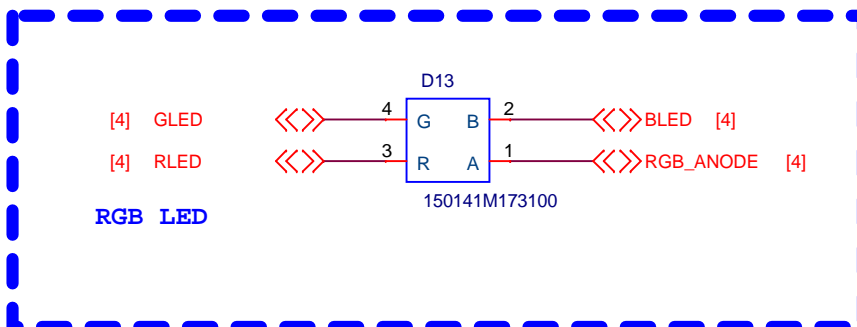
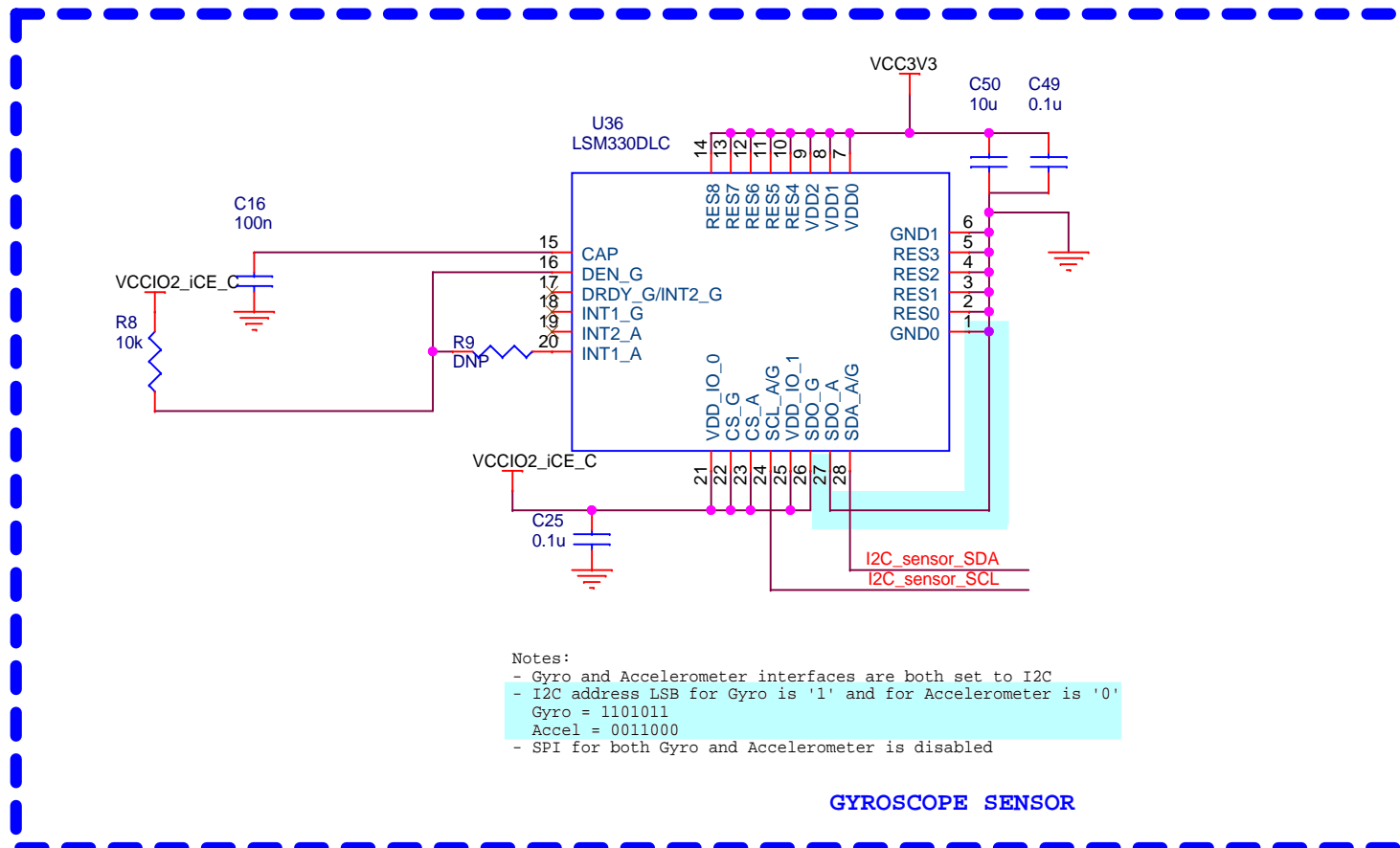
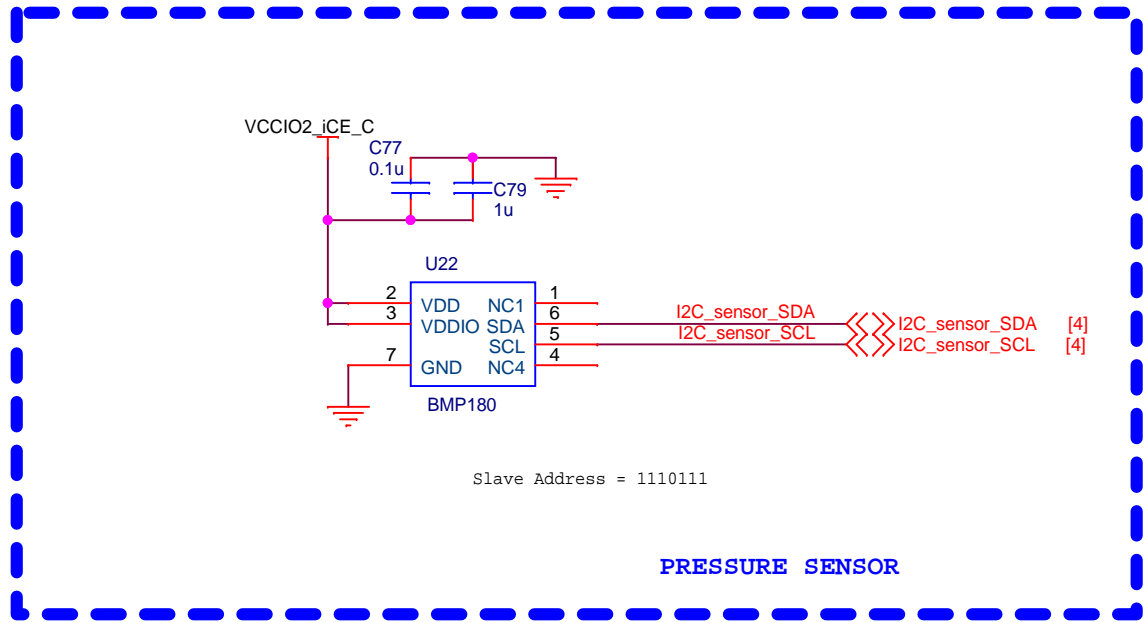
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Rotate this connector 180 degrees on board for proper mechanical



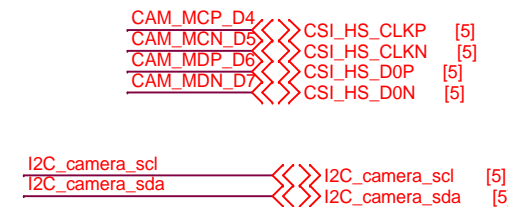




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iCE40 UltraPlus Mobile Development Platform

Title			Sensors & RGB Circuitry		
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CAM_D1 R43 0 DNI <<<>> SPARE_D0 [5,13]

CAM_D0 R53 0 DNI <<<>> SPARE_D1 [5,13]

CAM_PCLK R52 0 DNI <<<>> SPARE_D2 [5,13]

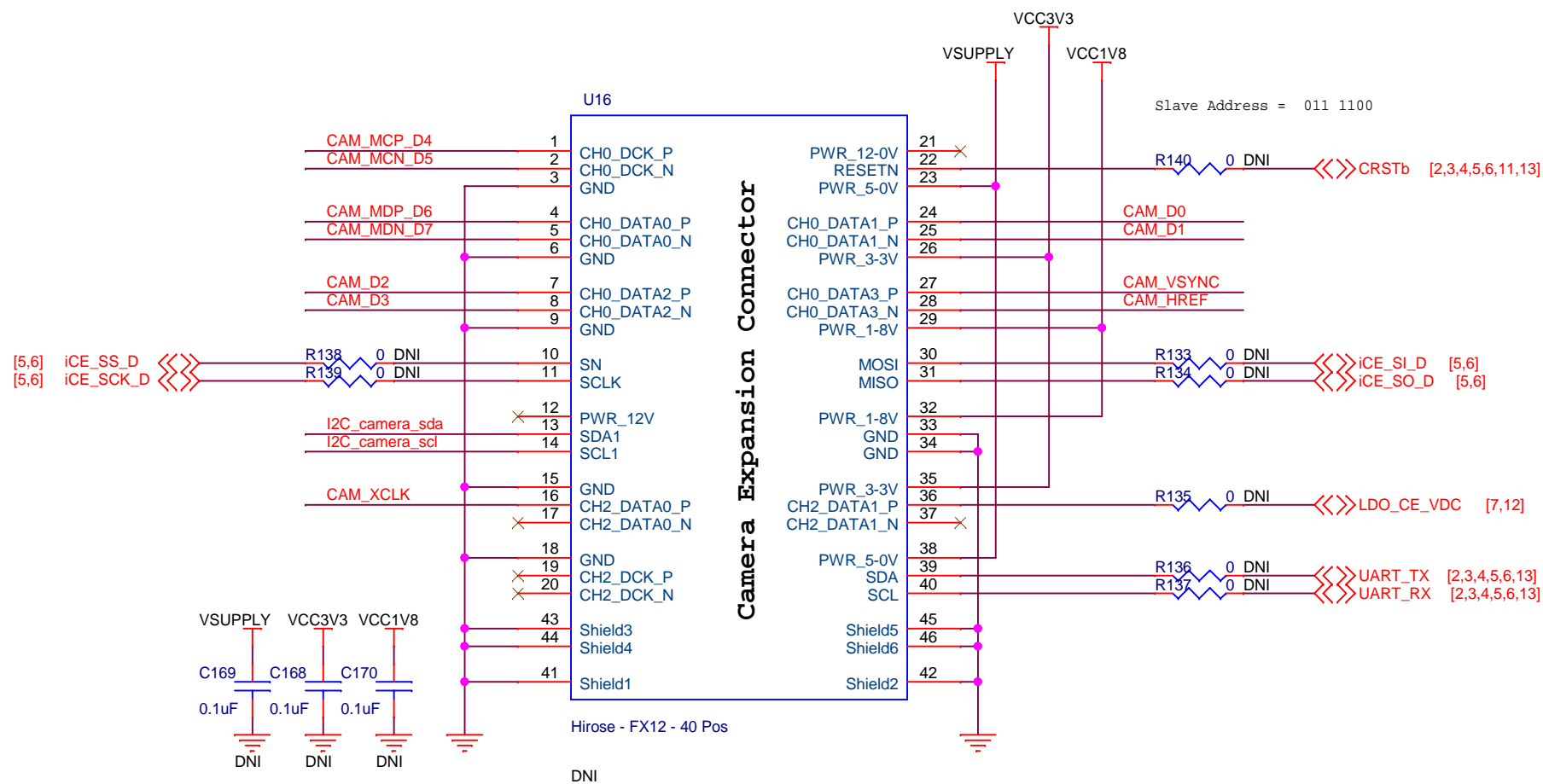
CAM_D3 <<<>> CAM_D3 [5]

CAM_D2 <<<>> CAM_D2 [5]

CAM_VSYNC R55 0 DNI <<<>> proc_cs [2,3,4,5,6]

CAM_HREF R54 0 DNI <<<>> proc_intr [2,3,4,5,6]

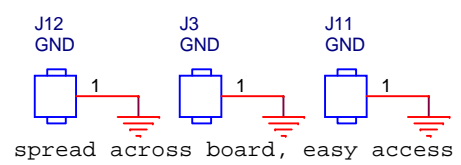
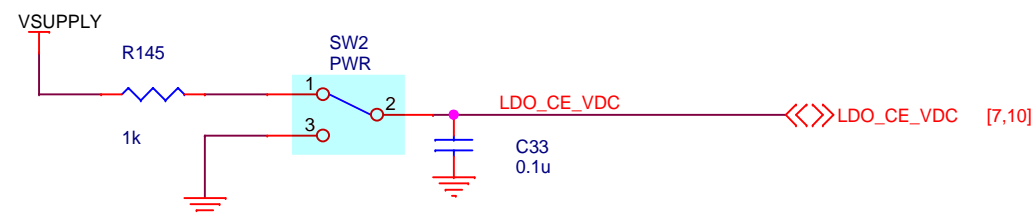
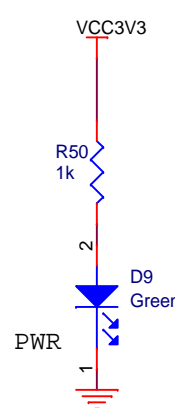
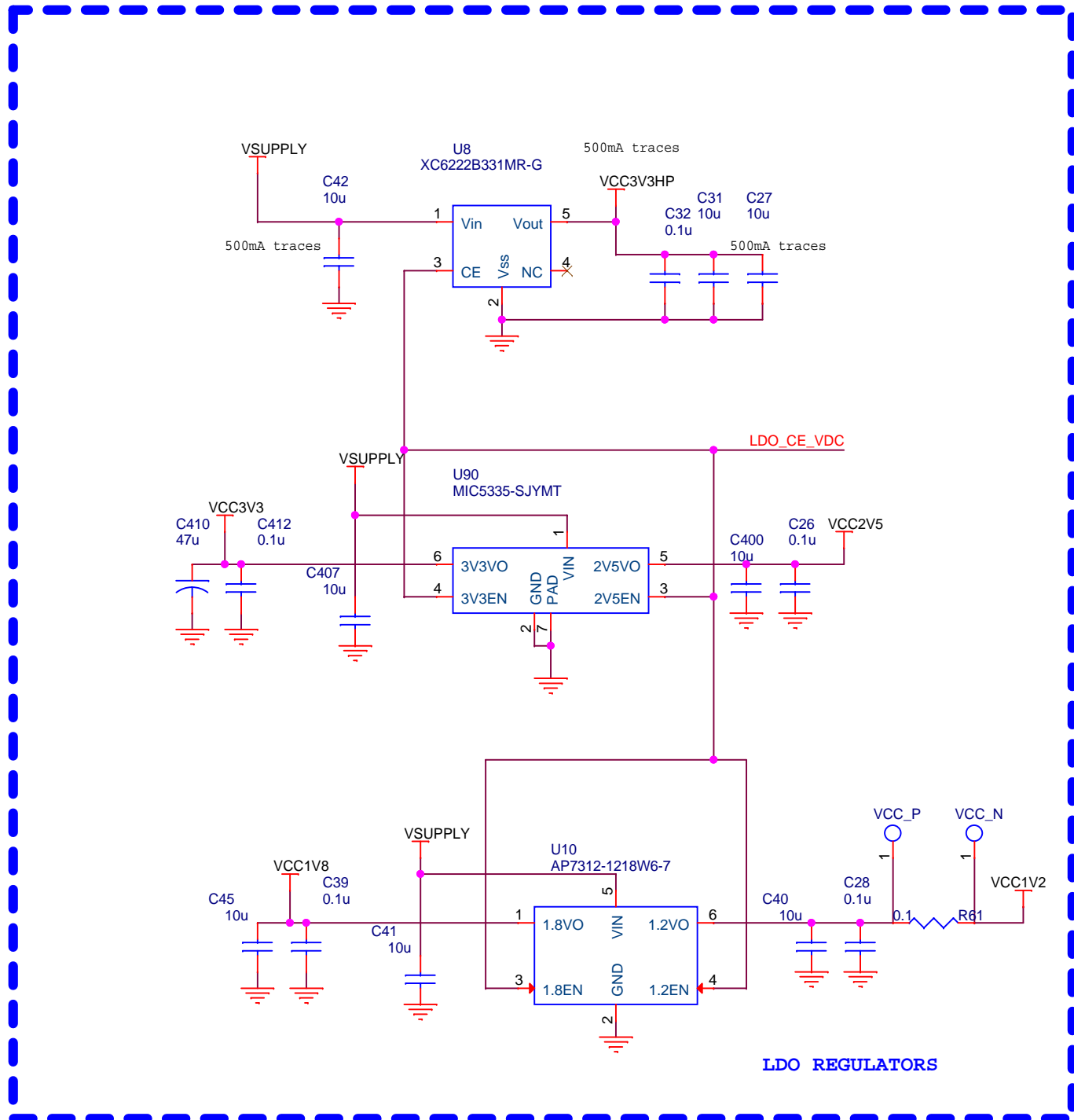
CAM_XCLK R56 0 <<<>> OSC_CLK [2,3,4,5,8,13]



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Title			
Camera Circuitry			
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Title Power Supplies

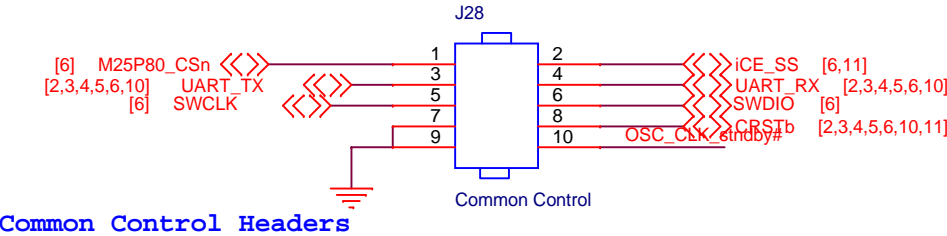
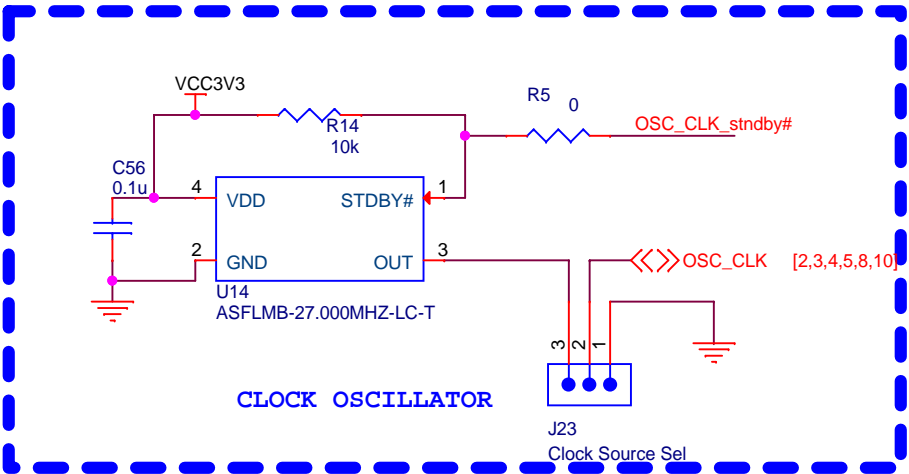
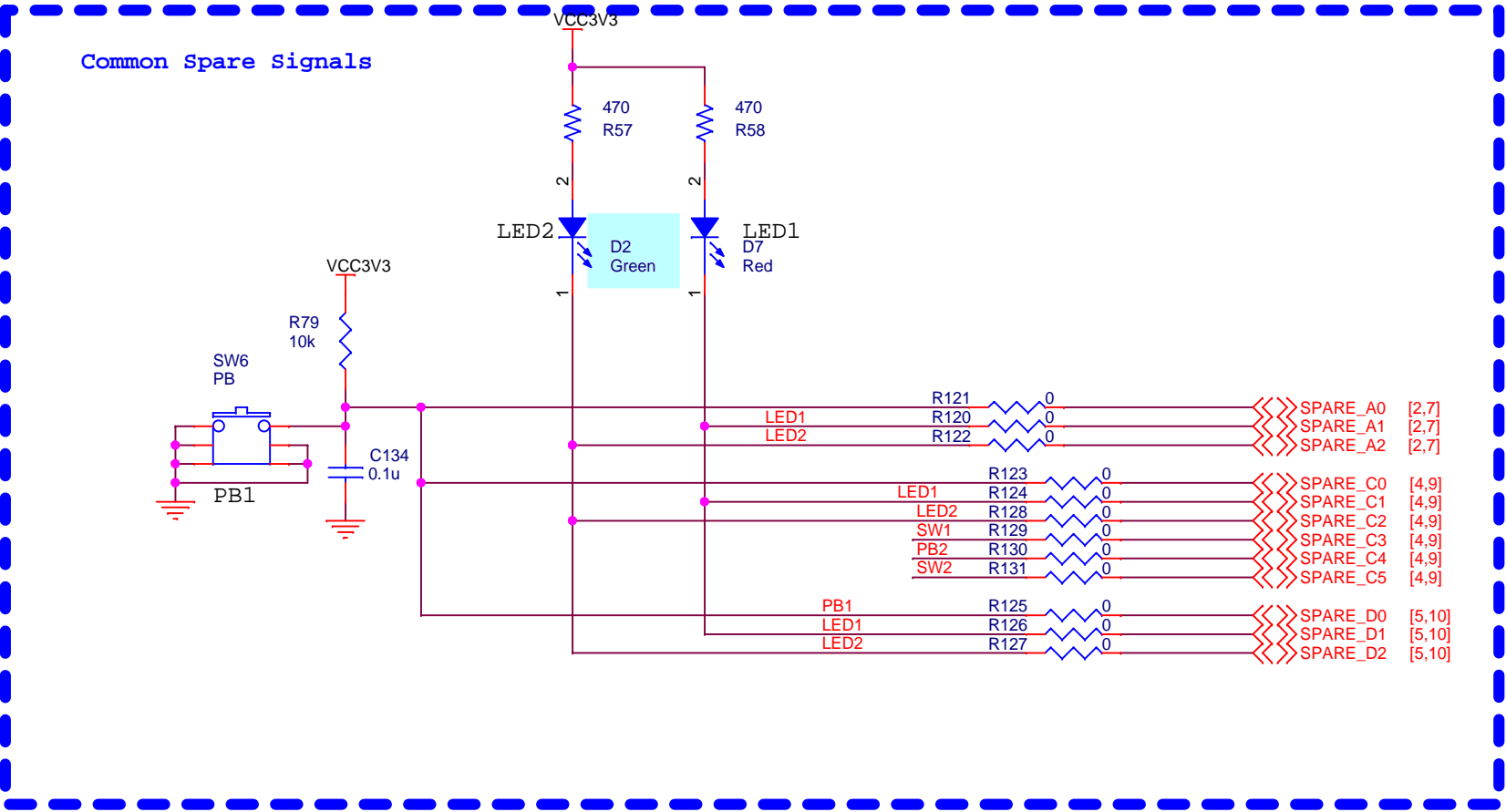
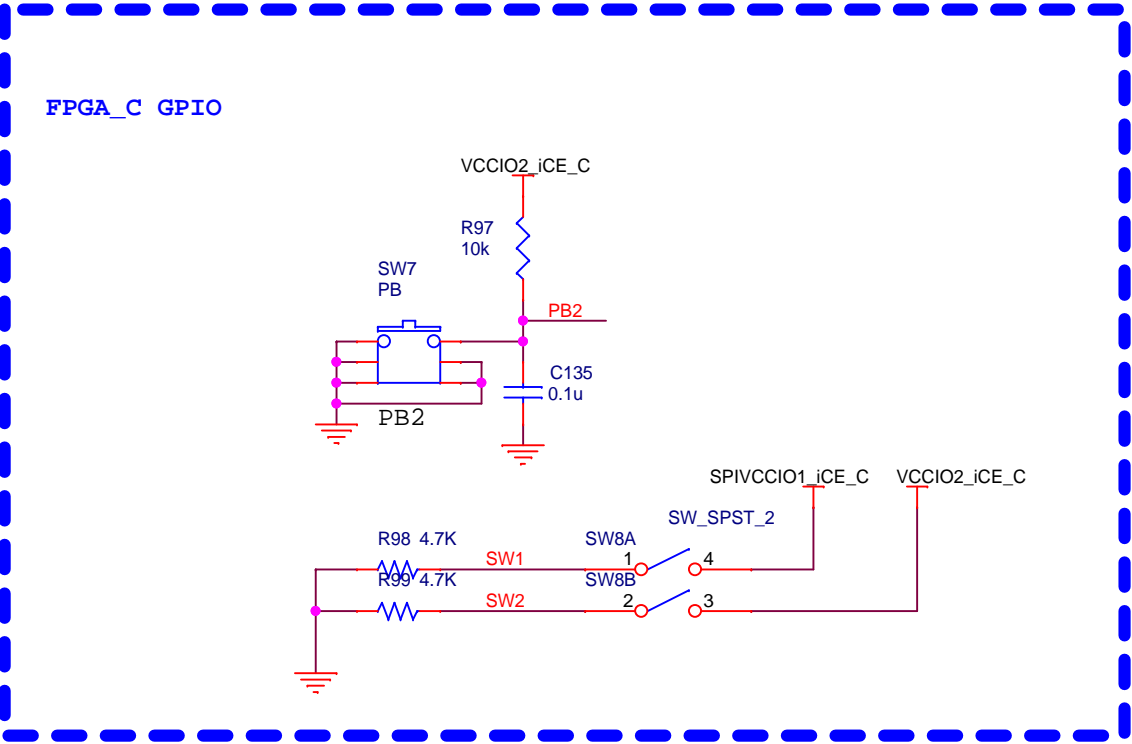
Size B Document Number Rev C

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SPARE_A0 shared with Display Controls (PB is default)
SPARE_A1 shared with Display Controls (LED is default)
SPARE_A2 shared with Display Controls (LED is default)

SPARE_C0 shared with Accel interrupt1 (PB is default)
SPARE_C1 shared with Accel interrupt2 (SW is default)
SPARE_C2 shared with PMOD (PB is default)
SPARE_C0 shared with PMOD (SW is default)
SPARE_C0 shared with PMOD (LED is default)
SPARE_C0 shared with PMOD (LED is default)

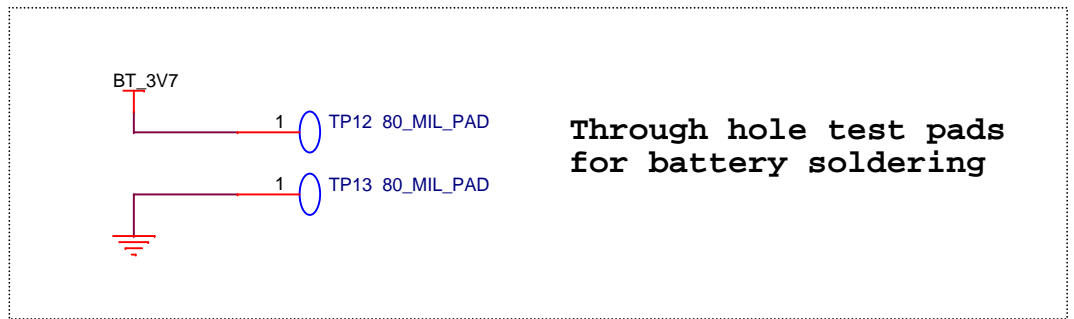
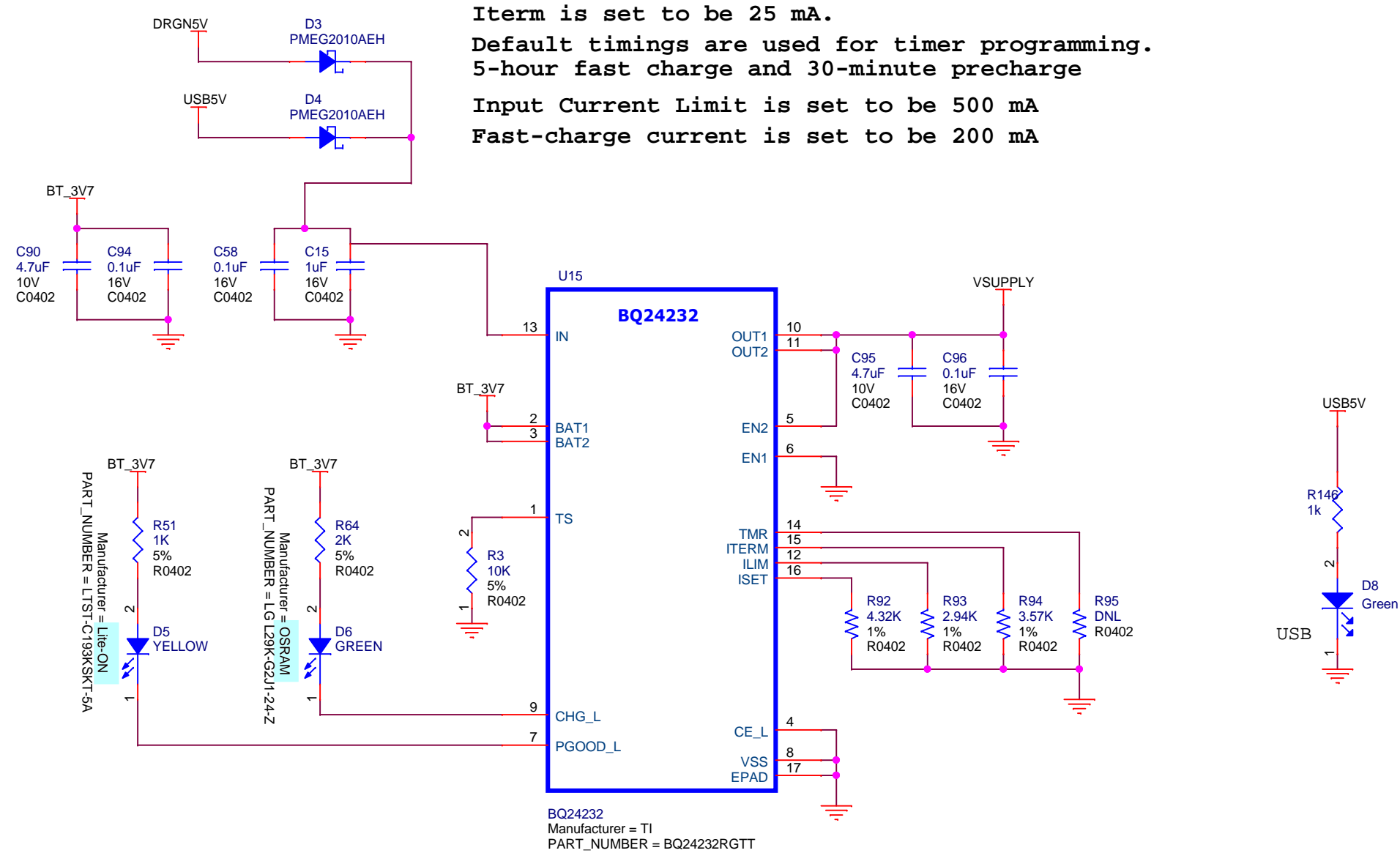
SPARE_D0 shared with Camera Parallel Interface (PB is default)
SPARE_D1 shared with Camera Parallel Interfaces (LED is default)
SPARE_D2 shared with Camera Parallel Interface (LED is default)



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Common Components					
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Title Battery Connector & Charger		
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		Rev C