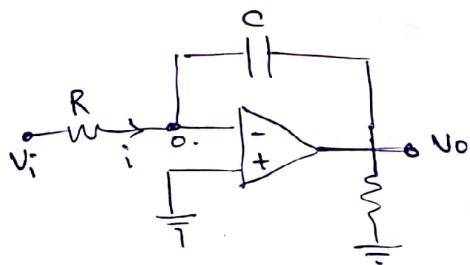


## Week-7:

integrator (ideal, practical)  
 differentiator  
 comparator.

→ integrator:



$$i = \frac{V_i}{R}, \quad i = \frac{d(-V_o)}{dt} \cdot C.$$

$$\therefore V_o = -\frac{V_i}{RC}$$

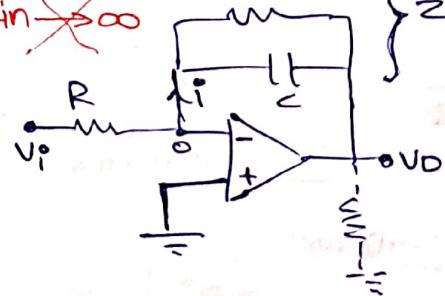
$$V_o = -\frac{1}{RC} \left( \int_0^t V_i(t) dt \right) - V_{C,t=0}.$$

integrator!

frequency domain:-

$$V_o(s) = \frac{-1}{RC} \frac{V_i(s)}{s} \Rightarrow \frac{V_o}{V_i} = \frac{-1}{RCS}$$

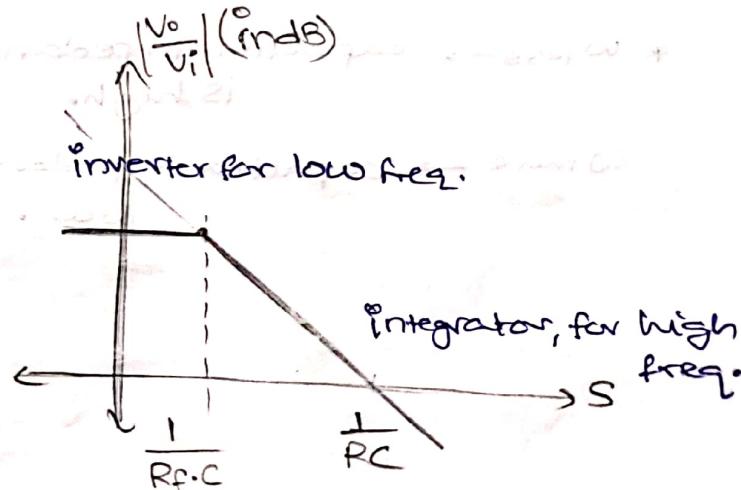
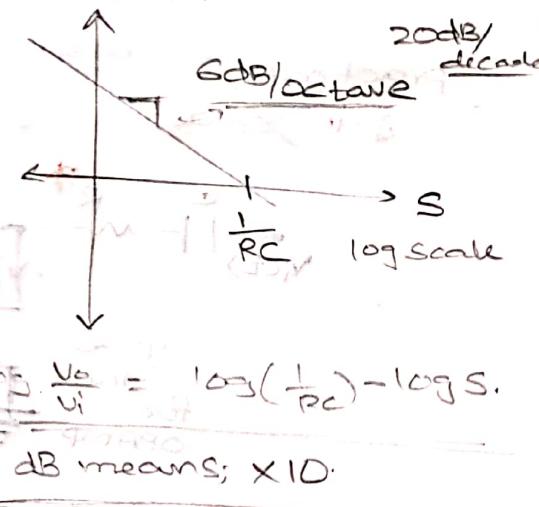
Practical: feedback res.



$$\therefore i = \frac{V_i}{R} = -\frac{V_o (1 + R_f C s)}{R_f}$$

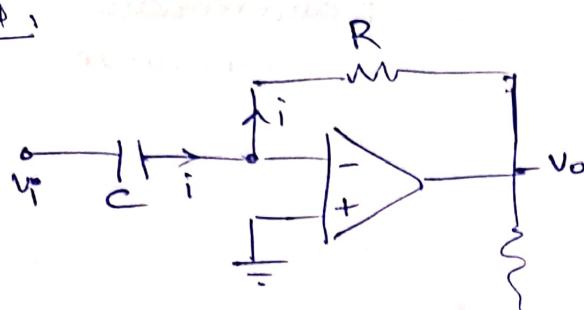
$$\therefore \frac{V_o}{V_i} = -\frac{R_f / R}{1 + R_f \cdot C \cdot s}$$

$$\frac{1}{Cs} = R_f$$



→ Differentiator:

ideal:



$$i = \frac{dVi}{dt} \cdot C \quad i = \frac{(-Vo)}{R}$$

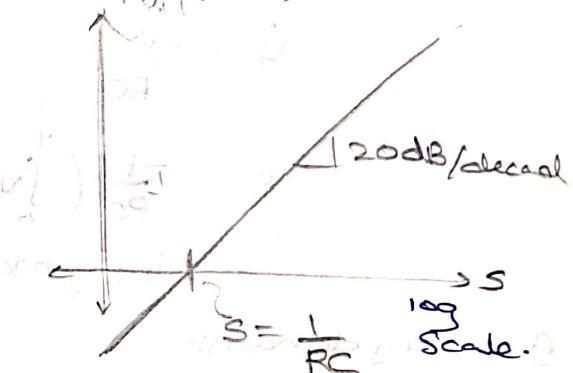
$$\therefore V_o = -RC \cdot \frac{dV_i(t)}{dt}$$

S-domain:

$$\frac{-V_o}{R} = V_i \cdot CS$$

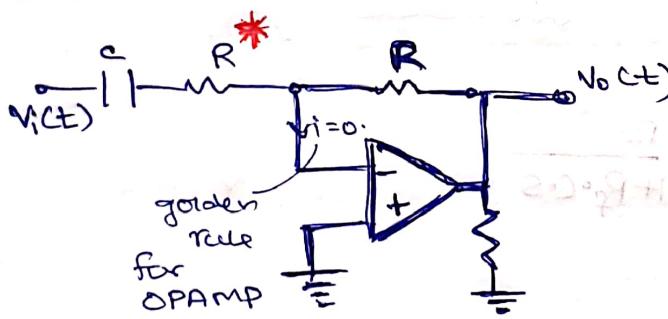
$$\therefore V_o = -RCS \cdot V_i$$

$$\frac{|V_o|}{|V_i|} (\text{in dB})$$



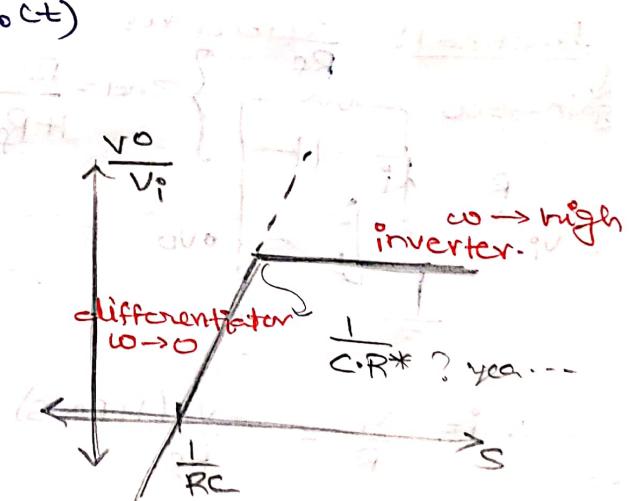
- practical:

gain  $\cancel{\rightarrow \infty}$



\*  $\omega$  less → capacitor impedance is high.

$\omega$  more → capacitor impedance is low.



## → comparator:

• opamp operating in open loop:-

- we safely say that

$$A_v \gg 1$$

∴  $V_o$  almost all the time

would be saturated.

an OPAMP:-

+V<sub>CC</sub>

$V_+$

$V_-$

-V<sub>CC</sub>

$V_o = A_v(V_+ - V_-)$

$V_o = \pm V_{CC}$

( $< V_{CC}$  impractical; but take  $V_{CC}$ )

like  $0.9 V_{CC}$ .

$V_o$

$V_{CC}$

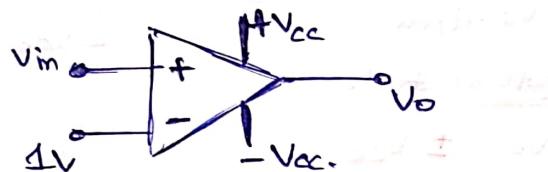
$V_o$

→ Duty cycle: How much time fraction?  $V_{in} > V_{ref}$ .

determine duty cycle of  $V_{out}$  for comparator circuit:-

$V_{in}$ 's peak to peak amplitude = 4V.

⇒ Amplitude = 2V.



( $2\sin\theta > 1$  for output to be high)

$$2\sin\theta \geq 1$$



$$\theta \geq 30^\circ$$

$$\text{duty cycle} = \frac{180 - 2(30)}{360} = \frac{150}{360} = \frac{5}{12}$$

→ DAC. digital to analogue converter:-

2 features of digital signal:-

- discrete wrt time.

- values are quantised.

analogue means material signals;

- intensity of sun

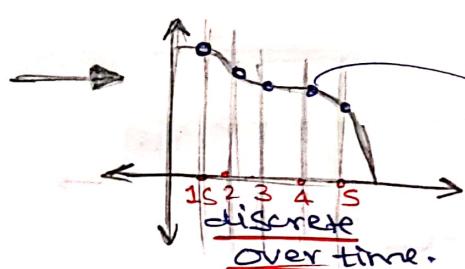
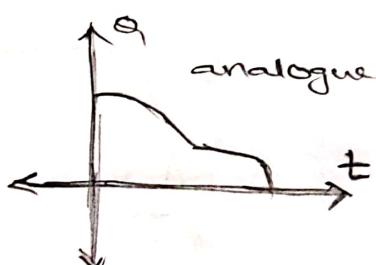
- temp.  $91^\circ C$

- pressure

continuous wrt time

e.g.  $91^\circ C$

may have continually varying values.

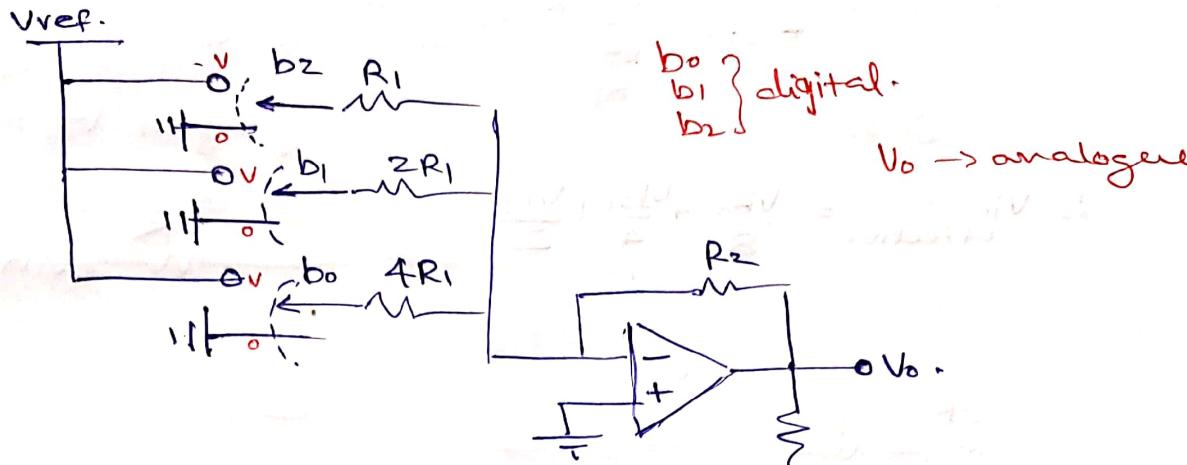


Say = 1.3V.

our digital signal may be quantised like  
or 1V 2V ...

•  $1.3V \rightarrow 1V$   
analogue digital

## Binary weighted DAC:-



$$V_o = \frac{R_2}{R_1} \left( b_2 + \frac{b_1}{2} + \frac{b_0}{2^2} \right)$$

$$= \frac{R_2}{2^2 R_1} (2^2 b_2 + 2^1 b_1 + 2^0 b_0)$$

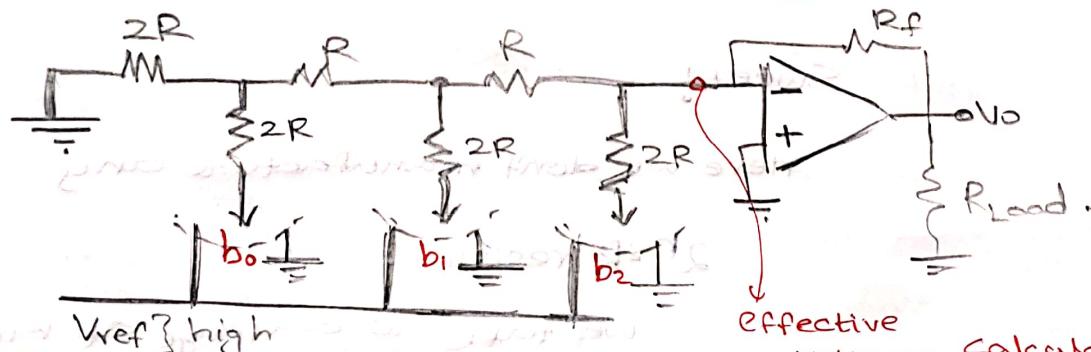
Binary evaluation.



## R-2R DAC:-

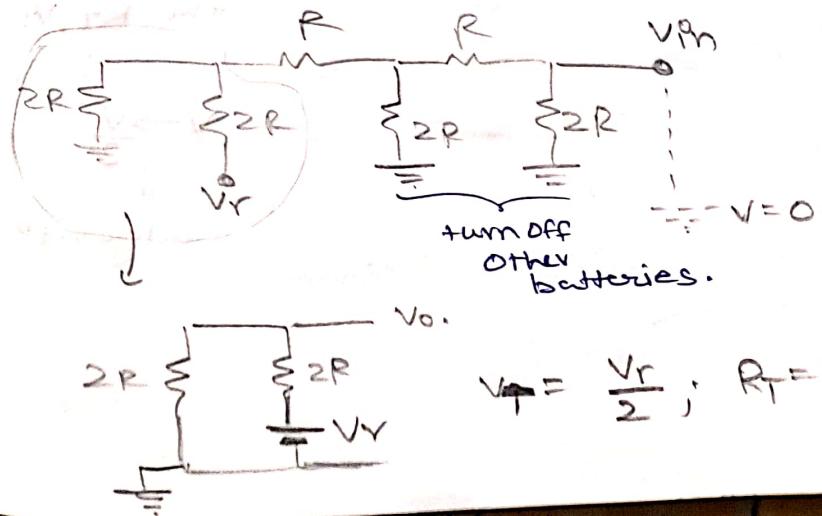
only network of R, 2R resistors.

But here; as num. bits increase; difficult to make  $2^n R$ .  
 ∴ Binary DAC not famous

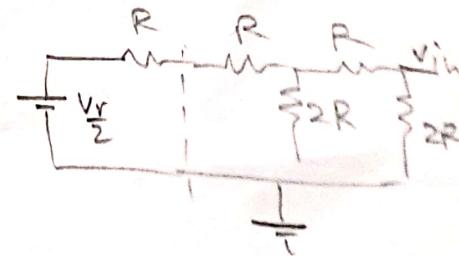


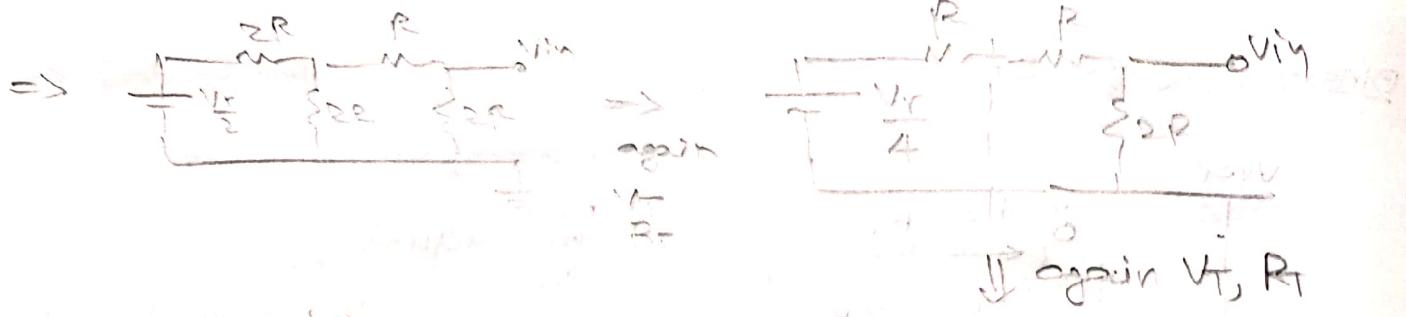
Effective Voltage; calculate by  
 by thevenin Superposition  
 equivalent of  $b_0, b_1, b_2, \dots$

Seeing  $b_0$ :

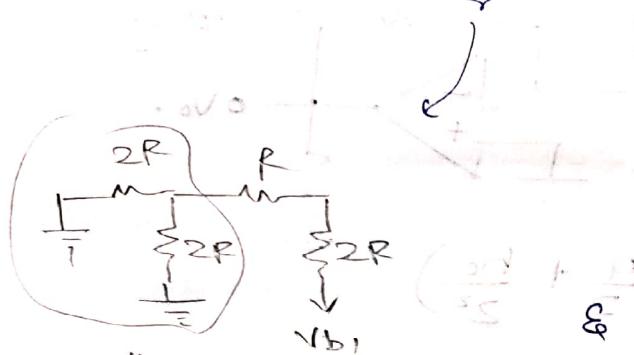


$$V_T = \frac{V_r}{2}; R_T = R.$$



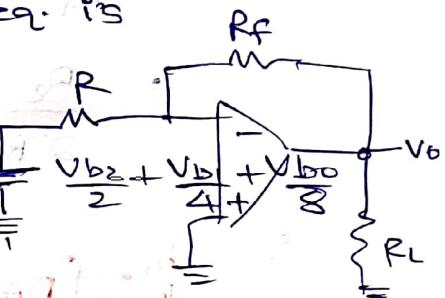


$$\therefore V_{in \text{ effective}} = \frac{V_{b2}}{8} + \frac{V_{b1}}{4} + \frac{V_{b2}}{2}$$

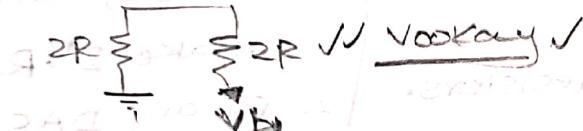


$$\left( \frac{2R}{3R} + \frac{1}{2} + \frac{1}{2} \right) \cdot 8 = 12V$$

$V_T$  eq. is



$$\therefore V_O = \frac{R_F}{R_{in}} \times \left( \frac{V_{b2}}{8} + \frac{V_{b1}}{4} + \frac{V_{b0}}{2} \right)$$



Sweet!

Here we don't manufacture any

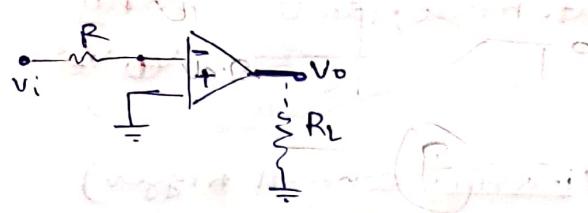
$2^{n+1}R$  resistor.

We take advantage of nice  
Algorithm.

the  $R_T, V_T$

$V \rightarrow \frac{V}{2}$   
algorithm.

## Feedback:



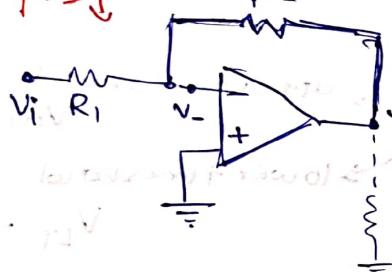
open loop comparator.

$$V_o = A_v (V_+ - V_-)$$

$$\frac{V_o}{V_i} = A_v = \frac{R_o}{R_1 + R_2}$$

(negative feedback)

means  
↑ → ↓



$$A_v (V_+ - V_-) = V_o$$

holds

$$V_- = \frac{V_i R_2}{R_1 + R_2} + \frac{V_o \cdot R_1}{R_1 + R_2} \quad \text{--- (1)}$$

$$V_o = A_c (V_+ - V_-) \quad \text{--- (2)}$$

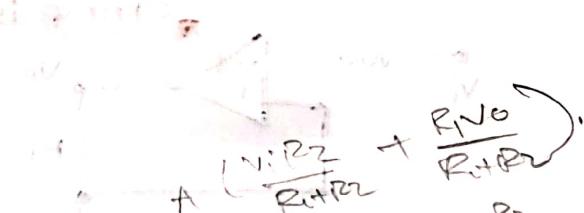
now; Vi is constant; V+ too!

(while disturbing  
the circuit from  
equilibrium)

say V- ↑ → Vo ↑ →  
from (1)      ↓  
                ↓  
                from (2)  
Hence  
stable  
(equilibrium.)

Hence; this setup when

OPAMP is amplifier

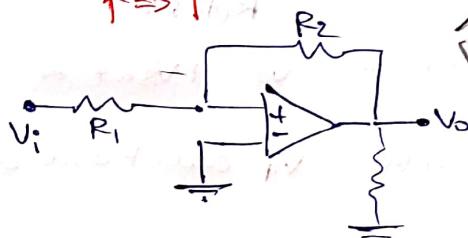


$$\frac{V_o}{V_i} = \frac{R_o}{R_1 + R_2} + \frac{R_o V_o}{R_1 + R_2}$$

$$\frac{V_o}{V_i} = \frac{A_c}{1 + A_c}$$

(positive feedback)

↑ → ↑



$$V_o = A_c (V_+ - V_-)$$

not hold.

$$V_+ = \frac{V_i R_2}{R_1 + R_2} + \frac{R_o V_o}{R_1 + R_2} \quad \text{--- (1)}$$

$$V_o = A_c (V_+ - V_-) \quad \text{--- (2)}$$

\* V<sub>+</sub>, V<sub>-</sub> being constant;  
disturb V<sub>o</sub>

V<sub>o</sub> ↑ → V<sub>+</sub> ↑ → V<sub>o</sub> ↑↑  
from (1, 2)

unstable equilibrium.

till V<sub>o</sub> is limited by  
saturation.

\* gain is increased greatly.

this setup when

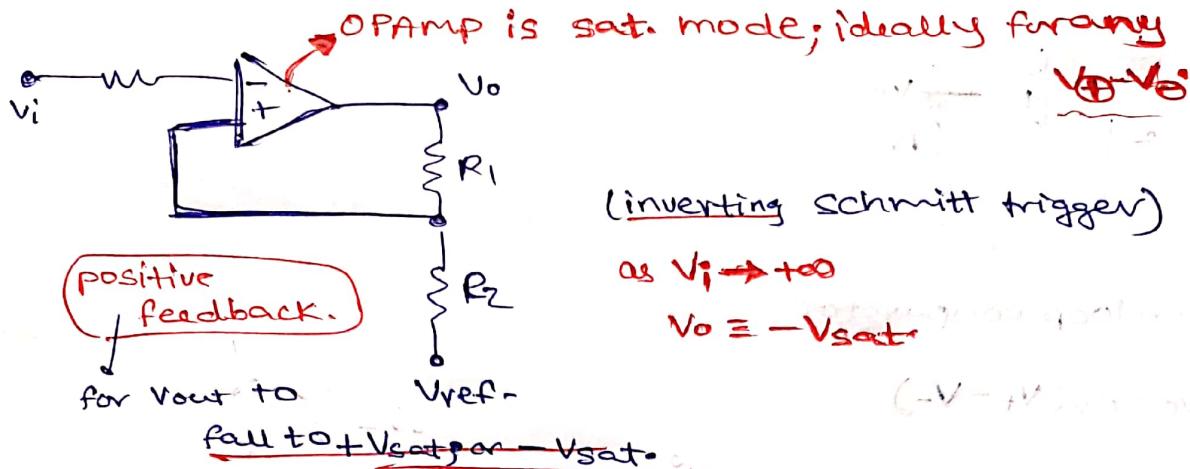
OPAMP is  
compensator.

Schmitt trigger.

\* note: this is a "non-inverting" op-amp and it is straight forward to understand.

## Schmitt trigger:-

A comparator; in which V<sub>ref</sub> is derived from a fraction of V<sub>out</sub>. } hence memory!



(inverting Schmitt trigger)

as  $V_i \rightarrow +\infty$

$$V_{out} = -V_{sat}$$

$$\therefore V_+ = \frac{R_2 V_{out} + R_1 V_{ref}}{R_1 + R_2}$$

since  $V_{out} = +V_{sat}$  or  $-V_{sat}$ ;

the  $V_+$  can have only 2 values

$$(-V_{sat}) \text{ or } (+V_{sat})$$

$$V_{LT} \text{ or } V_{UT}$$

upper threshold

lower threshold

$$V_{LT}$$

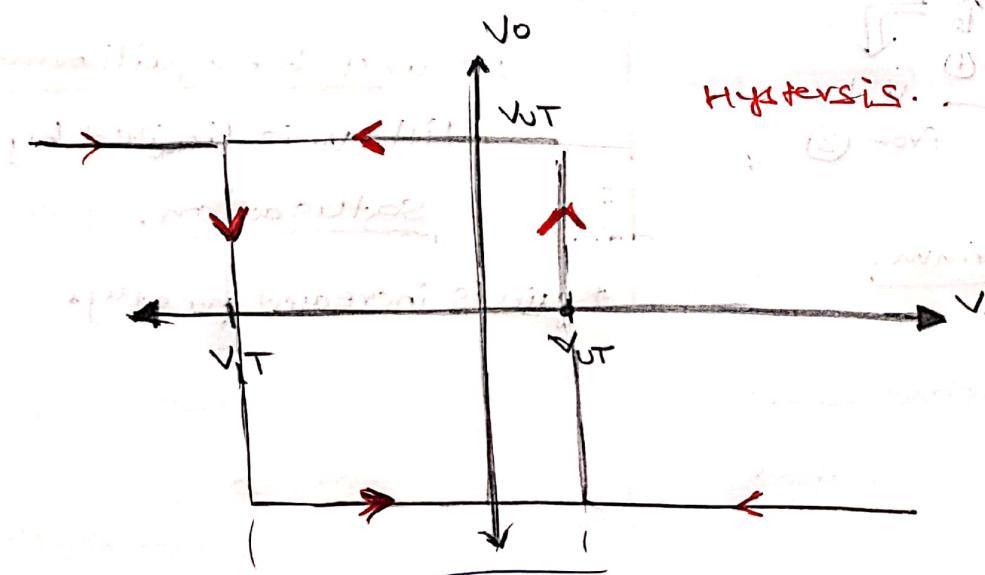
$$Eg V_{LT} < V_{UT}$$

Eg let  $V_{out} = V_{sat}$

$$\therefore ( \Leftrightarrow V_+ = V_{UT} ) = \frac{R_2 V_{sat} + R_1 V_{ref}}{R_1 + R_2}$$

$$V_{LT} = \frac{-R_2 V_{sat} + R_1 V_{ref}}{R_1 + R_2}$$

Hysteresis.

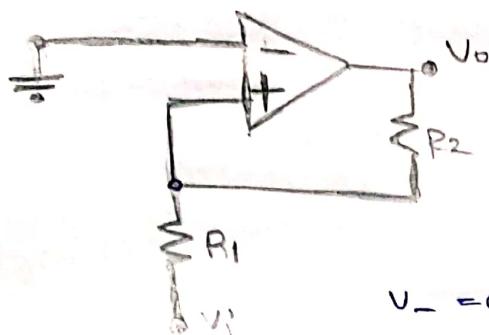


Hence; it has "memory"! even if  $V_i = 0$ ; Vout is not unique.  
it remembers.

- non-inverting Schmitt trigger:-

Positive feedback

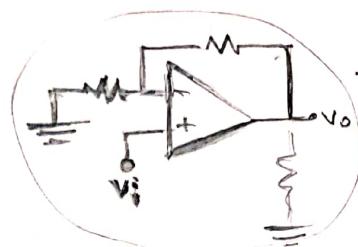
for  $V_{out}$  to fall to  $+V_{sat}$  or  $-V_{sat}$ .



$$V_- = 0.$$

$$V_+ = \frac{R_2 V_i + R_1 V_o}{R_1 + R_2}$$

negative feedback; used in case of Amplifying opamp



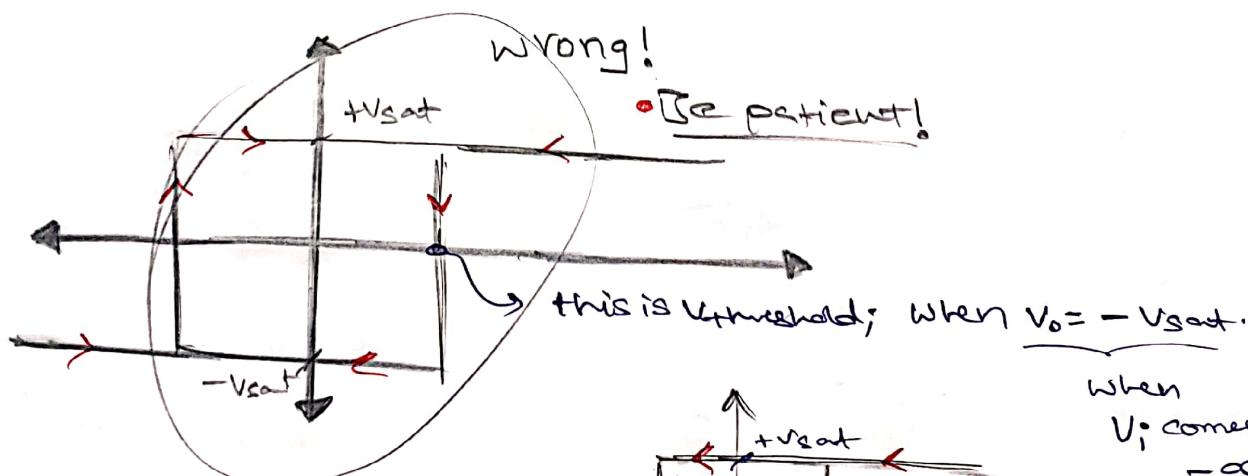
-ve feedback acts as amplifier.

∴ for threshold voltage;

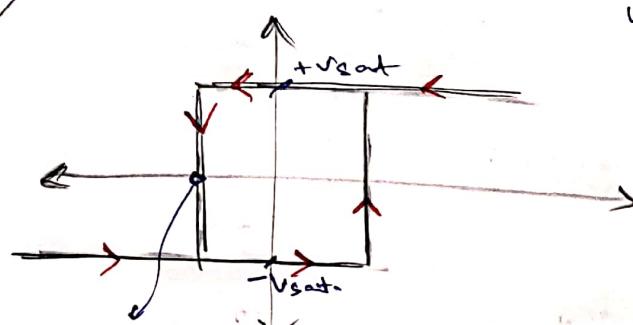
$$V_i^* = -\frac{R_1 V_o}{R_2}$$

$$\therefore \text{lower threshold } V_{LT} = -\frac{R_1 V_{sat}}{R_2}$$

$$V_{UT} = \frac{R_1 V_{sat}}{R_2}$$



when  $V_i$  comes from  $-\infty$ .



this is the  $V_{threshold}$ ; when  $V_o = +V_{sat}$ .

- square wave generator
- $\Delta^1$  wave generator ] extra.

## Week-8:-

+ digital circuits

+ logic gates

+ Boolean alg.

+ encoder, ADC

- \* All naturally occurring signals are analogue.

- sound  
- temperature  
- intensity.

$V_{out}$   
continuous  
in time &  
values.

- digital signal: 0 or 1

digital circuit: to manipulate these 0's, 1's.

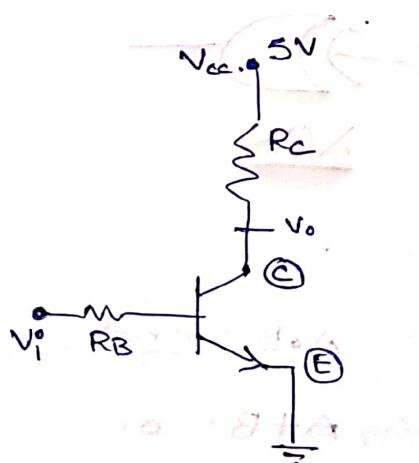
0 : low band 0V ;  $1\Omega$

1 : high band 5V ;  $10^5 \Omega$

### Advantages of digital data:-

- data signal distortion can be deferred easily.
- data can be processed using computers.
- can be stored in media.
- can program a functionality.

### \* BJT inverter:-



NOT gate.

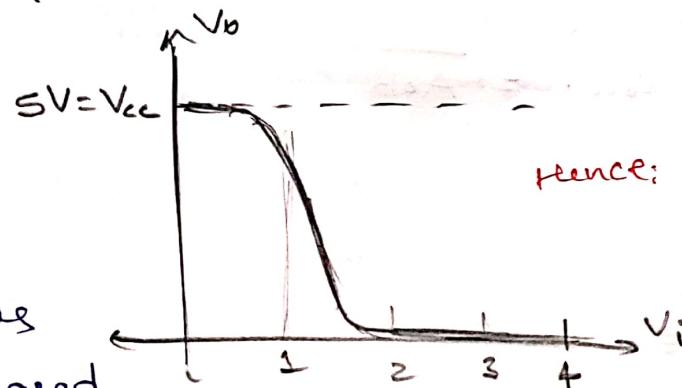
transistor  
acting as  
switch; based  
on

if  $V_{Base} \approx 0$ ; then transistor is off.

open switch.  $\Rightarrow$  no current flow.  
(hence, voltage flow)

if  $V_{Base} \approx$  high; then transistor is on.

closed switch.  $\Rightarrow$  full current flow.  
(no voltage flow...  
i.e.  $V_O = V_{cc}$ )



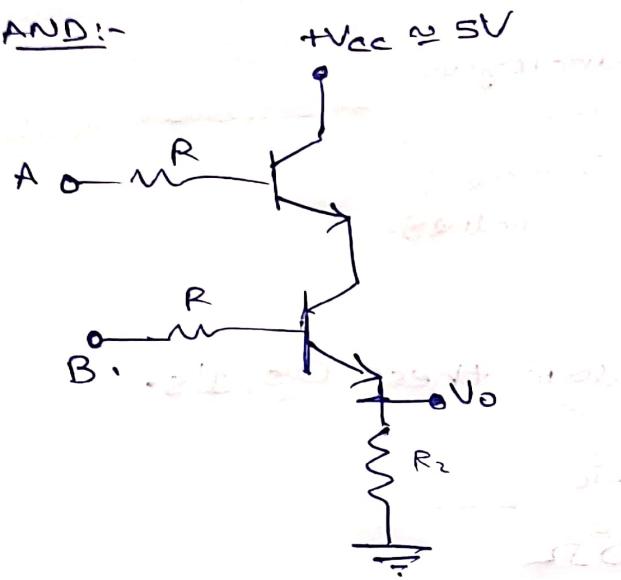
$V_i - low \Rightarrow V_o - high$

$V_i - high \Rightarrow V_o - low$

sway

Now; let's try to make gates; with BJTs

AND :-



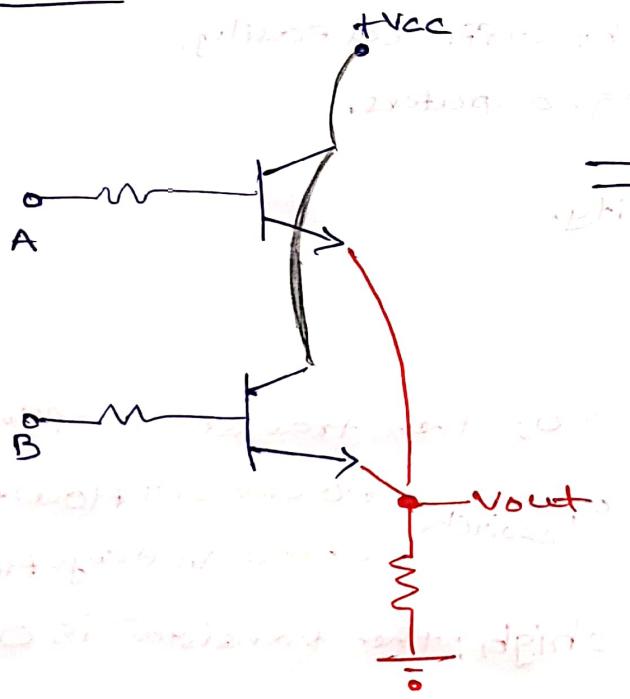
transistor as a switch.

when  $V_{base}$  is  $\uparrow$ ,  $I_C$  is  $\uparrow$



NAND

OR :-

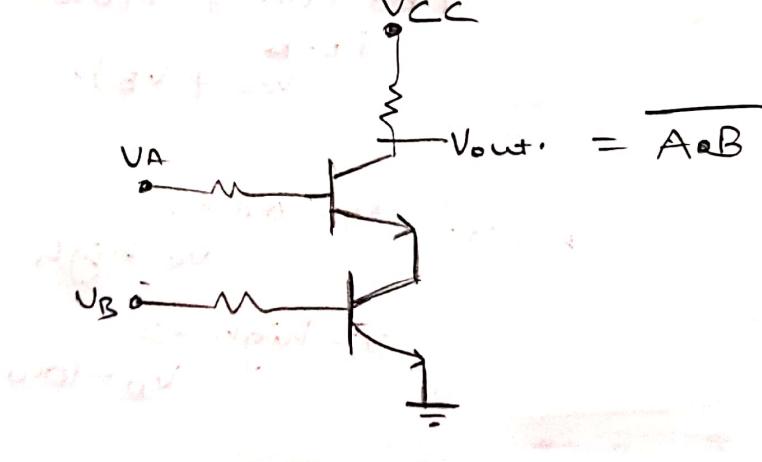


NOR



XOR

NAND :-



$A \cdot B$ : and

$A + B$ : or

70A  
70B

## Combinational Logic

digital circuits; formed using only logic gates; without involving

feedback loops

synchronized clock pulses

are known as combinational circuits.

Logic

- \* has inputs, logic gates, outputs.
- \* output depends on present inputs.

Not on past inputs; no memory.

- 1) Form truth table.  
2) Boolean expression can be obtained now.

SOP                      Canonical Forms              POS

Sum of products:- "Well established"

A	B	Product
0	0	0
0	1	all
1	0	b <sub>1</sub>
1	1	0

consider these two minterms

product of sums:-

A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0

Consider these two write sum form

a)  $\bar{A} \cdot B$   
b)  $A \cdot \bar{B}$

this is product form...

minterm form!

∴ minimum term  
of all inputs is answer.

a)  $A + B$

b)  $\bar{A} + \bar{B}$

max term format.

sum form

max term.

solution =  $(\bar{A} \cdot B) + (A \cdot \bar{B})$

$(A+B) \cdot (\bar{A}+\bar{B})$

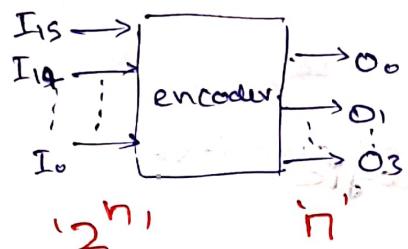
SOP; POS

may not be simplified boolean expressions.

Encoder: ADC : analogue to digital converter.

convert decimal to binary.

"binary encoder"



$$(2^n)$$

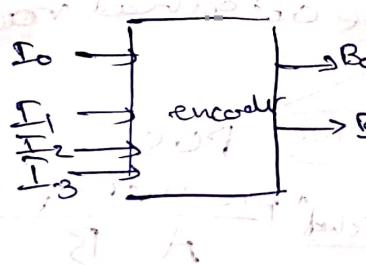
$$n$$

Becoz; n bits can represent  $2^n$  numbers.

\* convert decimals in 0-3 to binary.

4:2 Binary encoder.

meaning; output has 2-states.



Truth table:

I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	0	0	1
1	0	0	0	0	0

∴ we could say;

$$B_0 = \overline{I_3} \overline{I_2} \overline{I_1} I_0 + I_3 \overline{I_2} \overline{I_1} I_0 \quad ] \text{direct SOP.}$$

$$B_1 = \overline{I_3} \overline{I_2} I_1 \overline{I_0} + \overline{I_3} I_2 \overline{I_1} \overline{I_0} \quad ] \text{minterm.}$$

\* However; we need a 'simplified' expression for  $B_0$  &  $B_1$ :

otherwise; circuits will be costly.

for expression; we need  $2^4$  rows of truth

when data is 'don't care'  $\rightarrow X$ .

### K-map:-

#### Karnaugh map

		I <sub>1</sub> I <sub>0</sub>	00	01	11	10
		I <sub>3</sub> I <sub>2</sub>	00	01	X	1
		00	X	0	X	1
		01	0	X	X	X
		11	X	X	X	X
		10	1	X	X	X

B<sub>0</sub>

adjacent should have  
a common  
term.

!!

Rules for K-map grouping:- 1) write last row on top, priority encoder.  $\rightarrow$  to take some more simplified. (next pg).

- 1) Group adjacent cells containing 1 or X; in such away that maximum grouping is obtained.
- 2) Grouping shall be of sizes  $1, 2, 4, 8, 16, \dots 2^n$   $\therefore$  rows, columns are also  $2^n$  size.
- 3) grouping shall be horizontal or vertical.
- 4) Groups can overlap. (in order to have max. size for group).

- 5) No. of groups should be minimum as possible.

(to obtain simplified expression)

- 6) Once groups are obtained; write minterm for each group; taking their common input for each row/column & join with SOP.

to get minimal / simplified expression.

every '1' should be in a group.  
Should be 2<sup>n</sup> size;  
max possible, without  
containing any 0's.

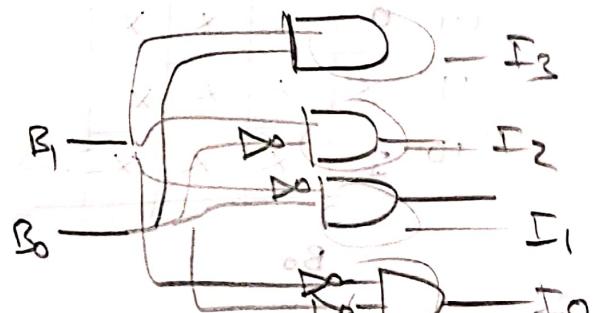
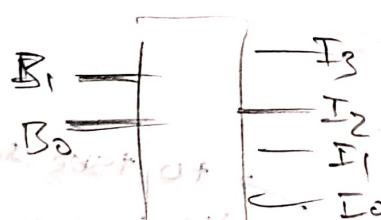
Interlap is allowed;

$I_3, I_0$

$I_3, I_2$	00	01	11	10	$I_1, I_0$
00	x	0	x	1	
01	0	x	x	x	
10	x	x	x	x	
11	1	x	x	x	
$I_{S0}$					

$B_0 = \underbrace{(I_3) + (I_1)}$  we only seek to maximize size around 1.

rough:



possible due to  $B_1, B_0 \in I_3$ ,  $I_2 \in I_1$  and  $I_0$  only gates!

hence  
combinatorial logic circuit

0	0	0	0	0	0	0
0	1	0	0	0	1	0

minimized AND gate output

$B_0$	0	1
0	0	0
1	0	1

$\therefore I_3 = (B_0 \cdot B_1)$

minimized AND gate output

$B_0$	0	1
0	0	0
1	1	0

$\therefore I_2 = (\overline{B_0} \cdot B_1)$

## Priority encoder:-

Now, even if multiple inputs are high, the MSB which is high is taken.

Hence:

$I_3 \ I_2 \ I_1 \ I_0 \quad B_1 \ B_0$  (Ans)

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

0 0 1 X 0 1

0 1 X X 1 0 0 0 0 0 0 0 0 0 0 0 0

~~0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0~~

~~0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0~~

input is

decimal...  $2^n$  input terminals;

which is fired; inp is that...

If  $I_3$  is fired;  $B_0$  is inp

Binary encoding is

$I_3 \ I_2$	00	01	11	10
00	*	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

size 21 ✓

grouped  
can be together!

size 23 ✓

$= I_2 \ I_1$

write last row  
on top  
again!

left row  
on right  
again!

$$= (I_3 \bar{I}_2 \bar{I}_1) + I_3$$

Simplest!

k-map! (half).

to increase  
grouping  
size.

\* Applications :-  
for analog to digital conversion!

Use

1) potential divider

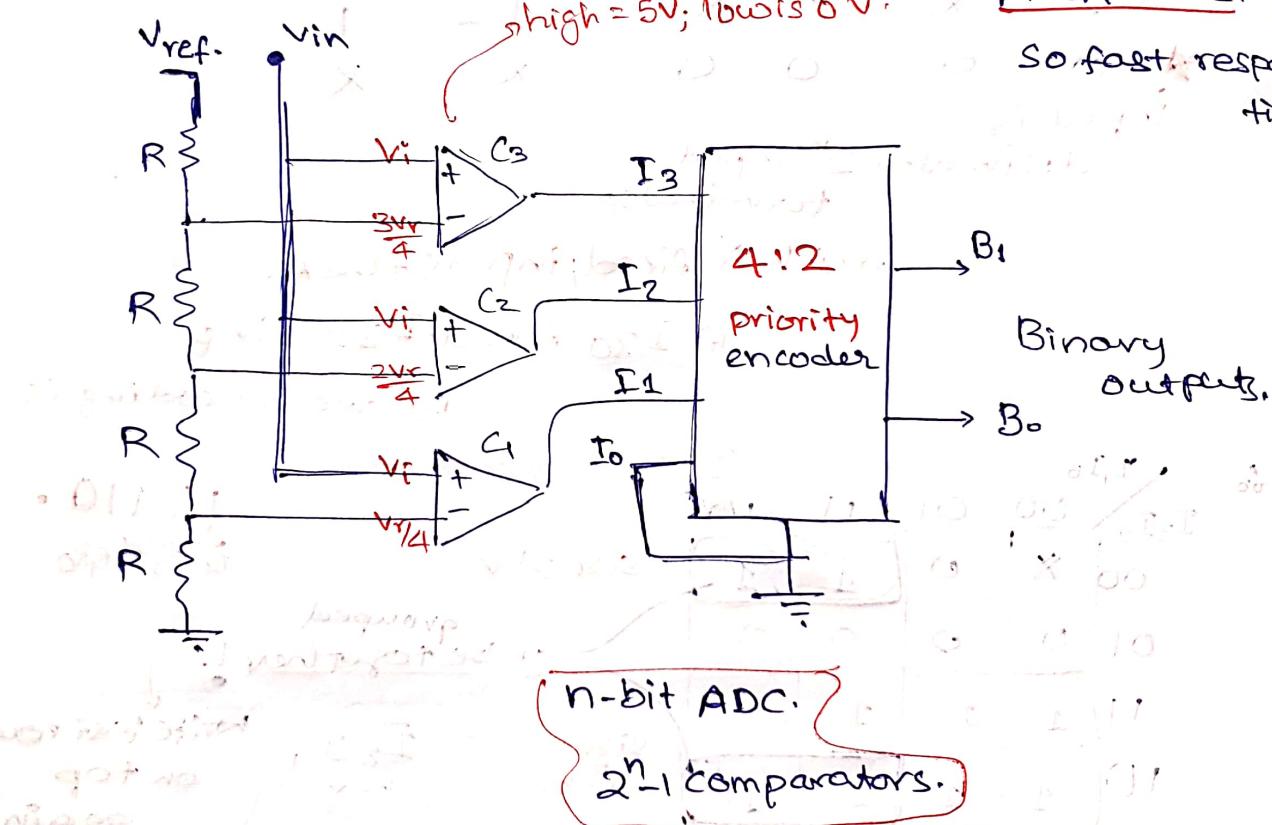
2) comparator.  $2^n$

3) send into  $2^m : n$  encoder  
binary.

→ 2-bit Analogue to digital encoder:-

Flash ADC.

So fast response time.



n-bit ADC.

$2^n - 1$  comparators.

now; truth table:-

<u>Working range</u>	<u>I<sub>3</sub></u>	<u>I<sub>2</sub></u>	<u>I<sub>1</sub></u>	<u>I<sub>0</sub></u>	<u>B<sub>1</sub></u>	<u>B<sub>0</sub></u>	<u>V</u>
$0 \leq V_{in} \leq V_{ref}/4$	0	0	0	0	0	0	0
$V_{ref}/4 \leq V_{in} \leq 2V_{ref}/4$	0	0	1	0	0	1	1
$2V_{ref}/4 < V_{in} \leq 3V_{ref}/4$	0	1	X	0	1	0	1
$V_{in} > 3V_{ref}/4$	1	X	X	0	1	1	1

Grounded

Valid bit  
to see if the input  
to encoder  
is valid  
(i.e.,  
at least one  
high is true)

## Resolution of ADC:-

the smallest input voltage change, which will result in the change in the digital output.

n-bit ADC :-

$$= \frac{V_{in(\max)}}{2^n}$$

is resolution.

$V_{in(\max)}$  is full scale voltage of given input signal.

\* for DAC;

$$R-2R \text{ maybe; resolution} = \frac{V_{out(\max)}}{2^n}$$

## → Sequential circuits:-

gates, encoder → combinational logic circuits..

{ Latch, flip-flops → sequential logic circuits  
build counters, registers, output depends on current inputs

ALUs. on current inputs

post outputs

post inputs (?).

- Have TIME elements

Eq: Resistor → no memory.

capacitor } Yes  
inductor } memory.

Clock:-

- complex digital circuits; designed for synchronous operations...

- transition of various signals, are synchronized with clock.

Clock signal - period

- positive-going transition or negative-going transition.



processor; 1GHz clock...  
2.3 GHz etc...

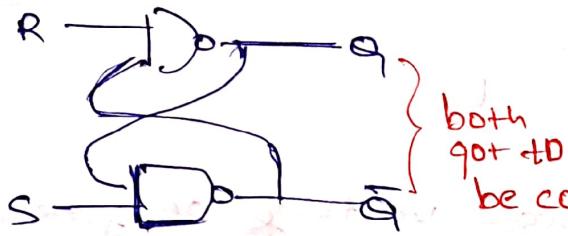
clock frequency determines overall speed of circuit.

## (Latch: to hold.)

→ RS Latch:

Reset - Set Latch.

i) NAND Latch:



both got to be complement!

every circuit is shown;

so that when

$S=1$   
 $R=0$ ;  $Q=1$ , Set.

$R=1$ ,  $Q=0$  re-set.

if  $R=0, S=0$

then  $Q=1, \bar{Q}=1$  not complement!

∴ invalid.

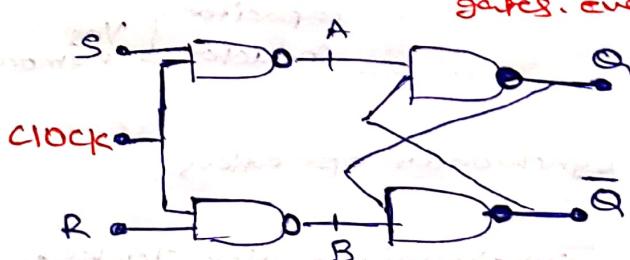
invalid ...

Truth table:-

reset	set.	$Q$	$\bar{Q}$	should be complement.
1	0	(Reset = 1)	1	↳ bcoz, $Q_1=1$
0	1	(Set = 1)	0	1) Say $Q=0$ then $Q_2=1 \equiv \bar{Q}$
1	1	Previous; $Q_{n+1}=Q_n$	1	2) say $Q_2=0$ $\therefore Q=1 \equiv \bar{Q}_2$
0	0	invalid	0	3) say $Q=1, Q_2=1$ $\in R=1, S=1$ or rather; "not used".

→ Clocked RS Latch.

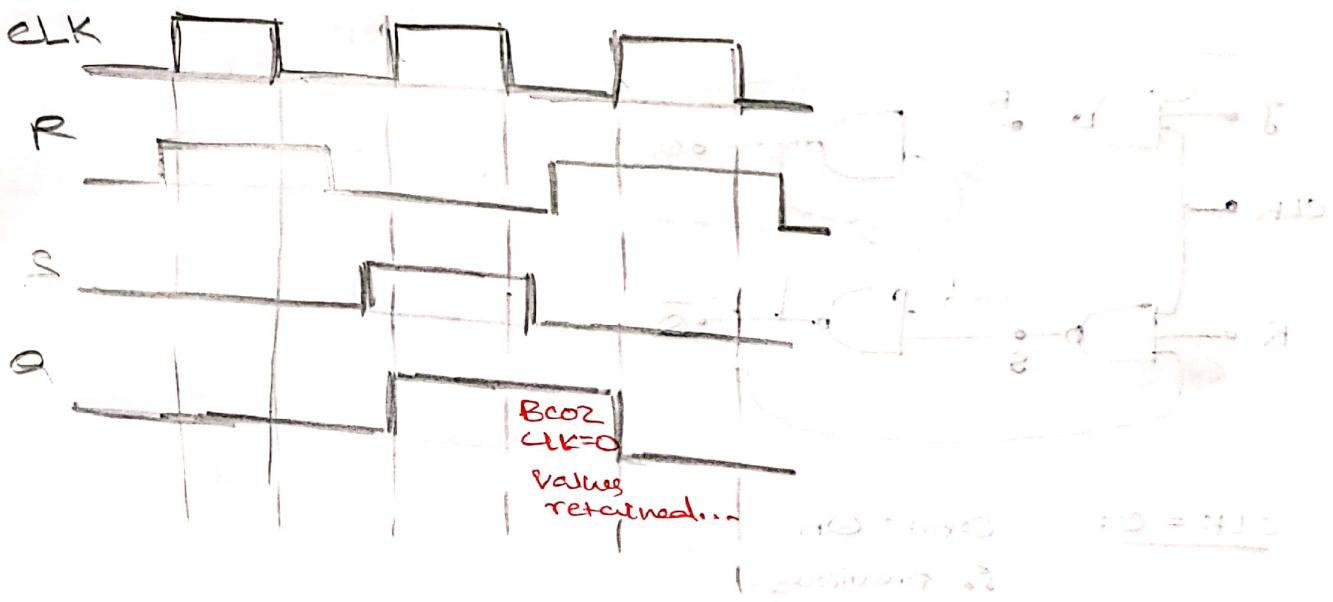
NAND gates. everywhere.



clock.	R.	S.	$Q$	$\bar{Q}$
0	x	x	previous.	
1	1	0	0	1
1	0	1	1	0
1	1	1	invalid	
1	0	0	previous.	

→ Timing diagrams:-

\* for clocked RS Latch:



→ edge triggered flip-flops:-

Clocked R.S-latch :- level-sensitive.

if  $CLK = 1$ ; then changing allowed.  
else, no changing.

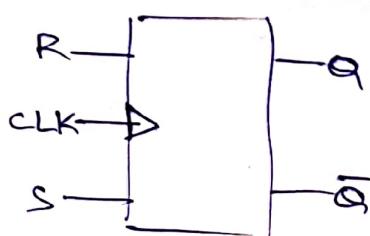
edge-sensitive flipflop :- edge-sensitive

circuit changing at active clock edge...

positive edge-triggered : during  $0 \rightarrow 1$ .

$Q = \text{HOLD} \& L = \text{HOLD}$  in  $CLK$

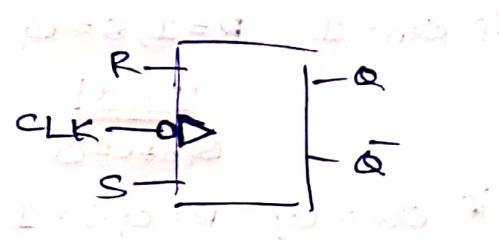
negative edge triggered : during  $1 \rightarrow 0$ .



+ve edge-triggered

flip-flop.

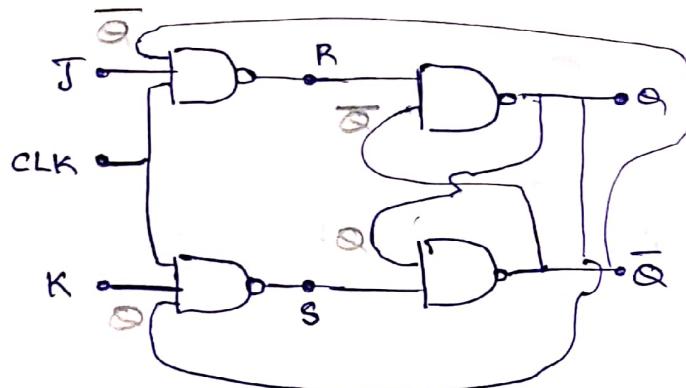
representation



negative edge triggered.

## $\rightarrow$ JK flipflops:-

↳ inputs are J, K. also scientist name - - - - -



$$\underline{\text{CLK} = 0}: \quad Q_{n+1} = Q_n \\ \text{so previous.}$$

$$\underline{\text{CLK} = 1}: \quad$$

$$a) J=0, K=0$$

$$Q_{n+1} = Q_n: \text{E = 4.5V}$$

~~b)  $J=1, K=0$~~

~~$Q_{n+1} = 1 \text{ (and so is } Q_n?)$~~

~~c)  $J=0, K=1$~~

~~$\overline{Q_{n+1}} = 1 \Rightarrow Q_{n+1} = 0$~~

~~d)  $J=1, K=1$~~

if  $Q_n = 1; R = 1, S = 0$

reset!

$$Q_{n+1} = 0$$

if  $Q_n = 0; R = 0, S = 1$

set!

$$Q_{n+1} = 1$$

$\therefore Q_{n+1} = \overline{Q_n} \quad \text{toggled!}$

∴ Truth table.

CLK	I	K	Qn+1
0	x	x	previous ( $Q_n$ )
1	0	0	previous ( $Q_n$ )
1	1	0	1
1	0	1	0
1	1	1	toggled ( $\bar{Q}_n$ )

level-sensitive

But in practise;

we employ edge-triggered  
flip-flops.

22.2

in. O

out. O

in. O

in.

O

O

O

1.5) height = 2

width = 1.25

height = 2

width = 1.25

length = 2.5

height = 2

## Week-9:-

\* average of a fun.  $f(t)$  in time period  $t_1-t_2$  is

$$\frac{\int_{t_1}^{t_2} f(t) dt}{t_2 - t_1}$$

\* if  $f(t)$  is periodic; with period  $T$ ;  
then  $\langle f(t) \rangle$  is defined as

$$\frac{\int_0^T f(t) dt}{T} \quad (\text{no interval is specified here}).$$

\* Avg. value; when  $f(t)$  is periodic & period is in radians -

$$= \frac{1}{2\pi} \cdot \int_0^{2\pi} f(\omega t) \cdot d(\omega t)$$

$$= \frac{1}{2\pi} \int_0^{2\pi} f(a) da$$

\*  $f(t) = \sin(\omega t - \theta)$

then  $\langle f(t) \rangle$  is always 0.

∴ for some usefulness,

$$\sqrt{\langle f^2(t) \rangle} \text{ is chosen... } (F_{rms})^2 = \frac{\int_0^T f^2(t) dt}{T}$$

RMS

## Power in AC circuit:-

By defn;  $P_{inst.} = V(t) \cdot i(t) = V_m \cdot I_{max} \cdot \sin(\omega t) \cdot \sin(\omega t - \theta)$

active power component of  $\bar{I}$ ;  $\parallel$  to  $\bar{V}$ .

$$P_{inst.} = \underbrace{V_m \cdot I_m \cdot \cos\theta \cdot \sin^2(\omega t)}_{\text{always of same sign.}} - \underbrace{V_m \cdot I_m \cdot \sin\theta \cdot \sin\omega t \cos\omega t}_{\text{avg. = 0.}}$$

reactive component.  
 $\bar{I}$   $\perp$  to  $\bar{V}$ .

Also:

$$P_{inst.} = \underbrace{\frac{V_m \cdot I_m \cdot \cos\theta}{2}}_{\text{useful, constant, active power.}} - \underbrace{\frac{V_m \cdot I_m \cdot \cos(2\omega t - \theta)}{2}}_{\text{Oscillating power}}$$

- concept of power, in AC circuits
- power factor.
- phasor representation.
- Network theorems on AC circuits
  - Thevenin
  - Norton
  - Superposition
  - Max power

Hence,  $P_{inst}$



$$\langle P_{inst} \rangle = \frac{V_m I_m \cos \theta}{2}$$

$$= V_{eff} \cdot I_{eff} \cdot \cos \theta$$

rms values.

effective value means

rms values.

- for current
- voltage

\* Active power

$$P = V_{eff} \cdot I_{eff} \cdot \cos \theta.$$

Reactive power

$$Q = V_{eff} \cdot I_{eff} \cdot \sin \theta. \quad [\text{no useful work.}]$$

just circulates in system.

$$\therefore \text{apparent power} = \sqrt{P^2 + Q^2}$$

$$\text{* power factor} = \cos \theta = \frac{P_{avg}}{V_{eff} \cdot I_{eff}} \quad (\text{lag/lead})$$

definition:  $V_{eff} \cdot I_{eff}$

inductive capacitive

P-factor determines

useful power

power in circuit - loss due to reactive load =  $\cos^2 \theta$

power factor

current in circuit

current in circuit

current in circuit

losses in circuit - useful power =  $\cos^2 \theta$

losses in circuit

→ phasor representation:

$$i_1 = I_m \cdot \sin(\omega t)$$

$$i_2 = I_m \cdot \sin(\omega t + \theta_2)$$

$$i_3 = i_1 + i_2$$

$$i_3 = I_m \cdot \sin(\omega t + \theta_3)$$

How to write  $I_3$  &  $\theta_3$  in known parameters?

(a) Add both  $i_1, i_2$  graphically & find eqn of resultant inscne.

(b) add trigonometrically.

Okay... but not easy to do in mind.

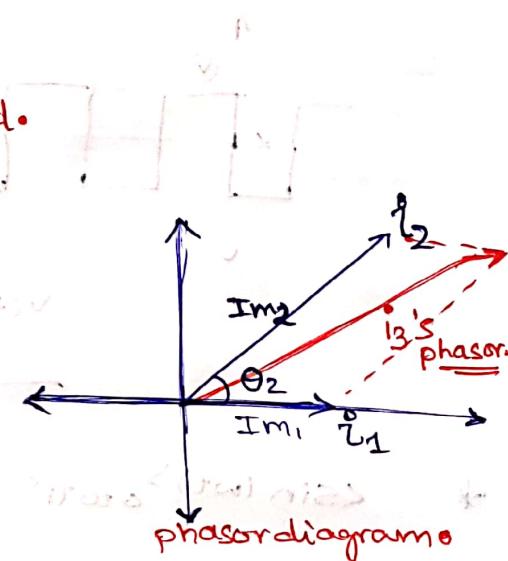
(c) lets use phasors!

$$i_1 = (\underline{\text{Im}} [I_m \cdot e^{j\omega t}]) \quad \text{the phasor.}$$

$$i_2 = \underline{\text{Im}} [I_m \cdot e^{j(\omega t + \theta_2)}]$$

$$i_2 = \underline{\text{Im}} [I_m \cdot e^{j\theta_2} \cdot e^{j\omega t}] \quad \begin{array}{l} \text{the} \\ \text{phasor} \end{array} \quad \begin{array}{l} \text{the time} \\ \text{operator.} \end{array} \quad \begin{array}{l} \text{Same for a} \\ \text{circuit?} \end{array}$$

$$\boxed{i_2 = \frac{I_m}{\sqrt{2}} \cdot e^{j\theta_2}} \quad \begin{array}{l} \text{RMS "phasor"} \\ \text{do } |i_2| \text{ for magnitude.} \end{array}$$



phasordiagramme

$$\text{Q) } i_1 = 10\sqrt{2} \sin(\omega t) \quad i_2 = 20\sqrt{2} \sin(\omega t + 60^\circ)$$

find sum?

So) always write r.m.s. phasors and add & convert back.

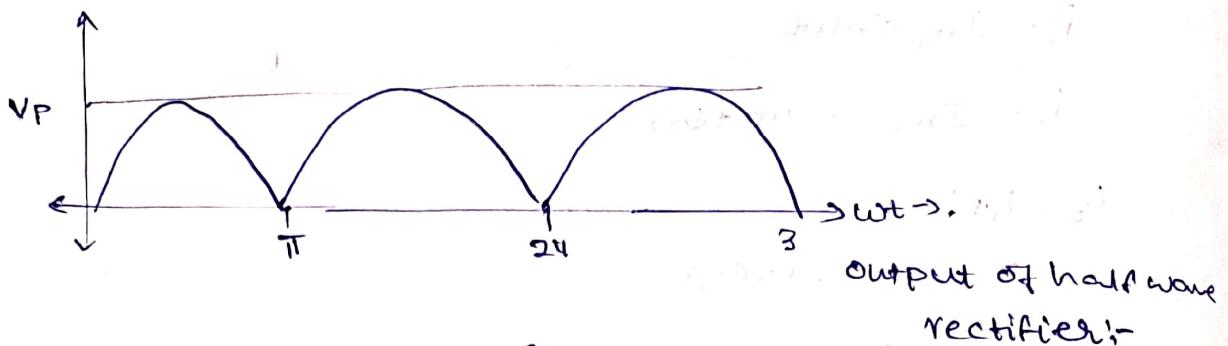
$$I_1 = 10 \cdot e^{j(0)} \quad I_2 = 20 \cdot e^{j(60^\circ)}$$
$$= 10 \quad = 20 \cdot \left( \frac{1}{2} + \frac{\sqrt{3}}{2} j \right)$$

$$\text{if } \bar{I} = I_m \cdot \angle \theta$$
$$i = I_m \sqrt{2} \cdot \sin(\theta + \omega t)$$

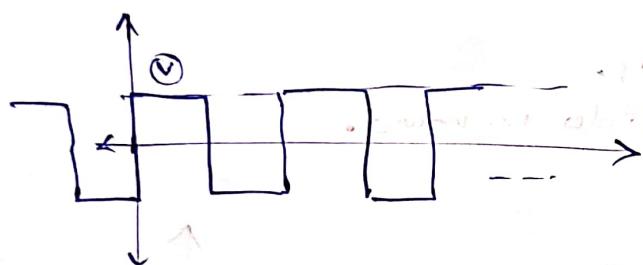
$$I_3 = 20 + 10\sqrt{3}i \quad (\text{kinda vector addn only}).$$

$$\therefore I_3's \text{ mag.} = 10\sqrt{7}. \text{ Phase} = \tan^{-1}\left(\frac{\sqrt{3}}{2}\right) = 41^\circ$$

$$\therefore I_3 = 10\sqrt{7} \cdot e^{j(41^\circ)} \Rightarrow i_3 = 10\sqrt{7} \cdot \sin(41^\circ + \omega t)$$



$$V_{out}(t) = \frac{2V_p}{\pi} - \frac{4V_p}{\pi} \left( \sum_{n=2,4,6,\dots}^{\infty} \frac{\cos(n\omega t)}{n^2 - 1} \right)$$



$$V(t) = \frac{4N}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n} \cdot \sin(n\omega t)$$

\*  $\langle \sin(\omega t) \rangle_{0 \text{ to } \pi}$  =  $\frac{2}{\pi} \left[ \int_0^{\pi} \left( \text{not } \frac{1}{2} \right) d\theta \right] \text{ and } = \frac{2}{\pi}$

a)  $V(t) = \frac{10}{V_1} + 5 \sin(\omega t)$

$V_{rms} = ?$

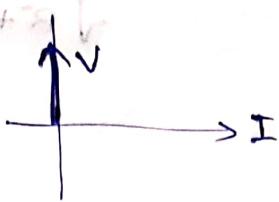
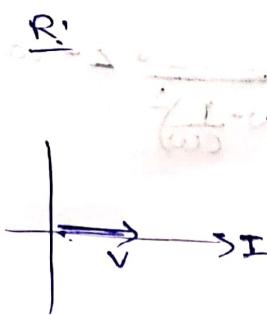
$V_{1 rms} = 10$

$V_{2 rms} = \frac{5}{\sqrt{2}}$

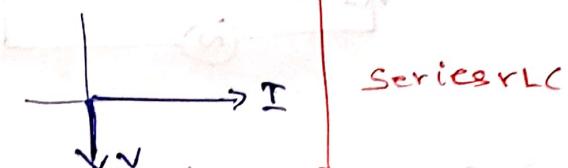
$V_{rms} = \sqrt{(V_{1 rms})^2 + (V_{2 rms})^2} = 10.6 V$

→ Steady state response!

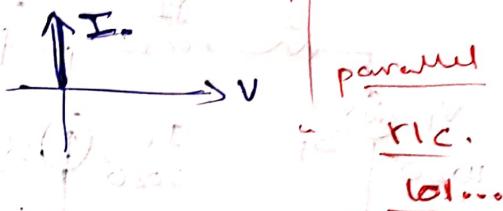
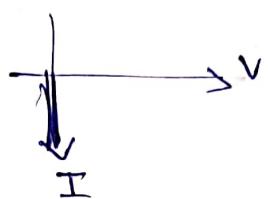
$$X_L = L\omega$$



$$X_C = \frac{1}{C\omega}$$



Series RLC



parallel  
RLC.  
circuit

$$\omega = 120\pi$$

$$R = 35\Omega$$

$$L = 0.0106 \text{ H}$$

$$V = 100\sqrt{2} \sin(\omega t)$$

Series RLC-circuit

find  $i_{\text{eff}}$

$$\bar{V} = 100 \angle 0^\circ$$

phasor

$$\bar{Z} = \bar{Z}_R + \bar{Z}_L$$

$$= 3 + j(120 \times 3.14 \times 0.0106)$$

$$= 3 + 4j$$

phasor

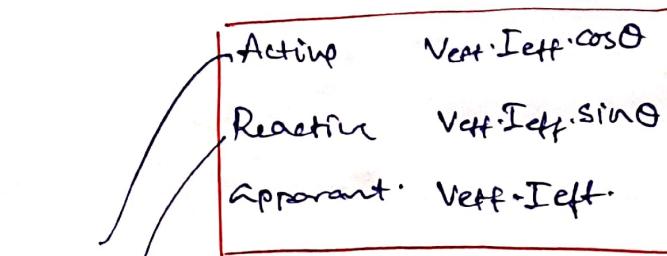
$$\bar{I} = \frac{\bar{V}}{\bar{Z}} = \frac{100 \angle 0^\circ}{3 + 4j} \approx \frac{100 \cdot e^{j0^\circ}}{5 \cdot e^{j53^\circ}} = 20 \cdot e^{-j53^\circ}$$

phasor

$$= 20 \angle -53^\circ$$

$$\therefore i_{\text{eff}} = |\bar{I}| = 20 \text{ A}$$

$$P_f = \cos(-53^\circ) = 0.6 \quad \text{log}$$



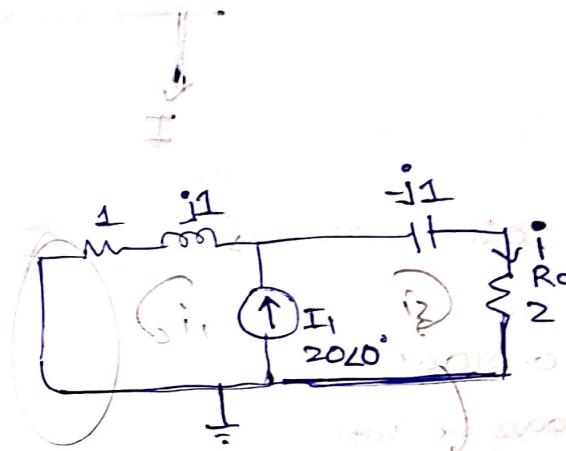
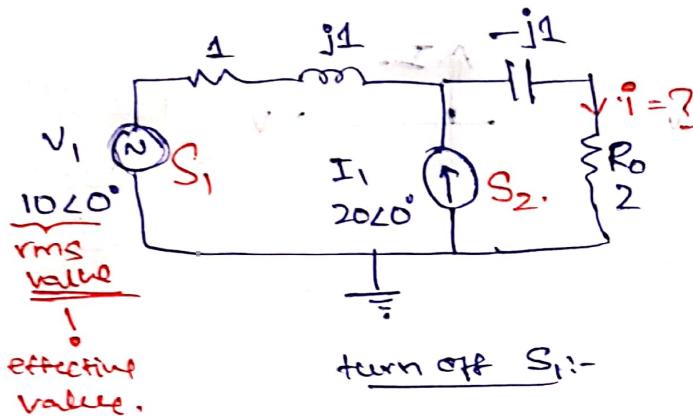
- Work done by  $\bar{I}_{\text{phasor}}$ 's component  $1/\text{el to voltage}$   
 \* by  $\bar{I}_{\text{phasor}}$  I component to  $\bar{V}$ .

\* for a series RLC circuit:-



$$I \angle 0^\circ = \frac{V \angle 0^\circ}{\sqrt{R^2 + (L\omega - \frac{1}{C\omega})^2}} \cdot \angle -\tan^{-1}\left(\frac{L\omega - \frac{1}{C\omega}}{R}\right)$$

i) Superposition:-



turn off S<sub>2</sub>:

$$Z_{\text{out}} = 3$$

$$i_2 = \frac{V_1}{Z_{\text{out}}} = \frac{10}{3}$$

$$\therefore V_1 = i_2 Z_{\text{out}} = 10 \cdot \frac{1}{3} + j \frac{4}{3} (S)$$

$$\frac{20}{3}(1+j)$$

$$\frac{20+20j}{3}$$

$$Z_{\text{eff}} = 1+j$$

$$i_1 = \frac{V_1}{1+j} \quad i_2 = \frac{V_1}{2-j}$$

$$20\angle 0^\circ = V_1 \cdot \left( \frac{1}{1+j} + \frac{1}{2-j} \right)$$

$$= \frac{1+j+2}{3-j} \cdot V_1$$

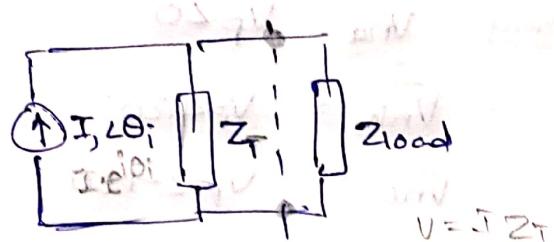
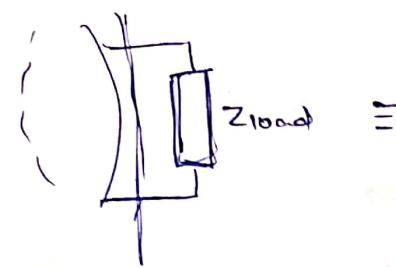
$$= \frac{3+j}{3-j} \cdot V_1$$

$$\therefore 20\angle 0^\circ = 20(1)$$

$$V_1 = \frac{20(1)(3+j)}{3}$$

$$\therefore i_2 = \frac{20(3+j)}{6-3j} \cdot \frac{4}{3} (S+j)$$

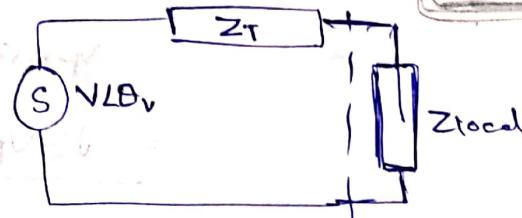
### Norton theorem:-



$$V = \sqrt{Z_T}$$

$$V = I \cdot e^{j\theta_i} \cdot Z_T$$

venevin:



$Z_T$  lookback ✓

Here instead of simple noso,

seeing  $I = \text{its } I \langle \text{number} \rangle \cdot e^{j\langle \text{angle} \rangle}$   
eff. value or rms value.

even impedance.

Conclusion:-

use nonphasors everywhere.

& find  $V_T, Z_T, I_T$

open circuit

short circuit.

physical value =  $\langle \text{number} \rangle \sqrt{2} \cdot \sin(\omega t + \langle \text{angle} \rangle)$

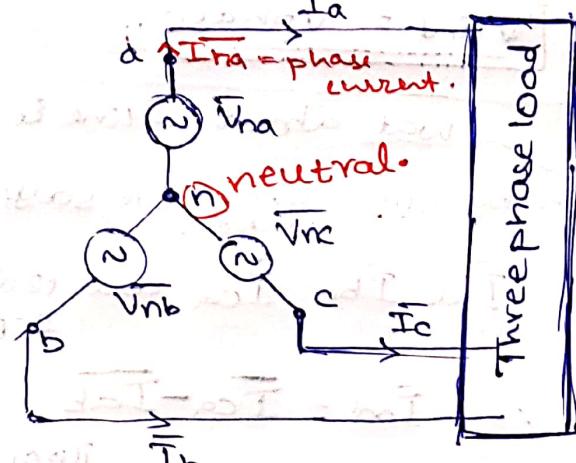
(But not Propedance)

impedance will be

$\langle \text{number} \rangle$  only.

Three-phase balanced system:-

i) Y-connection:  $\rightarrow$  line current.

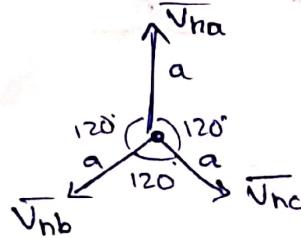


$V_{na}, V_{nb}, V_{nc}$ : phase voltages  
 $V_{ab}, V_{bc}, V_{ca}$ : Line-to-line voltages.

- compromises of three - single phase voltage sources

- identical Amplitude & frequency

- any 2, differ by phase angle  $120^\circ$



$$\text{Say } \bar{V}_{na} = V_p \angle 0^\circ$$

$$\bar{V}_{nb} = V_p \angle 120^\circ$$

$$\bar{V}_{nc} = V_p \angle -120^\circ$$

then

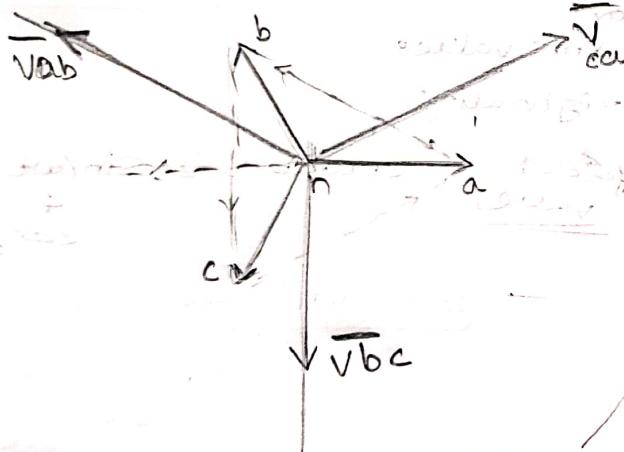
$$\bar{V}_{ab} = \bar{V}_{nb} - \bar{V}_{na}$$

$$= V_p \angle 120^\circ + V_p \angle 180^\circ$$

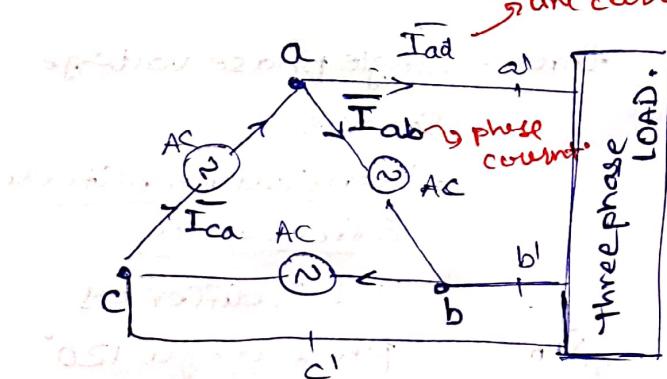
$$= \sqrt{3} V_p \angle 150^\circ$$

$$\therefore |\text{Vline-to-line}| = \sqrt{3} \cdot |\text{phase voltage}|$$

$$E_p \text{ Iline} = \text{Iphase.}$$



### \* $\Delta$ -3 phase connection:-



$$|\text{Vline}| = |\text{Vphase}|$$

what about  $I_{\text{line}}$  &  $I_{\text{phase}}$ ?

- by symmetry, we say;

$I_{ab}$   $I_{bc}$ ,  $I_{ca}$  are  $120^\circ$  phase separated.

$$I_{ad} = I_{ca} - I_{ab}$$

$$= I - I \cdot e^{j(120)}$$

$$I = I \left( \frac{1}{2} + j\frac{\sqrt{3}}{2} \right)$$

$$= \sqrt{3} I \left( \frac{\sqrt{3}}{2} - j\frac{1}{2} \right)$$

$$\therefore I_{\text{line}} = \sqrt{3} I_{\text{phase}}$$

Power in 3phase - Systems.

$$P_{\text{in one phase}} = V_I \cos \theta - V_I \cos(2\omega t - \theta)$$

now; 3-single phases are there now.

effective values.

$$P_{\text{net}} = 3 \underbrace{\frac{V_I}{P_p} \cos \theta}_{J} - V_I \cos(2\omega t - \theta) - V_I \cos(2\omega t - 120^\circ - \theta)$$

$$- V_I \cos(2\omega t + 120^\circ - \theta)$$

this  $\theta$  is same b/w  $i(t), v(t)$  for all three phases.

(By symmetry?)

$V_p$  → phase voltage  
 $V_L$  - Line voltage

$$\therefore P_{\text{avg}} = 3 V_p \cdot I_p \cdot \cos \theta \rightarrow \text{wrt. Phase}$$

Ex

$$\text{Y case; } V_L = \sqrt{3} V_p$$

$$I_L = I_p$$

$$\Delta \text{ case; } V_L = V_p$$

$$I_L = \sqrt{3} I_p$$

$$\therefore P_{\text{avg}} = \frac{3}{\sqrt{3}} \cdot V_L \cdot I_L \cdot \cos \theta \rightarrow \text{wrt. Line}$$

possible circuit!

