

CS-226 Course Project

2020-Spring Semester

Department of Computer Science

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FSM States

States:-

S₀:
 $PC \rightarrow mem_addr$ | $IR.wr$
 $mem_D \rightarrow IR$

S_α:
 $PC \rightarrow ALUa$ |
 $t_1 \rightarrow ALUb$ | $PC.wr$
 $ALUC \rightarrow PC$

S₁:
 $IR_{11-9} \rightarrow RF_A1$ | $t_1.wr$
 $IR_{8-6} \rightarrow RF_A2$ | $t_2.wr$
 $RF_D1 \rightarrow t_1$ | $t_3.wr$
 $RF_D2 \rightarrow t_2$
 $\vec{O}_{16} \rightarrow t_3$

S₂:
 $t_1 \rightarrow ALUa$ | $t_3.wr$
 $t_2 \rightarrow ALUb$
 $ALUC \rightarrow t_3$

S₂¹:
 $t_1 \rightarrow ALUa$ | $t_3.wr$
 $t_2 \rightarrow ALUb$ | $ALU.nand$
 $ALUC \rightarrow t_3$

S₃:
 $t_3 \rightarrow RF_D3$ | $RF.wr$
 $IR_{5-3} \rightarrow RF_A3$

S₄:
 $t_1 \rightarrow ALUa$ | $t_3.wr$
 $SE_6(IR_{5-0}) \rightarrow ALUb$
 $ALUC \rightarrow t_3$

S₅:
 $t_3 \rightarrow RF_D3$ | $RF.wr$
 $IR_{8-6} \rightarrow RF_A3$

S₆:
 $Imm9e16(IR_{8-0}) \rightarrow RF_D3$ | $RF.wr$
 $IR_{11-9} \rightarrow RF_A3$

S₇:
 $t_2 \rightarrow ALUa$ | $t_2.wr$ (asynchronous)
 $SE_6(IR_{5-0}) \rightarrow ALUb$
 $ALUC \rightarrow t_2$] synchronous

S₈:
 $t_2 \rightarrow mem_addr$ | $t_3.wr$
 $mem_D \rightarrow t_3$

S₉:
 $t_2 \rightarrow mem_addr$ | $mem.wr$
 $t_1 \rightarrow mem_in$

S₁₀:
 $IR_{11-9} \rightarrow RF_A3$ | $RF.wr$
 $t_3 \rightarrow RF_D3$

S11:

$t_1 \rightarrow \text{mem_addr} \quad | \quad t_2 \cdot \text{wr}$
 $\text{mem_D} \rightarrow t_2$

S12:

$t_2 \rightarrow \text{RF_D3} \quad | \quad \text{RF} \cdot \text{wr}$
 $t_3 \xrightarrow{2-D} \text{RF_A3} \quad | \quad t_3 \cdot \text{wr}$
 $t_3 \rightarrow \text{ALUa}$
 $t_1 \rightarrow \text{ALUb}$
 $\text{ALUC} \rightarrow t_3$

S19:

$t_1 \rightarrow \text{ALUa} \quad | \quad t_1 \cdot \text{wr}$
 $t_1 \rightarrow \text{ALUb}$
 $\text{ALUC} \rightarrow t_1$

S13:

$t_3 \rightarrow \text{ALUa} \quad | \quad t_3 \cdot \text{wr}$
 $t_1 \rightarrow \text{ALUb} \quad | \quad t_2 \cdot \text{wr}$
 $\text{ALUC} \rightarrow t_3$
 $t_3 \rightarrow \text{RF_A1}$
 $\text{RF_D1} \rightarrow t_2$

S14:

$t_1 \rightarrow \text{ALUa} \quad | \quad t_1 \cdot \text{wr}$
 $t_1 \rightarrow \text{ALUb} \quad | \quad \text{Mem} \cdot \text{wr}$
 $\text{ALUC} \rightarrow t_1$
 $t_1 \rightarrow \text{mem_addr}$
 $t_2 \rightarrow \text{mem_in}$

S15:

$\text{PC} \rightarrow \text{ALUa} \quad | \quad \text{PC} \cdot \text{wr}$
 $\text{SEQ}(\text{IR}_{8-0}) \rightarrow \text{ALUb}$
 $\text{ALUC} \rightarrow \text{PC}$

S16:

$\text{IR}_{11-9} \rightarrow \text{RF_A3} \quad | \quad \text{RF} \cdot \text{wr}$
 $\text{PC} \rightarrow \text{RF_D3} \quad | \quad t_2 \cdot \text{wr}$
 $\text{IR}_{8-6} \rightarrow \text{RF_A2}$
 $\text{RF_D2} \rightarrow t_2$

S17:

$\text{PC} \rightarrow \text{ALUa}$
 $\text{SEQ}(\text{IR}_{5-0}) \rightarrow \text{ALUb} \quad | \quad \text{PC} \cdot \text{wr}$
 $\text{ALUC} \rightarrow \text{PC}$

S18:

$t_2 \rightarrow \text{PC} \quad | \quad \text{PC} \cdot \text{wr}$

Instruction- State Transition

Instructions : State transitions:-

1) ADD:-

$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_x \dots S_0$

2) ADC:-

$S_0 \xrightarrow{C=1} S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_x \dots S_0$
 $\xleftarrow{C=0} S_0$

3) ADZ:-

$S_0 \xrightarrow{Z=1} S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_x \dots S_0$
 $\xleftarrow{Z=0} S_0$

4) ADI:-

$S_0 \rightarrow S_1 \rightarrow S_4 \rightarrow S_5 \rightarrow S_x \dots S_0$

5) NDU:-

$S_0 \rightarrow S_1 \rightarrow S_2' \rightarrow S_3 \rightarrow S_x \dots S_0$

6) NDC:-

$S_0 \xrightarrow{C=1} S_1 \rightarrow S_2' \rightarrow S_3 \rightarrow S_x \dots S_0$
 $\xleftarrow{C=0} S_0$

7) NDZ:-

$S_0 \xrightarrow{Z=1} S_1 \rightarrow S_2' \rightarrow S_3 \rightarrow S_x \dots S_0$
 $\xleftarrow{Z=0} S_0$

8) LHI:-

$S_0 \rightarrow S_6 \rightarrow S_x \dots S_0$

9) LW:-

$S_0 \rightarrow S_1 \rightarrow S_7 \rightarrow S_8 \rightarrow S_{10} \rightarrow S_x \dots S_0$

10) SW:-

$S_0 \rightarrow S_1 \rightarrow S_7 \rightarrow S_9 \rightarrow S_x \dots S_0$

11) LA:-

$S_0 \rightarrow S_1 \rightarrow S_{11} \xrightarrow{t_3 \neq "111"} S_{19} \rightarrow S_x \dots S_0$
 $\xleftarrow{t_3 = "111"} S_{19}$
 $S_{11} \downarrow S_{12}$

12) SAi:-

$S_0 \rightarrow S_1 \rightarrow S_{13} \xrightarrow{t_3 \neq "000"} S_{14} \rightarrow S_x \dots S_0$
 $\xleftarrow{t_3 = "000"} S_{14}$

13) BEQ:-

$S_0 \rightarrow S_1 \xrightarrow{t_1 = t_2} S_{17} \dots S_0$
 $\xleftarrow{\text{else}} S_x \dots S_0$

14) JAL:-

$S_0 \rightarrow S_{16} \rightarrow S_{15} \dots S_0$

15) JLR:-

$S_0 \rightarrow S_{16} \rightarrow S_{18} \dots S_0$

FSM Diagram

Control Signals

Column1	w1	w2	w3	w4	w5	w6	w7	m1	m12	m21	m20	m31	m30	m4	m51	m50	m61	m60	m71	m70	m8	m92	m91	m90	m101	m100	wc	wz	mz	alu_op
sa	1							0														0	1	1	0	1				
s0			1							0	1																			
s1					1	1	1							0			0	1	0	1	0									
s2					1												1	0				0	1	0	1	0	1	1		0
s2'					1												1	0				0	1	0	1	0	0	1		1
s3				1								1	0		1	1														
s4					1												1	0				0	0	1	1	0	1	1		
s5				1								0	1		1	1														
s6				1								0	0		0	1														
s7						1													1	0		0	0	1	1	1				
s8					1					0	0						0	0												
s9		1							0	0	0																			
s10				1								0	0		1	1											1	1	1	
s11						1				1	1								1	1										
s12				1	1							1	1		1	0	1	0				0	1	1	0	0				
s13					1	1								1			1	0	0	0		0	1	1	0	0				
s14		1					1		1	1	1										1	0	1	1	1	0				
s15	1							0														0	0	0	0	1				
s16				1		1						0	0		0	0			0	1										
s17	1							0														0	0	1	0	1				
s18	1							1																						
s19							1														1	0	1	1	1	0				

w = 1 means active/enable write.

default w is 0 (disabled)

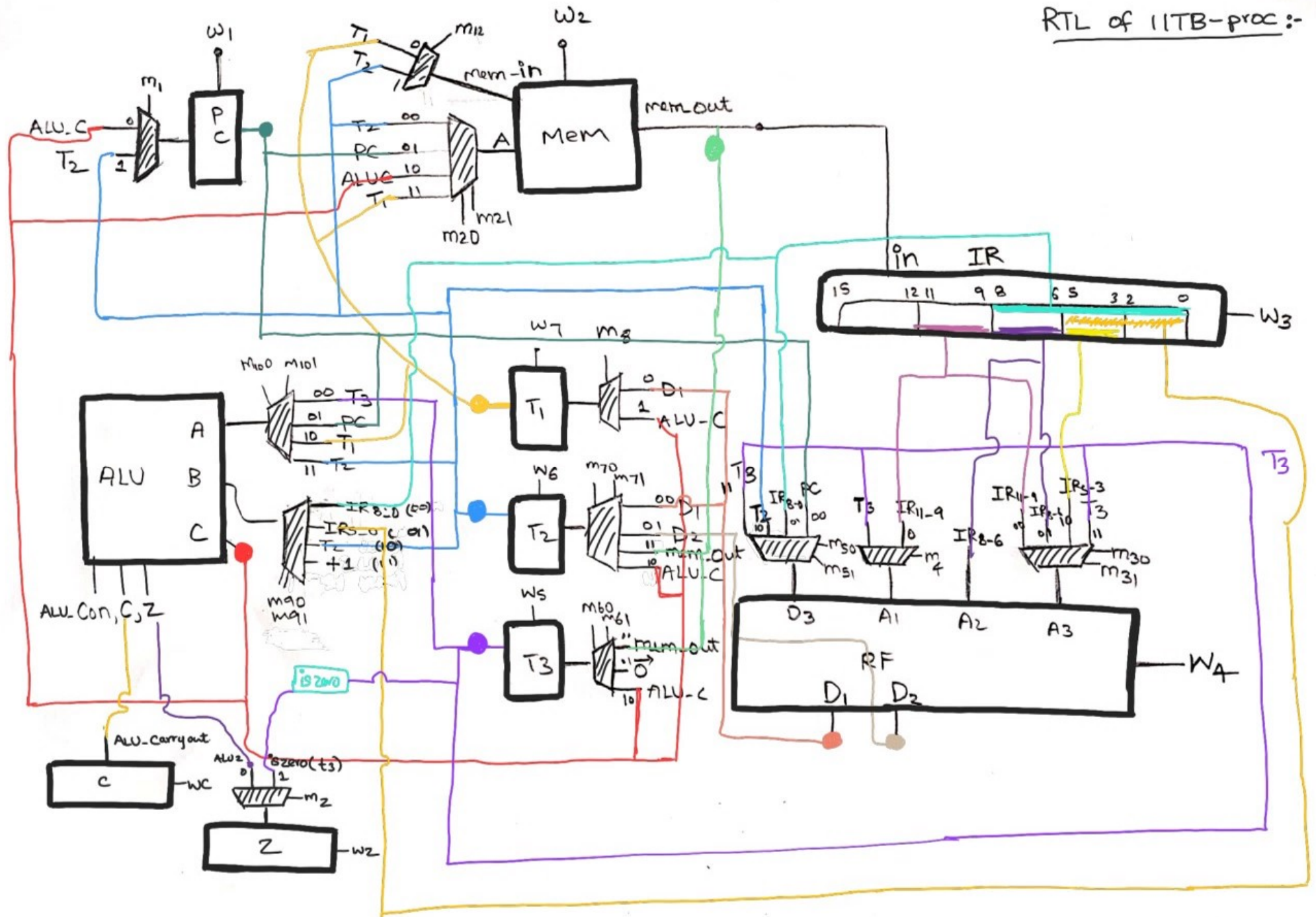
In w's coloum, empty implies 0

m's are mux selectors

In m's column, empty implies don't care.

RTL circuit

RTL of IITB-proc :-



RTL:

