# CS-226 Course Project

*2020-Spring Semester*

*Department of Computer Science*

*Indian Institute of Technology, Bombay - Powai*

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# FSM States

## States:-

**$S_0$:**

| | |
|---|---|
| $PC \longrightarrow mem\_addr$ | IR.WR |
| $mem\_D \longrightarrow IR$ | |

**$S_x$:**

| | |
|---|---|
| $PC \longrightarrow ALUa$ | PC.WR |
| $+1 \longrightarrow ALUb$ | |
| $ALUc \longrightarrow PC$ | |

**$S_1$:**

| | |
|---|---|
| $IR_{11-9} \longrightarrow RF\_A1$ | $t_1$-WR |
| $IR_{8-6} \longrightarrow RF\_A2$ | $t_2$.WR |
| $RF\_D1 \longrightarrow t_1$ | $t_3$.WR |
| $RF\_D2 \longrightarrow t_2$ | |
| $\overrightarrow{0}_{16} \longrightarrow t_3$ | |

**$S_2$:**

| | |
|---|---|
| $t_1 \longrightarrow ALUa$ | t3.WR |
| $t_2 \longrightarrow ALUb$ | |
| $ALUc \longrightarrow t_3$ | |

**$S_2'$:**

| | |
|---|---|
| $t_1 \longrightarrow ALUa$ | $t_3$.WR |
| $t_2 \longrightarrow ALUb$ | ALU.nand |
| $ALUc \longrightarrow t_3$ | |

**$S_3$:**

| | |
|---|---|
| $t_3 \longrightarrow RF\_D3$ | RF.WR |
| $IR_{5-3} \longrightarrow RF\_A3$ | |

**$S_4$:**

| | |
|---|---|
| $t_1 \longrightarrow ALUa$ | $t_3$.WR |
| $SE_6(IR_{5-0}) \longrightarrow ALUb$ | |
| $ALUc \longrightarrow t_3$ | |

**$S_5$:**

| | |
|---|---|
| $t_3 \longrightarrow RF\_D3$ | RF.WR |
| $IR_{8-6} \longrightarrow RF\_A3$ | |

**$S_6$:**

| | |
|---|---|
| $Imm9e16(IR_{8-0}) \longrightarrow RF\_D3$ | RF.WR |
| $IR_{11-9} \longrightarrow RF\_A3$ | |

**$S_7$:**

| | |
|---|---|
| $t_2 \longrightarrow ALUa$ (asyncronous) | $t_2$.W |
| $SE_6(IR_{5-0}) \longrightarrow ALUb$ (asyncronous) | |
| $ALUc \longrightarrow t_2$ (syncronous) | |

**$S_8$:**

| | |
|---|---|
| $t_2 \longrightarrow mem\_addr$ | $t_3$.WR |
| $mem\_D \longrightarrow t_3$ | |

**$S_9$:**

| | |
|---|---|
| $t_2 \longrightarrow mem\_addr$ | mem.WR |
| $t_1 \longrightarrow mem\_in$ | |

**$S_{10}$:**

| | |
|---|---|
| $IR_{11-9} \longrightarrow RF\_A3$ | RF.WR |
| $t_3 \longrightarrow RF\_D3$ | |

S11:

$t_1 \rightarrow$ mem_addr
mem_D $\rightarrow t_2$

| $t_2$.wr

S12:

$t_2 \rightarrow$ RF_D3
$t_{3\ 2\text{-}0} \rightarrow$ RF_A3
$t_3 \rightarrow$ ALUa
$+1 \rightarrow$ ALUb
ALUC $\rightarrow t_3$

| RF.wr
| $t_3$.wr

S13:

$t_3 \rightarrow$ ALUa
$+1 \rightarrow$ ALUb
ALUC $\rightarrow t_3$
$t_3 \rightarrow$ RF_A1
RF_D1 $\rightarrow t_2$

| $t_3$.wr
| $t_2$.wr

S14:

$t_1 \rightarrow$ ALUa
$+1 \rightarrow$ ALUb
ALUC $\rightarrow t_1$
$t_1 \rightarrow$ mem_addr
$t_2 \rightarrow$ mem_in

| $t_1$.wr
| Mem.wr

S15:

PC $\rightarrow$ ALUa
$SE_9(IR_{8\text{-}0}) \rightarrow$ ALUb
ALUC $\rightarrow$ PC

| PC.wr

S16:

$IR_{11\text{-}9} \rightarrow$ RF_A3
PC $\rightarrow$ RF_D3
$IR_{8\text{-}6} \rightarrow$ RF_A2
RF_D2 $\rightarrow t_2$

| RF.wr
| $t_2$.wr

S17:

PC $\rightarrow$ ALUa
$SE_6(IR_{5\text{-}0}) \rightarrow$ ALUb
ALUC $\rightarrow$ PC

| PC.wr

S18:

$t_2 \rightarrow$ PC

| PC.wr

S19:

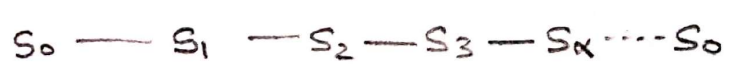
$t_1 \rightarrow$ ALUa
$+1 \rightarrow$ ALUb
ALUC $\rightarrow t_1$

| $t_1$.wr

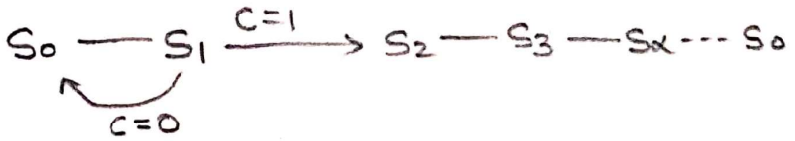
# Instruction-State Transition

# Instructions : State transitions :-

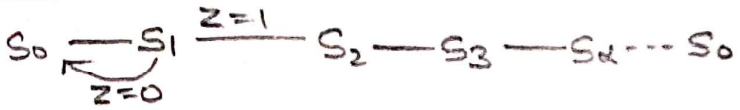
1) ADD :-




2) ADC :-



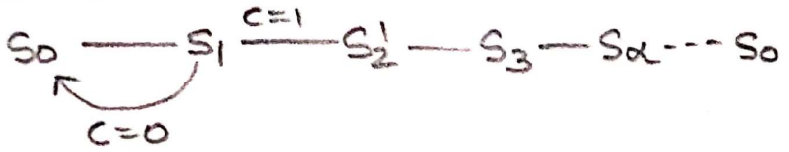

3) ADZ :-



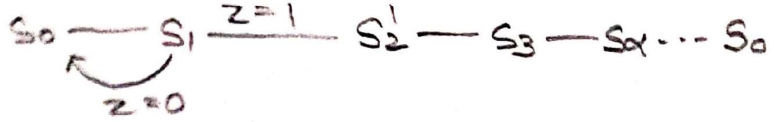

4) ADI :-


5) NDU :-


6) NDC :-

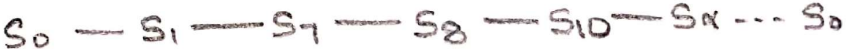



7) NDZ :-



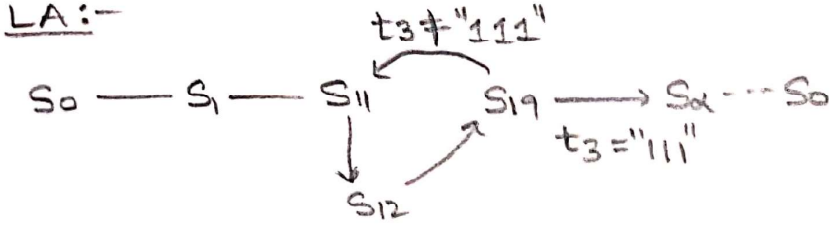

8) LHI :-


9) LW :-

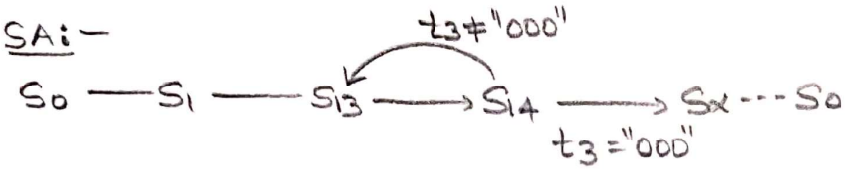



10) SW :-

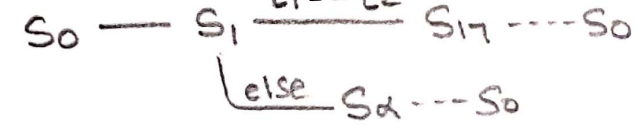

11) LA :-




12) SA :-




13) BEQ :-

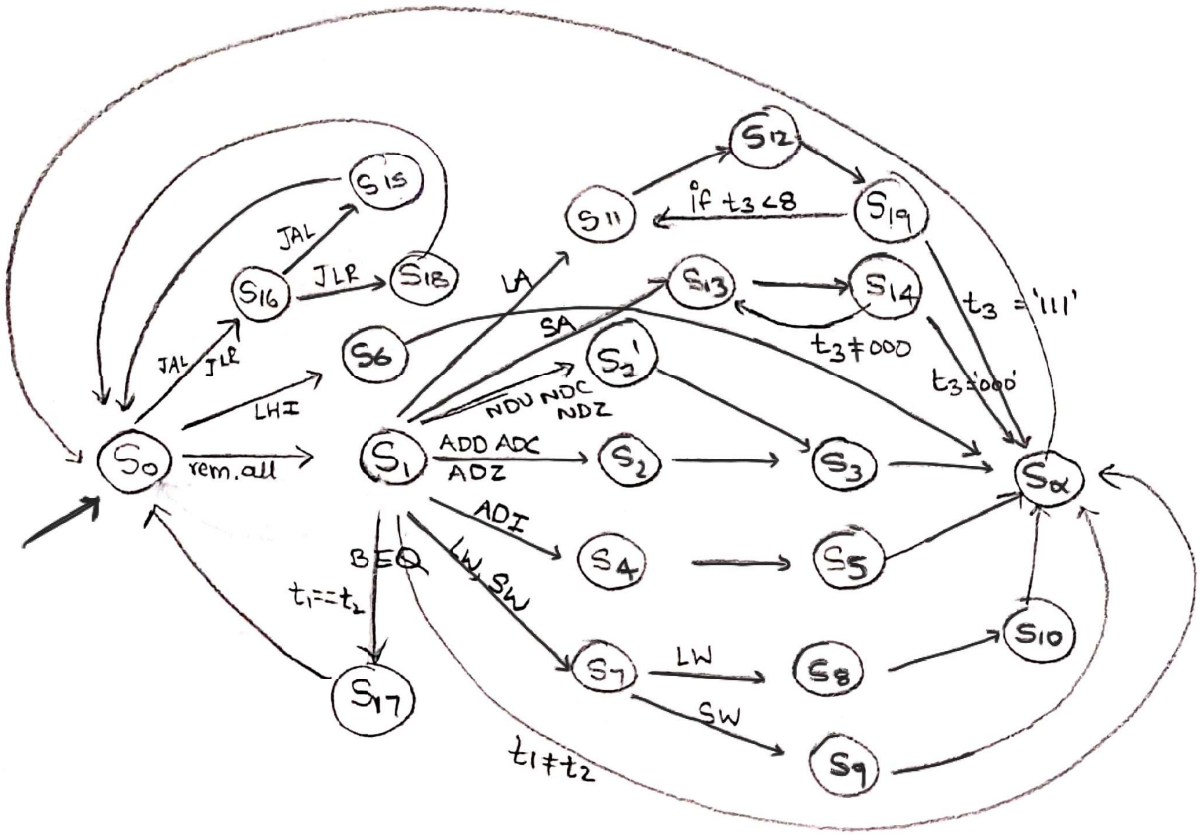



14) JAL :-


15) JLR :-

# FSM Diagram

# State diagram:-




Total 21 states

$S_\alpha, S_1 - S_{19}, S_2'$

These states have been implemented via one-hot encoding.

# Control Signals

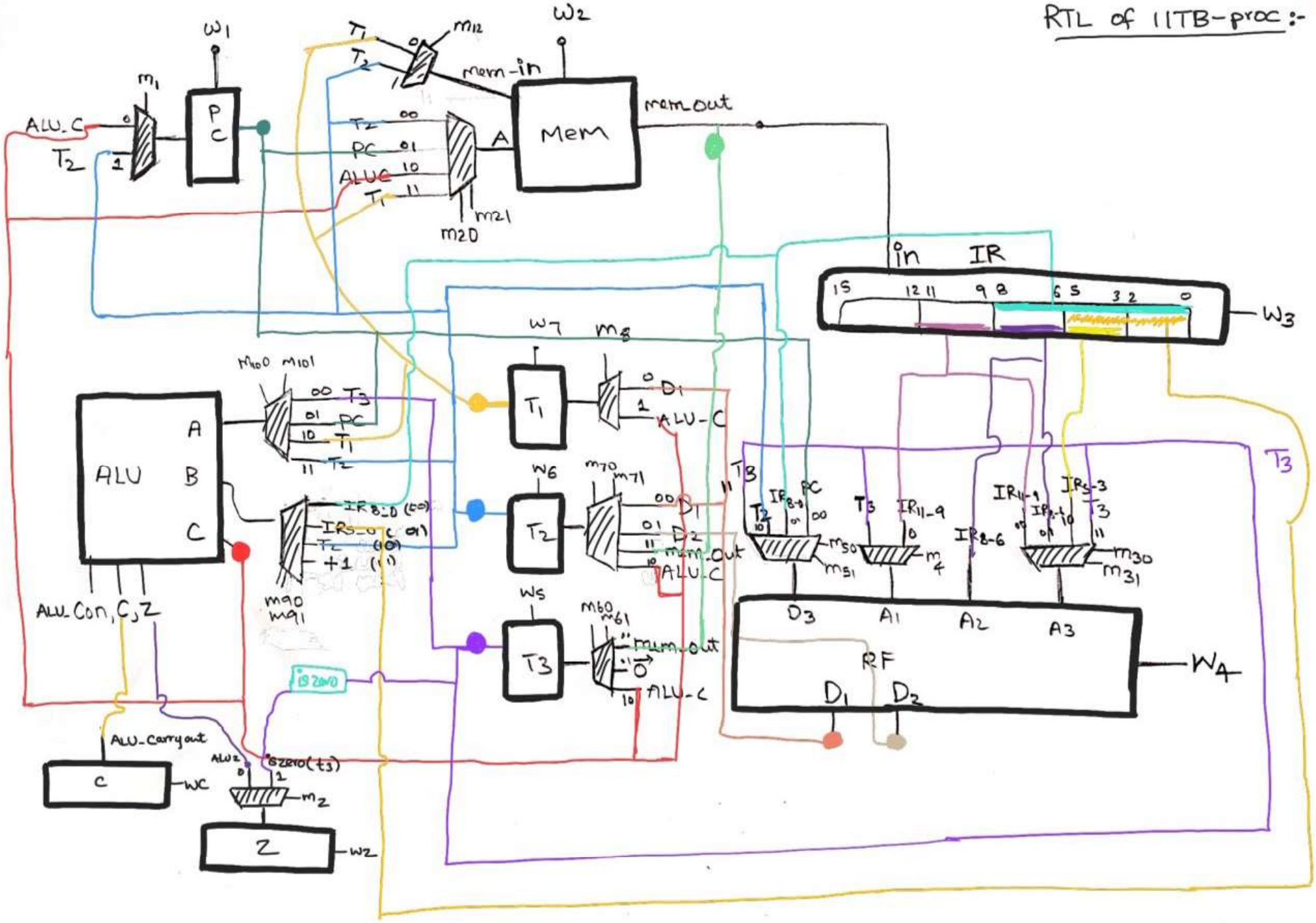
| Column1 | w1 | w2 | w3 | w4 | w5 | w6 | w7 | m1 | m12 | m21 | m20 | m31 | m30 | m4 | m51 | m50 | m61 | m60 | m71 | m70 | m8 | m92 | m91 | m90 | m101 | m100 | wc | wz | mz | alu_op |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **sa** | 1 | | | | | | | 0 | | | | | | | | | | | | | | 0 | 1 | 1 | 0 | 1 | | | | |
| **s0** | | | 1 | | | | | | | 0 | 1 | | | | | | | | | | | | | | | | | | | |
| **s1** | | | | | 1 | 1 | 1 | | | | | | | 0 | | | 0 | 1 | 0 | 1 | 0 | | | | | | | | | |
| **s2** | | | | | 1 | | | | | | | | | | | | 1 | 0 | | | | 0 | 1 | 0 | 1 | 0 | 1 | 1 | | 0 |
| **s2'** | | | | | 1 | | | | | | | | | | | | 1 | 0 | | | | 0 | 1 | 0 | 1 | 0 | 0 | 1 | | 1 |
| **s3** | | | | 1 | | | | | | | | 1 | 0 | | 1 | 1 | | | | | | | | | | | | | | |
| **s4** | | | | | 1 | | | | | | | | | | | | 1 | 0 | | | | 0 | 0 | 1 | 1 | 0 | 1 | 1 | | |
| **s5** | | | | 1 | | | | | | | | 0 | 1 | | 1 | 1 | | | | | | | | | | | | | | |
| **s6** | | | | 1 | | | | | | | | 0 | 0 | | 0 | 1 | | | | | | | | | | | | | | |
| **s7** | | | | | | 1 | | | | | | | | | | | | | 1 | 0 | | 0 | 0 | 1 | 1 | 1 | | | | |
| **s8** | | | | | 1 | | | | | 0 | 0 | | | | | | 0 | 0 | | | | | | | | | | | | |
| **s9** | | 1 | | | | | | | 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| **s10** | | | | 1 | | | | | | | | 0 | 0 | | 1 | 1 | | | | | | | | | | | 1 | 1 | 1 | |
| **s11** | | | | | | 1 | | | | 1 | 1 | | | | | | | | 1 | 1 | | | | | | | | | | |
| **s12** | | | | 1 | 1 | | | | | | | 1 | 1 | | 1 | 0 | 1 | 0 | | | | 0 | 1 | 1 | 0 | 0 | | | | |
| **s13** | | | | | 1 | 1 | | | | | | | | 1 | | | 1 | 0 | 0 | 0 | | 0 | 1 | 1 | 0 | 0 | | | | |
| **s14** | | 1 | | | | | 1 | | 1 | 1 | 1 | | | | | | | | | | 1 | 0 | 1 | 1 | 1 | 0 | | | | |
| **s15** | 1 | | | | | | | 0 | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 1 | | | | |
| **s16** | | | | 1 | | 1 | | | | | | 0 | 0 | | 0 | 0 | | | 0 | 1 | | | | | | | | | | |
| **s17** | 1 | | | | | | | 0 | | | | | | | | | | | | | | 0 | 0 | 1 | 0 | 1 | | | | |
| **s18** | 1 | | | | | | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| **s19** | | | | | | | 1 | | | | | | | | | | | | | | 1 | 0 | 1 | 1 | 1 | 0 | | | | |

w = 1 means active/enable write.
default w is 0 (disabled)
In w's coloum, empty implies 0

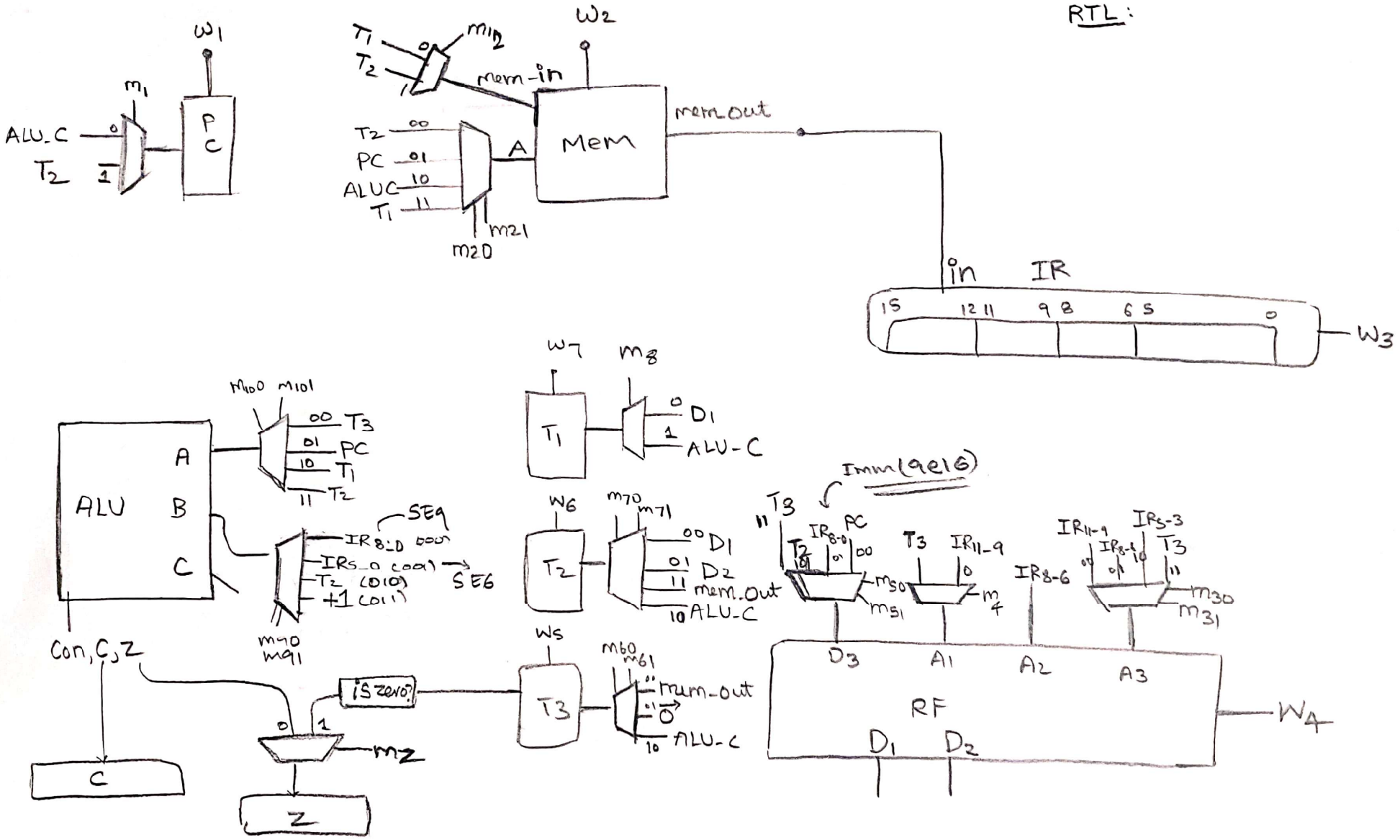
m's are mux selectors
In m's column, empty implies don't care.

# RTL circuit

# RTL of 11TB-proc :-



RTL:


W1
m1
ALU_C
T2
PC
W2
T1
T2
m12
mem-in
T2
PC
ALUC
T1
m20
m21
A
Mem
mem_out
in IR
15
12 11
9 8
6 5
0
W3
W7
m8
T1
D1
ALU-C
m100 m101
ALU
A
B
C
00 T3
01 PC
10 T1
11 T2
SE9
IR8:0 000
IR5_0 0001
T2 0010
+1 0011
SE6
m10
m11
W6
m70 m71
T2
00 D1
01 D2
11 mem_out
10 ALU-C
Imm(9e16)
T3
11
IR8-0
PC
T2
10
00
m50
m51
T3
IR11-9
0
m4
IR8-6
IR11-9
IR8-6
IR5-3
T3
m30
m31
Con, C, Z
W5
m60 m61
is zero?
T3
mem_out
0
ALU-C
m2
C
Z
D3
A1
A2
A3
RF
D1
D2
W4